ISOSMART™ HALF BRIDGE DRIVER CHIPSET*

Features

- 1200V or Greater Low-to High-Side Isolation.
- Drives Power Systems Operating On Up to 575 VAC Mains.
- dv/dt Immunity of Greater Than ±50V/ns.
- Proprietary Low-to High-Side Level-Translation and Communication.
- On-chip Negative Gate-Drive Supply to Ensure Power MOSFET or IGBT Turn-off.
- 5V Logic Compatible HCMOS Inputs with Hysteresis.
- Available in either the 16-pin DIP or the 16-pin Wide-Body, Small-Outline plastic packages (IXBD4410/4411).
- 20ns Switching Time with 100pF Load; 100ns Switching Time with 10,000pF Load.
- 100ns Propagation Delay Time.
- 2A Peak Output Drive Capability
- Self Shut-Down of Output in Response to Over-current or Short-circuit.
- Under-Voltage and Over-Voltage Vdd lockout protection.
- Protection from Cross Conduction of the Half Bridge.
- Logic Compatible Fault Indication from Both Low and High Side Driver (XBD4410/441).

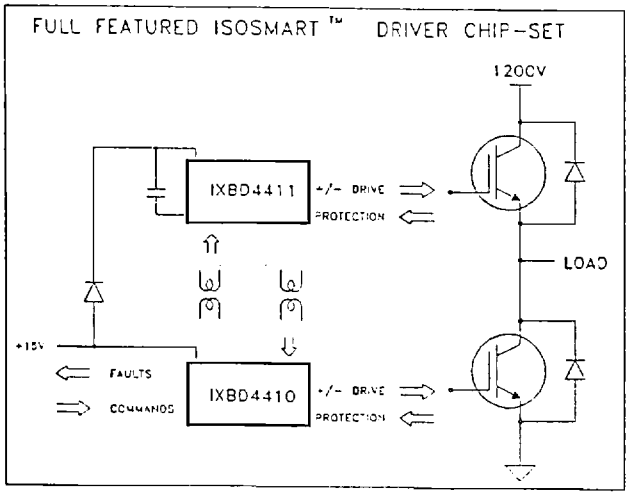
Description

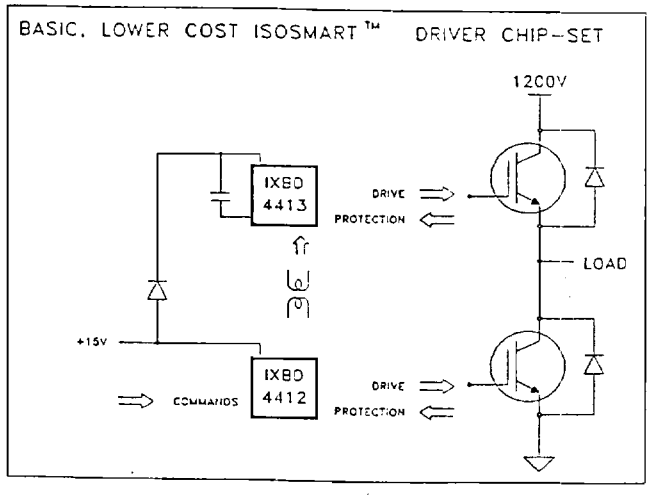
The IXBD4410/IXBD4411 and the IXBD4412/IXBD4413 ISOSMART™ chipsets are designed to control the gates of two power MOSFETs, or power IGBTs, that are connected in a half-bridge (phaseleg) configuration for driving multiple-phase motors, or used in applications that require half-bridge power circuits. The IXBD4410/IXBD4411 is a full-feature chipset consisting of tow 16-pin DIP or SO devices interfaced and isolated by tow small-signal ferrite pulse transformers. The IXBD4412/IXBD4413 is a basic, low-cost chipset consisting of two 8-pin DIP devices interfaced and isolated by a single pulse transformer. The small-signal transformers in both chipsets provide greater than 1200V isolation.

Even with commutating noise ambients greater than ±50V/nsec and up to 1200V potentials, these chipsets establish error-free two-way communications between the system ground-reference IXBD4410/IXBD4412 and the inverter output-reference IXBD4411/IXBD4413. They incorporate undervoltage Vdd or Vee lockout, and overcurrent or desaturation shutdown to protect the IGBT or power MOSFET drvices from damage.

Both chipsets provide the necessary gate drive signals to fully control the grounded-source low-side power device, as well as the floating-source high-side power device. Additionally, the IXBD4410/4411 chipset provides a negative-going, off-state gate drive signal for improved turn-off of IGBTs, or power MOSFETs, and a system logic-compatible status fault output, $\overline{FLT}$, to indicate overcurrent or desaturation, and undervoltage Vdd or Vee. During a status fault, both chipsets keep their respective gate drive outputs off; at Vee for the IXBD4410/4411 and at 0V for the IXBD4412/4413.

Datasheet Archive





IXYS0071

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ORDERING INFORMATION

Part Number	Description	Package	Temperature Range	
IXBD4410PI	Full-Feature Low-Side Driver	16-PIN PDIP	IND	-40 to +85°C
IXBD4410SI	Full-Feature Low-Side Driver	16-PIN SO	IND	-40 to +85°C
IXBD4411PI	Full-Feature High-Side Driver	16-PIN PDIP	IND	-40 to +85°C
IXBD4411SI	Full-Feature High-Side Driver	16-PIN SO	IND	-40 to +85°C
IXBD4412PI	Basic Low-Side Driver	8-PIN PDIP	IND	-40 to +85°C
IXBD4413PI	Basic High-Side Driver	8-PIN PDIP	IND	-40 to +85°C
IXBD4410KIT	Full-Feature Chipset Eval. Kit	PCB	COM	0 to +70°C
IXBD4412KIT	Basic Chipset Evaluation Kit	PCB	COM	0 to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IXBD4412/IXBD4413)	Vdd - GND	-0.5V to +24V
(IXBD4410/IXBD4411)	Vdd - Vee	-0.5V to +24V
Input Voltage (INH, INL)	Vin	-0.5V to Vdd +0.5V
Input Current (INL, INH, Im)	Iin	± 10mA
Peak Reverse Output Current (OUT)	Io (rev)	+2A
Maximum Power Dissipation	Pd	600mW
Operating Ambient Temperature Version	Ta	-40°C to +85°C
Maximum Junction Temperature	Tj	+150°C
Storage Temperature Range	TSTG	-55°C to +150°C
Lead Soldering Temperature	Tl(sldr)	+300°C for 10sec

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (IXBD4412/IXBD4413)	Vdd - GND	+10V to +20V
(IXBD4410/IXBD4411)	Vdd - Vee	+10V to +20V
	Vdd - LG	+10V to +16.5V
Maximum Common Mode dv/dt	LGh - LGl	±50V/nsec

D.C. ELECTRICAL CHARACTERISTICS (Ta=25°C, Vdd=15V, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INL, INH Inputs (referred to LG):						
Vt+	Positive-Going Threshold		3.5			V
Vt-	Negative-Going Threshold				1.0	V
Vih	Input Hysteresis			1.0		V
Iin	Input Leakage Current	Vin=Vdd or LG	-1		1	µA
Cin	Input Capacitance			10		pF
Open Drain Fault Output (referred to LG for IXBD4410/4411):						
Voh	HI Output	R pu=10KΩ to Vdd	Vdd-.05			V
Vol	LO Output	Io=4.0mA		.3	.5	V
OUT Output (referred to LG):						
Voh	HI Output	Io=-10mA	Vdd-.05			V
Vol	LO Output	Io=10mA		Vee+.05		V
Ro	Output HI Res.	Io=-1A		3	5	Ω
Ro	Output LO Res.	Io=1A		3	4	Ω
Ipk	Peak Output Current	CL=10nF	1.5	2.0		A
Im Input (referred to KG for IXBD4410/4411 and to LG for IXBD4412/4413):						
Vt+	Positive-Going Threshold		.24	.3	.45	V
Cin	Input Capacitance			10		pF
Rs	Shorting Device Output Resistance		50	75	100	Ω
Vee Supply (referred to LG for IXBD4410/4411):						
Vee	Output Voltage	Io=1mA Co=1µF	-5	-6.5	-7.5	V
Iout	Output Current	Vout=.85xVee	-20	-25		mA
Finv	Inverting Frequency			600		KHz
Veef	Undervoltage Fault Indication		-3.0	-3.0	-4.8	V
Vdd Undervoltage Lockout:						
Vuv	Drop Out		9.5	10.5	11.5	V
Vuh	Hysteresis		.1	.15	.3	V
Quiescent Power Supply Current:						
Idd	Vdd Current	Vin = Vdd or LG Io = 0			20	mA

A.C. ELECTRICAL CHARACTERISTICS (Ta=25°C, Vdd=15V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INL and INH Inputs:						
$t_{d(on)}$	Turn-On Delay (IXBD4410/4412)	CL=1nF		110	175	ns
t_r	Rise Time	CL=10nF		70	100	ns
		CL=1nF		15	20	ns
$t_{d(off)}$	Turn-Off Delay (IXBD4410/4412)	CL=1nF		70	150	ns
tr	Fall Time	CL=10nF		70	150	ns
		CL=1nF		15	20	ns
$t_{d(off)}$	IXBD4410/4412 Turn-on vs. IXBD4410/4413 Turn-off Delay	CL=1nF		60	150	ns
$t_{d(on)}$	IXBD4410/4412 Turn-on vs. IXBD4410/4413 Turn-off Delay	CL=1nF		60	150	ns
Fault Output Delay for any Fault Conditions (IXBD4410/4411):						
t_{FLT}	$\overline{FLT}$ Delay	Rpu=2KΩ, CL=20pf		200	300	ns
Overcurrent Protection Delay:						
t_{oc}	Driver-Off Delay	CL=1 nF		200	300	ns

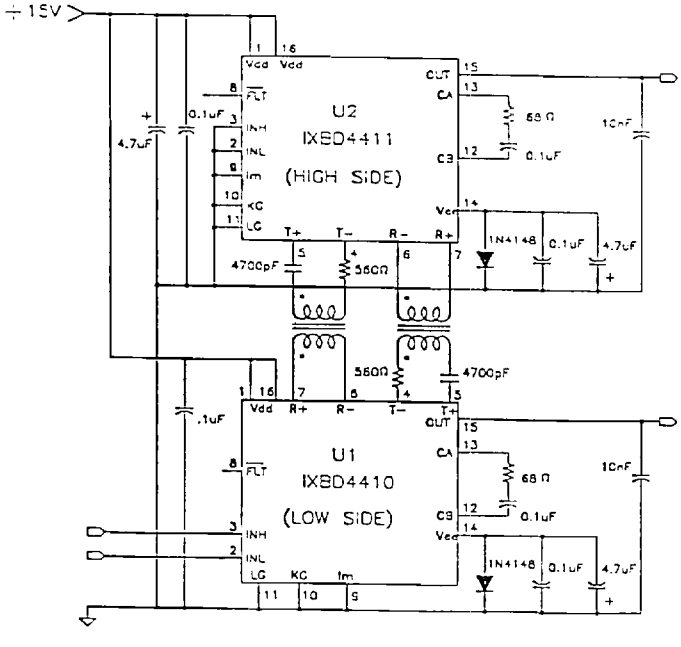


Fig. 1A: IXBD4410/4411 Switching Time Test Circuit

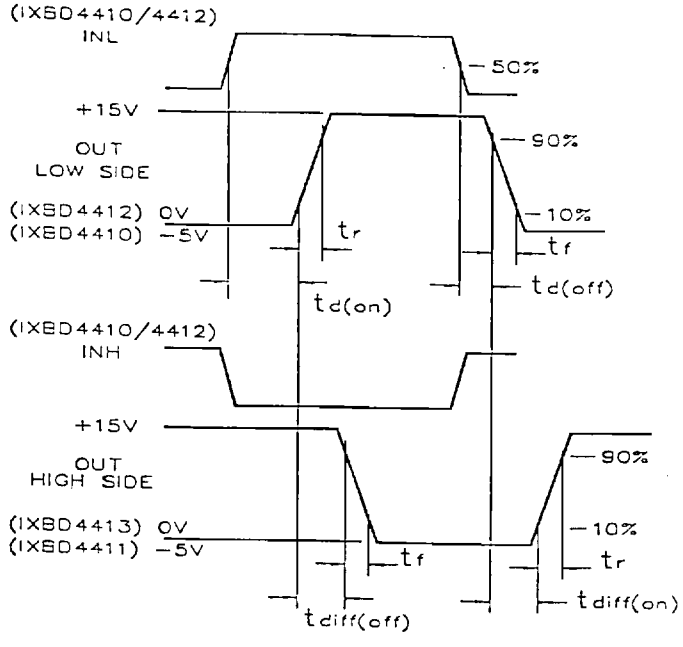
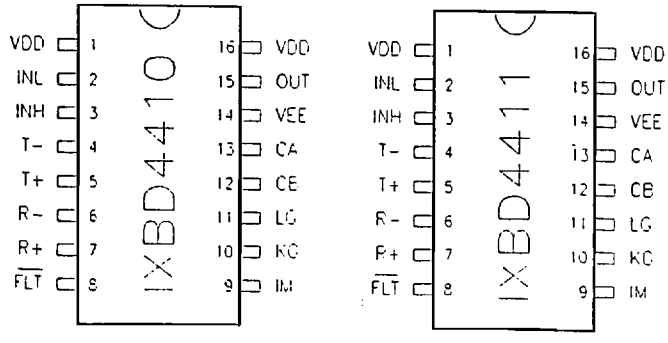


Fig. 1B: Output Signal Waveform

IXBD4410/IXBD4411 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
VDD	1 16	VDD Positive power supply.
INL	2	Logic input signal referenced to LG (logic ground). In the IXBD4410, A "high" to this pin turns on its gate drive output and resets its fault logic. A "low" to this pin turns off the gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG).
INH	3	Logic input signal referenced to LG (logic ground). In the IXBD4410, this signal is transmitted to the IXBD4411 "high-side" driver through pins 4 and 5 (T- and T+). A "high" to this pin turns on the IXBD4411 gate drive output and resets its fault logic. A "low" to this pin turns off the IXBD4411 gate drive output. In the IXBD4411 this pin is not used and should be connected to its ground (LG).
T- T+	4 5	Transmitter output complementary drive signals. Direct drive of the low signal transformer, which is connected to the receiver of the chipset's companion device. In the IXBD4410, this signal transmits the on/off command to its companion IXBD4411. In the IXBD4411, this signal transmits the fault indication to its companion IXBD4410 driver.
R- R+	6 7	Receiver input complementary signal. Directly connected to the low signal transformer, which is driven by the chipset's companion device. In the IXBD4410, this input receives the fault indication from its companion IXBD4411 driver. In the IXBD4411, this input receives the on/off command from its companion IXBD4410 driver.
$\overline{FLT}$	8	Low/high side fault output. In the IXBD4410, this output indicates a fault condition of either device of the chipset. A "high" indicates no fault, A "low" indicates that either overcurrent, VDD or VEE under-voltage occurred. In case of over current, this output will remain active "low" until the next input cycle of the respective driver. In case of under-voltage, this output will remain "low" until the proper voltage is restored. The IXBD4411 does not have a $\overline{FLT}$ output, and its pin 8 should be tied to LG.
IM	9	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 70Ω resistor. Any voltage at this pin above the threshold of .3V typical, will turn the output (pin 15) off. This pin is used for power device overcurrent protection.
KG	10	Kelvin ground. This ground is used as Kelvin connection for overcurrent or desaturation sensing.
LG	11	Logic and power ground.
CB CA	12 13	Capacitor terminals for negative charge pump (VEE); "+" terminal is CB (pin 12).
VEE	14	Negative supply terminal.
OUT	15	Gate drive output. In the IXBD4410 this output responds to the INL signal. A "high" at INL will turn it on ("high"), a "low" will turn it off ("low"). In the IXBD4411, this output responds to the transmitted signal from the companion IXBD4410. A "high" at INH of the IXBD4410drives will turn it on ("high"). A "low" will turn it off ("low"). This output will turn off ("low") also in response to any fault condition.

Pin Configuration



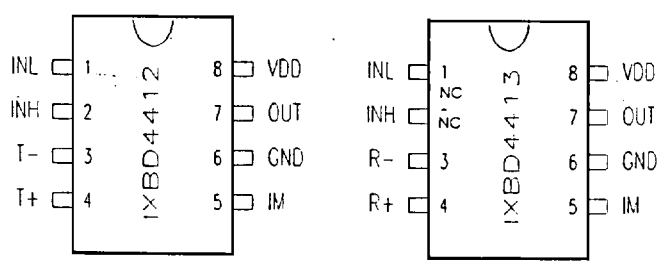
IXBD4412 (Low-Side Driver) PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
INL	1	Logic input signal referenced to GND. A "high" to this pin turns on the gate drive output and resets the fault logic. A "low" to this pin turns off the gate drive output.
INH	2	Logic input signal referenced to GND. A "high" to this pin is transmitted to the "high-side" driver (IXBD4413), turns on the "high-side" gate drive output and resets its fault logic. A "low" to this pin is transmitted to the "high-side" driver (IXBD4413) and turns off its gate drive output.
T-	3	Transmitter output complementary signal. Direct drive of the low signal transformer, which is connected to the receiver of the companion IXBD4413 "high-side" driver. This signal transmits the on/off command to the companion driver.
T+	4	
IM	5	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 50Ω resistor. Any voltage at this pin, above the threshold of .3V typical, will turn the output (pin 7) off. This pin is used for power device over-current protection.
GND	6	Logic and power ground.
OUT	7	Gate drive output. This output responds to the INL signal. A "high" at INL will turn it on ("high"), A "low" will turn it off ("low"). Any fault condition will also turn this output off ("low").
VDD	8	Positive power supply.

IXBD4413 (High-Side Driver) PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
INL	1	Not used. Connect to GND (pin 6).
INH	2	Not used. Connect to GND (pin 6).
R-	3	Receiver input complementary signal. Directly connected to the low signal transformer, which is driven by the companion IXBD4412 "low-side" driver. This input receives the on/off command from its companion "low-side" IXBD4412 driver.
R+	4	
IM	5	Current sense or desaturation detection input. This input is active only while the OUT pin is "high" (on). When the OUT pin is "low" (off) this input is pulled to ground through a 50Ω resistor. Any voltage at this pin, above the threshold of .3V typical, will turn the output (pin 7) off. This pin is used for power device overcurrent protection.
GND	6	Logic and power ground.
OUT	7	Gate drive output. This output responds to the transmitted signal from the companion IXBD4412 "low-side" driver. A "high" at INH of the "low-side" driver (IXBD4412) will turn this output on ("high"), A "low" will turn off ("low"). Any fault condition will also turn this output off ("low").
VDD	8	Positive power supply.

Pin Configuration



Chipset Overview

The ISOSMART™ chipsets are pairs of integrated circuits providing isolated high- and low-side drivers for phaseleg motor control, or any other application which utilizes a half bridge, 2- or 3-phase drive configuration. They consist of two drive control inputs (INL and INH) for two power-MOSFET/IGBT gate-drive outputs. Both inputs operate from a common ground, and are activated by HCMOS compatible logic levels. The low-side output operates near input ground, while the high-side output operates from a floating ground that is nominally the source connection of the high-side phaseleg power device. Both outputs typically provide 2 Amperes of transient current drive for fast switching of the phaseleg power device.

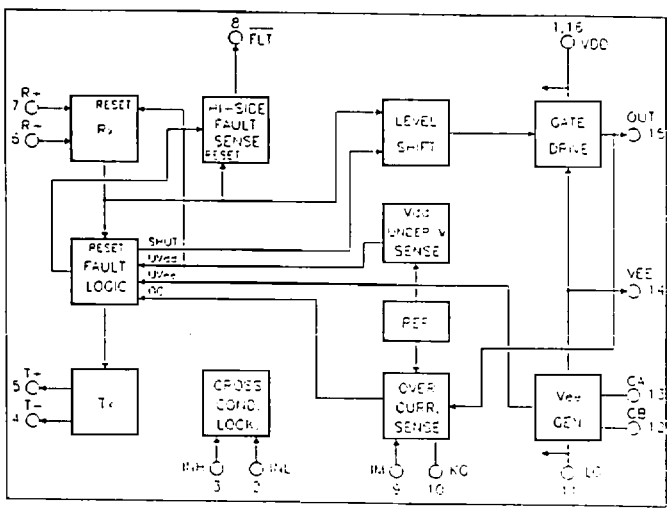


Figure 2: IXBD4411, high-side driver block diagram

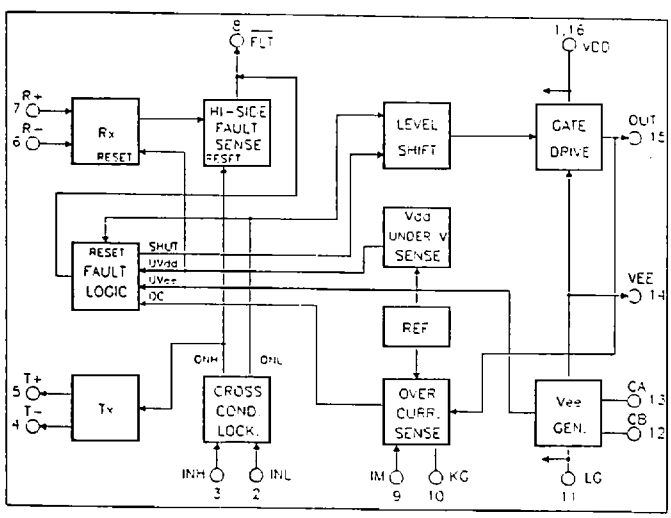


Figure 3: IXBD4410, low-side driver block diagram

The full featured ISOSMART™ driver chipset incorporates a IXBD4410 as the low-side driver and a IXBD4411 as the high-side driver. When input "INL" is set to a positive logic level, the low-side gate output goes high (turns on); when "INH" is set to a positive logic level, the high-side gate drive output goes high. The high-side IC is isolated from the low-side IC by a magnetic barrier, across which the turn on/off signal is transmitted to the high-side gate drive. In the case of the IXBD4410/4411 chipset, the IXBD4411 fault signal is also transmitted back to the IXBD4410 driver. This isolation only depends on the low cost communications transformer, which is designed to withstand 1200V or more.

There are two magnetic transmission channels between the low- and high-side IC's for bi-directional communication (IXBD4410/4411). One sends a signal from the low-side IXBD4410 IC up to the high-side IXBD4411 IC, and the other sends a signal back from the high-side to the low-side IC. The signal that is sent up controls the IXBD4411 gate-drive output. The signal sent from the IXBD4411 back to the IXBD4410 indicates a high-side fault has occurred (overcurrent, or under-voltage of the high-side ±power supplies). This is detected at the IXBD4410 driver and sets "$\overline{\text{FLT}}$" pin low, to indicate the high-side fault.

The fault signal that is returned from the IXBD4411 is strictly for status; any gate-drive shutdown because of a high-side fault is done barely within the high-side IXBD4411, and does not depend on the integrity or presence of the magnetic transmission medium. The IXBD4411 gate-drive will turn-off the power device whenever an overcurrent or under voltage condition arises. The overcurrent sensing is active only while the gate driver output is "high" (on). The overcurrent fault condition is latched and is reset on the next INH gate input positive transition. The $\overline{\text{FLT}}$ (pin 8) of the IXBD4411 is not used and should be grounded.

The low-side IXBD4410 driver provides an output pin 8 ($\overline{\text{FLT}}$) to indicate that a high-side (IXBD4411) or a low-side (IXBD4410) fault. This output pin is an "open-drain" output. The IXBD4410 low-side driver fault indications are similar to the IXBD4411 high-side driver indications as outlined above. A "graphic" logic diagram of the chipset's $\overline{\text{FLT}}$ function is presented in Figure 4. Note that this diagram presents the logic of this function at the "low-side" IXBD4410 driver and is not the actual circuit. It describes the combined logic of the "fault logic" and "hi-side fault sense" blocks in both the IXBD4410 and IXBD4411 as shown in Figures 2 and 3.

The basic, lower cost ISOSMART™ chipset consists of a pair of 8 pin DIP ICs: IXBD4412 (low-side driver) and the IXBD4413 (high-side driver). It operates similarly to the IXBD4410/4411 pair, but does not include the negative drive or the fault indications option. This pair requires only a single magentic isolated transmission channel.

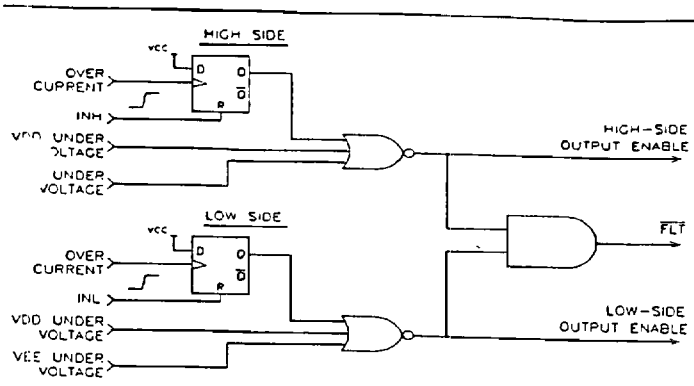


Figure 4: Logic representation of IXBD4410 FLT signal

The most efficient method of providing power for the high-side driver is by bootstrapping. This method is illustrated in the functional drawing on page one and in the application example (Figure 8 and 9) by diode D1 and capacitor C1. Using this method, the power is drawn through a high-voltage diode onto a reservoir capacitor whenever the floating high-side ground returns to near the real ground of the low-side driver; when the high-side gate is turned on, and the floating ground moves towards a higher potential, the bootstrapping diode back-biases, and the high-side driver draws its power solely from the reservoir capacitor. Power may also be provided via any isolated power supply (usually an extra secondary on the system housekeeping supply switching transformer).

E . the IXBD4410 and IXBD4411 contain on-board negative charge pumps to provide negative gate drive, which ensures turn-off of the high- or low-side power device in the presence of currents induced by power device Miller capacitance or from inductive ground transients. These charge pumps provide -5V relative to the local driver ground when Vdd is at +15V, and at rated average currents of 25mA. The charge pump requires two external capacitors (C7 & C11 in Figure 8). The charge pump frequency is nominally 600KHz. The charge pump clock is turned off whenever the difference between the Vdd and Vee supplies exceed 20V, to prevent exceeding the breakdown rating of the IC.

Both the IXBD4410 and IXBD4411 drivers possess two local grounds each, a common logic ground, and "Kelvin" ground. The Kelvin ground and logic grounds are first connected directly to each other, and then to the Kelvin-source of the power device for accurate over-current measurement in the presence of inductive transients on the power device source terminal.

Power MOSFET or IGBT overcurrent sensing utilizes an on -chip comparator with a typical 300mV threshold. In a typical application, the current mirror pin of the power MOSFET or IGBT is connected to a grounded, low-value resistor, and to the overcurrent comparator input on the high- or low-side driver. The comparator will respond typically within 150ns to an overcurrent condition to shutdown the driver output. The power switches could be protected also by desaturation detection (see Figures 6,8 &9).

To assure maximum protection for the phaseleg power devices, the chipset incorporates the following power MOSFET and IGBT protection circuits:

- Power device overcurrent or desaturation protection. The IXBD4410/4411/4412/4413 will turn off the driven device within 150ns of sensing an output overcurrent, or desaturation condition.

- Gate-drive lockout circuitry to prevent cross conduction (simultaneous conduction of the low- and high-side phaseleg power devices), either under normal operating conditions or when a fault occurs.

- During power-up, the chipset's gate-drive outputs will be low (off), until the voltage reaches the under-voltage trip point.

- Under-voltage gate-drive lockout on the low- and/or high-side driver whenever the respective positive power supply falls below 9.5V typically.

- Under-voltage gate-drive lockout on the low- and high-side driver whenever the respective negative power supply rises above -3V typically (IXBD4410/4411).

Application Information

- 1-, 2- or 3-Phase Motor Control
- Switched Mode Power Supplies
- 1-, or 3-Phase UPS Systems
- Induction Heating and Welding
- Switching Amplifiers
- General power Conversion Circuits

Introduction

The IXBD4410/4411/4412/4413 chipset devices are specifically designed as MOS-gated transistor drivers in half-bridge power converters, 1-, 2- and 3-phase motor controls, and UPS applications. The phaseleg PWM command is normally generated by previous (user provided) circuitry. It must be decomposed into two separate logic signals, one for the high-side and one for the low-side power transistors, with appropriate deadtime for each state transition. The deadtime insures non-overlapping conduction even if the turn-on and turn-off delay times of the power devices are unequal. The minimum deadtime should be greater than

t_{dth}. A separate circuit, or an IC device like IXYS' IXDP630 deadtime generator, can be used to perform this function. The ISOSMART™ chipset family of devices do not generate deadtime, although there is an internal lockout that prohibits one device form being commanded "on" before the other is commanded "off". This simplifies start-up and shutdown protection circuitry, preventing logic error during power-up from turning on both high-and low-side transistors simultaneously.

Negative VEE Charge Pump Circuit Design

The on-chip Vee generator provided in the IXBD4410/4411 generates a negative power supply, regulated at 20 Volts below the positive Vdd rail. (Note: this circuit is not present in the lower-cost IXBD4412/4413 chipset). If Vdd is +10V, Vee will be -10V. If Vdd is +15V, Vee will be -5V. This negative drive potential in the off-state is either desirable or required in many instances. When switching a clamped inductive load (Figure 5), the turn-on of Q2 will commutate the freewheeling diode around Q1. Whether this diode is intrinsic (as in a MOSFET) or extrinsic (IGBT or bipolar), its reverse recovery is critical to proper circuit operation.

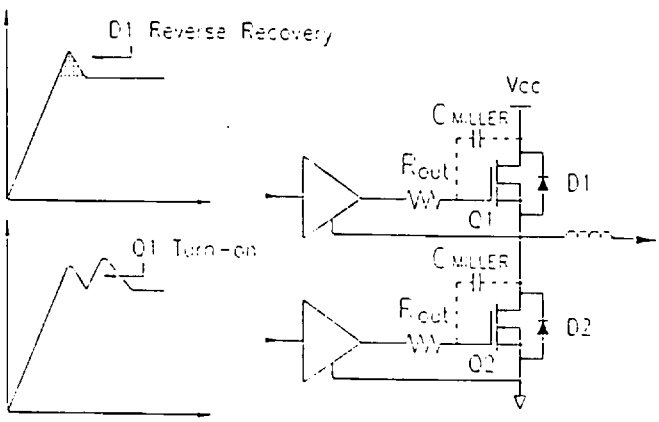


Figure 5: Switching a clamped inductive load

At high turn-on di/dt in Q2, and near its rated voltage, the recovery of D1 can get quite "snappy" (the di/dt in the second half of the recovery process, after the diode has begun to recover its blocking capability, can get very large), creating a very high dv/dt across Q1. This dv/dt is impressed across the Miller capacitance of Q1, forcing a large current to flow out the gate terminal of the device, If this current pulse causes a high enough voltage drop across the output impedance of the gate drive circuit, Rout, Q1 will be turned on.

The Q1 conduction in every instance Q2 is turned on (and Vice Versa), aside from degrading efficiency, can lead to catastrophic failure of both power transistors. At high temperature, where the -6 to -7 mV/°C tempco of IGBT/MOSFET threshold reduces the voltage required to create a failure, this problem is even more likely to occur. In an industrial module package (e.g.: a 150 A 1200V IGBT phaseleg module), the series inductance contributed by the long gate leads and connectors further complicate the design.

In a heavily snubbered converter, or in a power supply design with low transformer leakage inductance, the design problem is relatively simple and negative drive is seldom required. In these applications, the IXBD4412/4413 is adequate. However, in a modern snubberless or lightly snubbered converter design, it is important to keep the gate drive impedance high enough during transistor turnoff to limit the reapplied dV/dt (the transistor is its own 'active' snubber). This is always important for EMI control, and in the case of IGBTs may be required to achieve the necessary RBSOA. At the same time, it is mandatory to keep the off-state gate drive impedance very low to assure the transistor remain off during induced dV/dt (including diode recovery (dV/dt). In some instances, it is simply not possible to satisfy both criteria with 0V applied in the off-state. In these cases. the IXBD4410/4411 with Vee negative bias generator must be used.

The internal Vee generator is a charge pump circuit. Referring to Figure 8, an external charge pump capacitor is required between the CA and CB terminals (C7, C11), and an output reservoir capacitor between Vee and GND (C10, C14). A 0.1µF charge pump capacitor (C7, C11) is recommended. The voltage regulation method used in the IXBD4410/4411 allows a 1 to 2V ripple frequency depends on the size of the Vee output reservoir capacitor (C10,C14) and the average load current. The minimum recommended output reservoir (C10, C14) is 4.7µF tantalum, or 10µF if aluminum electrolytic construction is chosen. Note that this reservoir capacitor is in addition to a good quality high frequency bypass capacitor (0.1µF) that should be placed from VEE to GND (C9, C13).

A small resistor in series with the charge pump capacitor, (R7, R8) reduces the peak charging currents of the charge pump. A value or 68Ω or greater is recommended, as illustrated in the applications example in Figure 8.

Current Sense / Desaturation Detection Circuit

All members of the ISOSMART™ driver family provide a very flexible overcurrent / short circuit protection capability that works with both standard three-terminal power transistors, and with 4- and 5-terminal current sensing power devices like the IXYS MirrorFET™. Overcurrent detection is accomplished as illustrated in Figure 6A (for a current mirror power device) and Figure 6B (for a standard three terminal power transistor). Desaturation detection is accomplished with the same internal circuits by measuring the

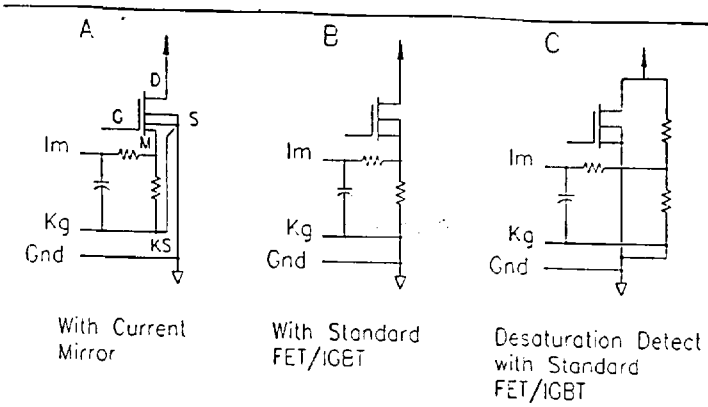


Figure 6: Alternative Overcurrent Protection Circuits

voltage across the power transistor in the on-state with an external resistor divider (Figure 6C).

The IM input trip point V_{TIM}, typically 300 mV, is referenced to the Kelvin ground pin KG.

Current mirror MOSFETs and IGBTs allow good control of peak let-thru currents and excellent short circuit protection when combined with the ISOSMART™ driver family of devices. The sense resistor is chosen to develop 300 mV at the desired peak transistor current, assuming a mirror ration of1400:1, and a trip point of 30A is desired:

$$Rsense = (300mV)/(1400/30A) = 14\Omega$$
$$(use\ 15\Omega\ CC).$$

It is important to realize that C_{oss} per unit area of the mirror cell is much larger that C_{oss} per unit area of the bulk of the die (due to periphery effects). This causes a large transient current pulse at the mirror output whenever the transistor switches (CdV/dt currents), which can cause false overcurrent trigger. The RC filter indicated in Figure 6A will eliminate this problem.

Standard three-terminal MOSFET and IGBT devices (in discrete as well as modern industrial single transistor and phaseleg modules) can also be protected from short circuit with the ISOSMART™ driver family devices. In discrete device designs, where the source/emitter terminal is available, overcurrent protection with an external power resistor can be implemented. The resistor is placed in series with the device emitter, with the full device current flowing through it (Fig. 6B). The sense resistor is again selected to develop 300 mV at the desired peak transistor current, assuming a trip point of 30A is desired:

$$Rsense = (300mV)/(30A) = 10\ m\ \Omega$$
$$(use\ 10m\Omega,\ 10\Omega\ non\text{-}inductive\ current\ sense\ resistor.$$

It is important to recognize that "non-inductive" is a relative term, especially when applied to current sense resistor construction and characterization. There is always significant series inductance inserted with the sense resistor, and Ldl/dt voltage transients can cause false overcurrent trigger.

The RC filter indicated in Figure 6B will eliminate this problem. Choosing the RC pole at the current sense resistor RL zero should exactly compensate for series inductance. Because the exact value is not normally known (and can vary depending on PC layout and component lead dress) this is not normally a good idea. Usually, the RC time constant should be two to ten times longer than the suspected RL time constant.

Desaturation detection as in Figure 6C is probably the most common method of short circuit protection in use today. While not strictly an "overcurrent" detector, if the power transistor gain, and consequently short circuit let-thru current, is well controlled (as with modern MOSFETs and IGBTs) this methodology offers very effective protection.

Both the IXBD4410/4411 one-phase (half-bridge) circuits in Figure 8 and the IXBD4412/4413 circuit in Figure 9 uses desaturation detection. In Figure 8, the voltage across the two power MOS devices (or IGBTs) are monitored by two sets of voltage-divider networks, R10 and R11 for the high-side gate driver, and R13 and R14 for the low-side gate driver. The dividers are set to trip the IM input comparators when either power MOS device V_{DS} exceeds a reasonable value, perhaps 50V (usually a value of 10% of the nominal DC bus voltage works well). R10 or R13 are chosen to tolerate the applied steady state DC bus voltage at an acceptable power dissipation. Dielectric withstand capability, power handling, temperature rise, and PC board creep and strike spacings, must all be carefully considered in the design of the voltage-divider networks.

In the off-state, the voltage across the power MOS device may go as high as the DC bus potential. To keep this normal condition from setting the internal fault flip-flop of the IXBD4410 or the IXBD4411, an internal CMOS switch is turned on and placed across IM and KG pins shorting them together. This effectively discharges C8 or C12 in Figure 8 and maintains zero potential with respect to KG at IM.

When the command arrives to switch on the power MOS device, the CMOS switch shorting IM to KG is turned off. The driven power MOS device is switched on approximately 100ns to 1µs later, and with typical load conditions, its drain-to-source potential, V_{DS}, may take an additional 10µs of delay to collapse to the normal on-state voltage level. To prevent false triggering due to this, C8 or C12 in parallel combination with R10 and R11, or R13 and R14, delays the IM input signal. During this turn-on interval, the voltageacross C8 or C12 will rise until the power MOS device finally comes on and pulls the voltage across C8 or C12 back down. If the MOS device load circuit is shorted, its V_{DS} voltage cannot callapse at turn-on. In this case, the voltage across C8 or C12 rises rapidly until it reaches 300mV, tripping the fault

flip-flop and shutting down the driver output. At the same time, C8 or C12 must be kept small enough that the added delay does not slow down the detection of a short circuit event so much that the power MOS device fails before the driver realizes that it is in trouble. The desaturation detection circuit in Figure 9 functions identically to the one in Figure 8 as just described. Current limit or desaturation detection is latched, and reset on a cycle-by-cycle basis with the rising edge of the respective input command.

Three Phase Motor Control Example

Figure 7 is a block diagram of a typical 3-phase PWM voltage-source inverter motor control. The power circuit consists of six power switching transistors with freewheeling diodes around each of them. The control function may be performed digitally by a microprocessor, microcontroller, DSP chip, or user custom IC; or it may be performed by a PC board full of random logic and analog circuits. In any of these cases, the PWM command for all six power transistors is generated in one circuit, and this circuit is usually referred to system ground potential - the bottom terminal of the power bridge.

The ISOSMART™ family of drivers is the interface between the world of control logic and the world of power, 5V input logic commands precisely control actions at high voltage and current (1000V and 100A in a typical application). Figure 8 is a detailed schematic of one phase of three 3-phase motor control, showing the interconnection of the IXBD4410/4411 and its associated circuitry.

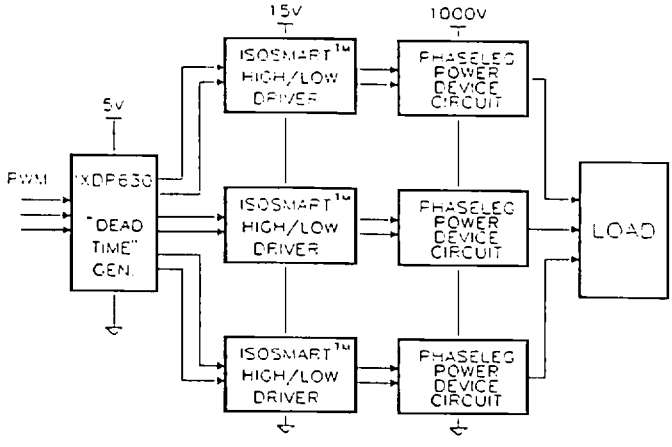


Figure 7: Typical 3-phase motor control system Block Diagram

This application utilizes the full feature set of the IXBD4410/4411 family of devices in a 460VAC line operated inverter. In situations that would not benefit from the negative gate drive, and do not require the fault status output, the IXBD4412/4413 chipset may prove adequate, Figure 9 is a complete schematic of one phase of a 3-phase inverter using the lower cost IXBD4412/4413 chipset. Notice the very large reduction in total parts count. With the smaller 8-pin packages of the devices themselves, the IXBD4412/4413 chip set offers a 70% reduction in PC board real estate for a modest reduction in feature set compared to the IXBD4410/4411 devices.

PCB Layout Considerations

The IXBD4410/4411/4412/4413 is intended to be used in high voltage, high speed, high dV/dt applications.

To ensure proper operation, great care must be taken in laying out the printed circuit board. The layout critical areas include the communication links, current sense, gate drive, and supply bypassing.

The communication path should be as short as possible. Added inductance disturbs the frequency response of the signal path, and these distortions may cause false triggering in the receiver. The transformer should be placed between the two ICs with the orientation of one IC reversed (Figure 10).

Capacitance between the high- and low-side should be minimized. No signal trace should run underneath the communication path, and high- and low-side traces should be separated on the PCB. The dV/dt of the high-side during power stage switching may cause false logic transitions in low-side circuits due to capacitive coupling.

The low signal pulse transformer provides the isolation between high-and low-side circuits. For 460 VAC line operation, a spacing of 4mm is recommended between low- and high-side circuits, and a transformer HIPOT specification of at least 1500 VACrms is required. This creep spacing is usually adequate to control leakage currents on the PCB with up to 1200 VDC applied after 10 to 15 years of accumulated dust and particulates in a standard industrial environment. In other environments, or at other line voltages, this spacing should be appropriately modified.

The current sense/desaturation detect input is noise sensitive. The 300 mV trip point is referred to the KG (Kelvin ground) pin, and the applied signal must be kept as clean as possible, A filter is recommended, preferably a monolithic ceramic capacitor placed as close to the IC as possible directly between IM and KG. To preserve maximum noise immunity, the KG pin should first be connected directly to the LG pin, and the pair then sent directly to the power transistor source/emitter terminal, or (if a desaturation detection circuit is used) to the bottom of the divider resistor chain.

All supply pins must be bypassed with a low impedance capacitor (preferably monolithic ceramic construction) with minimum lead length. The output driver stage draws 3A (typical) currents during transitions at dI/dt values in excess

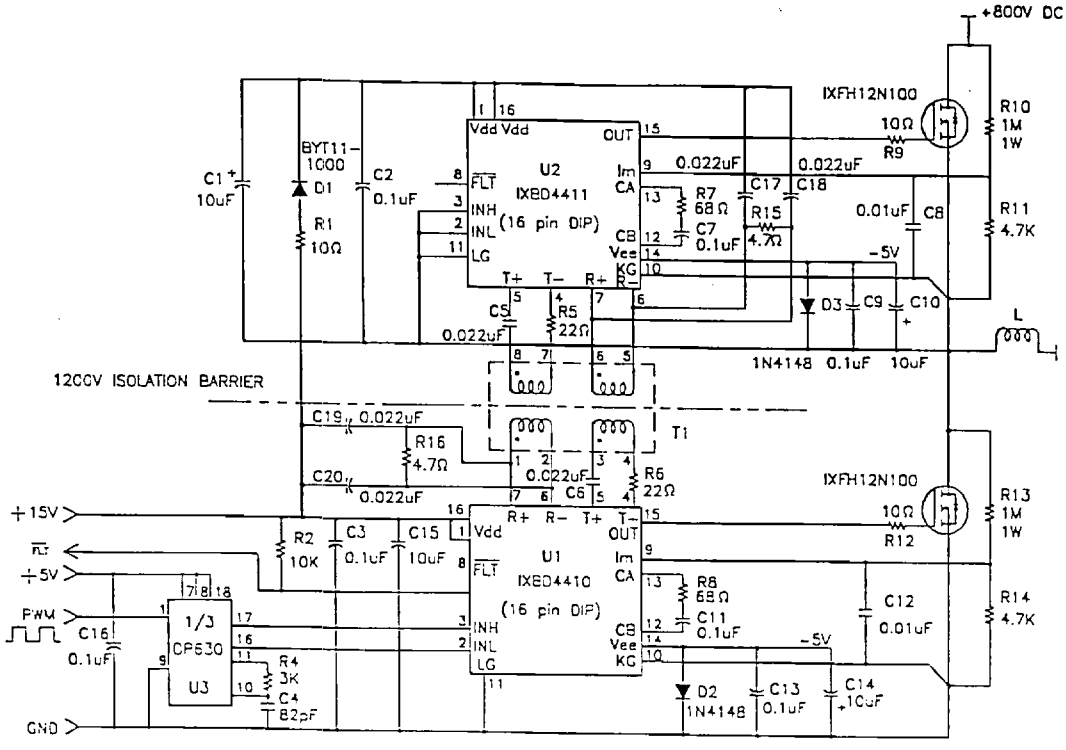


Figure 8: IXBD4410/4411 Detailed one phase circuit

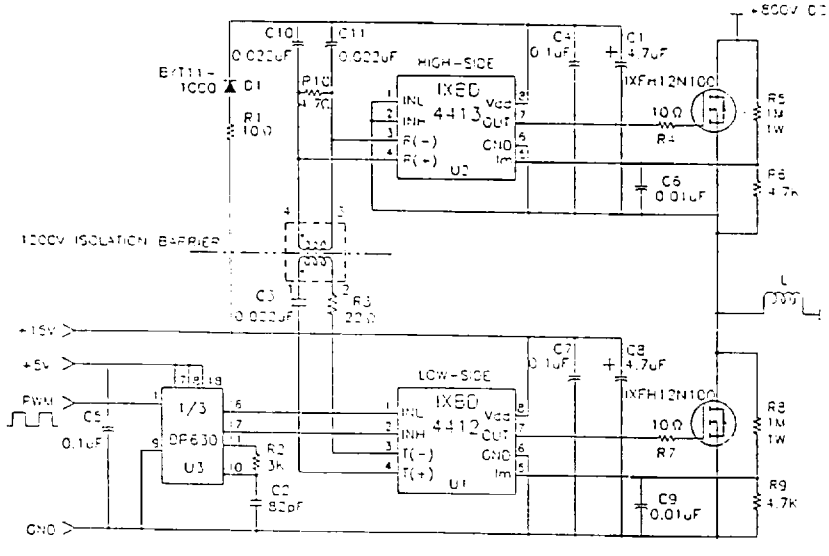


Figure 9: Lower cost IXBD4412/4413 single phase circuit

of 100A/µs. Supply line inductance will cause supply and ground bounce on the chip that can cause problems (logic oscillations and, in severe cases, possible latchup failure) without proper bypassing. These bypass elements are in addition to the reservoir capacitors required for the negative Vee supply and the high-side bootstrapped supply if these features are used.

Power Circuit Noise Considerations

In a typical transistor inverter, the output MOSFET may switch on or off with dI/dt >500A/µs. Referring to Figure 11 and assuming that the FET source terminal has a one inch path on the PCB to system ground, a voltage as high as V = 27nH• 500 A/µs = 13.5V can be developed. If the FET switched 25A, the transient will last as long as (25/500) µs or 50ns, which is more than the typical 6 or 7ns propagations or of a 74HC series gate.

Figure 11 illustrates an example layout problem. The power circuit consists of three power transistors (MOSFETs in this example). With the ISOSMART™ gate driver chipset grounded as in option (b), the communication path from the IXDP630 will operate without errors. The PC trace induced voltages are not common with the digital path, so the input of the gate driver will not see or respond to them.

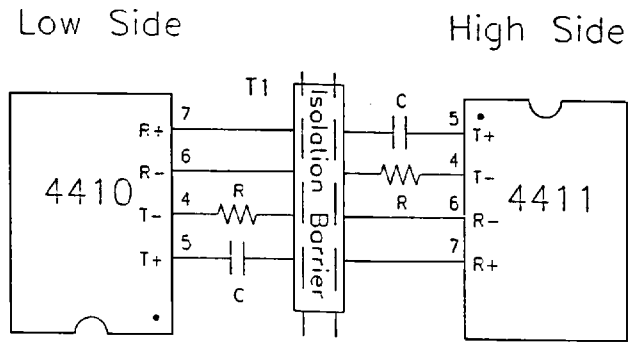


Figure 10: Suggested IC Orientation

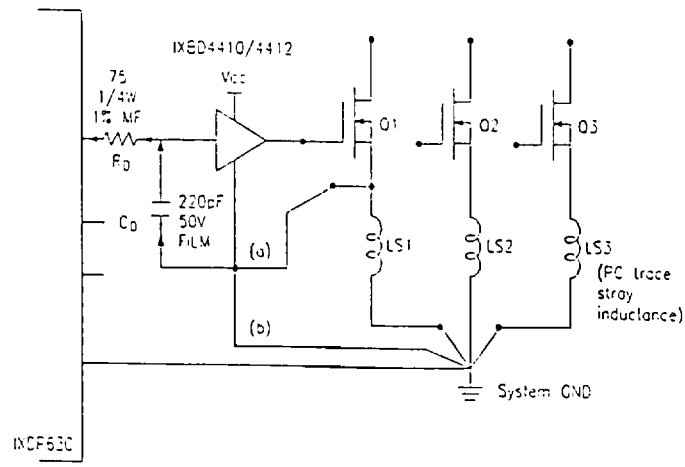


Figure 11: Potential layout problems that create functional problems

Unfortunately, the MOSFET will not operate properly. The voltage induced across LS1 when Q1 is turned on, acts as source degeneration, modifying the turn-on behavior of the FET. If LS1= 27nH, and Vcc is 15V (assuming the gate plateau of the FET is 6V), the di/dt at turn-on will be regulated by the driver/FET/LS1 loop to about 200 A/µs; quite a surprise when your circuit requires 500A/µs to operate correctly.

It is possible to make use of this behavior to create a turn-on or turn-off dI/dt limiter (perhaps to snub the upper free wheeling diode reverse recovery). While possible, this is normally not desirable or practical where two or more transistors are controlled. Equalizing the parasitic impedances of three traces while positioning the transistors next to their heat sink and meeting UL/VDE voltage spacings is just too difficult.

Grounding the gate driver as in option (a) solves the FET turn on problem by eliminating LS1 from the source feedback loop. Now, unfortunately, the gate driver will oscillate every time it is turned on or off. As the IXDP630 output goes "high", thegate drive output follows (after its propagation delay) and the FET starts to conduct. The voltage transient induced across LS1 (V=LS1· di/dt) raises the local ground (point a) until it exceeds Voh(630)-Vil(4410/4412) and the driver (after its propagation delay) turns the FET off. Now the FET current falls, V(LS1) drops, point (a) drops to system ground (or slightly below), and the driver detects a "1" at its input. After its propagation delay, it again turns the MOSFET on, continuing the oscillation for one more cycle.

To eliminate this problem, a ground level transformation circuit must be added, that rejects this common mode transient. The simplest is a de-coupling circuit, also illustrated in Figure 11. The capacitor voltage (on Cd) remains constant while the transient voltage is dropped across Rd and the driver detects no input transition, eliminating the oscillation. This circuit does add significantly to turn-on and turn-off delay time, and cannot be used if the transient lasts longer than the allowable delays. Delay times must be considered in selection of system dead time.

The most complex (and most effective) method of eliminating the effects of transients between grounds is isolation. Optocouplers and pulse transformers are the most commonly used isolation techniques, and work very well in this case. The IXDP630/631 has been specifically designed to directly drive a high speed optocoupler like the Hewlett Packard HCPL22XX family or the General Instrument 740L60XX optologic family. These optos are especially well suited to motor control and power conversion equipment due to their very high common mode dV/dt rejection capabilities.

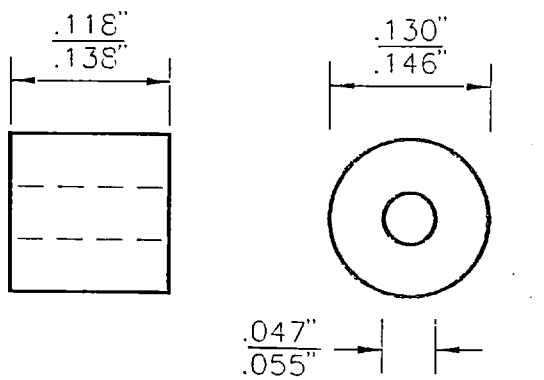


Figure 12: Ferrite bead dimensions

Transformer Considerations

The transformer is the communication link and isolation barrier between the high- and low-side ICs. The high-side gate and fault signals are transmitted through the transformer while maintaining the proper isolation. The transmitter signal is in the form of a square wave, but the receiver responds only to the logic edges. This allows for much smaller transformer designs, since a 10kHz switching frequency does not require a 10KHz pulse transformer.

The recommended transformer for this ISOSMART™ driver chipset is fabricated using a very small ferrite shield bead (see Figure 13), onto which a six-turn primary and a two-turn secondary winding of 36AWG magnet wire are made. The two windings are segment wound to achieve primary-to-secondary isolation of up to 2500VAC. The six-turn primaries are connected to the respective IXBD4410/4411 transmitter outputs and the two-turn secondaries are connected to their respective receiver inputs.

The nominal electrical specifications of the transformer are as follows:

- Open circuit inductance (100KHz; 20mV): 3µH
- Interwinding capacitance: 2.0pF
- Primary leakage inductance: 0.1µH
- Turns ratio: 6:2
- Primary-to-secondary isolation (1min): 1500VACrms
- Core permeability (µi): 125

The recommended ferrite bead is Fair Rite Products' part number 2661000101. It's approximate cost is 2 cents in large volumes and is manufactured by:

Fair-Rite Products Corp.
Wallkill, NY
Phone: (914) 895-2055

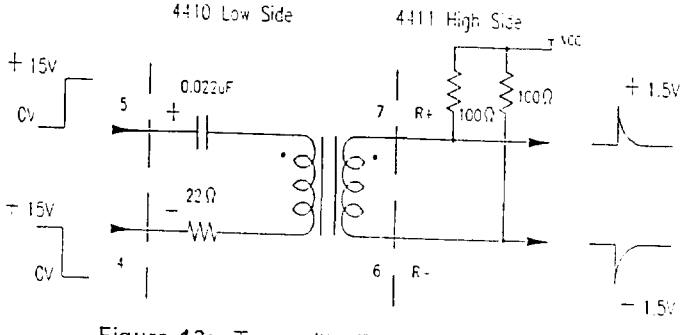


Figure 13: Transmitter/Receiver Waveforms

Several transformer manufacturers have produced custom transformers for the IXBD4410/4411 chip set, to the above specifications:

1) 12 pin DIP outline- *Part Number 500 - 1914*
BH Electronics
Buinsville, MN
Phone: (612) 894-9690

2) 8 pin DIP outline- *Part Number 23Z129*
Fil-Mag
San Diego, CA
Phone: (619) 569-6577

As seen in the application drawings (Figures 8, 9 and 13) a coupling capacitor (22nF) and a damping resistor (22Ω) are added in series with the primary side of the transformer. The capacitor will control the small amount of energy needed to transfer the signal to the companion driver. The resistor will control the damping of the signal and limit the peak transmitter output current. The receiver is designed to operate over a wide common mode input range. To reduce noise pickup, the receiver has ±250mV of input hysteresis.

If the signal is being distorted at the transmitter, the transmitter is probably running into current limit. A decrease in the coupling capacitance or an increase in the damping resistance should solve this problem. The receiver operates over a wide input range. The minimum amplitude for one side of the receiver is about 1 volt and a maximum of about 3 volts. It is critical that there be no overshoot on the transformer secondary waveform. Each signal should be slightly overdamped. If significant overshoot exists, the received signal may be logically inverted. An increase of the damping resistor will solve this problem.

Applications Hotline

For applications assistance, parts availability and the latest updates, please contact our Applications Hotline at (408) 982-4312 and ask for Sam Ochi or fax him at (408) 496-0670.

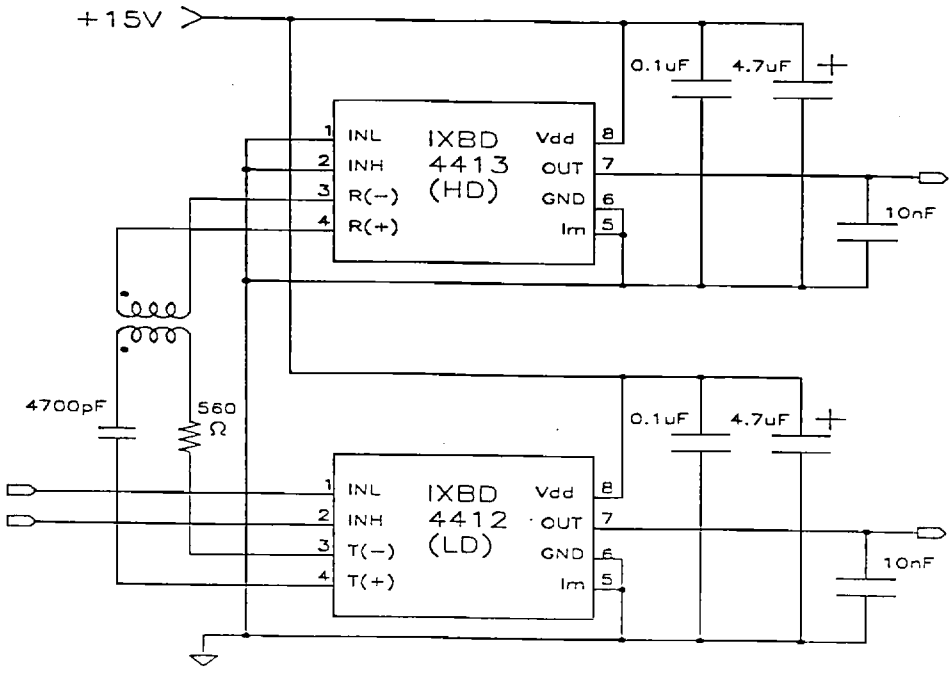
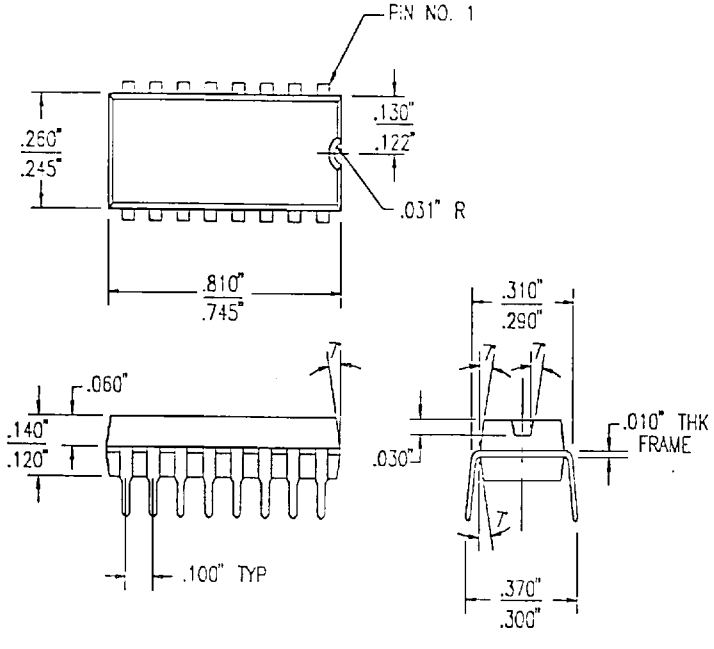
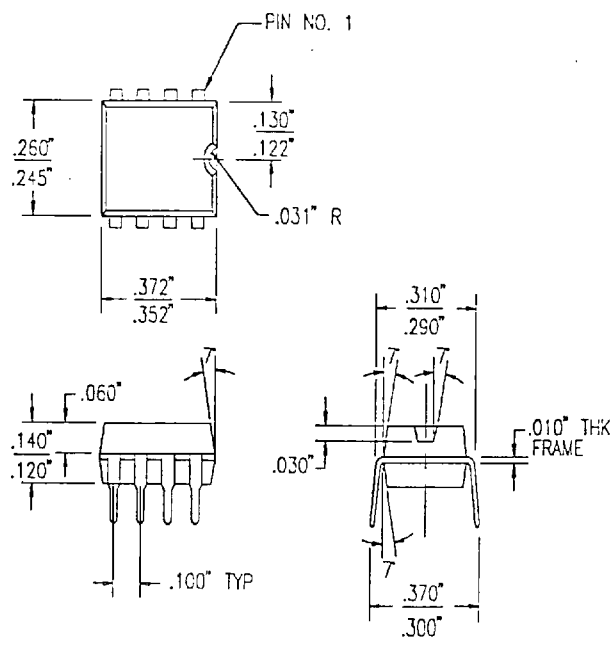


Figure 14: IXBD4412/4413 Switching Time Test Circuit

Package Outline

IXBD4410/4411



IXBD4412/4413