

CD40160B, CD40161B, CD40162B, CD40163B Types

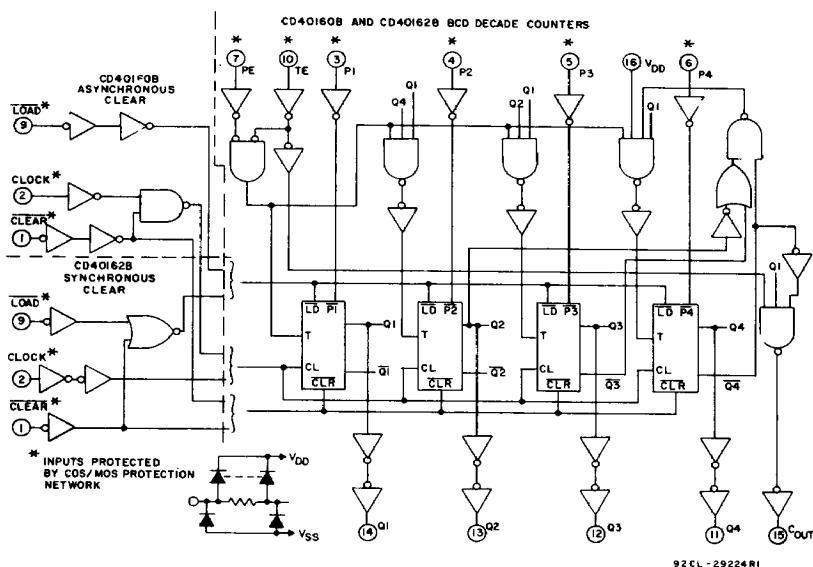


Fig. 3—Logic diagrams for CD40160B and CD40162B BCD decade counters.

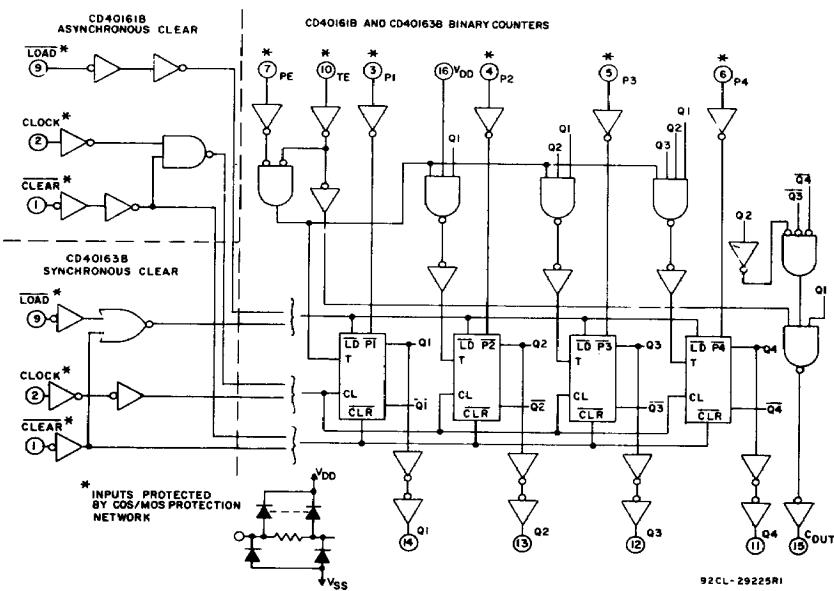


Fig. 4—Logic diagrams for CD40161B and CD40163B binary counters.

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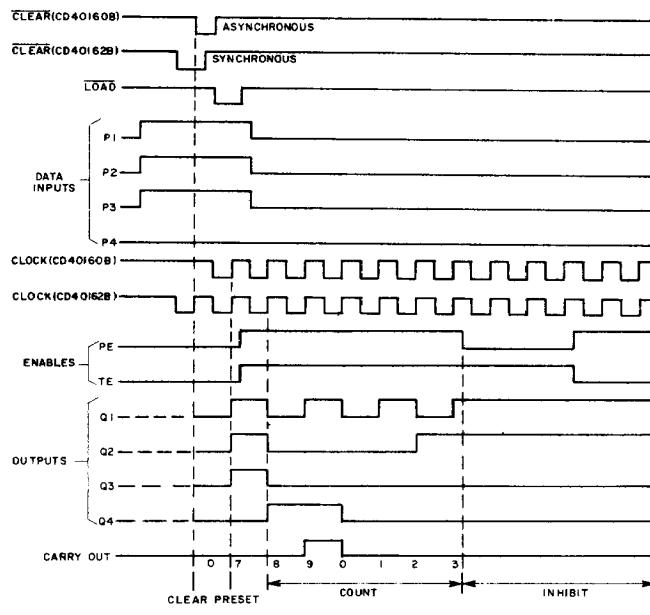


Fig. 14—Timing diagram for CD40160B, CD40162B.

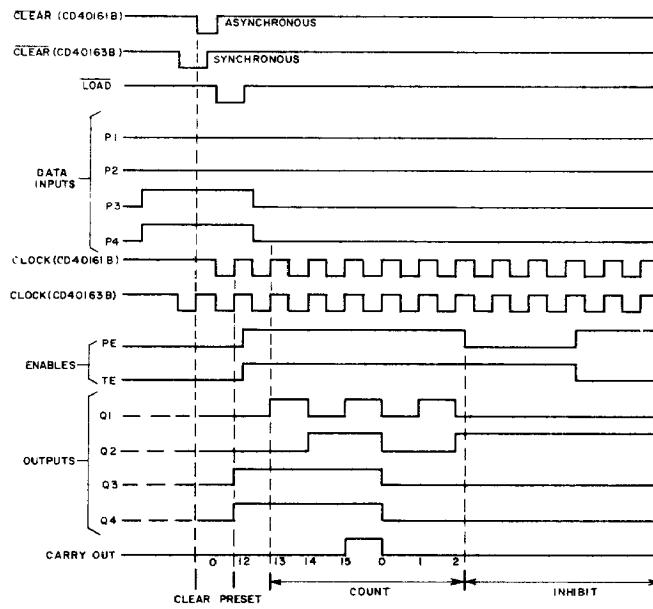


Fig. 15—Timing diagram for CD40161B, CD40163B.

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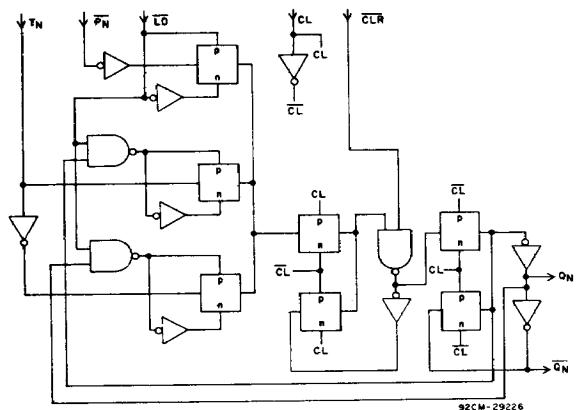


Fig. 16— Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).

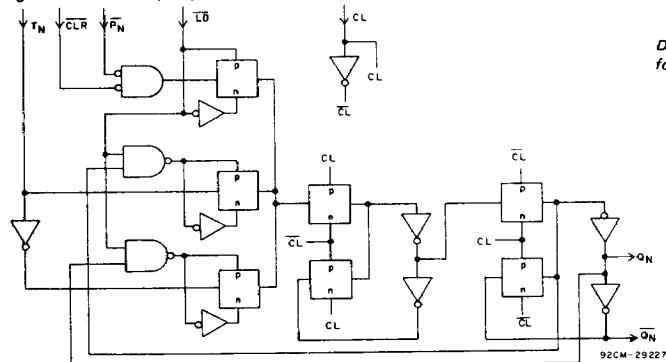
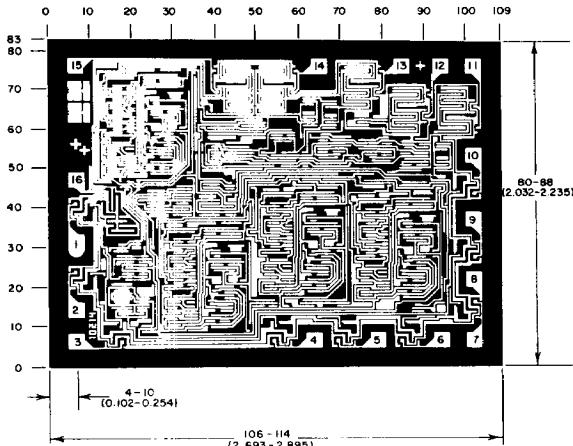


Fig. 17— Detail of flip-flops for CD40162B and CD40163B (synchronous clear).



Dimensions and pad layout for CD40160BH. Dimensions and pad layout for CD40161BH, CD40162BH, and CD40163BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

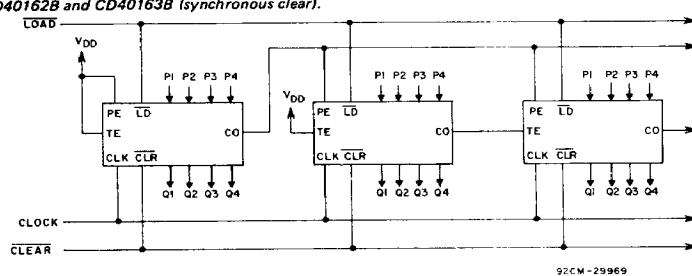


Fig. 18— Cascaded counter packages in the parallel-clocked mode.

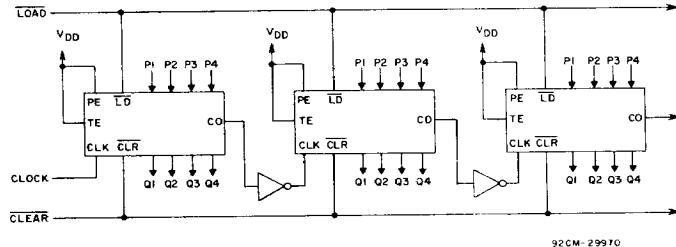


Fig. 19— Cascaded counter packages in the ripple-clocked mode.