# 88PG839

## Ultra Low Power, 2MHz, 2A Output Current Field Programmable Hysteretic Step-Down Switching Regulator



**Datasheet**

Microsoft Use Only

Doc. No. MV-S106081-02, Rev. D
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## Document Conventions

| | |
|---|---|
|  | **Note:** Provides related information or information of special importance. |
|  | **Caution:** Indicates potential damage to hardware or software, or loss of data. |
|  | **Warning:** Indicates a risk of personal injury. |

## Document Status

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| Doc Status: 2.00 | Technical Publication: 0.xx |

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# 88PG839

## Ultra Low Power, 2MHz, 2A Output Current Field Programmable Hysteretic Step-Down Switching Regulator

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## PRODUCT OVERVIEW

The Marvell® 88PG839 is a high performance, hysteretic step-down switching regulator that utilizes a proprietary, internally compensated Pulse Width Modulation (PWM) control to regulate the output voltage. The regulator offers fast transient response time and requires no external compensation. The device operates from an input voltage range of 2.7V to 5.5V and delivers up to 2A DC output current. The switching frequency is typically 2MHz, allowing the use of low profile surface mounted inductors and low value ceramic capacitors.

The step-down regulator includes programmable ability to easily set the output voltage with external resistors. The output voltage range is 0.64V to 3.63V. The output voltage can be changed On-the-Fly (OTF) from a nominal value by a percentage through connecting the OTF pin to a high level, making it ideal for portable applications. The adjustment percentage is user programmable from -20% to +10% by a resistor connected between PSET pin and ground.

The 88PG839 can be externally set to Pulse Frequency Modulation (PFM) or Pulse Width Modulation (PWM) mode via the PFM pin. The quiescent current in PFM mode is less than 32µA. The regulator can achieve 95% efficiency under loaded conditions.

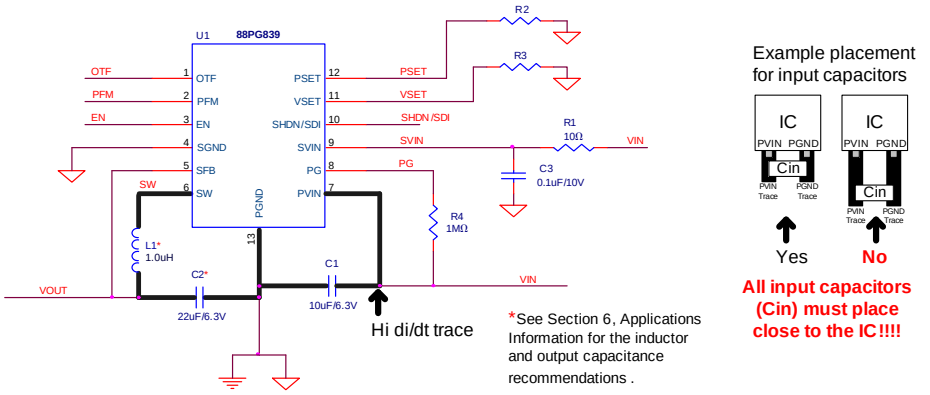
### Features

- Input voltage range 2.7V to 5.5V
- Output voltage range 0.64V to 3.63V
- Hysteretic step-down regulator
- 32µA (typical) quiescent current
- 3mm x 4mm DFN-12 package
- 2MHz switching frequency
- Small and low-profile inductors
- Stable with low-ESR ceramic output capacitor
- -20% to +10% On-the-Fly output voltage adjustment
- Internal compensation
- Up to 95% efficiency
- 2A DC output current
- 72 output voltage selections using AnyVoltage™ Technology
- Built-in under/over voltage lockout
- Thermal shutdown protection
- Soft start to minimize the in-rush current

### Applications

- Portable computing
- Personal Digital Assistant (PDA)
- Cell phones
- Ultra-Mobile PC (UMPC)

**Figure 1: Typical Application Circuit**




**Caution!** **This is a very high frequency device, and proper PCB layout is required. Refer to Section 6, Applications Information, on page 47 for further information.**

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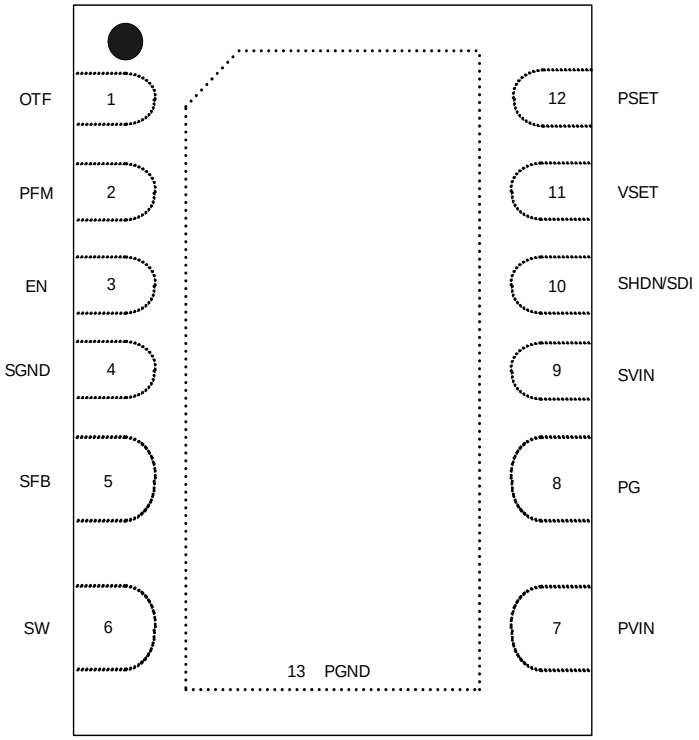
# 1 Signal Description

## 1.1 Pin Configuration

**Figure 2: DFN-12 Pin Configuration (Top View)**



## 1.2 Pin Description

**Table 1: Pin Types**

| Pin Type | Description |
|---|---|
| I | Input |
| O | Output |
| S | Supply |
| NC | Not Connected |
| GND | Ground |

**Table 2: Pin Description**

| Pin # | Pin Name | Pin Type | Pin Function |
|---|---|---|---|
| 1 | OTF | I | On-the-Fly<br>Logic input for dynamic output voltage change:<br>• Logic high sets the output voltage that is determined from the VSET and PSET resistors.<br>• Logic low sets the output voltage that is determined from the VSET resistor only.<br>• **Do not float this pin.** |
| 2 | PFM | I | Pulse Frequency Modulation<br>• Logic input to set the operation mode. Connect PFM to SVIN to select PFM mode under light load conditions and connect PFM to SGND to select forced PWM mode in light load condition. See Section 6, Applications Information for the inductor and output capacitance recommendations when operating and PFM and PWM mode.<br>• **Do not float this pin.** |
| 3 | EN | I | Enable<br>• Logic high enables the switching step-down regulator.<br>• In shutdown, the switch node for the step-down regulator is high impedance. Logic low disables the step-down switching regulator. The low signal has to be at least 20µs to disable the switching regulator. (See Table 5, Electrical Characteristics, on page 17 for detailed logic high and logic low specifications)<br>• SHDN/SDI must be kept low to enable EN function<br>• **Do not float this pin.** |
| 4 | SGND | GND | Signal Ground<br>• This pin must be connected to PGND and make a star connection to system ground. |
| 5 | SFB | I | Switching Regulator Output Voltage Sense Feedback<br>• Senses the output voltage of the switching regulator.<br>• Connect to the output capacitor of the switching regulator. |

**Table 2: Pin Description (Continued)**

| Pin # | Pin Name | Pin Type | Pin Function |
|---|---|---|---|
| 6 | SW | O | Switch Node<br>• Internally connected to the drains of the high side and low side MOSFETs.<br>• Connect to the external inductor. |
| 7 | PVIN | S | Switching Regulator Power Input<br>• Power input voltage. Internally connected to the source of the high side MOSFET. **Connect a ceramic input capacitor between PVIN and PGND and place it as close as possible to PVIN and PGND pins.** See Section 6, Applications Information for example.<br>• The voltage between SVIN and PVIN should equal to 50mV or less. |
| 8 | PG | O | Switching Regulator Power Good Output<br>• It is an open-drain output.<br>• Connect a 100kΩ pull-up resistor from this pin to $V_{OUT}$ or a logic rail that is equal to or less than SVIN.<br>• The PG is held low when the output voltage is outside its regulation band and goes high after the output voltage is within regulation.<br>• **In shutdown, the PG will be actively on.** |
| 9 | SVIN | S | Signal Input Voltage<br>• Input voltage to the internal circuitry. See Table 5, Electrical Characteristics, on page 17 for input voltage range.<br>• **Connect a decoupling capacitor between SVIN an SGND and position it as close as possible to the IC.** See Section 6, Applications Information for example.<br>• The voltage between SVIN and PVIN should equal to 50mV or less. |
| 10 | SHDN/SDI | I | Shutdown / Serial Data Input<br>• Logic high disables the switching step-down regulator. In shutdown, the switch node for the step-down regulator is high impedance. Logic high enables the step-down switching regulator.<br>• EN must be kept high to enable the shutdown function.<br>• Input data into this pin is used to program the output voltage (see Section 3.3.1, Serial Programmability of Switching Regulator (SDI), on page 22).<br>• To program the output voltage using serial interface, the part must be in PWM mode (see Section 3.5).<br>• **Do not share this pin with other serial interface pins.**<br>• **Do not float this pin.** |
| 11 | VSET | I | Switching Regulator Voltage Set<br>To set the nominal output voltage values:<br>• Connect VSET to SVIN or GND in conjunction with PSET connected to SVIN or GND to set four nominal output voltages.<br>• Connect a resistor from VSET to GND to set eight nominal output voltages. See Table 9, VSET and PSET Logic Programming, on page 24 for resistor values and Output Voltage Settings.<br>• The total capacitance across this pin and SGND must be 25pF or less. Use resistor values with a 5% tolerance or better. OTF pin must be kept low to maintain nominal output voltages.<br>• **Do not float this pin.** |

**Table 2: Pin Description (Continued)**

| Pin # | Pin Name | Pin Type | Pin Function |
|---|---|---|---|
| 12 | PSET | I | Switching Regulator Percent Set<br>To set the margining percentage set to output voltage:<br>• Set the nominal output voltage in conjunction with VSET as described above.<br>• Connect an external resistor to ground to set the percentage change of the output voltage. See Table 9, VSET and PSET Logic Programming, on page 24 for resistor values and Output Voltage Settings.<br>• The total capacitance across this pin and SGND must be 25pF or less. Use resistor values with a 5% tolerance or better.<br>• **Do not float this pin.** |
| 13 | PGND | GND | Power Ground<br>• It must be connected to the negative terminals of the input and output capacitors. |

# 2 Electrical Specifications

## 2.1 Absolute Maximum Ratings

**Table 3: Absolute Maximum Ratings[1]**

**Note**: Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

| Parameter | Range | Units |
|---|---|---|
| $V_{PVIN}$ to PGND | -0.3 to 6.0 | V |
| $V_{PVIN}$ to $V_{SVIN}$ | -0.3 to 0.3 | V |
| PGND to SGND | -0.3 to 0.3 | V |
| $V_{SW}$ to PGND[2] | -0.3 to ($V_{PVIN}$ + 0.3) | V |
| $V_{SFB}$ to SGND | -0.3 to ($V_{SVIN}$ + 0.3) | V |
| $V_{VSET}$, $V_{PSET}$ to SGND | -0.3 to ($V_{SVIN}$ + 0.3) | V |
| $V_{PFM}$, $V_{OTF}$,$V_{EN}$, $V_{SHDN/SDI}$, $V_{PG}$ to SGND | -0.3 to ($V_{SVIN}$ + 0.3) | V |
| Operating Ambient Temperature Range[3] | -40 to 85 | °C |
| Maximum Junction Temperature | 150 | °C |
| Storage Temperature Range | -65 to +150 | °C |

1. Exceeding the absolute maximum rating may damage the device.
2. Capable of -1.0V for less than 50ns and 7V for less than 200ns.
3. Specifications over the -40°C to 85°C operating temperature ranges are assured by design, characterization, and correlation with statistical process controls.

## 2.2 Recommended Operating Conditions

**Table 4: Recommended Operating Conditions[1]**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{SVIN}$ | Signal Input Voltage | 2.7 | | 5.5 | V |
| $V_{PVIN}$ | Power Input Voltage | 2.7 | | 5.5 | V |
| $\theta_{JA}$ | Package Thermal Resistance[2] | | 66.2 | | °C/W |
| $\theta_{JC}$ | | | 43.8 | | °C/W |
| $T_{JMAX}$ | Maximum Operational Junction Temperature | | | 125 | °C |

1. This device is not guaranteed to function outside the specified operating range.
2. Simulated on a 3”x4.5” 4-Layer JEDEC PCB with 2 thermal vias.

# 2.3 Electrical Characteristics

**Table 5: Electrical Characteristics**

The following applies unless otherwise noted (refer to schematic shown in Figure 1): $V_{SVIN} = V_{PVIN} = V_{EN} = 3.3V$, $V_{PSET} = V_{SHDN/SDI} = SGND = PGND$, $V_{BUCK} = 1.5V$, $T_A = 25°C$. **Bold Values indicate 0°C ≤ $T_A$ ≤ 85°C.** Specifications over temperature are assured by design, characterization, and correlation with statistical process controls.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{SVIN}$ | Signal Input Voltage | $V_{SVIN} = V_{PVIN}$ | **2.7** | | **5.5** | **V** |
| $V_{PVIN}$ | Power Input Voltage | $V_{SVIN} = V_{PVIN}$ | **2.7** | | **5.5** | **V** |
| $I_{Q\_PFM}$ | Total Quiescent Current (PFM Mode) | No load<br>$V_{PFM} = V_{SVIN} = V_{PVIN}$ | | 32 | **50** | µA |
| $I_{Q\_PWM}$ | Total Quiescent Current (PWM Mode) | No load<br>$V_{PFM} = V_{SGND}$ | | 6 | **9** | mA |
| $I_{SHDN}$ | Shutdown Supply Current | $V_{SHDN/SDI} = V_{SVIN} = V_{PVIN}$,<br>$V_{EN} = 0V$ | | | **10** | µA |
| $V_{UVLO}$ | Under Voltage Lockout | High Threshold, $V_{SVIN}$ increasing | | 2.600 | **2.700** | V |
| | | Low Threshold, $V_{SVIN}$ decreasing | **2.400** | 2.500 | | V |
| $V_{OVP}$ | Over Voltage Protection | High Threshold, $V_{SVIN}$ increasing | | 5.780 | **5.975** | V |
| | | Low Threshold, $V_{SVIN}$ decreasing | **5.500** | 5.670 | | |
| $T_{OTS}$ | Over-Temperature Thermal Shutdown | High Threshold, $T_J$ increasing (Disable regulator) | | 150 | | °C |
| | | Low Threshold, $T_J$ decreasing (Enable regulator) | | 110 | | °C |
| $V_{IH}$ | EN, SHDN/SDI, OTF, and PFM Input Voltage Threshold | Logic High | | | **2** | V |
| $V_{IL}$ | EN, SHDN/SDI, OTF, and PFM Input Voltage Threshold | Logic Low | **0.4** | | | V |
| $I_{EN}$ | Enable Input Current | $V_{EN} = V_{SVIN} = V_{PVIN}$ | | | **10** | µA |
| | | $V_{EN} = 0V$ | **-10** | | | µA |
| $I_{OTF}$ | OTF Input Current | $V_{OTF} = V_{SVIN} = V_{PVIN}$ | | | **10** | µA |
| | | $V_{OTF} = 0V$ | **-10** | | | µA |
| $I_{PFM}$ | PFM Input Current | $V_{PFM} = V_{SVIN} = V_{PVIN}$ | | | **10** | µA |
| | | $V_{PFM} = 0V$ | **-10** | | | µA |

## 2.4 Switching Step-down Regulator

**Table 6: Switching Step-down Regulator**

The following applies unless otherwise noted (refer to schematic shown in Figure 1): $V_{SVIN} = V_{PVIN} = V_{EN} = 3.3V$, $V_{PSET} = V_{SHDN/SDI} = SGND = PGND$, $V_{BUCK} = 1.5V$, $T_A = 25°C$. **Bold Values indicate 0°C ≤ $T_A$ ≤ 85°C.** Specifications over temperature are assured by design, characterization, and correlation with statistical process controls.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage (PWM Mode) | $V_{OTF} = V_{SVIN}$, $R_{VSET}$ = 18k, $R_{PSET}$ = 100k, PWM mode, $I_{LOAD}$ = 0 – 1.2A | | | 1.025 | | V |
| | | Over Temperature[1] | | **-2** | | **+2.5** | % |
| | | Over Temperature[2] | | **-4** | | **+4** | % |
| | | $V_{OTF} = SGND$, $R_{VSET}$ = 100k, PWM mode, $I_{LOAD}$ = 0 – 1.2A | | | 1.8 | | V |
| | | $V_{OTF} = SGND$, $V_{VSET} = V_{SVIN}$, $V_{PSET} = SGND$, PWM mode, $I_{LOAD}$ = 0 – 1.2A | | | | | V |
| | | Over Temperature | | **-4** | | **+4** | % |
| $V_{OUT}$ | Output Voltage (PFM Mode) | $V_{OTF} = V_{SVIN}$, $R_{VSET}$ = 18k, $R_{PSET}$ = 100k, PFM mode, $I_{LOAD}$ = 10mA | | | 1.025 | | V |
| | | Over Temperature | | **-7** | | **+7** | % |
| | | $V_{OTF} = SGND$, $R_{VSET}$ = 100k, PFM mode, $I_{LOAD}$ = 10mA | | | 1.8 | | V |
| | | $V_{OTF} = SGND$, $V_{VSET} = V_{SVIN}$, $V_{PSET} = SGND$, PFM mode, $I_{LOAD}$ = 10mA | | | | | V |
| | | Over Temperature | | **-7** | | **+7** | % |
| $P_{SET}$ | Percentage Set | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 0 | | -20 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 11k | | -10 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 18k | | -7.5 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 30k | | -5.0 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 51k | | -2.5 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 100k | | 2.5 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 160k | | 5.0 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 270k | | 7.5 | | % |
| | | $V_{OTF} = V_{SVIN}$ | $R_{PSET}$ = 470k | | 10 | | % |

### Table 6: Switching Step-down Regulator (Continued)

The following applies unless otherwise noted (refer to schematic shown in Figure 1): $V_{SVIN} = V_{PVIN} = V_{EN} = 3.3V$, $V_{PSET} = V_{SHDN/SDI} = SGND = PGND$, $V_{BUCK} = 1.5V$, $T_A = 25°C$. **Bold Values indicate 0°C ≤ $T_A$ ≤ 85°C.** Specifications over temperature are assured by design, characterization, and correlation with statistical process controls.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{LNREG}$ | Output Voltage Line Regulation | $V_{SVIN} = V_{PVIN}$ = 3.0V to 5.0V, $I_{LOAD}$ = 1A | | -0.8 | | % |
| $V_{LDREG}$ | Output Voltage Load Regulation | $V_{SVIN} = V_{PVIN}$ = 5.0V, $I_{LOAD}$ = 500mA to 2A | | 0.9 | | % |
| $R_{DSON\_HS}$ | High Side Switch On Resistance | $V_{SVIN} = V_{PVIN}$ = 5V | **84** | 140 | **196** | mΩ |
| | | | **102** | 170 | **238** | mΩ |
| $R_{DSON\_LS}$ | Low Side Switch On Resistance | $V_{SVIN} = V_{PVIN}$ = 5V | **60** | 100 | **140** | mΩ |
| | | | **69** | 115 | **161** | mΩ |
| $I_{LIM}$ | Peak Switch Current Limit | | **2.2** | 3 | **3.9** | A |
| $I_{LSW\_HS}$ | High Side Switch Leakage Current | $V_{SHDN/SDI} = V_{SVIN} = V_{PVIN}$, $V_{SW} = V_{SVIN} = V_{PVIN}$ | | | **10** | µA |
| $I_{LSW\_LS}$ | Low Side Switch Leakage Current | $V_{SHDN/SDI} = V_{SVIN} = V_{PVIN}$, $V_{SW}$ = PGND | | | **10** | µA |
| $f_{sw}$ | Switching Frequency | PWM mode | 1.4 | 2 | 2.6 | MHz |
| $D_{MAX}$ | Maximum Duty Cycle | | | 100 | | % |
| $T_{HICCUP}$ | Hiccup Mode Time Interval | | | 2 | | ms |
| $t_{DEGLITCH}$ | Deglitch | | | 25 | | µs |
| $I_{FB}$ | FB Leakage Current | $V_{EN}$ = 0V, $V_{PVIN} = V_{FB} = V_{SHDN/SDI} = V_{SVIN} = V_{PVIN}$ | | 1 | **10** | µA |
| $I_{FB}$ | FB Leakage Current | $V_{EN} = V_{FB} = V_{SVIN} = V_{PVIN}$, $V_{VSET}$ = < 1.8V, $V_{OTF} = V_{SHDN/SDI}$ = SGND | | 1 | | µA |
| $I_{FB}$ | FB Leakage Current | $V_{EN} = V_{FB} = V_{SVIN} = V_{PVIN}$, $V_{VSET}$ = > 1.5V, $V_{OTF} = V_{SHDN/SDI}$ = SGND | | 6 | | µA |
| $V_{PGTH}$ | Power Good (PG) Threshold Voltage | | | $V_{OUT}$ × 90% | | V |
| $V_{PGL}$ | Maximum PG Output Low Voltage | $I_{SINK}$ = 2mA, $V_{EN} = V_{SVIN}$ | | 0.4 | | V |
| $t_{DELAY}$ | PG Delay Time | | | 1.2 | | ms |
| $I_{PG}$ | PG Leakage Current | $V_{EN}$ = 0V | | | **1** | µA |

1. This rating is for the 88PG839-A1-NAE2C000-T181 / 88PG839-A1-NAE2C000TT181 (Tape and Reel) part number only.

2. The rating is for the 88PG839-A1-NAE2C000 / 88PG839-A1-NAE2C000-T (Tape and Reel) part number only.

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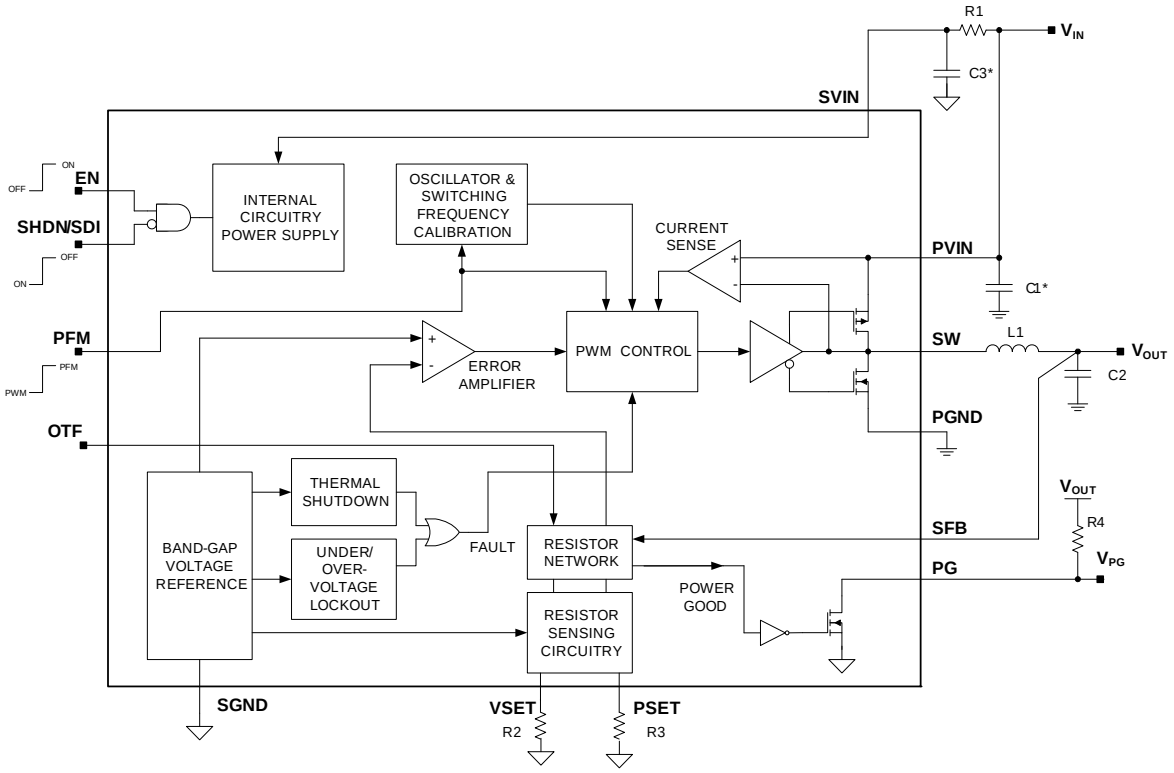
# 3 Functional Description

## 3.1 Overview

The 88PG839 step-down switching regulator uses a proprietary Pulse Width Modulation (PWM) control scheme to regulate the output voltage. If Pulse Frequency Modulation (PFM) pin is set high, the regulator changes automatically from PWM to PFM mode under light load conditions. If PFM pin is set low, the regulator is in forced PWM mode. This control scheme offers a number of advantages, which include fast transient response time, small output ripple, and no external compensation required. When PVIN drops down close or below the target output voltage, the regulator is capable of operating in drop out mode by turning on the upper switch continuously (100% ON mode).

**Figure 3: Block Diagram**




**Note(*): All input capacitors must be placed close to the IC.**

## 3.2 Soft Start

Soft start is used in "Hot-Plug" applications to reduce the inrush current during startup of the switching regulator. The 88PG839 controls the rise time of the output voltage. The output ramp rate is between 0.5V/ms to 3V/ms depending on the output voltage setting and the internal clock frequency. However, the output ramp is independent of output capacitance and load current.

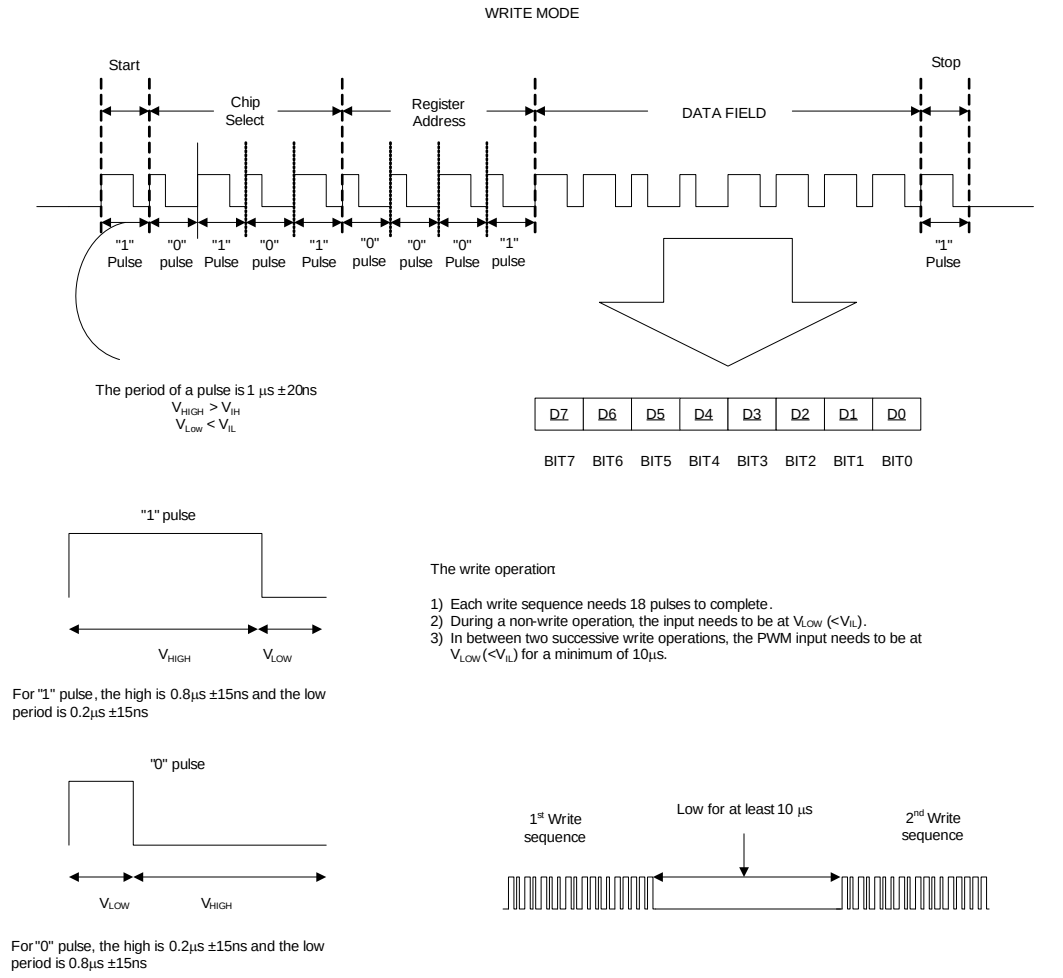
## 3.3 Output Voltage Setting

### 3.3.1 Serial Programmability of Switching Regulator (SDI)

The output voltage of the step-down switching regulator can be programmed by using serial data (shown in Figure 4) into the Serial Data Input (SDI) pin in PWM mode by connecting PFM pin in low state or high state with heavy load. The serial interface is disabled when the PFM pin connects to low state at a light load.

| | |
|---|---|
| ! | **Caution: Do not share the SHDN/SDI pin with other serial interface pins.** |

**Figure 4: Serial Programmability**



The first 4 bits (MSB-bits) of the data field are used to select the output voltage where the second 4 bits (LSB-bits) of the data field are used to trim the output voltage (percent of output voltage). The default value for the data field is as follows:

**Table 7: Default Value of Data Field**

| | Data Field | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Description** | **Voltage Set** | | | | **Percent Set** | | | |
| **Bits** | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Default Value** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

On power up, the output voltage is set according to $V_{PSET}$ and $V_{VSET}$. The output voltage can then be field programmed by setting bit 3 and bit 7 to “1”. The output voltage and percent set are selected according to Table 8. For PSET voltage options, OTF pin has to connect to logic high.

**Table 8: Voltage and Percentage Set**

| | Data Field | | | | $V_{OUT}$ (V) | Data Field | | | | Percent Set |
|---|---|---|---|---|---|---|---|---|---|---|
| **Bits** | 7 | 6 | 5 | 4 | | 3 | 2 | 1 | 0 | |
| **Value** | 0 | 0 | 0 | 0 | Default power up value | 0 | 0 | 0 | 0 | Default power up value |
| | 1 | 0 | 0 | 0 | 0.8 | 1 | 0 | 0 | 0 | -10% |
| | 1 | 0 | 0 | 1 | 1.0 | 1 | 0 | 0 | 1 | -7.5% |
| | 1 | 0 | 1 | 0 | 1.2 | 1 | 0 | 1 | 0 | -5.0% |
| | 1 | 0 | 1 | 1 | 1.5 | 1 | 0 | 1 | 1 | -2.5% |
| | 1 | 1 | 0 | 0 | 1.8 | 1 | 1 | 0 | 0 | +2.5% |
| | 1 | 1 | 0 | 1 | 2.5 | 1 | 1 | 0 | 1 | +5.0% |
| | 1 | 1 | 1 | 0 | 3.0 | 1 | 1 | 1 | 0 | +7.5% |
| | 1 | 1 | 1 | 1 | 3.3 | 1 | 1 | 1 | 1 | +10% |

All combinations of the VSET (Table 10) can be used with all combinations of the PSET (Table 10) to provide maximum flexibility in output voltage selection (Table 10).

### 3.3.2 Logic Programmability

The output voltage of the step-down switching regulator can be programmed for the standard output voltages by connecting the VSET and PSET pins to “0” (SGND) and/or “1” (SVIN). This is useful for standard output voltages, and eliminates the use of an external resistor to set the output voltage. The OTF pin provides an additional feature to reduce the output voltage by -20%.

**Table 9: VSET and PSET Logic Programming**

| $V_{VSET}$ | $V_{PSET}$ | $V_{OUT}$ (V) | |
|---|---|---|---|
| | | OTF = 0 (SGND) | OTF = 1 (SVIN) |
| SGND | SGND | 1.0 | 0.8 |
| SGND | SVIN | 1.5 | 1.2 |
| SVIN | SGND | 1.8 | 1.44 |
| SVIN | SVIN | 2.5 | 2.0 |
| $11k\Omega \le R_{VSET} \le 470k\Omega$ | SGND | $V_{OUT}$[1] | $V_{OUT}$ (1-20%) |
| SGND or SVIN | $11k\Omega \le R_{PSET} \le 470k\Omega$ | High Impedance | |

1. See Table 10.

### 3.3.3 Programmability—AnyVoltage® Technology

The output voltage is programmable using VSET and PSET resistors between 11kΩ and 470kΩ (Table 10). The VSET and PSET resistors are read once during startup after the output voltage is powered on. To configure the output to a different voltage, power has to recycle or the device has to turn OFF and back ON using the EN or SHDN/SDI pin.

Using a VSET resistor value greater than 619kΩ or less than 7.68kΩ disables the step-down switching regulator and sets the SW pin to high impedance. When the PSET pin is not used, it must be connected to ground. The VSET and PSET pins are sensitive to excessive leakage currents and stray capacitance. The output voltage can be programmed to the lower output voltage if there is contamination, especially for a $R_{VSET}$ and $R_{PSET}$ of 470kΩ or higher values. The parasitic resistance on these nodes must be greater than 3MΩ, and the stray capacitance must be less than 25pF.

After the output voltage is on, it can be changed on-the-fly (OTF) from 0% to a percentage between -20% and +10% when the OTF pin connection is high (Table 10). The percentage value is determined by the PSET resistor.

**Table 10: VSET and PSET Programming Table for 5% Resistors**

| | | Percent Set (%) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | OTF=0 (SGND) | OTF = 1 (SVIN) | | | | | | | |
| | | | 0Ω | 11k | 18k | 30k | 51k | 100k | 160k | 270k | 470k |
| | | 0% | -20% | -10% | -7.50% | -5.00% | -2.50% | 2.50% | 5.00% | 7.50% | 10% |
| Voltage Set (V) | 11k | 0.8 | 0.64 | 0.72 | 0.74 | 0.76 | 0.78 | 0.82 | 0.84 | 0.86 | 0.88 |
| | 18k | 1.0 | 0.8 | 0.9 | 0.925 | 0.95 | 0.975 | 1.025 | 1.05 | 1.075 | 1.1 |
| | 30k | 1.2 | 0.96 | 1.08 | 1.11 | 1.14 | 1.17 | 1.23 | 1.26 | 1.29 | 1.32 |
| | 51k | 1.5 | 1.2 | 1.35 | 1.388 | 1.425 | 1.463 | 1.538 | 1.575 | 1.613 | 1.65 |
| | 100k | 1.8 | 1.44 | 1.62 | 1.665 | 1.71 | 1.755 | 1.845 | 1.89 | 1.935 | 1.98 |
| | 160k | 2.5 | 2.0 | 2.25 | 2.313 | 2.375 | 2.438 | 2.563 | 2.625 | 2.688 | 2.75 |
| | 270k | 3.0 | 2.4 | 2.7 | 2.775 | 2.85 | 2.925 | 3.075 | 3.15 | 3.225 | 3.3 |
| | 470k | 3.3 | 2.64 | 2.97 | 3.053 | 3.135 | 3.218 | 3.383 | 3.465 | 3.548 | 3.63 |

## 3.4 Enable and Shutdown

To simplify the interface to different control logic, both Enable (EN) and Shutdown (SHDN/SDI) pins are available for controlling the 88PG839. If a positive logic is selected, the EN pin is used and the SHDN/SDI pin is pulled below $V_{IL}$. Voltage above $V_{IH}$ at the EN pin enables the regulator, while voltage below $V_{IL}$ disables the regulator. If a negative logic is desired, the SHDN/SDI pin is used and the EN pin is pulled above $V_{IH}$. Voltage above $V_{IH}$ at the SHDN/SDI pin shuts down the regulator, while voltage below $V_{IL}$ powers on the regulator.

## 3.5 PFM and PWM Mode Selection

When PFM pin is connected to low state, the regulator is in the forced PWM mode, where the regulator runs at a constant frequency. The quiescent current of the forced PWM mode increases to $I_{Q\_PWM}$. When PFM pin is connected to a high state, the regulator runs in PFM mode, where the switching frequency decreases when the load current reduces, thus improving the light load efficiency.

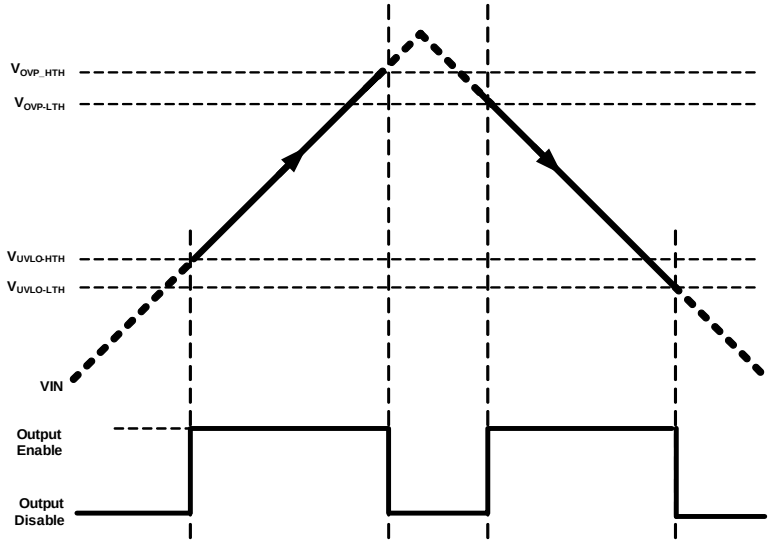
## 3.6 Under Voltage Lockout (UVLO)

This feature ensures that both internal MOSFETs have adequate voltage levels to operate properly. When the input voltage is below UVLO low threshold both MOSFETs are off until the input rises above the UVLO high threshold. The switching node (SW) is in high Z state when the input voltage is less than UVLO high threshold.

## 3.7 Over Voltage Protection (OVP)

An over voltage comparator guards against line transient overshoots, as well as other serious conditions that may damage the IC. When the input voltage is above OVP high threshold the output turns off and the switching node (SW) is high Z. The device will remain at this state until the input voltage comes back below OVP low threshold.

**Figure 5: UVLO and OVP Waveforms**



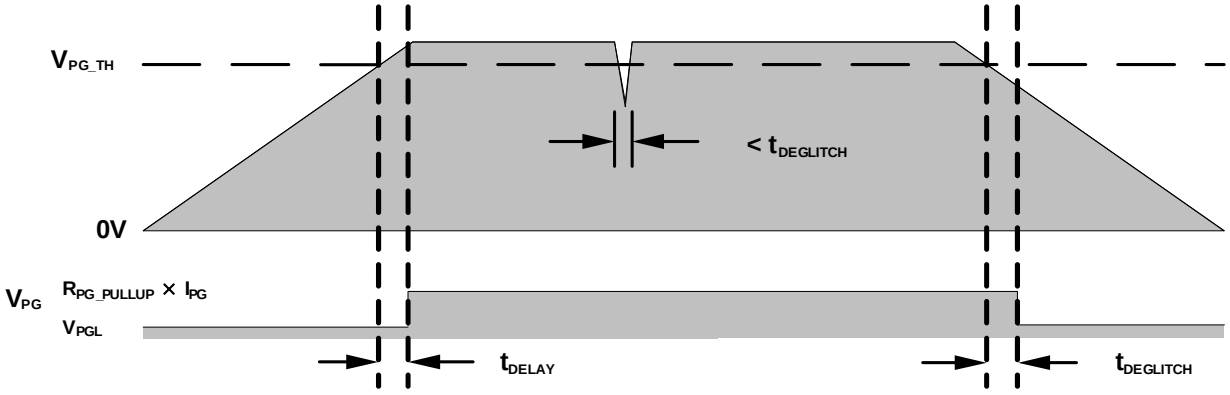

## 3.8 Thermal Shutdown

When the junction temperature exceeds OTS high threshold, the thermal shutdown circuitry disables the 88PG839. The device is enabled when the junction temperature is decreased to OTS low threshold.

# 3.9 Power Good (PG)

The PG is an active-high, open-drain output. The output is held low when the output voltage of the step-down regulator is below the threshold. When the output voltage is above the threshold, the power good pin goes high after 1.2ms delay time ($t_{DELAY}$). The threshold voltage is 0.9% × $V_{OUT}$ (typical). **In shutdown, PG will be actively on.**

**Figure 6: Power Good Operating Waveform**



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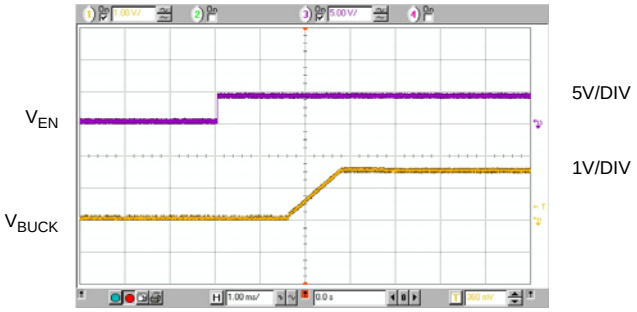
# 4 Functional Characteristics

## 4.1 Startup Waveforms

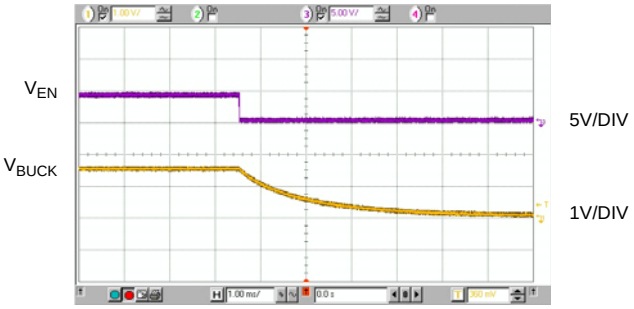
.

**Figure 7: Startup Using Enable Pin**




$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

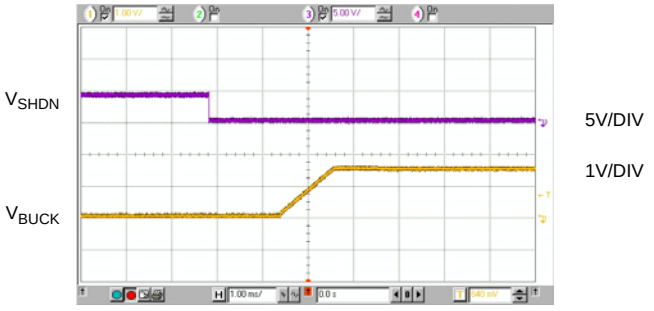
**Figure 8: Turn Off Using Enable Pin**




$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

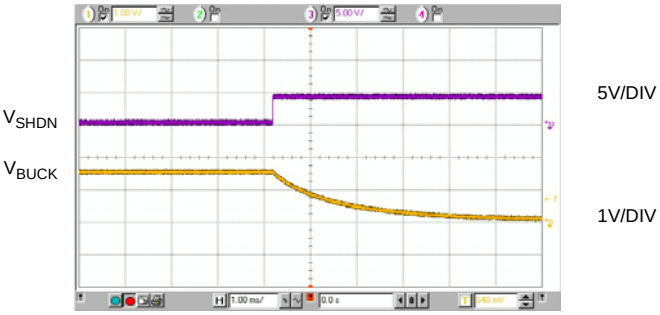
.

**Figure 9: Startup Using Shutdown Pin**




$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

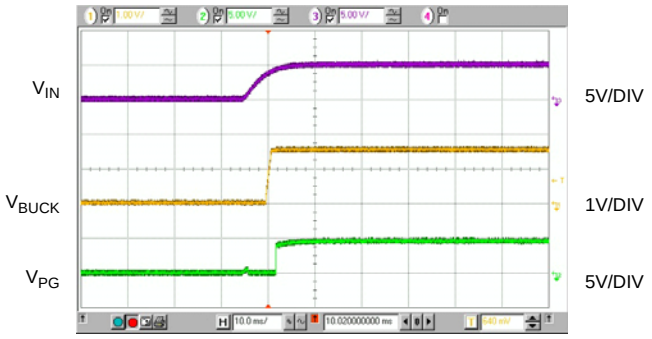
**Figure 10: Turn Off Using Shutdown Pin**




$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

.

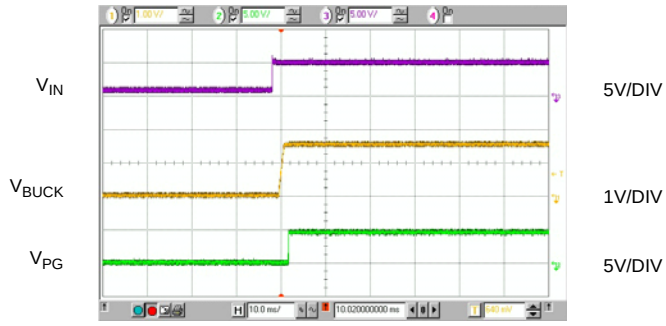
**Figure 11: Soft Start**




10ms/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

**Figure 12: Hot Plug**

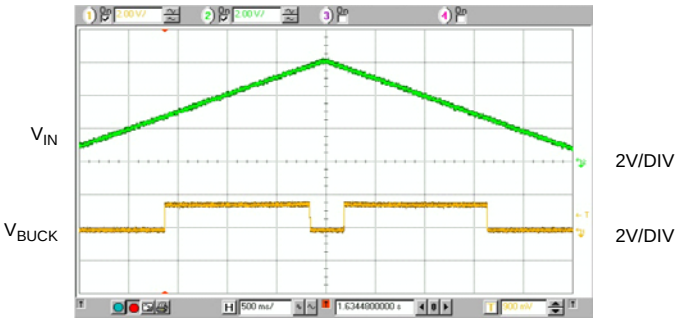



10ms/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω

.

**Figure 13: UVLO and OVP Thresholds**

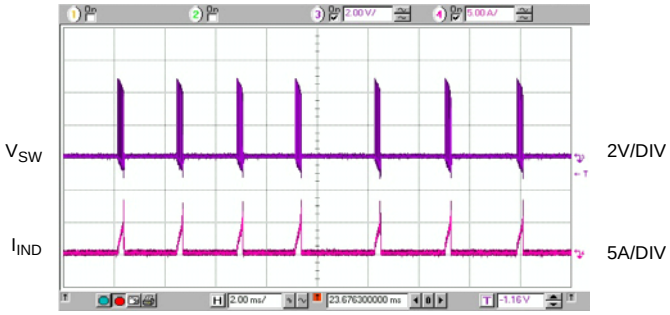



500ms/DIV

$V_{IN}$ = 0V to 6V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 50Ω
$V_{UVLO(HTH)}$ = 2.61V
$V_{UVLO(LTH)}$ = 2.52V
$V_{OVP(HTH)}$ = 5.67V
$V_{OVP(LTH)}$ = 5.56V

# 4.2 Short-Circuit Waveform

**Figure 14: Step-Down Short Circuit**

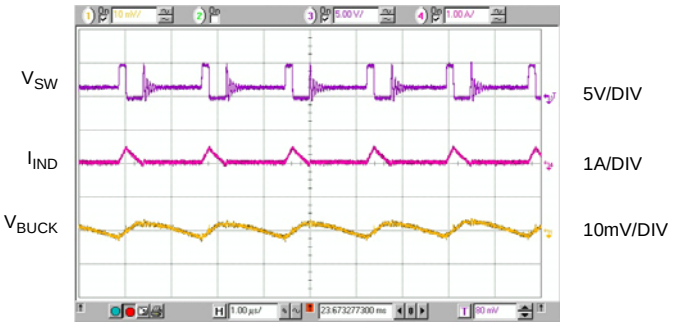



$V_{IN}$ = 5V $V_{OUT(BUCK)}$ = GND

# 4.3 Switching Waveforms

**NOTE:** For repeatability of measuring output ripple ($V_{OUT(P-P)}$) for the BUCK regulator, the standard test procedure limits the scope bandwidth to 20MHz and uses a coax cable with very short leads terminated into 50Ω. The coax leads must be routed away from the switching node as much as possible.

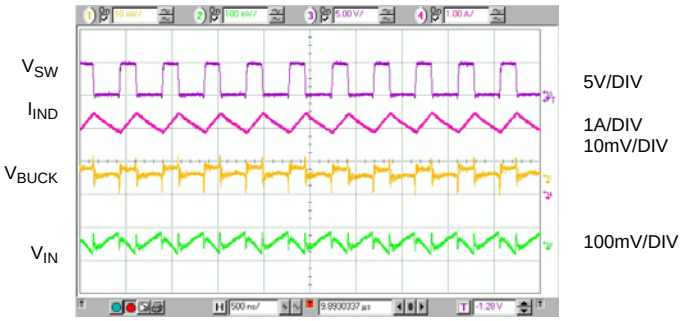
**Figure 15: DCM Mode**




$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$V_{OUT(P-P)}$ = 8.2mV
$I_{LOAD(BUCK)}$ = 20mA + 50Ω
$I_{IND(PK)}$ = 518mA
Frequency = 288kHz

.

**Figure 16: PWM Mode**

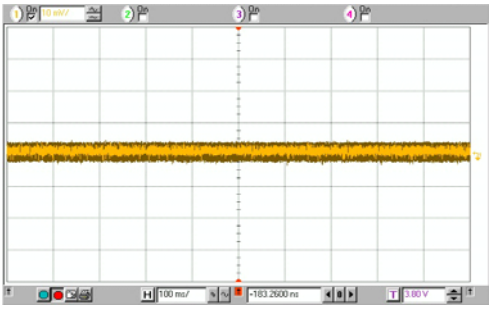



$C_{IN}$ = 10µF
$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$V_{IN(P-P)}$ = 72.9mV
$I_{LOAD(BUCK)}$ = 2A + 50Ω
$V_{OUT(P-P)}$ = 12.0mV
$I_{IND(P-P)}$ = 690.6mA
$I_{IND(PK)}$ = 2.45A
Frequency = 2.13MHz

.

**Figure 17: PWM Output Ripple Voltage**

$V_{BUCK}$



10mV/DIV

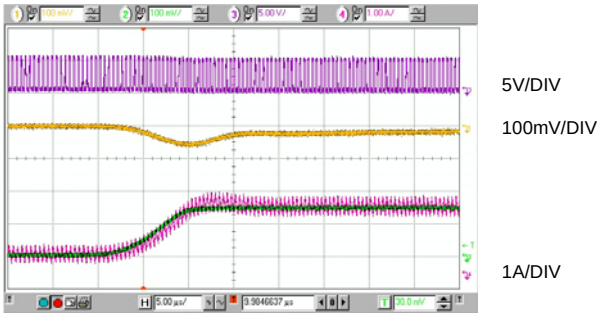
100ms/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 1A + 50Ω
$V_{OUT(P-P)}$ = 7.6mV

## 4.4 Load Transient Waveforms

.

**Figure 18: Slow Load Rise Time**

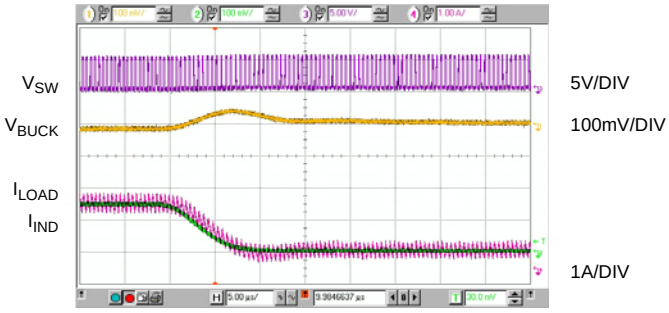



5µs/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 500mA to 2A

$C_{OUT}$ = 10µF
$t_{RISE}$ = 0.2A/µs

**Figure 19: Slow Load Fall Time**



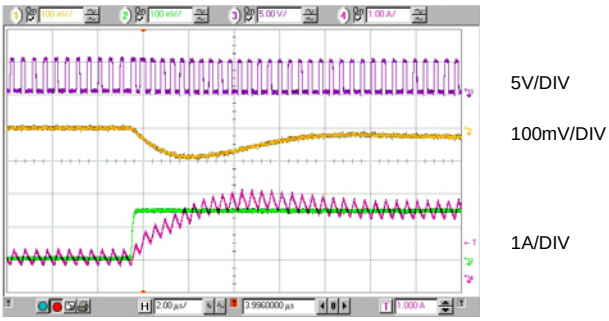

5µs/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 2A to 500mA

$C_{OUT}$ = 10µF
$t_{FALL}$ = 0.2A/µs

.

**Figure 20: Fast Load Rise Time**

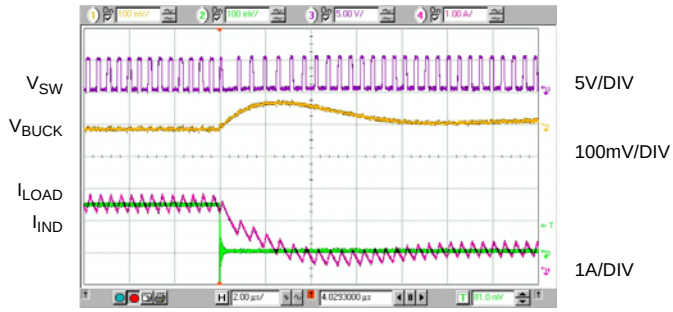



2µs/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 500mA to 2A

$C_{OUT}$ = 10µF
$t_{RISE}$ = 10A/µs

**Figure 21: Fast Load Fall Time**



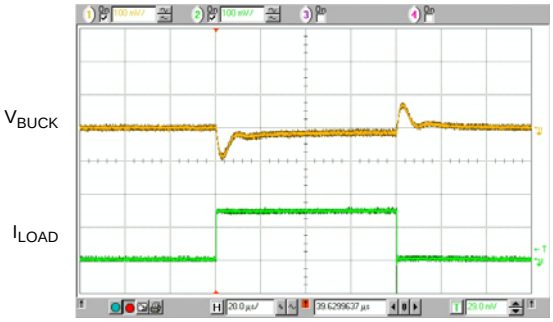

2µs/DIV

$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{LOAD(BUCK)}$ = 2A to 500mA

$C_{OUT}$ = 10µF
$t_{FALL}$ = 48A/µs

.

**Figure 22: Load Transient Response**




$V_{IN}$ = 5V
$V_{OUT(BUCK)}$ = 1.5V
$I_{OUT(BUCK)}$ = 500mA to 2A
$C_{OUT}$ = 10µF
$t_{RISE}$ = 10A/µs, $t_{FALL}$ = 48A/µs

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# 5 Typical Characteristics

## 5.1 Efficiency

**Figure 23: Efficiency vs. Output Current (PFM = High)**

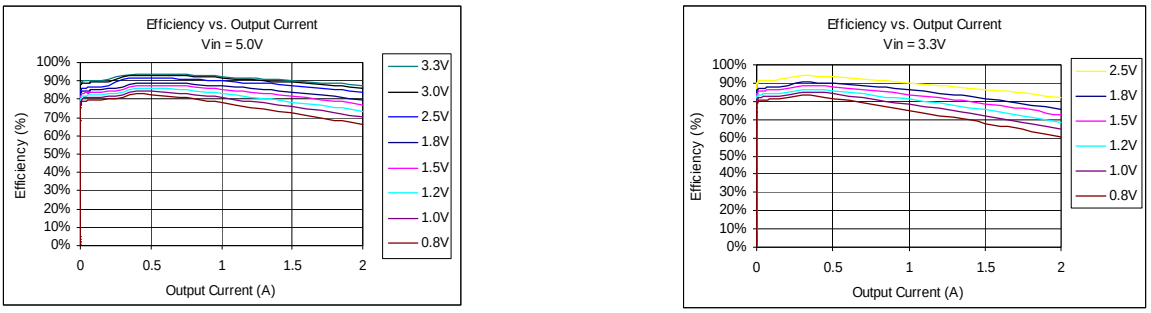
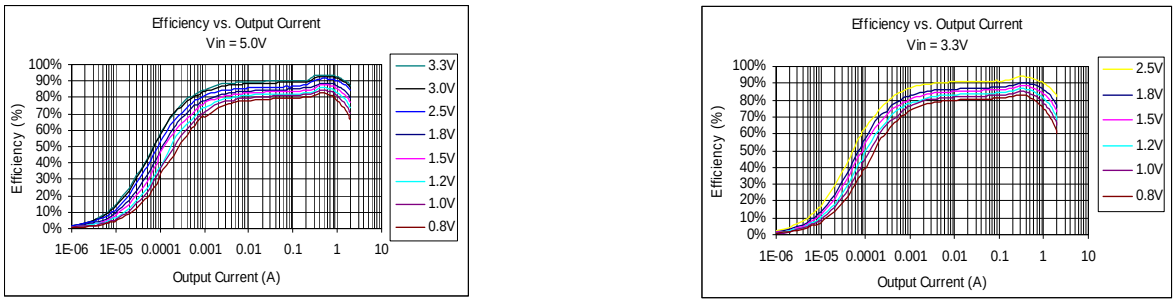
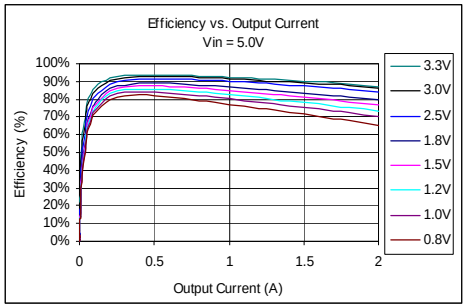
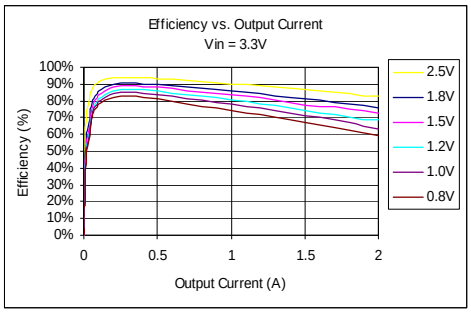



**Figure 24: Efficiency vs. Output Current in Log Scale (PFM = High)**

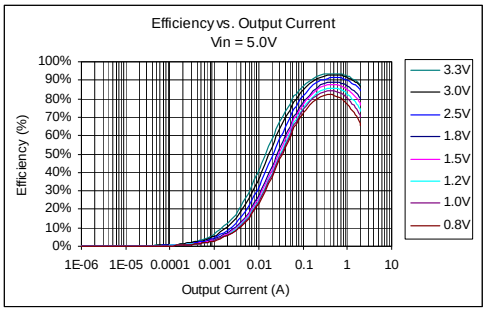


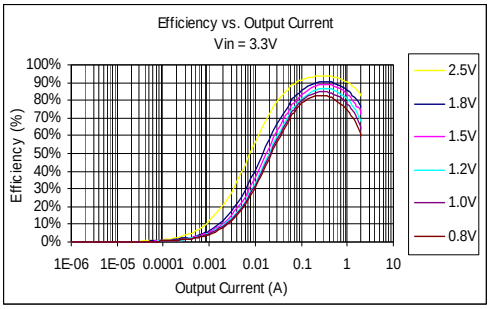
## Figure 25: Efficiency vs. Output Current (PFM = Low)



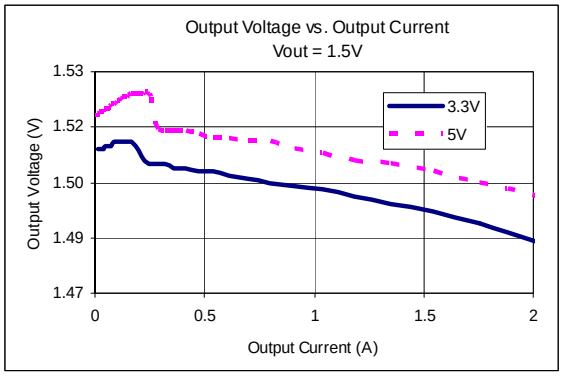

## Figure 26: Efficiency vs. Output Current in Log Scale (PFM = Low)



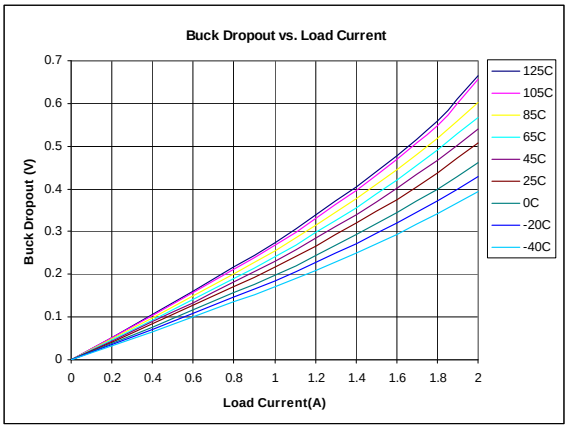
# 5.2 Load Regulation

**Figure 27: Output Voltage vs. Output Current**



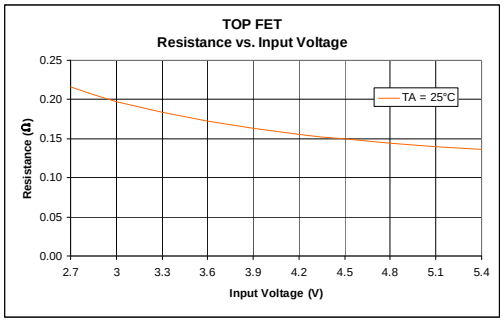

# 5.3 Dropout Voltage

**Figure 28: Step-down Regulator Dropout**



# 5.4 RDS (ON) Resistance

**Figure 29: Resistance vs. Input Voltage**



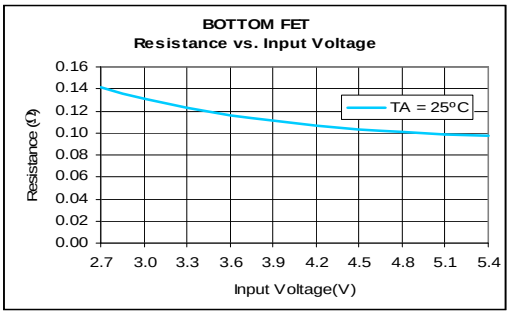
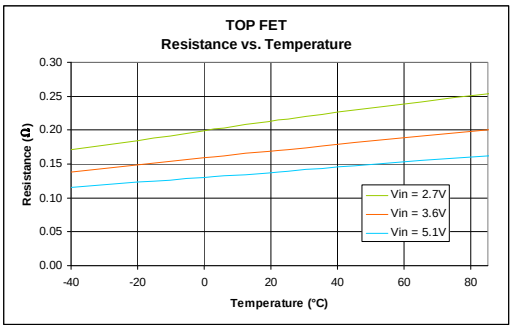
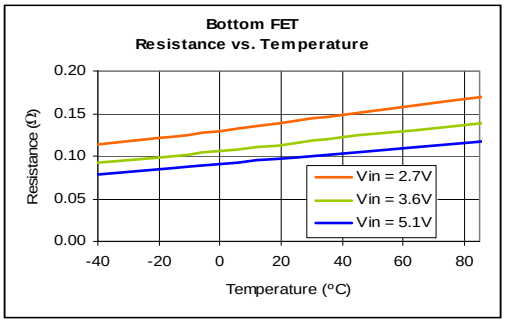




**Figure 30: Resistance vs. Temperature**

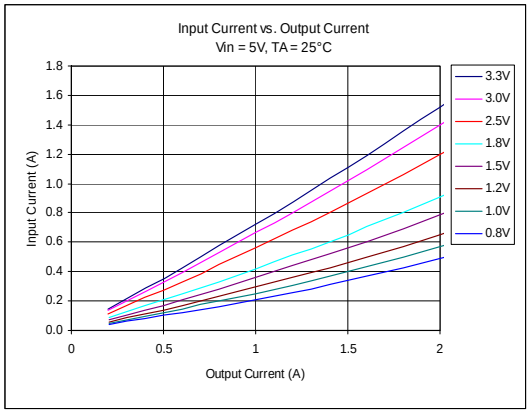


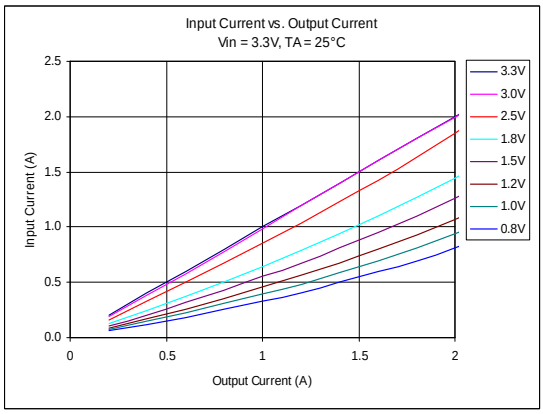



# 5.5 IC Case and Inductor Temperature

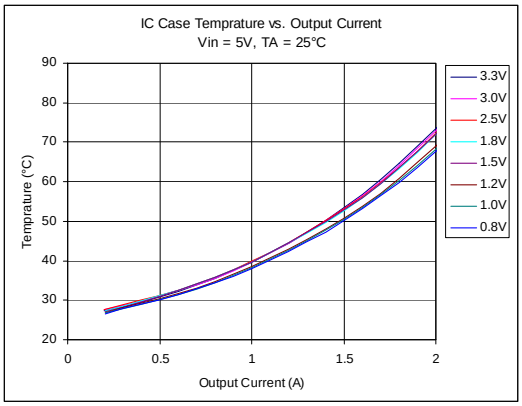
The following data was taken using a 0.88 square inch PCB 1 oz. copper and L = 1µH. Actual results depend upon the size of the PCB proximity to other heat emitting components.

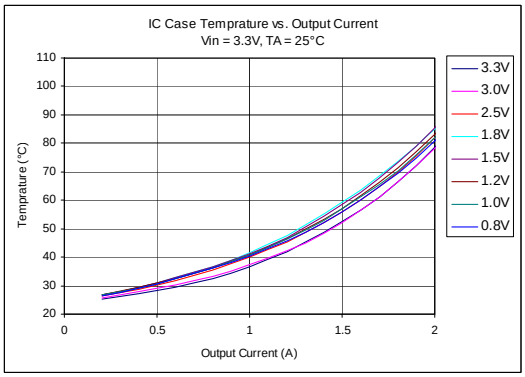
### Figure 31: Input Current vs. Output Current



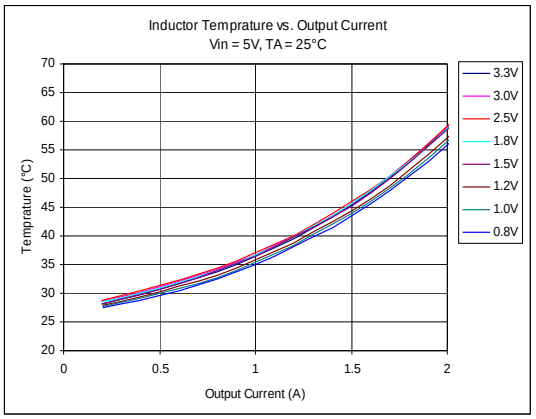



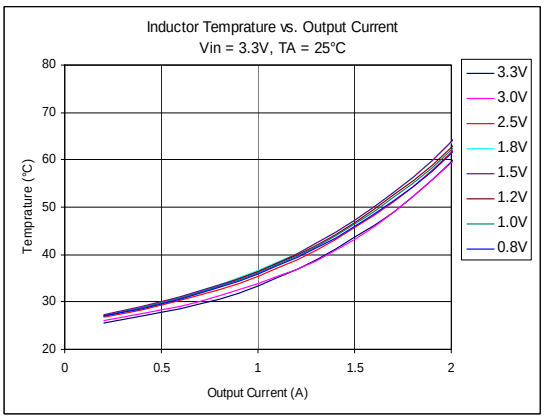

### Figure 32: IC Case Temperature vs. Output Current




### Figure 33: Inductor Temperature vs. Output Current

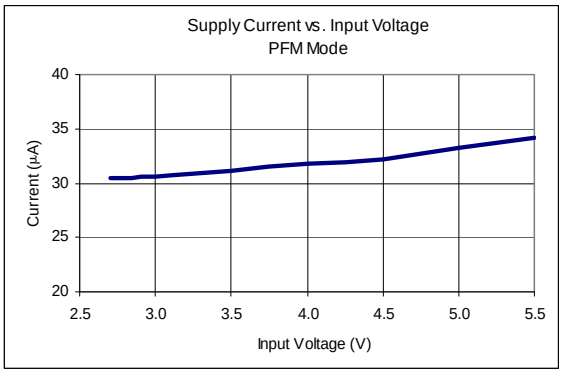


# 5.6 Input Voltage

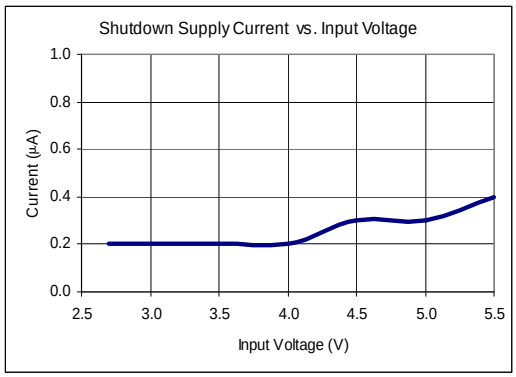
.

**Figure 34: Supply Current vs. Input Voltage**




$I_{LOAD(BUCK)}$ = No Load; $V_{OUT(BUCK)}$ = 1.5V

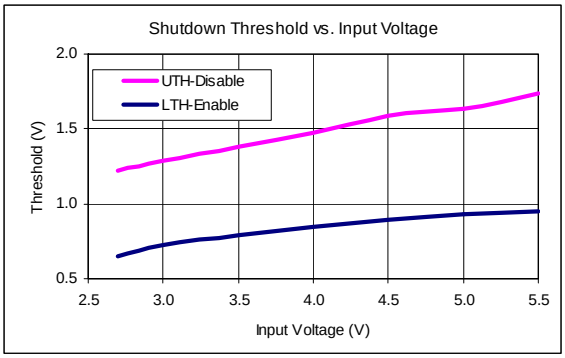
**Figure 35: Shutdown Supply Current vs. Input Voltage**




$I_{LOAD(BUCK)}$ = No Load; $V_{EN}$= 0V; $V_{SHDN}$ = $V_{IN}$

.

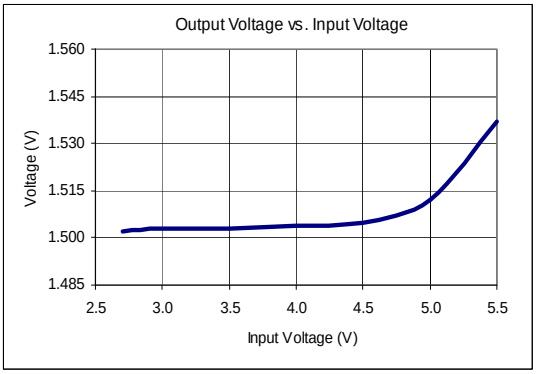
**Figure 36: Shutdown Enable Threshold vs. Input Voltage**




$I_{LOAD(BUCK)}$ = 10mA; $V_{OUT(BUCK)}$ = 1.5V

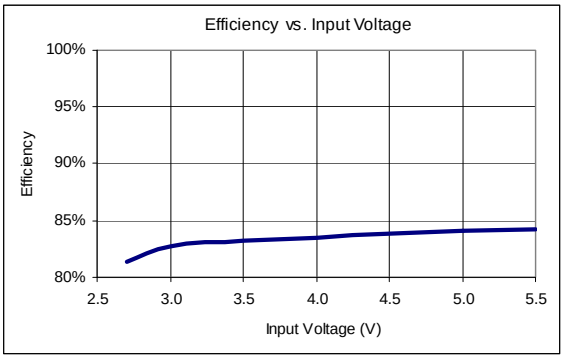
. .

### Figure 37: Output Voltage vs. Input Voltage



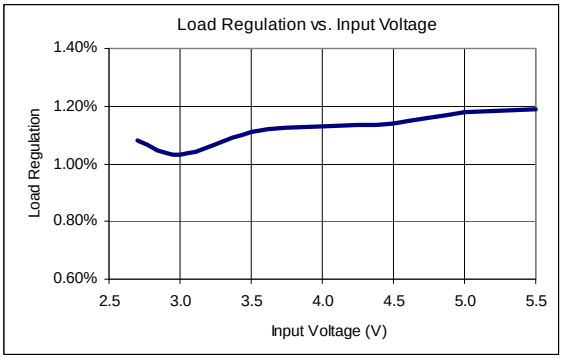

$I_{LOAD(BUCK)}$ = 500mA

### Figure 38: Efficiency vs. Input Voltage



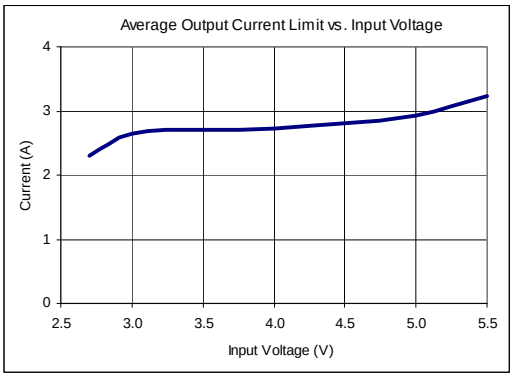

$I_{LOAD(BUCK)}$ = 1A; $V_{OUT(BUCK)}$ = 1.5V

### Figure 39: Load Regulation vs. Input Voltage



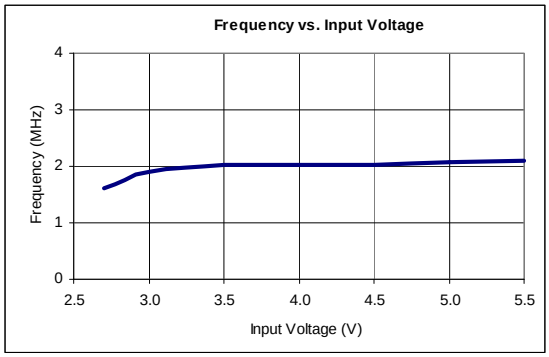

$I_{LOAD(BUCK)}$ = 500mA-2A; $V_{OUT\ (BUCK)}$ = 1.5V

### Figure 40: Average Output Current Limit vs. Input Voltage




$V_{OUT\ (BUCK)}$ = 1.5V

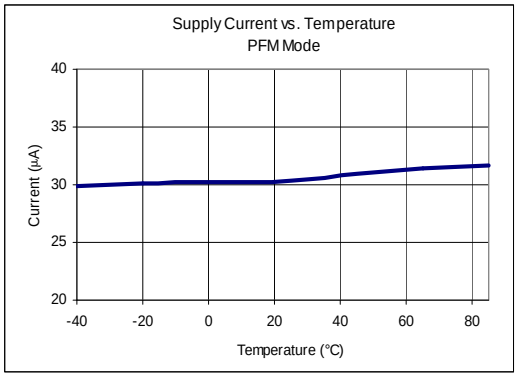
### Figure 41: Frequency vs. Input Voltage




$I_{LOAD(BUCK)}$ = 1A; $V_{OUT(BUCK)}$ = 1.5V

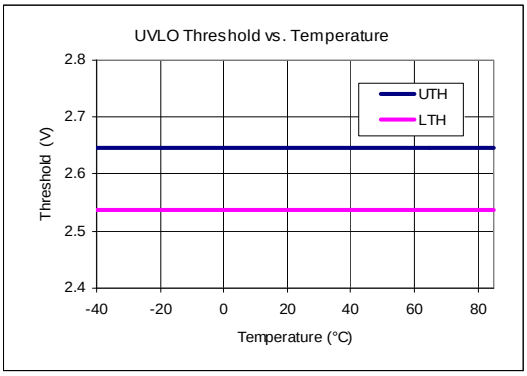
# 5.7 Temperature

**Figure 42: Supply Current vs. Temperature**



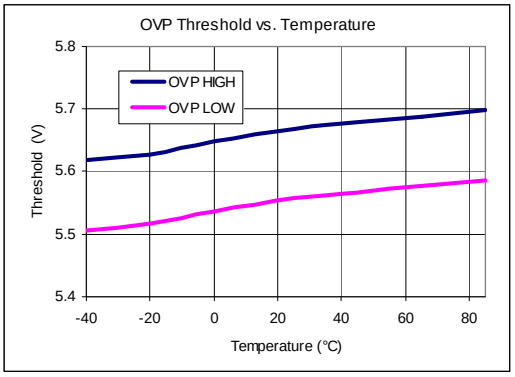

$V_{IN}$ = 3.6V; $I_{LOAD(BUCK)}$ = No Load

**Figure 43: UVLO Threshold vs. Temperature**



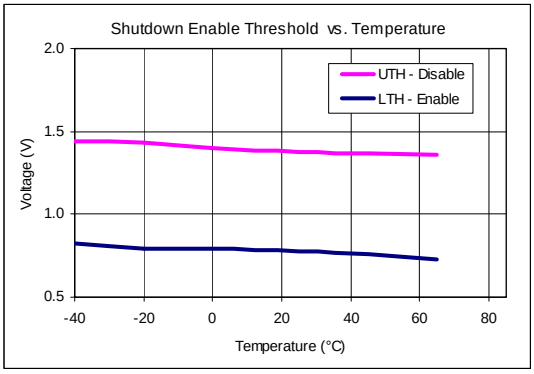

$I_{LOAD(BUCK)}$ = 10mA

**Figure 44: OVP Threshold vs. Temperature**



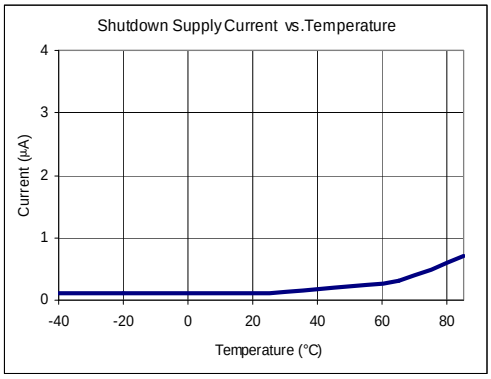

$I_{LOAD(BUCK)}$ = 10mA

**Figure 45: Shutdown Enable Threshold vs. Temperature**




$V_{IN}$ = 3.6V; $I_{LOAD(BUCK)}$ = 10mA;$V_{OUT\ (BUCK)}$ = 1.5V; $V_{EN}$ = $V_{IN}$

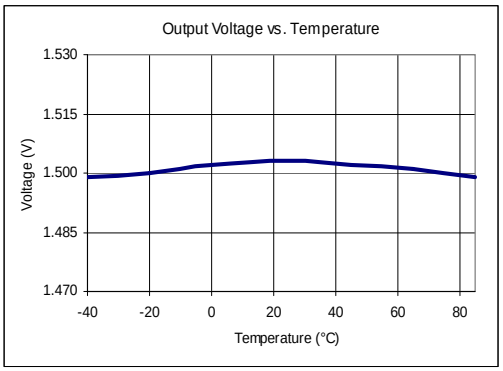
### Figure 46: Shutdown Supply Current vs. Temperature




$V_{IN}$ = 3.6V; $I_{LOAD(BUCK)}$ = No Load; $V_{EN}$= 0V; $V_{SHDN}$ = $V_{IN}$

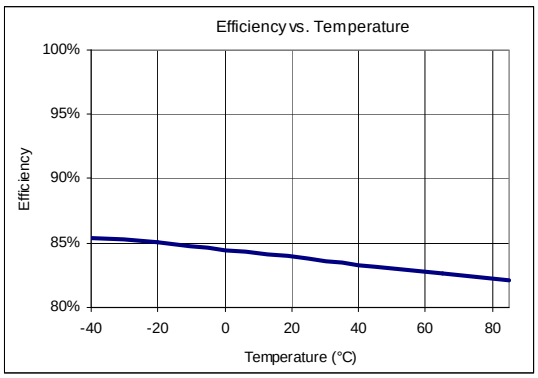
. .

### Figure 47: Output Voltage vs. Temperature



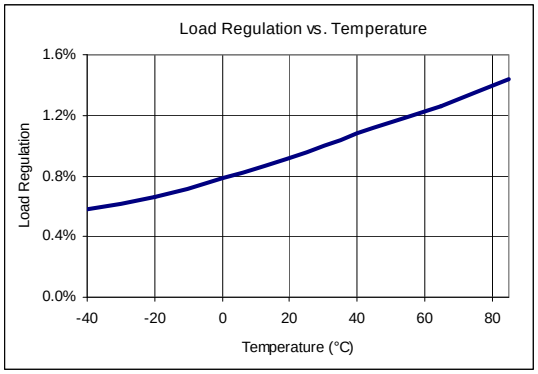

$V_{IN}$ = 3.6V; $I_{LOAD(BUCK)}$ = 500mA

### Figure 48: Efficiency vs. Temperature



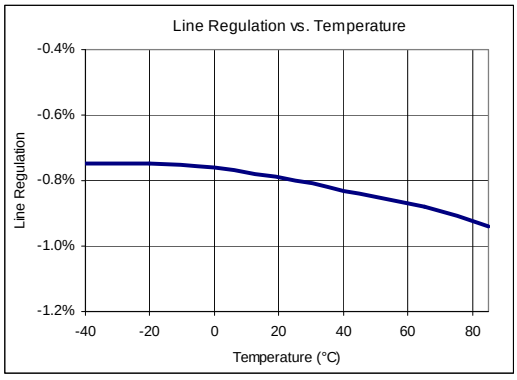

$V_{IN}$ = 3.6V; $V_{OUT(BUCK)}$ = 1.5V; $I_{LOAD(BUCK)}$ = 1A

### Figure 49: Load Regulation vs. Temperature




$V_{IN}$ = 5V; $I_{LOAD(BUCK)}$ = 500mA-2A;
$V_{OUT(BUCK)}$ = 1.5V

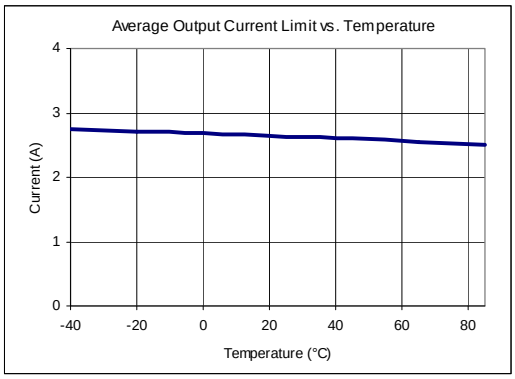
### Figure 50: Line Regulation vs. Temperature




$V_{IN}$ = 3V-5V; $I_{LOAD(BUCK)}$ = 1A;
$V_{OUT(BUCK)}$ = 1.5V

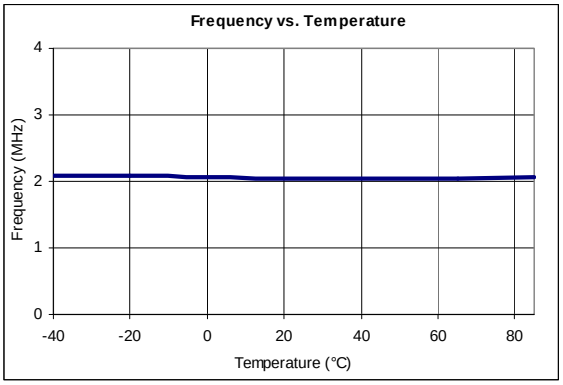
.

**Figure 51: Average Output Current Limit vs. Temperature**




$V_{IN}$ = 3.6V; $V_{OUT(BUCK)}$ = 1.5V

**Figure 52: Frequency vs. Temperature**




$V_{IN}$ = 3.6V; $V_{OUT(BUCK)}$ = 1.5V; $I_{LOAD(BUCK)}$ = 1A

# 6 Applications Information

## 6.1 Inductor and Output capacitance recommendations

When operating in PFM mode (PFM pin = SVIN), it is recommended to use inductor values operating at the specified output voltage range in Table 11. The recommended output capacitance is 22µF. Additional output capacitance can be used but the LC product do not exceed 5 × (1.3µH) × (28.6µF).

**Table 11: Capacitance Recommendations**

| $V_{OUT}$ Range | L Values |
|---|---|
| 0.64V =< Vout =< 1.32V | L = 1.0µH +/-30% |
| 1.20V =< Vout =< 1.96V | L = 1.8µH +/-30% |
| 2.00V =< Vout =< 3.33V | L = 2.2µH +/-30% |

When operating in PWM mode (PFM pin = SGND), it is recommended to use inductor values L > 1.0µH -30% for output voltage range and LC product do not exceed 5 × (1.3µH) × (28.6µF).

## 6.2 PC Board Layout Concideration and Guidelines

| | |
|---|---|
| ! | **Caution: To avoid noise and abnormal operating behavior, follow these layout recommendations** |

The PC board layout is very critical in any switching converter. An improper layout can contribute to system instability, excessive Electromagnetic Interference (EMI), and high switching loss. Follow these basic guidelines for good PC layout:

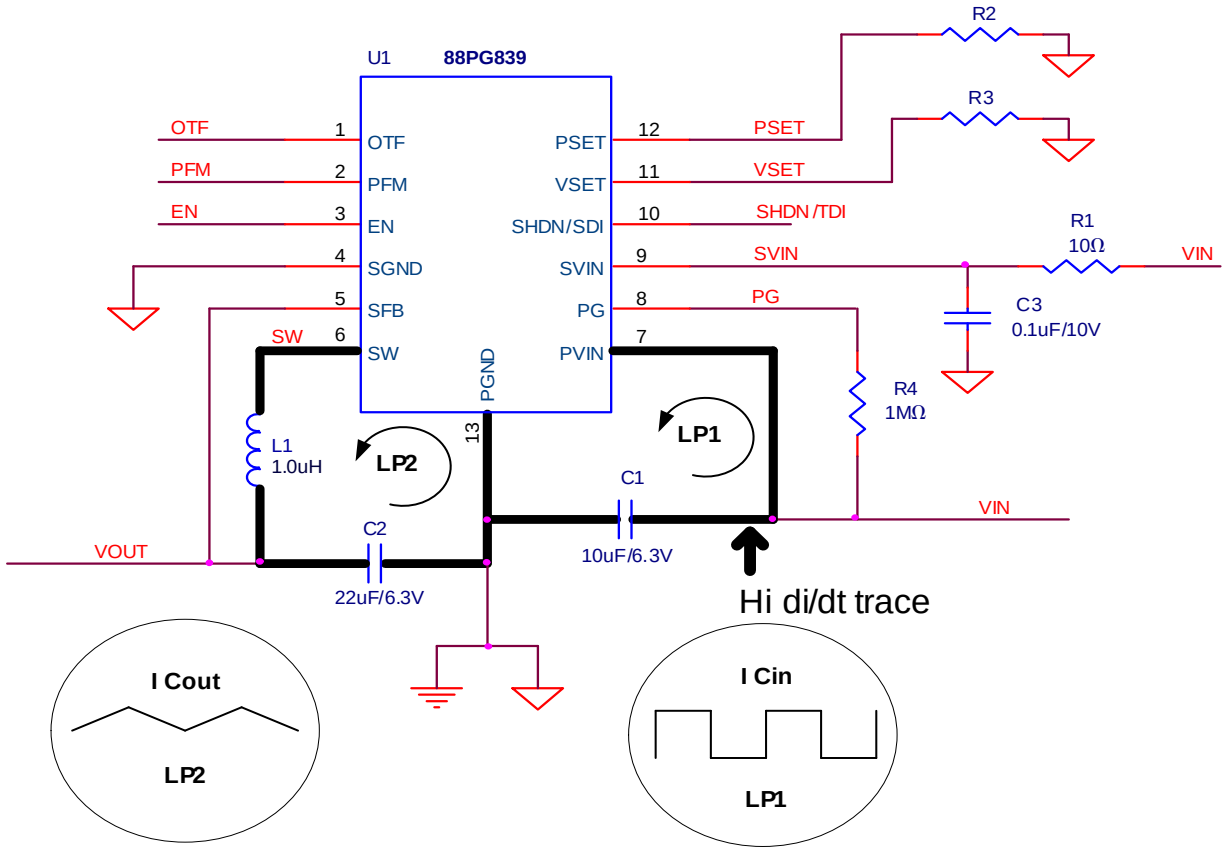
1. Do not lay out the inductor first. **The input capacitor placement is the most critical for proper operation.** The AC current circulating through the input capacitor and loop 1 (LP1) are square wave with rise and fall times of 8ns and slew rates as high as 300A/µs (see Figure 53). At these fast slew rates, stray PCB inductance can generate a voltage spike as high as 3V per inch of PCB trace, $V_{IND}$ = L × di/dt. **Therefore, the Ceramic input capacitor must be place as close as possible to the PVIN and PGND pins with as short and wide trace as possible.** Also, the PVIN and PGND traces must be placed on the top layer. This will isolate the fast AC currents from interfering with the analog ground plane.
2. Keep loop 2 (LP2) as small as possible and connect the (-) terminal of the output capacitor as close to the (-) terminal of the input capacitor. A back-to-back placing of bypass capacitors, as shown in Figure 53, is recommended for best results.
3. This is a 2-layer board with 1 ground plane and 1 routing layer.
4. Copy the routing layer in Figure 54 on page 50 as much as possible and place it on the top layer. The ground plane in Figure 55 on page 51 can be placed on any other layer. Use the recommend BOM in Section 6.3, Bill of Materials, on page 52. Contact the factory if substitutions are made.
5. Review the recommended solder pad layout and notes in Figure 57 on page 54. Make sure that you place a dot on the top silk screen to indicate the location of pin 1, see Figure 54. Ensure

that the dot is outside the package outline. This way you can visually inspect the package orientation after assembly.

6. Do not replace the Ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor as long as the Ceramic input capacitor is placed next to the IC.
7. Use either X7R or X5R type ceramic capacitors.
8. Any type of capacitor can be placed in parallel with the output capacitor.
9. Low-ESR capacitors like the POSCAP from Sanyo can replace the Ceramic output capacitors as long as the capacitor value is the same or greater. Note that the Ceramic capacitors provide the lowest noise and smallest foot print solution.
10. Use planes for the ground, input and outputs power to maintain good voltage filtering and to keep power losses low.
11. If there is not enough space for a power plane for the input supply, then the input supply trace must be at least 3/8 inch wide.
12. If there is not enough space for a power plane for the output supplies, then place the output as close to the load as possible with a trace of at least 3/8 inch wide.

13. The device has two internal grounds, analog (SGND) and power (PGND). The analog ground ties to all the noise sensitive signals (VSET, and SVIN) while the power ground ties to the higher current power paths. Noise on an analog ground can cause problems with the IC's internal control and bias signals. For this reason, separate analog and power ground traces are recommended. The signal ground is connected to the power ground at one point, which is the (-) terminal of the output capacitor.
14. Keep the switching node (SW) away from the SFB pin and all sensitive signal nodes, minimizing capacitive coupling effects. If the SFB trace must cross the SW node, cross it at a right angle.
15. Try not to route analog or digital lines in close proximity to the power supply, especially the SW node. If this can't be avoided, shield these lines with a power plane placed between the SW node and the signal lines.
16. The type of solder paste recommended for QFN packages is "No clean", due to the difficulty of cleaning flux residues from beneath the QFN package.

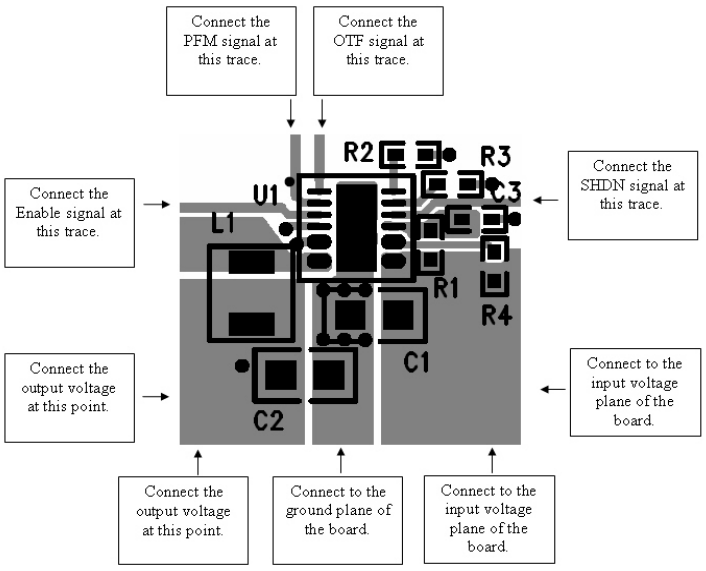
**Figure 53: PCB Board Schematic**



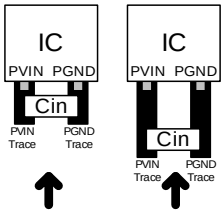
## 6.2.1 PC Board Layout Examples

- Actual board size = 580 mil x 540 mil
- Total copper layers = 2 (Top and Bottom)
- All the components are on the top layer

**Figure 54: Top Silk Screen, Top Traces, Vias, and Copper (Not to scale)**

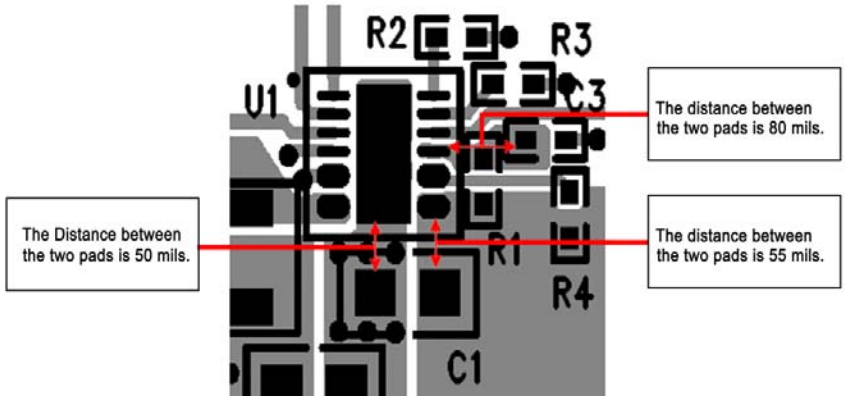



Example placement for input capacitors



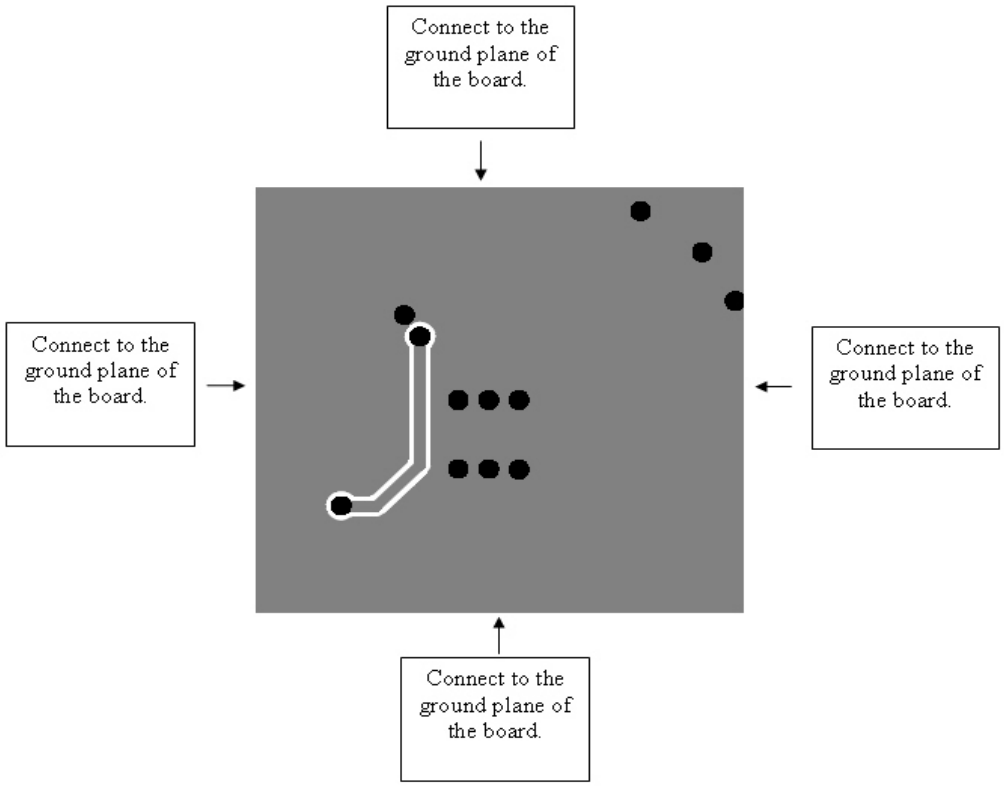

Yes **No**

**All input capacitors (Cin) must place close to the IC !!!!**



.

**Figure 55: Bottom Silk Screen, Top Traces, Vias, and Copper (Not to scale)**



## 6.3 Bill of Materials

**Table 12: BOM**

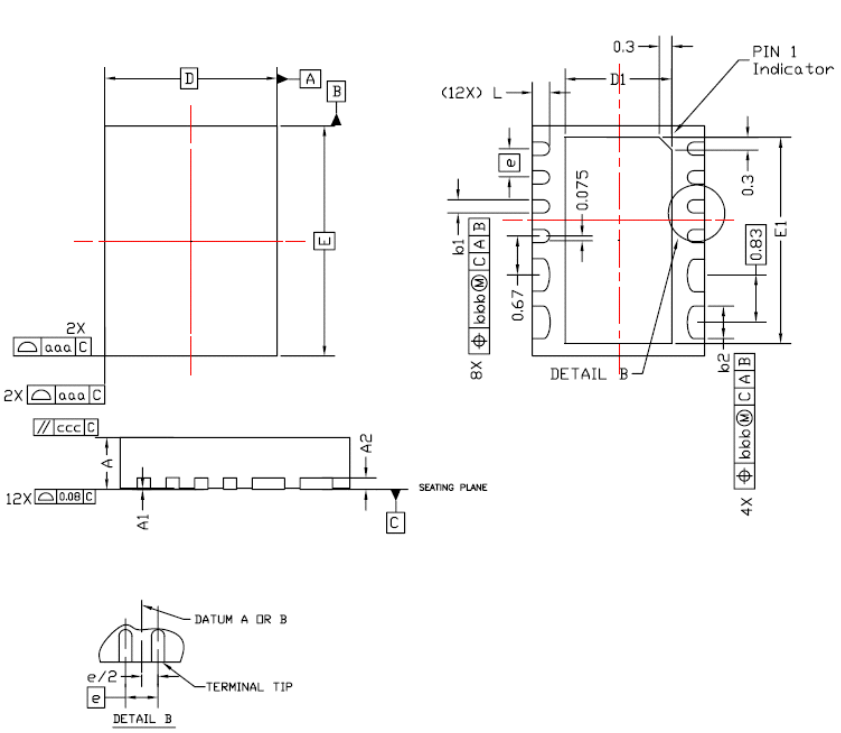
| Item | Qty | Ref | Manufacturer Part Number | Manufacturer | Description |
|---|---|---|---|---|---|
| **1** | **1** | **U1** | **88PG839** | **Marvell** | **Ultra Low Power, 2MHz, 2A Output Current Field Programmable Hysteretic Step-Down Switching Regulator** |
| 2 | 1 | C1 | GRM219R60J106KE19D | Murata | CAP CER 10µF 6.3V X5R 10% 0805 |
| 3 | 1 | C2 | GRM21BR60J226ME39L | Murata | CAP CER 22µF 6.3V X5R 20% 0805 |
| 4 | 1 | C3 | C1005X5R1A104K | TDK Corporation | CAP CER .10µF 10V X5R 10% 0402 |
| 5 | 1 | L1 | 1071AS-1R0N | TOKO | DE2815C Series, 1.0µH, 2.10A, 40mΩ, H=1.5mm, L=3.0mm, W=3.2mm |
| 6 | 1 | R1 | ERJ-2RKF10R0X | Panasonic ECG | RES 10.0Ω 1/16W 1% 0402 SMD |
| 7 | 1 | R2 | | | See Table 10, VSET and PSET Programming Table for 5% Resistors, on page 25, 1/16W 1% 0402 SMD |
| 8 | 1 | R3 | | | See Table 10, VSET and PSET Programming Table for 5% Resistors, on page 25, 1/16W 1% 0402 SMD |
| 9 | 1 | R4 | CRCW04021M00FKTD | Vishay/Dale | RES 1.00MΩ 1/16W 1% 0402 SMD |

**Table 13: BOM for Microsoft Application**

| Item | Qty | Ref | Manufacturer Part Number | Manufacturer | Description |
|---|---|---|---|---|---|
| **1** | **1** | **U1** | **88PG839** | **Marvell** | **Ultra Low Power, 2MHz, 2A Output Current Field Programmable Hysteretic Step-Down Switching Regulator** |
| 2 | 1 | C1 | GRM219R60J106KE19D | Murata | CAP CER 10µF 6.3V X5R 10% 0805 |
| 3 | 3 | C2 | GRM21BR60J226ME39L | Murata | CAP CER 22µF 6.3V X5R 20% 0805 |
| 4 | 1 | C3 | C1005X5R1A104K | TDK Corporation | CAP CER .10µF 10V X5R 10% 0402 |
| 5 | 1 | L1 | VLCF4028T-3R3N1R6-2 | TDK Corporation | VLCF Series, 3.3µH, 2.31A, 48mΩ, H=2.8mm, L=4.0mm, W=4.0mm |
| 6 | 1 | R1 | ERJ-2RKF10R0X | Panasonic ECG | RES 10.0Ω 1/16W 1% 0402 SMD |
| 7 | 1 | R2 | | | See Table 10 on page 25, 1/16W 1% 0402 SMD |
| 8 | 1 | R3 | | | See Table 10 on page 25, 1/16W 1% 0402 SMD |
| 9 | 1 | R4 | CRCW04021M00FKTD | Vishay/Dale | RES 1.00MΩ 1/16W 1% 0402 SMD |

# 7.1 Mechanical Drawings

**Figure 56: 3mm x 4mm 12-Lead DFN Mechanical Drawing**




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | | 0.20 REF | | | 0.008 REF | |
| b1 | 0.18 | 0.23 | 0.28 | 0.007 | 0.009 | 0.011 |
| b2 | 0.51 | 0.56 | 0.61 | 0.020 | 0.022 | 0.024 |
| D | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| D1 | 1.60 | 1.70 | 1.80 | 0.063 | 0.067 | 0.071 |
| E | 3.90 | 4.00 | 4.10 | 0.153 | 0.157 | 0.161 |
| E1 | 3.40 | 3.50 | 3.60 | 0.134 | 0.138 | 0.142 |
| e | | 0.50 BSC | | | 0.020 BSC | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| aaa | --- | --- | 0.15 | --- | --- | 0.006 |
| bbb | --- | --- | 0.10 | --- | --- | 0.004 |
| ccc | --- | --- | 0.10 | --- | --- | 0.004 |

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSED JEDEC MO-220.

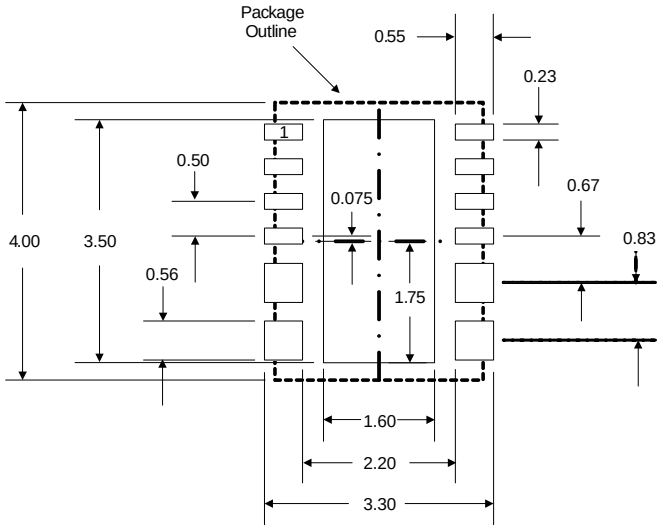
**Notes:**

- All dimensions in mm.
- See Section 8, Part Order Numbering/Package Marking, on page 55 for package marking and pin 1 location.

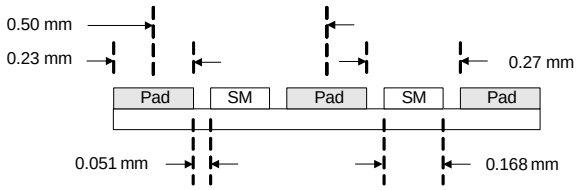
# 7.2 Typical Pad Layout Dimensions

## 7.2.1 Recommended Solder Pad Layout

**Figure 57: 3mm x 4mm DFN-12 Land Pattern (mm)**




3x4 DFN-12
Land Pattern (mm)




DFN Lead with
Non-Solder Mask Defined Terminal

**Note**

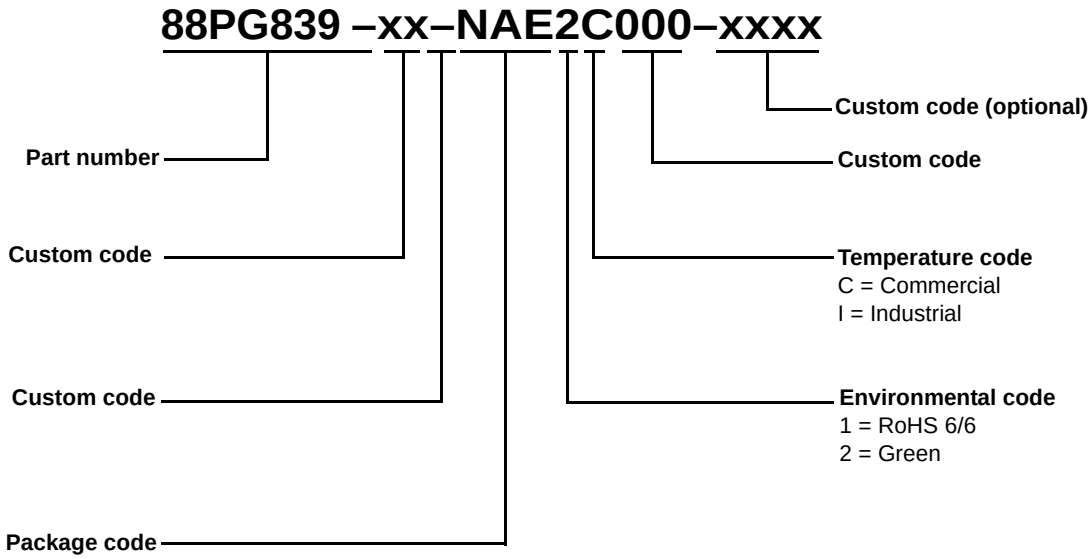
- Top view
- The “1” indicates pin 1
- Drawing not to scale
- Oversize solder mask (SM) by 4 mils over pad size (2 mil annular ring)
- 0.168mm solder mask between pads
- Tolerance ±0.05mm

# 8 Part Order Numbering/Package Marking

## 8.1 Part Order Numbering Scheme

Figure 58 shows the part order numbering scheme. Refer to a Marvell Field Application Engineer (FAE) or sales representative for further information when ordering parts.

**Figure 58: Sample Part Number**




## 8.2 Part Ordering Options

The standard ordering part numbers for the respective solutions are the following:

**Table 14: Part Order Options[1]**

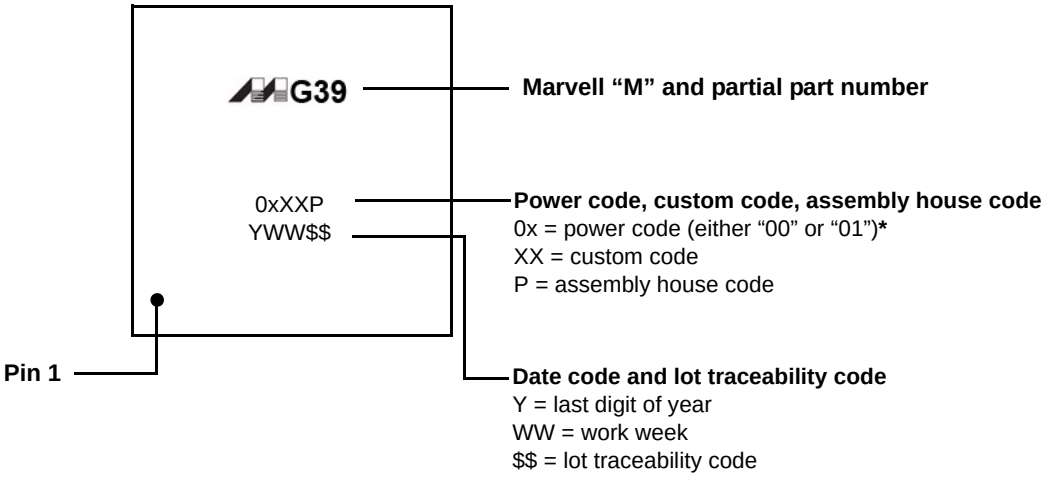
| Package Type | Part Order Number |
|---|---|
| 12-pin DFN, 3mm x 4mm | 88PG839-A1-NAE2C000-T181 |
| 12-pin DFN, 3mm x 4mm | 88PG839-A1-NAE2C000TT181 (Tape and Reel) |
| 12-pin DFN, 3mm x 4mm | 88PG839-A1-NAE2C000 |
| 12-pin DFN, 3mm x 4mm | 88PG839-A1-NAE2C000-T (Tape and Reel) |

1. Please review Table 6, Switching Step-down Regulator, on page 18 PWM Mode output voltage over temperature ratings for part order number differences.

## 8.3 Package Marking

Figure 59 shows a sample package marking and pin 1 location.

**Figure 59: Package Marking and Pin 1 Location**




The above example is not drawn to scale. Location of markings are approximate.

***Note:** The power code (either “00” or “01”) is determined by the part order number used.

- Power code “00” = Part Order Number 88PG839-A1-NAE2000-T181
- Power code “01” = Part Order Number 88PG839-A1-NAE2000

# A Revision History

**Table 15: Revision History**

| Document Type | Document Revision |
|---|---|
| Release | Rev. D |
| • Electrical Characteristics: Table 6: Changed PG Leakage Current values.<br>• Applications: Bill of Materials edits. | |


Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.752.9028

www.marvell.com

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