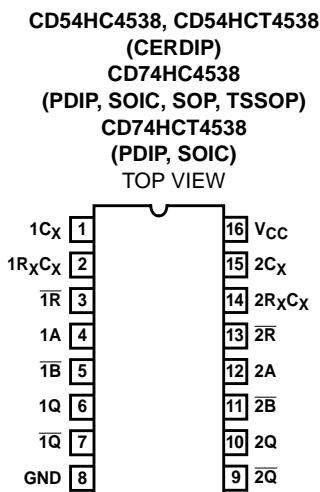


High-Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator

Features

- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of R_X , C_X
- Triggering from the Leading or Trailing Edge
- Q and \bar{Q} Buffered Outputs Available
- Separate Resets
- Wide Range of Output Pulse Widths
- Schmitt Trigger Input on A and \bar{B} Inputs
- Retrigger Time is Independent of C_X
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Pinout



Description

The 'HC4538 and 'HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor (R_X) and an external capacitor (C_X) control the timing and the accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and \bar{Q} terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of R_X and C_X .

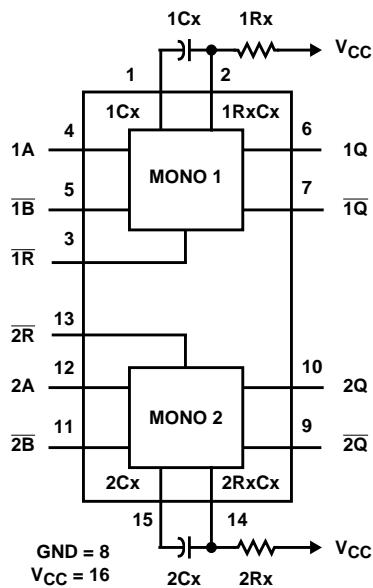
Leading-edge triggering (A) and trailing edge triggering (\bar{B}) inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to GND and an unused \bar{B} should be tied to V_{CC} . On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-triggerable mode \bar{Q} is connected to \bar{B} when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering (\bar{B}) is used. The period (τ) can be calculated from $\tau = (0.7) R_X C_X$; R_{MIN} is 5k Ω . C_{MIN} is 0pF.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4538F3A	-55 to 125	16 Ld CERDIP
CD54HCT4538F3A	-55 to 125	16 Ld CERDIP
CD74HC4538E	-55 to 125	16 Ld PDIP
CD74HC4538M	-55 to 125	16 Ld SOIC
CD74HC4538MT	-55 to 125	16 Ld SOIC
CD74HC4538M96	-55 to 125	16 Ld SOIC
CD74HC4538NSR	-55 to 125	16 Ld SOP
CD74HC4538PW	-55 to 125	16 Ld TSSOP
CD74HC4538PWR	-55 to 125	16 Ld TSSOP
CD74HC4538PWT	-55 to 125	16 Ld TSSOP
CD74HCT4538E	-55 to 125	16 Ld PDIP
CD74HCT4538M	-55 to 125	16 Ld SOIC
CD74HCT4538MT	-55 to 125	16 Ld SOIC
CD74HCT4538M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS	
\bar{R}	A	\bar{B}	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	↑	↑
H	↑	H	↑	↑

H = High Level, L = Low Level, ↑ = Transition from Low to High,

↓ = Transition from High to Low, ↑↑ One High Level Pulse,

↑↓ One Low Level Pulse, X = Irrelevant.

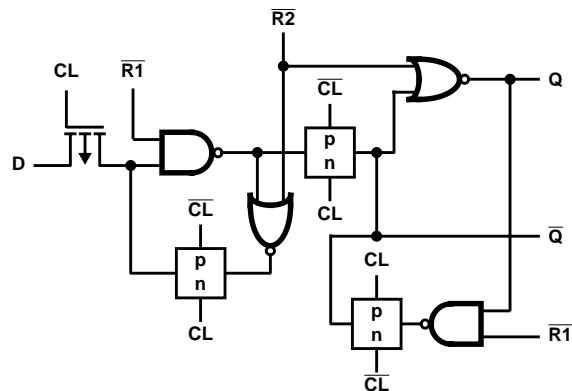


FIGURE 1. FF DETAIL

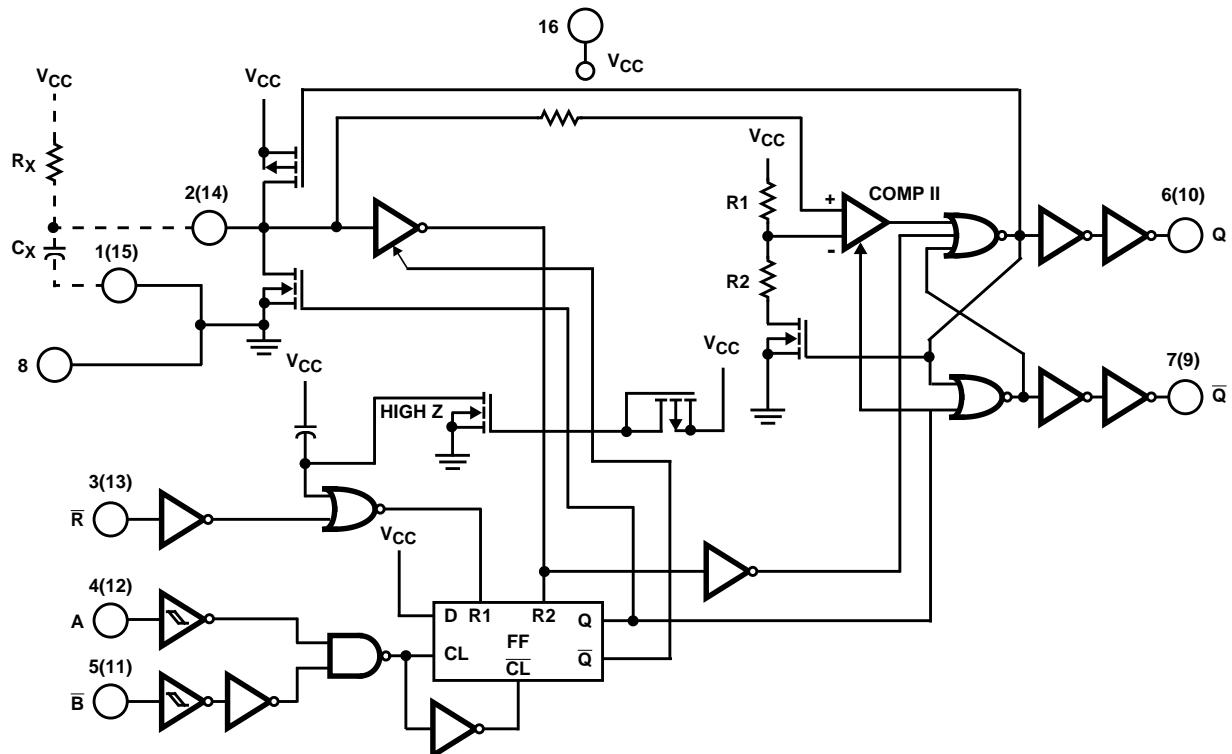


FIGURE 2. LOGIC DIAGRAM (1 MONO)

FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V _{CC} TO TERMINAL NUMBER		GND TO TERMINAL NUMBER		INPUT PULSE TO TERMINAL NUMBER		OTHER CONNECTIONS	
	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂	MONO ₁	MONO ₂
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:

1. A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
2. A non-triggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



FIGURE 3. INPUT PULSE TRAIN

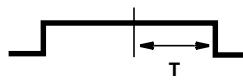


FIGURE 4. RETRIGGERABLE MODE PULSE WIDTH (A MODE)

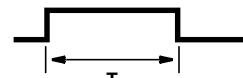


FIGURE 5. NON-RETRIGGERABLE MODE PULSE WIDTH (A MODE)

CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538

Absolute Maximum Ratings

DC Supply Voltage, V _{CC}	-0.5V to 7V
DC Input Diode Current, I _{IK}		
For V _I < -0.5V or V _I > V _{CC} + 0.5V	±20mA
DC Output Diode Current, I _{OK}		
For V _O < -0.5V or V _O > V _{CC} + 0.5V	±20mA
DC Output Source or Sink Current per Output Pin, I _O		
For V _O > -0.5V or V _O < V _{CC} + 0.5V	±25mA
DC V _{CC} or Ground Current, I _{CC}	±50mA

Thermal Information

Package Thermal Impedance, θ _{JA} (see Note 5):	
E (PDIP) Package
M (SOIC) Package
NS (SOP) Package
PW (TSSOP) Package
Maximum Junction Temperature 150°C
Maximum Storage Temperature Range -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) 300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T _A	-55°C to 125°C
Supply Voltage Range, V _{CC} (Note 3)		
HC Types2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V _I , V _O	0V to V _{CC}
Input Rise and Fall Times, t _r , t _f		
Reset Input:		
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)
Trigger Inputs A or B:		
2V	Unlimited (Max)
4.5V	Unlimited (Max)
6V	Unlimited (Max)
External Timing Resistor, R _X (Note 4)5kΩ (Min)
External Timing Capacitor, C _X (Note 4)	0 (Min)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Unless otherwise specified, all voltages are referenced to ground.
- The maximum allowable values of R_X and C_X are a function of leakage of capacitor C_X, the leakage of the 'HC4538, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 30mA. Susceptibility to externally induced noise signals may occur for R_X > 1MΩ.
- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V

CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
		TTL Loads	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current A, B, R	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Input Leakage Current R _X C _X (Note 6)			-	6	-	-	±0.05	-	±0.5	-	±0.5	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	µA
Active Device Current Q = High & Pins 2, 14 at V _{CC} /4	I _{CC}	V _{CC} or GND	0	6	-	-	0.6	-	0.8	-	1	mA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Input Leakage Current R _X C _X (Note 6)			-	5.5	-	-	±0.05	-	±0.5	-	±0.5	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Active Device Current Q = High & Pins 2, 14 at V _{CC} /4	I _{CC}	V _{CC} or GND	0	5.5	-	-	0.6	-	0.8	-	1	mA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 7)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTES:

6. When testing I_{IL} the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.
7. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538

HCT Input Loading Table

INPUT	UNIT LOADS
All	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g.
360 μ A max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HC TYPES												
Input Pulse Widths A, \bar{B}	t _{WH} , t _{WL}	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
\bar{R}	t _{WL}	2	80	-	-	100	-	-	120	-	-	ns
		4.5	16	-	-	20	-	-	24	-	-	ns
		6	14	-	-	17	-	-	20	-	-	ns
Reset Recovery Time	t _{REC}	2	5	-	-	5	-	-	5	-	-	ns
		4.5	5	-	-	5	-	-	5	-	-	ns
		6	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t _{rT}	5	-	175	-	-	-	-	-	-	-	ns
HCT TYPES												
Input Pulse Widths A, \bar{B}	t _{WH} , t _{WL}	4.5	16	-	-	20	-	-	24	-	-	ns
		\bar{R}	t _{WL}	4.5	20	-	-	25	-	-	30	-
Reset Recovery Time	t _{REC}	4.5	5	-	-	5	-	-	5	-	-	ns
Retrigger Time (Figure 11)	t _{rT}	5	-	175	-	-	-	-	-	-	-	ns

CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538

Switching Specifications $C_L = 50\text{pF}$, Input $t_r, t_f = 6\text{ns}$, $R_X = 10\text{K}\Omega$, $C_X = 0$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC} (\text{V})$	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay A, \bar{B} to Q	t_{PLH}	$C_L = 50\text{pF}$	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	43	-	54	-	64	ns
A, \bar{B} to \bar{Q}	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	43	-	54	-	64	ns
\bar{R} to Q	t_{PHL}	$C_L = 50\text{pF}$	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	43	-	54	-	64	ns
\bar{R} to \bar{Q}	t_{PLH}	$C_L = 50\text{pF}$	2	-	-	250	-	315	-	375	ns
			4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	43	-	54	-	64	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Output Pulse Width $R_X = 10\text{k}$, $C_X = 0.1\mu\text{F}$	τ	$C_L = 50\text{pF}$	3	0.64	-	0.78	0.612	0.812	0.605	0.819	ms
			5	0.63	-	0.77	0.602	0.798	0.595	0.805	ms
Output Pulse Width Match, Same Package	-	-		-	± 1	-	-	-	-	-	%
Power Dissipation Capacitance (Notes 8, 9)	C_{PD}	$C_L = 15\text{pF}$	5	-	136	-	-	-	-	-	pF
Input Capacitance	C_I	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10	pF
HCT TYPES											
Propagation Delay A, \bar{B} to Q	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
A, B to Q	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns

CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538

Switching Specifications $C_L = 50\text{pF}$, Input $t_r, t_f = 6\text{ns}$, $R_X = 10\text{K}\Omega$, $C_X = 0$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX
\bar{R} to Q	t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	ns
\bar{R} to \bar{Q}	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22
Output Pulse Width $R_X = 10\text{k}$, $C_X = 0.1\mu\text{F}$	τ	$C_L = 50\text{pF}$	5	0.63	-	0.77	0.602	0.798	0.595	0.805
Output Pulse Width Match, Same Package		-	-	-	-	± 1	-	-	-	%
Power Dissipation Capacitance (Notes 8, 9)	C_{PD}	$C_L = 15\text{pF}$	5	-	134	-	-	-	-	pF
Input Capacitance	C_I	$C_L = 50\text{pF}$	-	10	-	10	-	10	-	10

NOTES:

8. C_{PD} is used to determine the dynamic power consumption, per one shot.
9. $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \sum (C_L V_{CC}^2 f_O)$ where f_i = input frequency, f_O = output frequency, C_L = output load capacitance, C_X = external capacitance V_{CC} = supply voltage assuming $f_i \ll \frac{1}{\tau}$

Test Circuits and Waveforms

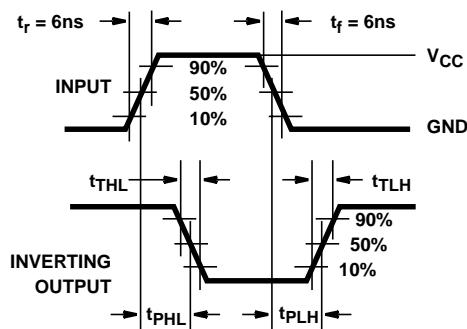


FIGURE 6. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

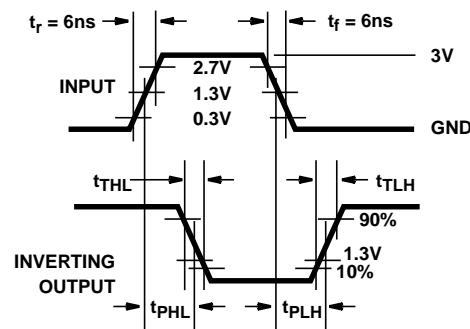


FIGURE 7. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Typical Performance Curves

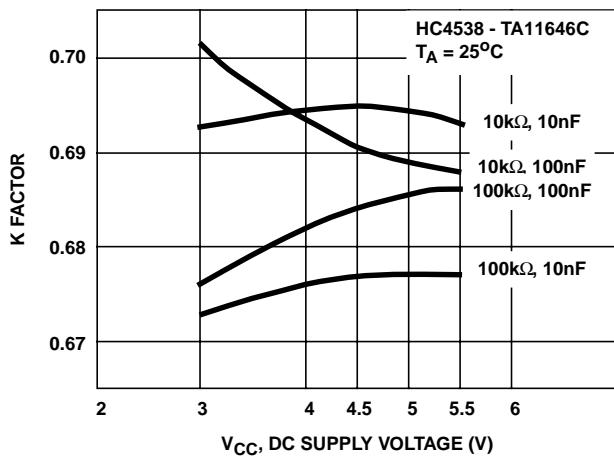


FIGURE 8. K FACTOR vs DC SUPPLY VOLTAGE (V_{CC}) - V

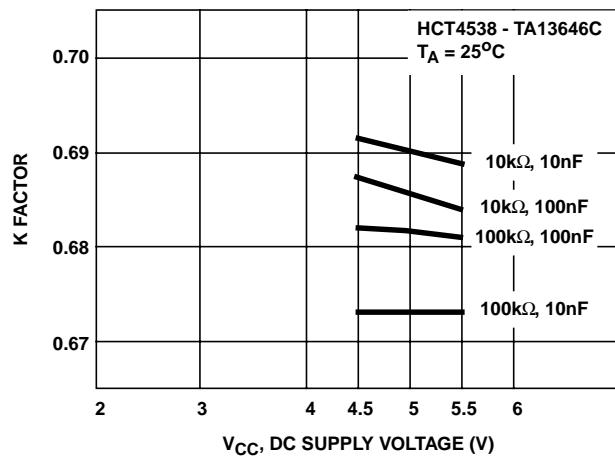


FIGURE 9. K FACTOR vs DC SUPPLY VOLTAGE (V_{CC}) - V

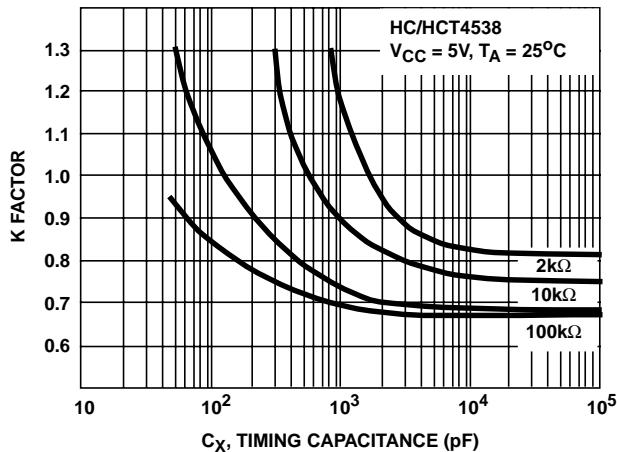


FIGURE 10. K FACTOR vs C_X

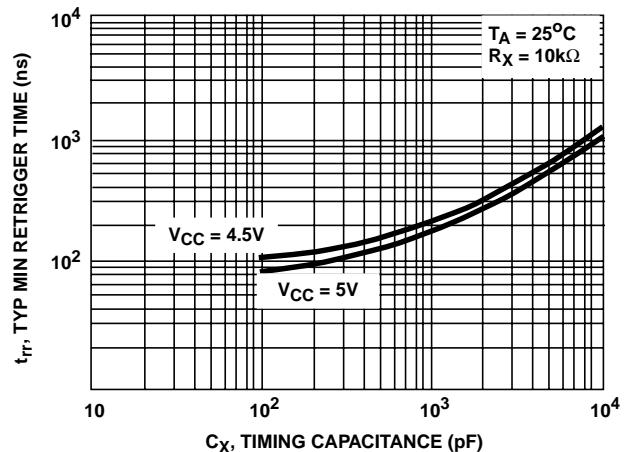


FIGURE 11. MINIMUM RETRIGGER TIME vs TIMING CAPACITANCE

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is $\geq 0.5\mu F$, a protection diode with a 1 ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Figure 12.

An alternate protection method is shown in Figure 13, where a 51Ω current-limiting resistor is inserted in series with C_X . Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

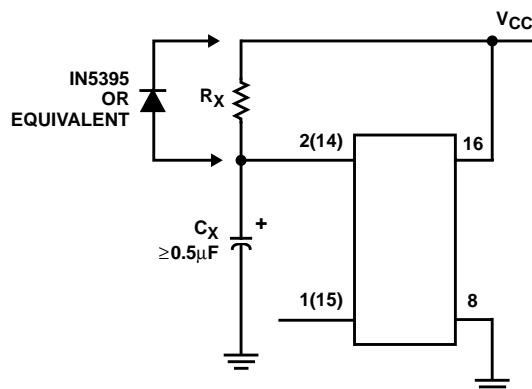


FIGURE 12. RAPID POWER-DOWN PROTECTION CIRCUIT

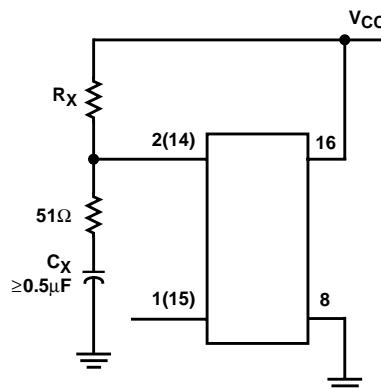


FIGURE 13. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8688601EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4538F	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4538F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HCT4538F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD74HC4538E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4538EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4538M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4538PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4538E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4538EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4538M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4538M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4538M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4538ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
no Sb/Br)								
CD74HCT4538MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4538MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

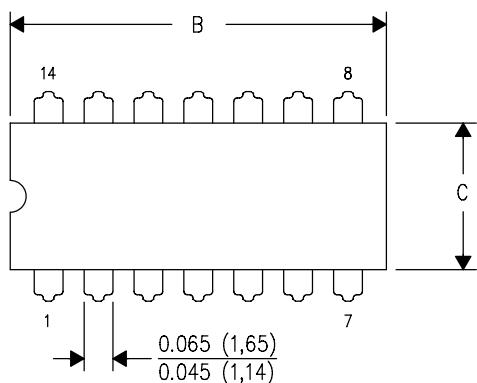
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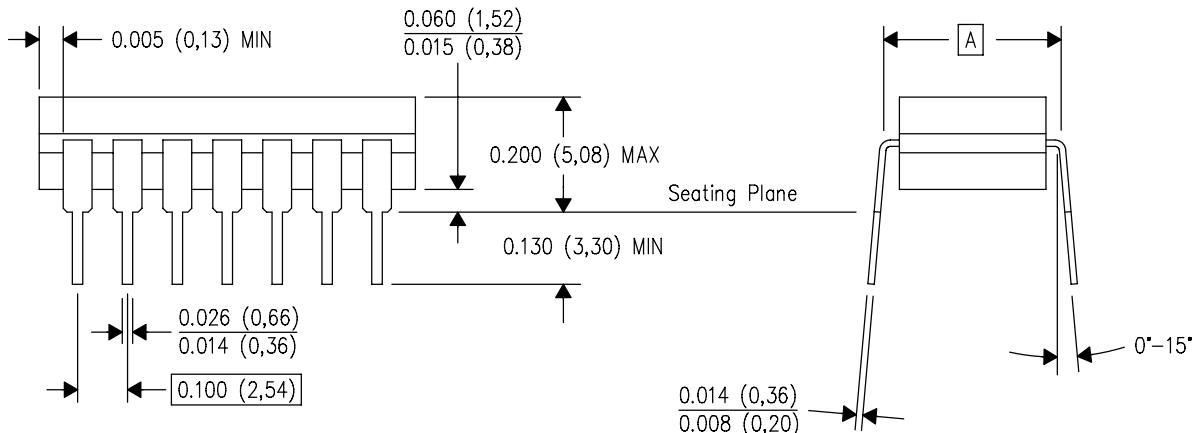
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



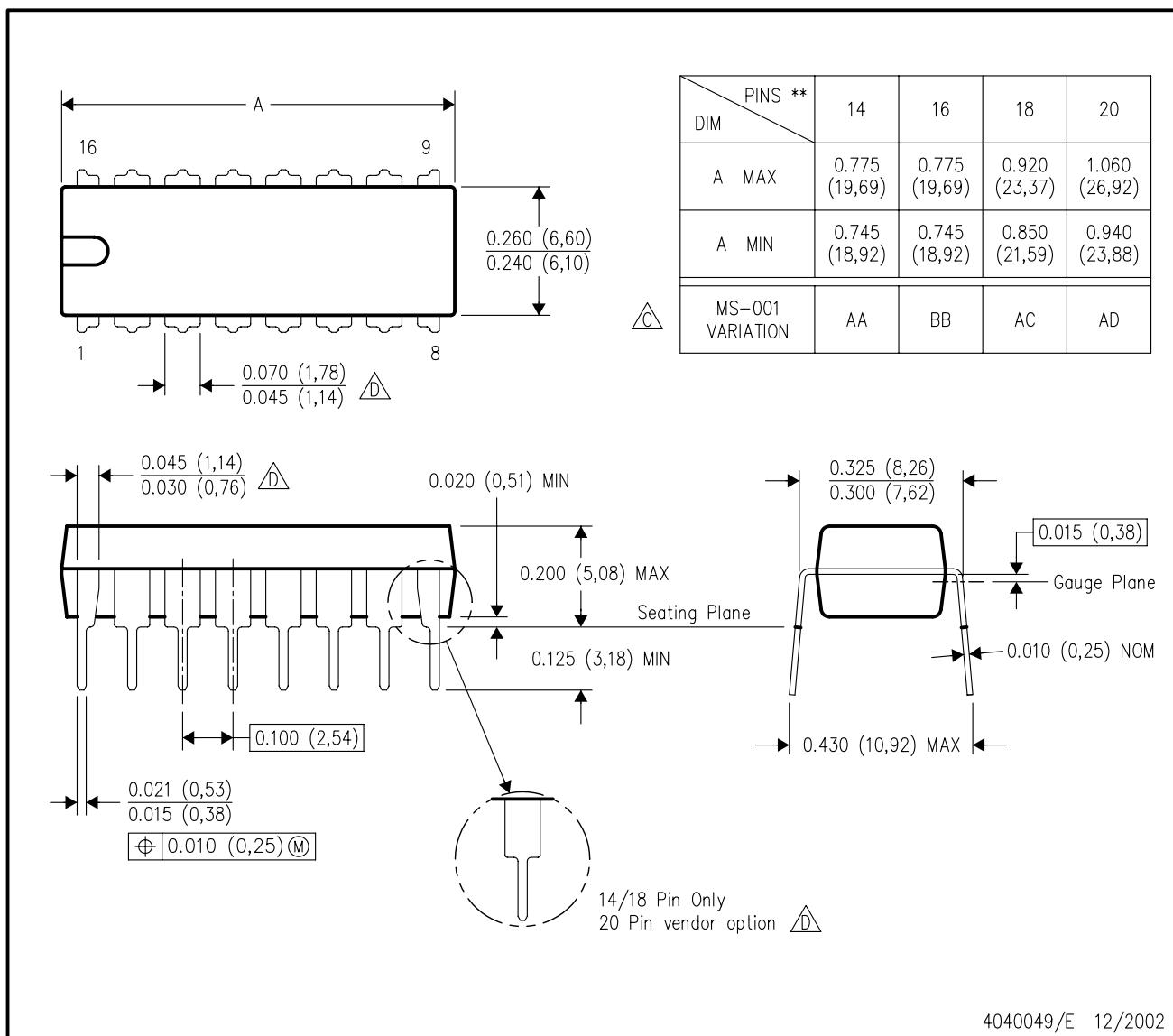
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

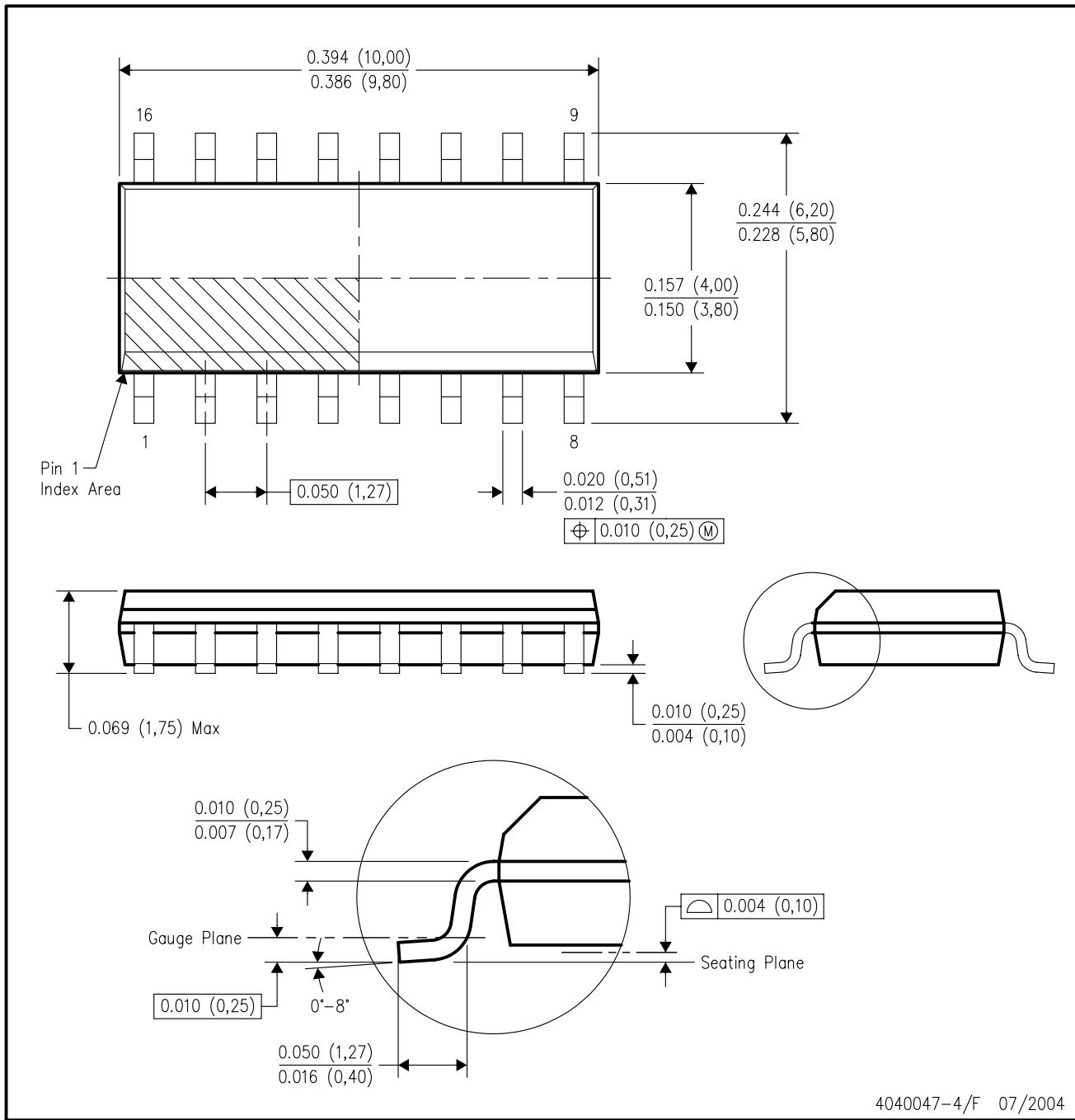
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

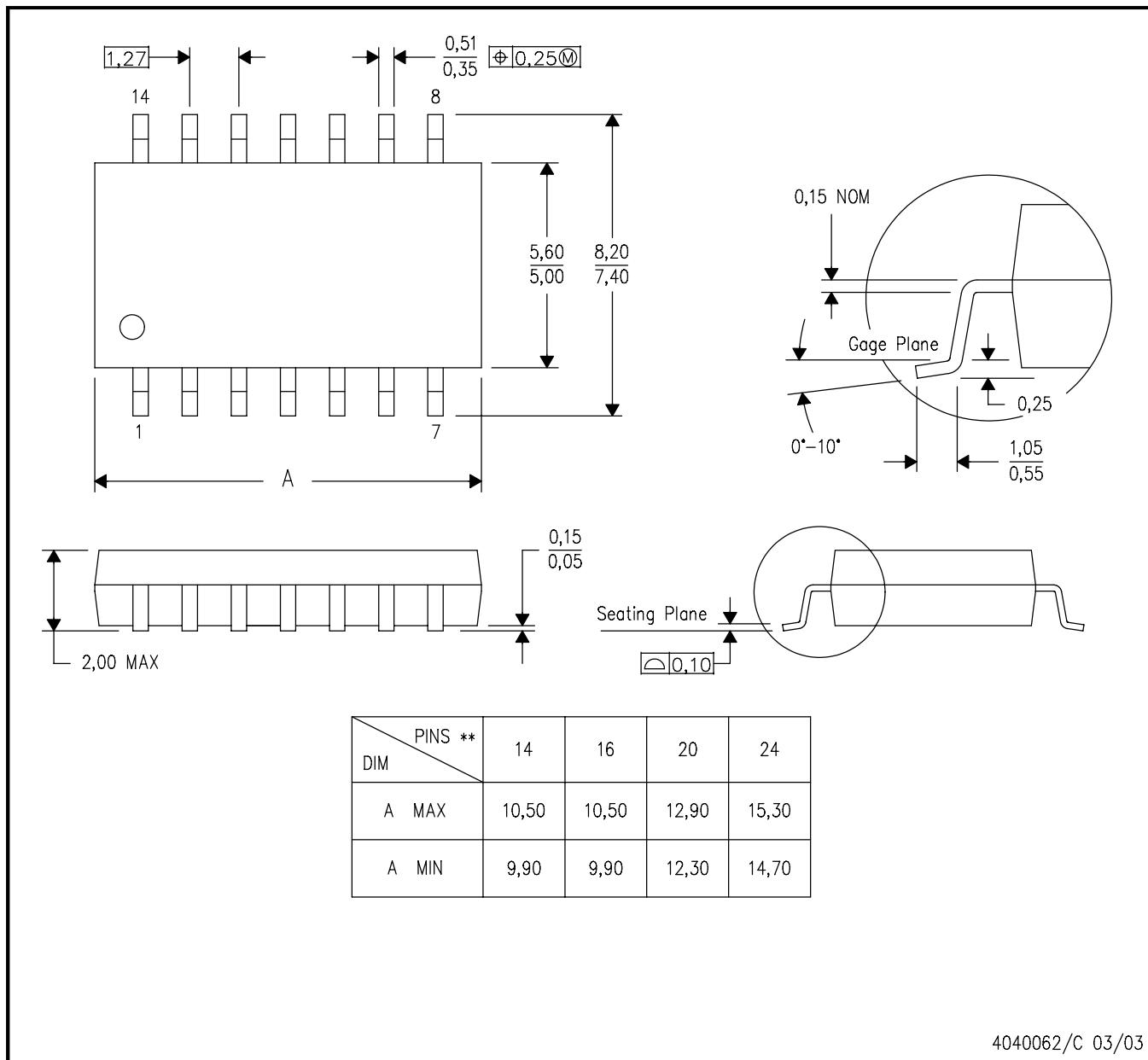
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

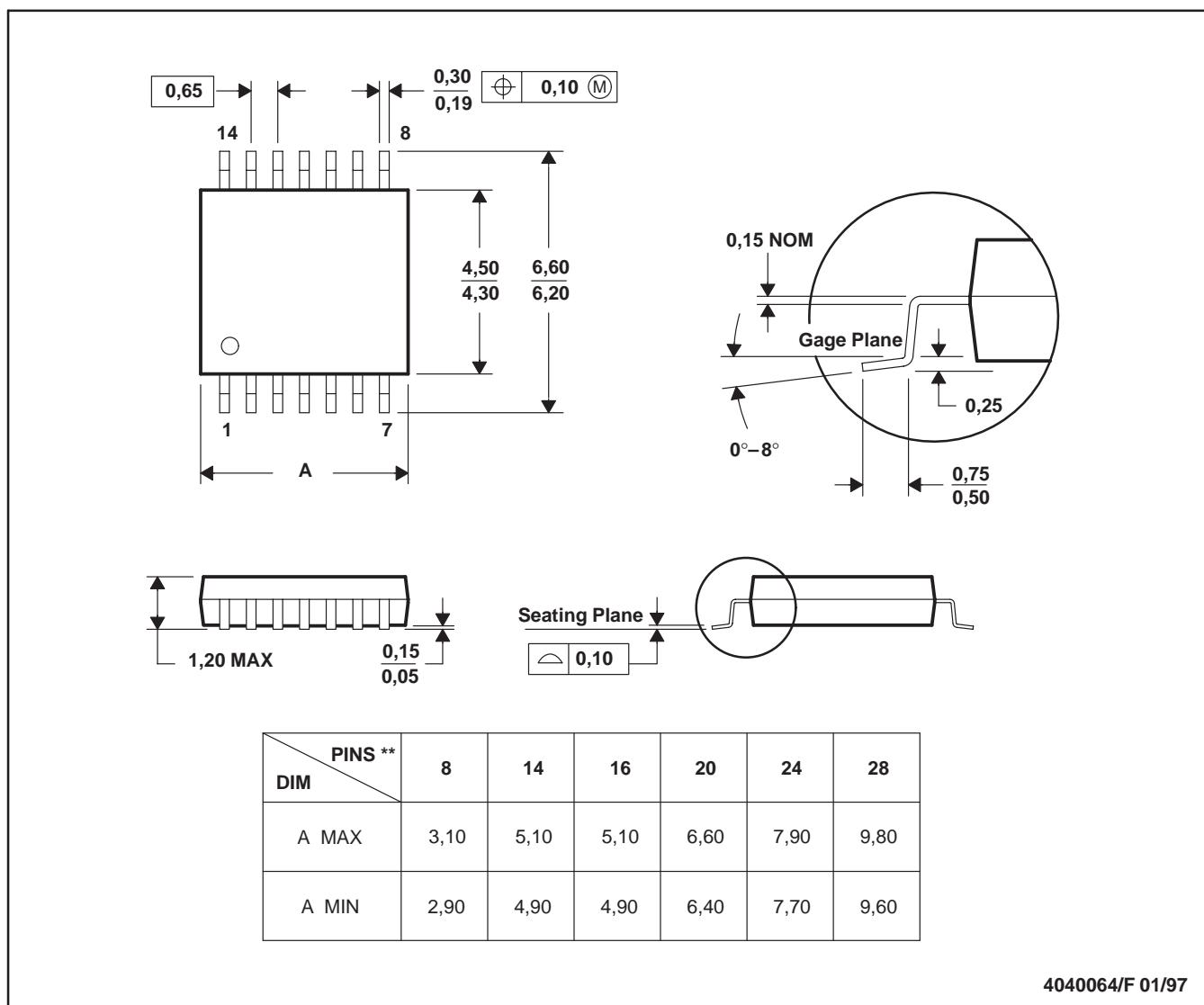


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.15.
 - Falls within JEDEC MO-153

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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CD74HC4538, Status: ACTIVE

High Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrators

 View ROHS Compliant Devices clear gif

View RoHS Compliant Devices

 clear gif clear gif Features Quality & Pb-Free Data Related Products Tools & Software Samples Pricing/Packaging Inventory Symbols/Footprints Technical Documents Applications Notes Simulation Models Reference Designs Refine Your Selection

- Logic: Monostable Mu

Support

- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomencla

Datasheet Dow nload Datasheet

CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538 (Rev. E) (cd74hc4538.pdf, 382 KB)

16 Oct 2003 Download

	CD54HC4538	CD74HC4538
Voltage Nodes(V)	6, 5, 2	2, 5, 6
Vcc range(V)		2 to 6
	Samples	Samples
	Inventory	Inventory

Product Information Features Save this to your personal library

Retriggerable/Resettable Capability

Trigger and Reset Propagation Delays Independent of Rx, Cx

Triggering from the Leading or Trailing Edge

Q and Q\ Buffered Outputs Available

Separate Resets

Wide Range of Output Pulse Widths

Schmitt Trigger Input on A and B\ Inputs

Retrigger Time is Independent of Cx

Fanout (Over Temperature Range)

- Standard Outputs 10 LSTTL Loads

Bus Driver Outputs 15 LSTTL Loads

Wide Operating Temperature Range . . . -55°C to 125°C

Balanced Propagation Delay and Transition Times

Significant Power Reduction Compared to LSTTL Logic ICs

HC Types

2V to 6V Operation

- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V

HCT Types

- 4.5V to 5.5V Operation

Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)- CMOS Input Compatibility, I_I = 1μA at V_{OL}, V_{OH} Description

The 'HC4538 and 'HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor (Rx) and an external capacitor (Cx) control the timing and the accuracy for the circuit. Adjustment of Rx and Cx provides a wide range of output pulse widths from the Q and Q\ terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of Rx and Cx.

Leading-edge triggering (A) and trailing edge triggering (B)\ inputs are provided for triggering from either edge of the input pulse. An unused "A" input should be tied to GND and an unused B\ should be tied to V_{CC}. On power up the IC is reset. Unused resets and sections must be terminated. In normal operation

the circuit retriggers on the application of each new trigger pulse. To operate in the non-triggerable mode Q\ is connected to B\ when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering (B)\ is used. The period () can be calculated from $T = (0.7) R_X C_X$; R_{MIN} is 5k Ω . C_{MIN} is 0pF.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
CD74HC4538E	ACTIVE	-55 to 125	0.44 1KU	PDIP (N) 16	View	25	<input type="checkbox"/>	Contact TI Distributor or Sales Office
CD74HC4538EE4	ACTIVE	-55 to 125	0.44 1KU	PDIP (N) 16	View	25	<input type="checkbox"/>	Request Free Samples
CD74HC4538M	ACTIVE	-55 to 125	0.40 1KU	SOIC (D) 16	View	40	<input type="checkbox"/>	Contact TI Distributor or Sales Office
CD74HC4538M96	ACTIVE	-55 to 125	0.40 1KU	SOIC (D) 16	View	2500	<input type="checkbox"/>	Purchase Samples
CD74HC4538M96G4	ACTIVE	-55 to 125	0.44 1KU	SOIC (D) 16	View	2500	<input type="checkbox"/>	Purchase Samples
CD74HC4538ME4	ACTIVE	-55 to 125	0.40 1KU	SOIC (D) 16	View	40	<input type="checkbox"/>	Request Free Samples
CD74HC4538MG4	ACTIVE	-55 to 125	0.44 1KU	SOIC (D) 16	View	40	<input type="checkbox"/>	Purchase Samples
CD74HC4538MT	ACTIVE	-55 to 125	0.43 1KU	SOIC (D) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC4538MTE4	ACTIVE	-55 to 125	0.43 1KU	SOIC (D) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC4538NSR	ACTIVE	-55 to 125	0.40 1KU	SO (NS) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4538NSRE4	ACTIVE	-55 to 125	0.40 1KU	SO (NS) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4538PW	ACTIVE	-55 to 125	0.40 1KU	TSSOP (PW) 16	View	90	<input type="checkbox"/>	Purchase Samples
CD74HC4538PWG4	ACTIVE	-55 to 125	0.31 1KU	TSSOP (PW) 16	View	90	<input type="checkbox"/>	Purchase Samples
CD74HC4538PWR	ACTIVE	-55 to 125	0.40 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4538PWG4	ACTIVE	-55 to 125	0.31 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4538PWT	ACTIVE	-55 to 125	0.43 1KU	TSSOP (PW) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC4538PWTE4	ACTIVE	-55 to 125	0.43 1KU	TSSOP (PW) 16	View	250	<input type="checkbox"/>	Purchase Samples

Inventory

	TI Inventory Status			Reported Distributor Inventory				View all Distributors	Choose a Region	
CD74HC4538E	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase			
	2000*	>10k 16 Jan	10 Weeks	Americas	Avnet	>1k	<input type="checkbox"/>			
					DigiKey	82	<input type="checkbox"/>			
					Newark InOne	732	<input type="checkbox"/>			
					Abacus Polar	>1k	<input type="checkbox"/>			
				Europe	Avnet-SILICA	>1k	<input type="checkbox"/>			
					EBV Elektronik	575	<input type="checkbox"/>			
					Spoerle	>1k	<input type="checkbox"/>			
CD74HC4538EE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005						
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase			

	2000*	>10k 16 Jan	10 Weeks	None Reported View Distributors			
CD74HC4538M	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	53*	>10k 22 Dec	4 Weeks	Americas	Avnet	>1k	
					DigiKey	234	
					Newark InOne	>1k	
				Europe	Arrow Northern Europe	14	
					Avnet-SILICA	>1k	
					EBV Elektronik	>1k	
					Spoerle	>1k	
CD74HC4538M96	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	91 7 Dec	4 Weeks	Europe	EBV Elektronik	>1k	
		>10k 23 Dec					
CD74HC4538M96G4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 28 Dec	10 Weeks	None Reported View Distributors			
CD74HC4538ME4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	53*	>10k 22 Dec	4 Weeks	None Reported View Distributors			
CD74HC4538MG4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 28 Dec	10 Weeks	None Reported View Distributors			
CD74HC4538MT	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 21 Dec	10 Weeks	None Reported View Distributors			
CD74HC4538MTE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 21 Dec	10 Weeks	None Reported View Distributors			
CD74HC4538NSR	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	8000*	6635 12 Dec	10 Weeks	None Reported View Distributors			
		110 23 Jan					
		616 30 Jan					
		215 20 Feb					
		723 27 Feb					
CD74HC4538NSRE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

	8000*	6635 12 Dec	10 Weeks	None Reported View Distributors			
		110 23 Jan					
		616 30 Jan					
		215 20 Feb					
		723 27 Feb					
CD74HC4538PW	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	900 12 Dec	12 Weeks	None Reported View Distributors			
CD74HC4538PWG4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1451 30 Nov	12 Weeks	None Reported View Distributors			
		>10k 3 Apr					
CD74HC4538PWR	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
CD74HC4538PWRG4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
CD74HC4538PWT	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	250*		12 Weeks	None Reported View Distributors			
CD74HC4538PWTE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	250*		12 Weeks	None Reported View Distributors			

* Our information is updated daily, so please check back with us ** Lead time information is not available at this time. However, soon if this does not meet your needs. You may also contact our information is updated daily so please check back with us your [TI Authorized Distributor](#), including those [listed above](#), for soon. Please contact your preferred [TI Authorized Distributor](#) for real time stock information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
CD74HC4538E	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
CD74HC4538EE4	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
CD74HC4538M	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538M96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538M96G4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538ME4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538MG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538MT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538MTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538NSR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538NSRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538PW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538PWG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538PWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538PWRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538PWT	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4538PWTE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

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