

THOMSON SEMICONDUCTORS

TL494
TL494I

PULSE WIDTH MODULATION CONTROL CIRCUIT

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

This device features :

- Complete Pulse Width Modulation control circuitry
- On-chip oscillator with master or slave operation
- On-chip error amplifiers
- On-chip 5 volt reference
- Adjustable dead-time control
- Uncommitted output transistors capable of 200 mA current source or sink
- Output control for push-pull or single-ended operation

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	
		DP	DG
TL494	0°C to +70°C	•	•
TL494I	-25°C to +85°C	•	•

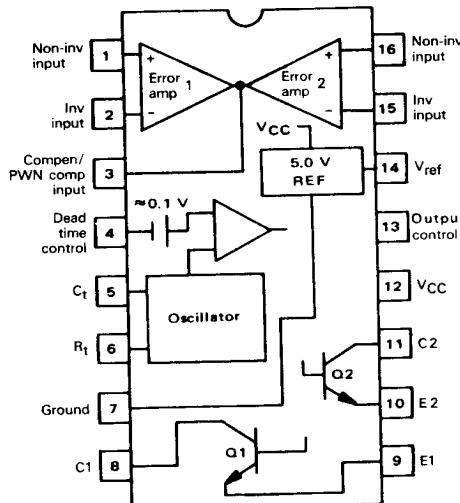
Example : TL494DP, TL494DG

PULSE WIDTH MODULATION CONTROL CIRCUIT

CASE CB-79



PIN ASSIGNMENT



THOMSON SEMICONDUCTORS

Sales headquarters

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THOMSON
COMPONENTS

MAXIMUM RATINGS

(Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494	TL494I	Unit
Power supply voltage	V _{CC}	42	42	V
Collector output voltage	V _{C1} , V _{C2}	42	42	V
Collector output current (each transistor)	I _{C1} , I _{C2}	250	250	mA
Amplifier input voltage	V _I	V _{CC} + 0.3	V _{CC} + 0.3	V
Power dissipation @ T _{amb} ≤ 45°C	P _{tot}	1000	1000	mW
Operating junction temperature	T _J	+ 150	+ 150	°C
Operating ambient temperature range	T _{amb}	0 to + 70	- 25 to + 85	°C
Storage temperature range	T _{stg}	- 65 to + 150	- 65 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Junction-ambient thermal resistance	R _{th(j - a)}	100 80	°C/W
Junction-case thermal resistance	R _{th(j - c)}	25 30	°C/W

FIGURE 1 — BLOCK DIAGRAM

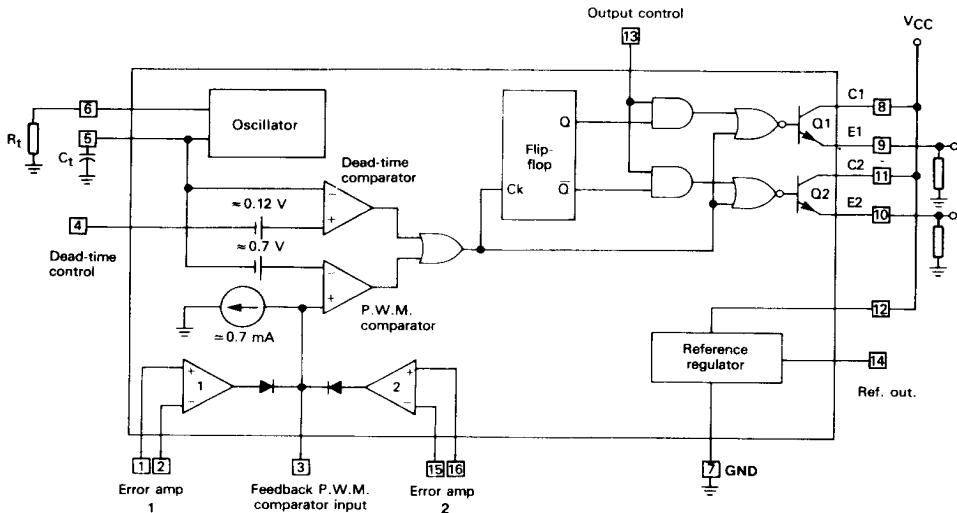
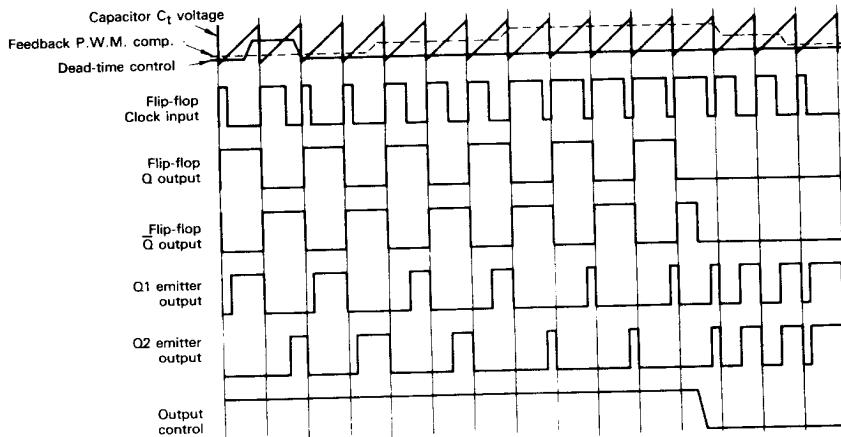


FIGURE 2 — TIMING DIAGRAMS



DESCRIPTION

The TL494 is a fixed frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal linear sawtooth oscillator is frequency-programmable by two external components, R_t and C_t . The oscillator frequency is determined by :

$$f_{osc} = \frac{1.1}{R_t \cdot C_t}$$

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_t to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagrams shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a

means for the error amplifiers to adjust the output pulse width from the maximum percentON-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from -0.3 V to ($V_{CC} - 2$ V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output ONtime, dominates control of the loop.

When capacitor C_t is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum ON-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 5\%$ with a thermal drift of less than 50 mV over an operating temperature range of 0 to +70°C.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	7.0	15	40	V
Collector output voltage	V_{C1}, V_{C2}	—	30	40	V
Collector output current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier input voltage	V_i	-0.3	—	$V_{CC} - 2.0$	V
Current into feedback terminal	I_{fb}	—	—	0.3	mA
Reference output current	I_{ref}	—	—	10	mA
Timing resistor	R_t	1.8	30	500	kΩ
Timing capacitor	C_t	0.00047	0.001	10	μF
Oscillator frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS(V_{CC} = +15 V, f_{osc} = 10 kHz unless otherwise specified).For typical values T_{amb} = +25°C for min./max. values, T_{amb} is the operating ambient temperature range that applies unless otherwise specified.**REFERENCE SECTION**

Characteristic	Symbol	Min	Typ	Max	Unit
Reference voltage (I _O = 1.0 mA, T _{amb} = +25°C)	V_{ref}	4.75	5.0	5.25	V
Reference voltage change with temperature over full operating temperature range	$\Delta_{ref(\Delta T)}$	—	1.3	2.6	%
Line regulation (V _{CC} = +7.0 V to +40 V)	K _{VL}	—	2.0	25	mV
Load regulation (I _O = 1.0 mA to 10 mA)	K _{VO}	—	3.0	15	mV
Short-circuit output current (V _{ref} = 0 V, T _{amb} = +25°C)	I _{SC}	—	35	—	mA

OUTPUT SECTION

Characteristic	Symbol	Min	Typ	Max	Unit
Collector off-state current (V _{CC} = +40 V, V _{CE} = +40 V)	I _{C(off)}	—	2.0	100	μA
Emitter off state current (V _{CC} = +40 V, V _C = +40 V, V _E = 0 V)	I _{E(off)}	—	—	100	μA
Collector-emitter saturation voltage Common-emitter (V _E = 0 V, I _C = 200 mA) Emitter-follower (V _C = 15, I _E = -200 mA)	V _{sat(C)} V _{sat(E)}	— —	1.1 1.5	1.3 2.5	V
Output control pin current Low state (V _{OC} ≤ 0.4 V) High state (V _{OC} = V _{ref})	I _{OCL} I _{OCH}	— —	10 0.2	— 3.5	μA mA
Output voltage rise time Common-emitter (See Figure 12) Emitter-follower (See Figure 13)	t _r	— —	100 100	200 200	ns
Output voltage fall time Common-emitter (See Figure 12) Emitter-follower (See Figure 13)	t _f	— —	25 40	100 100	ns

ERROR AMPLIFIER SECTION

Characteristic	Symbol	Min	Typ	Max	Unit
Input offset voltage (V_O (Pin 3) = +2.5 V)	V_{IO}	—	2.0	10	mV
Input offset current (V_O (Pin 3) = +2.5 V)	I_{IO}	—	5.0	250	nA
Input bias current (V_O (Pin 3) = +2.5 V)	I_{IB}	—	0.1	1.0	μ A
Input common-mode voltage range ($V_{CC} = +7.0$ V to +40 V)	V_{ICR}	0.3	—	$V_{CC} - 2.0$	V
Open-loop voltage gain ($\Delta V_O = 3.0$ V, $V_O = +0.5$ to +3.5 V, $R_L = 2.0$ k Ω)	A_{VOL}	70	95	—	dB
Unity-gain crossover frequency ($V_O = +0.5$ to +3.5 V, $R_L = 2.0$ k Ω)	f_C	—	350	—	kHz
Phase margin at unity-gain ($V_O = +0.5$ to +3.5 V, $R_L = 2.0$ k Ω)	φ_m	—	65	—	deg.
Common-mode rejection ratio ($V_{CC} = +40$ V)	CMR	65	90	—	dB
Power supply rejection ratio ($\Delta V_{CC} = 33$ V, $V_O = +2.5$ V, $R_L = 2.0$ k Ω)	$PSRR$	—	100	—	dB
Output sink current (V_O (Pin 3) = +0.7 V)	I_O^-	0.3	0.7	—	mA
Output source current (V_O (Pin 3) = +3.5 V)	I_O^+	2.0	—4.0	—	mA

PWM COMPARATOR SECTION (Test Circuit Figure 11)

Characteristic	Symbol	Min	Typ	Max	Unit
Input threshold voltage (Zero duty cycle)	V_{th}	—	3.5	4.5	V
Input sink current (V (Pin 3) = +0.7 V)	I_I^-	0.3	0.7	—	mA

DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)

Input bias current (Pin 4) - ($V_I = 0$ to +5.25 V)	I_{IB} (DT)	—	2.0	10	μ A
Maximum duty cycle, Each output, push-pull mode $V_I = 0$ V, $C_t = 0.1$ μ F, $R_t = 12$ k Ω $V_I = 0$ V, $C_t = 0.001$ μ F, $R_t = 30$ k Ω	DC_{max}	45	48	50	%
Input threshold voltage (Pin 4) Zero duty cycle Maximum duty cycle	V_{th}	— 0	2.8	3.3	V

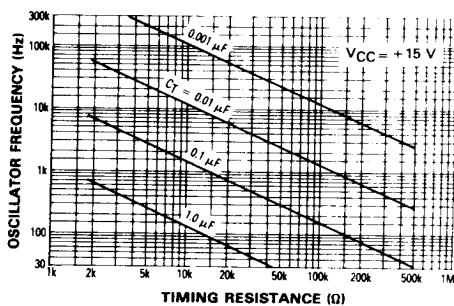
OSCILLATOR SECTION

Frequency ($C_t = 0.001$ μ F, $R_t = 30$ k Ω)	f_{osc}	—	40	—	kHz
Standard deviation of frequency* ($C_t = 0.001$ μ F, $R_t = 30$ k Ω)	σ_{osc}	—	3.0	—	%
Frequency change with voltage ($V_{CC} = +7.0$ V to +40 V, $T_{amb} = +25^\circ$ C)	$\Delta f_{osc}(\Delta V)$	—	0.1	—	%
Frequency change with temperature ($\Delta T_{amb} = +25^\circ$ C to T_{amb} low, +25°C to T_{amb} high)	$\Delta f_{osc}(\Delta T)$	—	1.0	2.0	%

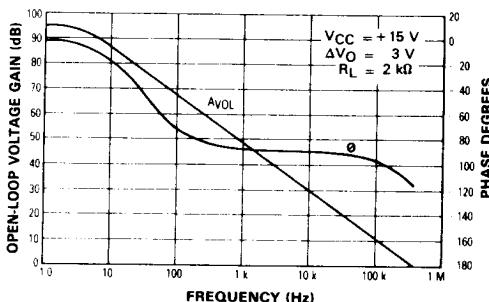
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula

$$\sigma = \sqrt{\frac{N}{\sum_{n=1}^{N-1} (X_n - \bar{X})^2}}$$

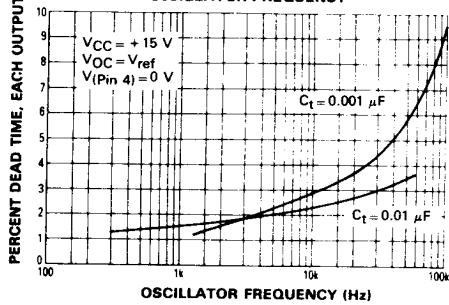
**FIGURE 3 – OSCILLATOR FREQUENCY
VERSUS TIMING RESISTANCE**



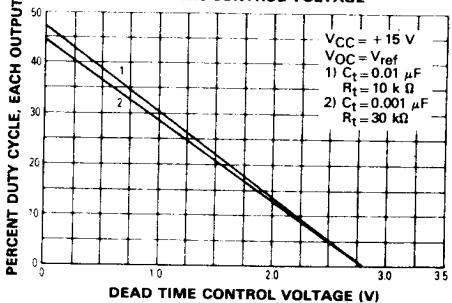
**FIGURE 4 – OPEN LOOP VOLTAGE GAIN AND PHASE
VERSUS FREQUENCY**



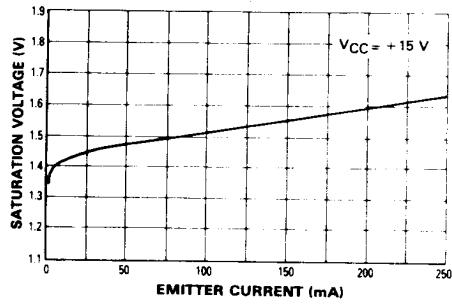
**FIGURE 5 – PERCENT DEAD TIME VERSUS
OSCILLATOR FREQUENCY**



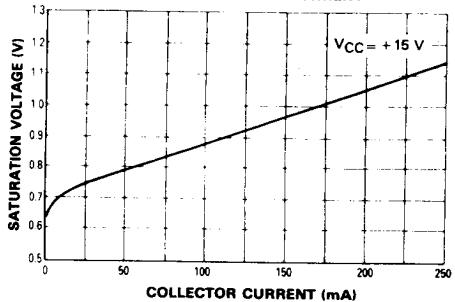
**FIGURE 6 – PERCENT DUTY CYCLE VERSUS
DEAD-TIME CONTROL VOLTAGE**



**FIGURE 7 – Emitter-Follower Configuration,
OUTPUT-SATURATION VOLTAGE
VERSUS Emitter CURRENT**



**FIGURE 8 – COMMON-EMITTER CONFIGURATION
OUTPUT-SATURATION VOLTAGE
VERSUS COLLECTOR CURRENT**



**FIGURE 9 — STANDBY-SUPPLY CURRENT
VERSUS SUPPLY VOLTAGE**

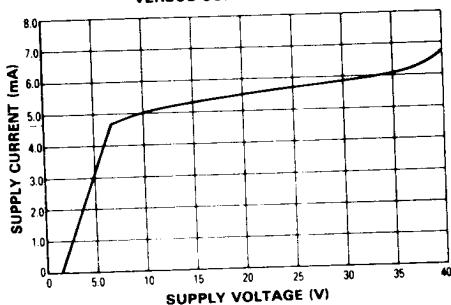


FIGURE 10 — ERROR AMPLIFIER CHARACTERISTICS

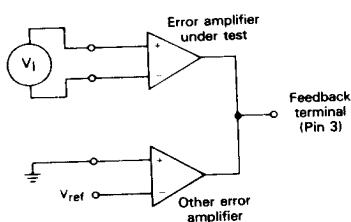


FIGURE 11 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

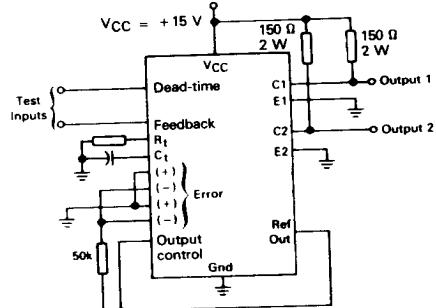


FIGURE 12 — COMMON-Emitter CONFIGURATION TEST CIRCUIT AND WAVEFORM

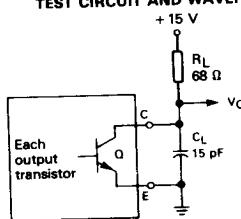


FIGURE 13 — Emitter-Follower Configuration Test Circuit and Waveform

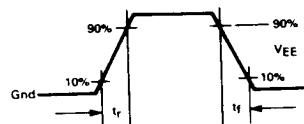
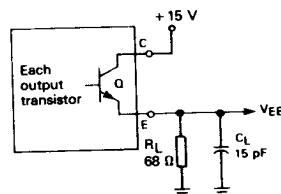


FIGURE 14 – ERROR-AMPLIFIER SENSING TECHNIQUES

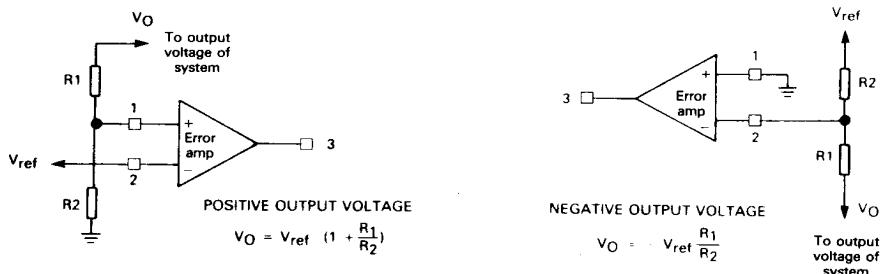


FIGURE 15 – DEAD-TIME CONTROL CIRCUIT

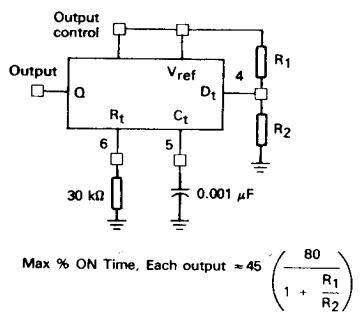


FIGURE 16 – SOFT-START CIRCUIT

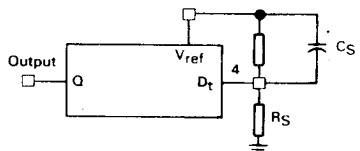


FIGURE 17 – OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS

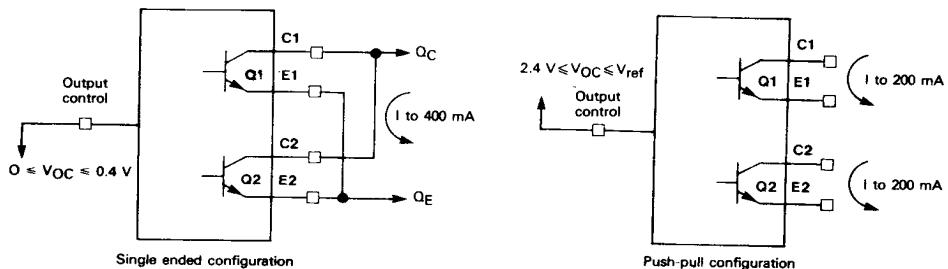


FIGURE 18 — SLAVING TWO OR MORE CONTROL CIRCUITS

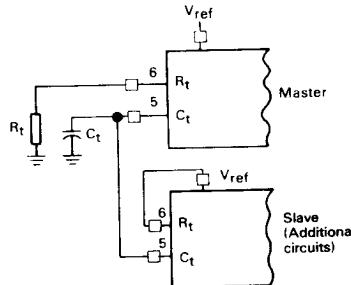
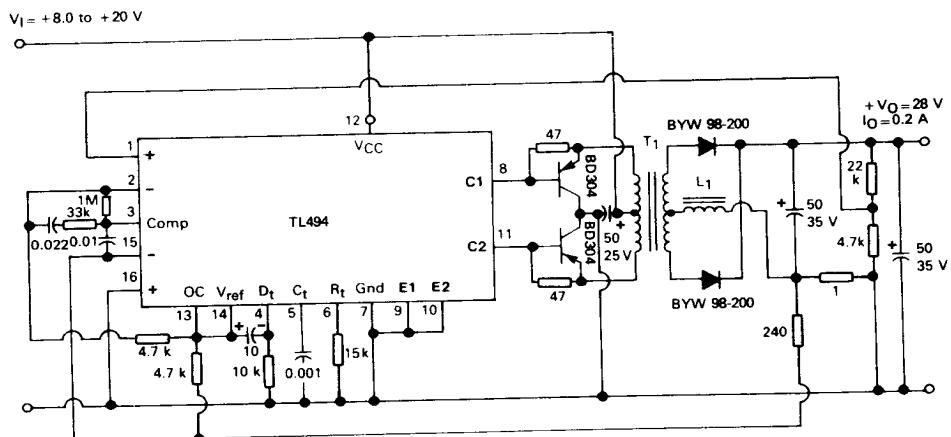


FIGURE 19 — PULSE-WIDTH MODULATED PUSH-PULL CONVERTER

All capacitors in μF , resistors in Ω unless otherwise specified

L1 — 3.5 mH @ 0.3A

T1 — Primary: 20T C.T. #28 AWG

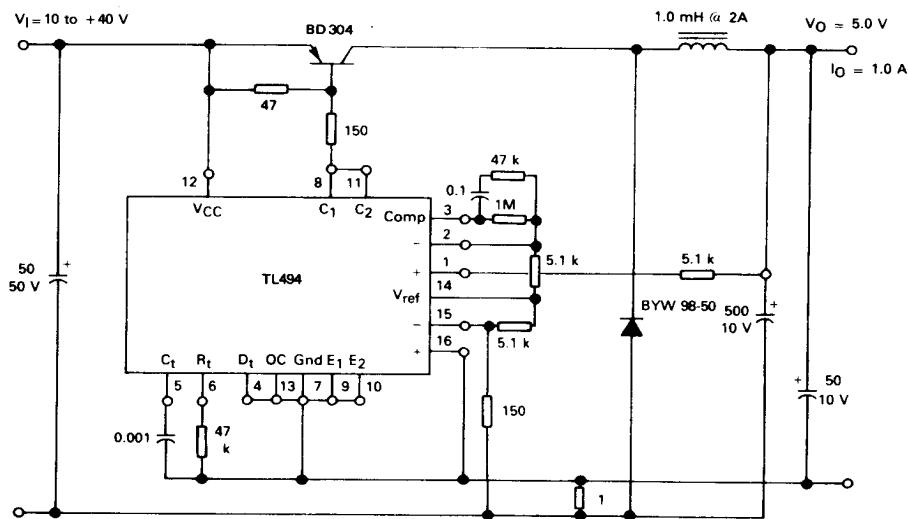
Secondary: 120T C.T. #36 AWG

Core : T22 - FP 14 x 8 - SE ' FERRINOX'®

LCC COMPONENTS

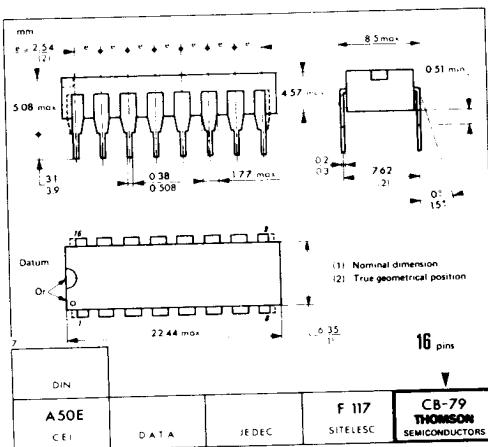
TEST	CONDITIONS	RESULTS
line regulation	$V_I = +8.0 \text{ to } +20 \text{ V}$	3.0 mV 0.01 %
Load regulation	$V_I = +12.6 \text{ V}, I_O = 0.2 \text{ to } 200 \text{ mA}$	5.0 mV 0.02 %
Output ripple	$V_I = +12.6 \text{ V}, I_O = 200 \text{ mA}$	40 mVpp
Short circuit current	$V_I = +12.6 \text{ V}, R_L = 0.1 \Omega$	250 mA
Efficiency	$V_I = +12.6 \text{ V}, I_O = 200 \text{ mA}$	72 %

FIGURE 20 — PULSE-WIDTH MODULATED STEP-DOWN CONVERTER



TEST	CONDITIONS	RESULTS
line regulation	$V_I = +10 \text{ V to } +40 \text{ V}$	14 mV 0.28 %
Load regulation	$V_I = +28 \text{ V}, I_O = 1 \text{ mA to } 1 \text{ A}$	3.0 mV 0.06 %
Output ripple	$V_I = +28 \text{ V}, I_O = 1.0 \text{ A}$	65 mV _{pp}
Short circuit current	$V_I = +28 \text{ V}, R_L = 0.1 \Omega$	1.6 A
Efficiency	$V_I = +28 \text{ V}, I_O = 1 \text{ A}$	71 %

CB-79

DP SUFFIX
PLASTIC PACKAGEDG SUFFIX
CERDIP PACKAGE

These specifications are subject to change without notice.
Please inquire with our sales offices about the availability of the different packages.

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THOMSON SEMICONDUCTORS

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