DSP56311 Evaluation Module

Hardware Reference Manual

DSP56311EVMUM/D
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Preface

This reference manual describes in detail the hardware on the DSP56311 Evaluation Module (DSP56311EVM)

Audience

This manual is intended for Motorola DSP56311 application developers.

Organization

This manual is organized into two chapters and two appendixes as follows:

- Chapter 1, “Introduction,” provides an overview of the DSP56311EVM and its features.
- Chapter 2, “DSP56311EVM Technical Summary,” describes in detail the DSP56311EVM hardware.
- Appendix A, “DSP56311EVM Schematics,” contains the schematics for the DSP56311EVM.
- Appendix B, “DSP56311EVM Parts List,” contains the bill of materials for the DSP56311EVM.

Suggested Reading

In addition to this manual, refer to the following site on the World Wide Web for more documentation on the DSP56311 chip and the DSP56311EVM kit:

http://www.mot.com/SPS/DSP/documentation/DSP56300.html

Conventions

Signal names used in this document are indicated as active high signals or active low signals. Active high signals (logic one) do not have any special symbol attached to the signal name, like A0 or RESET. However, active low signals (logic zero) are noted with a reverse slash sign like WE\ or OE\.

Hexadecimal values start with a “$” sign, like $0FF0 or $80. Decimal values do not have any symbol attached to the number, like 10 or 34. Binary values start with the letter “b” attached to the number, like b1010 or b0011.

Definitions, Acronyms and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined as follows for reference.

Codec	Acronym for COder/DECoder; a part used to convert analog signals to digital (coder) and digital signals to analog (decoder)
DMA	Acronym for Direct Memory Access
DSP	Acronym for Digital Signal Processor
ESSI	Acronym for Enhanced Synchronous Serial Interface port on Motorola's family of DSPs
EVM	Acronym for Evaluation Module
JTAG	Acronym for Joint Test Action Group. A bus protocol/interface used for test and debug
OnCE™	Acronym for On-Chip Emulation; a debug bus and port created by Motorola to allow a means for low-cost hardware to provide a professional quality debug environment
PBGA	Acronym for Plastic Ball Grid Array
PCB	Acronym for Printed Circuit Board
PEROM	Acronym for Programmable Erasable Read Only Memory
PLL	Acronym for Phase-Lock Loop
RAM	Acronym for Random-Access Memory
ROM	Acronym for Read-Only Memory
SCI	Acronym for Serial Communications Interface Port on Motorola's family of DSPs
SRAM	Acronym for Asynchronous Static Random Access Memory
THD	Acronym for Total Harmonic Distortion
USB	Acronym for Universal Serial Bus
WISD	Acronym for Wireless Infrastructure Subscriber Division

References

For additional information, please refer to the following documentation:

[1] *DSP56300 Family Manual*, (order number DSP56300FM/D)

[2] *DSP56311 User's Manual*, (order number DSP56311UM/D)

[3] *DSP56311 Technical Data*, (order number DSP56311/D)

These documents are available on the World Wide Web at:

http://www.mot.com/SPS/DSP/documentation/DSP56300.html

Chapter 1
Introduction

The DSP56311 Evaluation Module (EVM) is used to demonstrate the abilities of the DSP56311 and provide a hardware tool allowing the development of applications that use the DSP56311.

The DSP56311EVM is an evaluation module board that includes a DSP56311 part, peripheral expansion connectors, external memory, and a voice codec. The peripheral expansion connectors are used for signal monitoring and user-feature expandability.

The DSP56311EVM is designed for the following purposes:

- To allow new users to become familiar with the features of the 56300 architecture. The tools and examples provided with the DSP56311EVM facilitate evaluation of the feature set and the benefits of the family.
- To serve as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, and then run and debug the software using a debugger via the JTAG/OnCE^{TM} port. The breakpoint features of the OnCE port enable the user to easily specify break conditions and to execute user-developed software at full speed, until the break conditions are satisfied. The ability to examine and modify all user-accessible registers, memory, and peripherals through the OnCE port greatly facilitates the task of the developer.
- To serve as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the DSP's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the DSP chip is available to the user.

1.1 DSP56311EVM Architecture

The DSP56311EVM is used to facilitate the evaluation of various features of the DSP56311 part. The DSP56311EVM can be used to develop real-time software and hardware products based on the DSP56311. The DSP56311EVM provides the features necessary for a user to write and debug software, to demonstrate the functionality of that software, and to be able to interface with the customer's application specific device(s). The DSP56311EVM is flexible enough to allow the user to fully exploit the features of the DSP56311. See Figure 1-1.

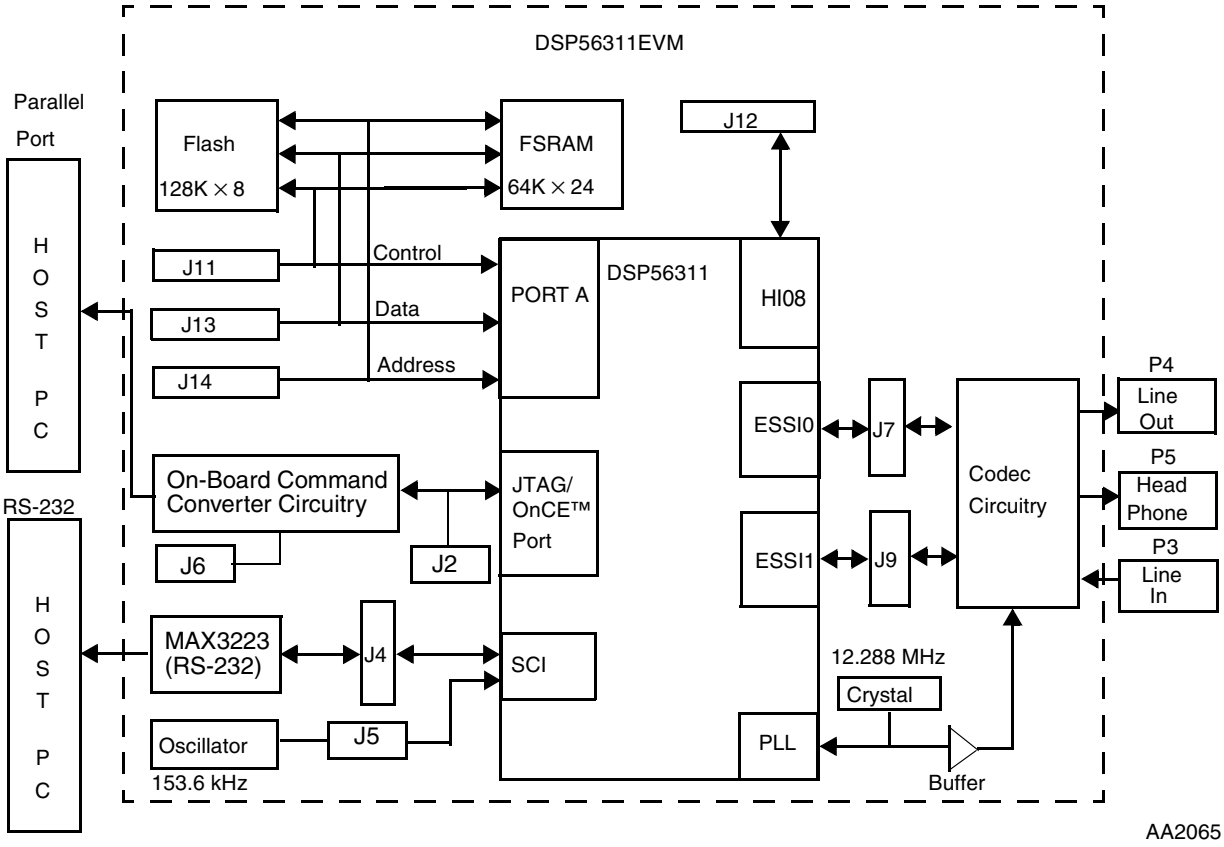

Figure 1-1. DSP56311EVM Functional Block Diagram

1.2 DSP56311EVM Configuration Jumpers

Nine jumper connectors (J1, J3, J4, J5, J6, J7, J8, J9, J10), as shown in Figure 1-2, are used to configure various features on the DSP56311EVM board. Table 1-1 describes the default jumper group settings.

Refer to Figure 1-2 and Table 1-1 for the default jumper settings.

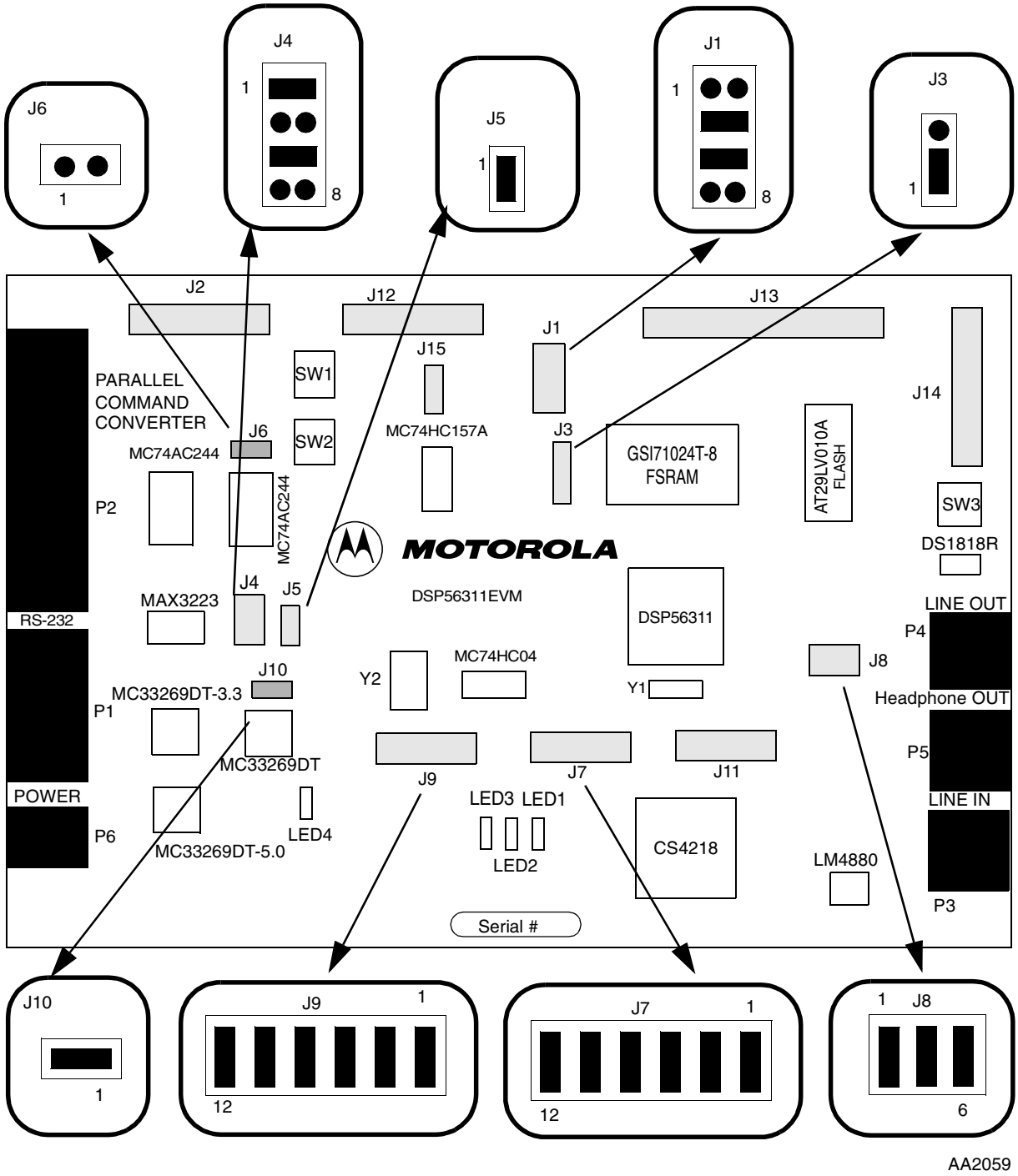

Figure 1-2. DSP56311EVM Component Layout and Default Jumper Settings

Table 1-1. DSP56311EVM Default Jumper Options

Jumper	Comment	Jumper Connections	Document Section
J1	Selects DSP Mode 1 operation upon exit from reset	3-4, 5-6	2.4, 2.3.2.2
J3	Selects unified memory map configuration for FSRAM	1-2	2.3.1.1
J4	Connects serial port connector signals RxD and TxD to DSP's SCI port	1-2, 5-6	2.7.1
J5	Connects on-board 156.3 kHz oscillator to SCI port's SCLK input (used for baud rate generation)	1-2	2.7.1
J6	Enables on-board parallel command converter interface	Open	2.6
J7	Selects DSP's ESSI0 port interface for use with on-board Codec	1-2, 3-4, 5-6, 7-8, 9-10, 11-12	2.7.2
J8	Selects 48 kHz sample rate for codec	1-2, 3-4, 5-6	2.5
J9	Selects DSP's ESSI1 port interface for use with on-board codec	1-2, 3-4, 5-6, 7-8, 9-10, 11-12	2.7.3
J10	Core Current Measurement Jumper — Connecting jumper applies power to DSP core	1-2	3.8

1.2.1 Connecting the DSP56311EVM to the PC and Power

Figure 1-3 shows the method for connecting the PC and the external power supply to the DSP56311EVM board.

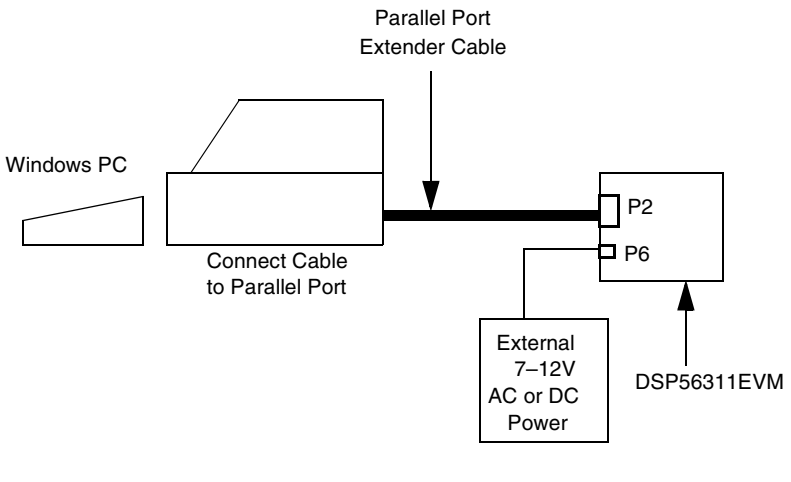

Figure 1-3. Connecting the DSP56311EVM Cables

Perform the following steps to complete the cable connections:

1. Connect the male end of the DB25 parallel port extender cable to the parallel port connection on the PC.
2. Connect the female end of the DB25 parallel port extender cable to P2 on the DSP56311EVM board. This connection allows the PC to control the boards functions. P2 is shown in Figure 1-3 on page 1-4.
3. Make sure that the external 7–12V AC or DC power supply *does not* have power supplied to it.
4. Connect the 2.1 mm output power plug into P6 on the DSP56311EVM board. P6 is shown in Figure 1-3 on page 1-4.
5. Apply power to the power supply. The green Power LED (LED4) lights up when power is correctly applied.

Chapter 2
DSP56311EVM Technical Summary

This chapter describes in detail the DSP56311EVM hardware.

2.1 DSP56311EVM Features

The main features of the DSP56311EVM include the following:

- DSP56311 24-bit digital signal processor
- FSRAM for expansion memory and flash memory for stand-alone operation
- 16-bit CD-quality audio codec
- Command converter circuitry

2.2 DSP56311 Description

A full description of the DSP56311 part, including functionality and user information, is provided in the following documents included as a part of this kit:

- ***DSP56311 Technical Data*** **(order number DSP56311/D):** Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements, and available packaging
- ***DSP56311 User's Manual*** **(order number DSP56311UM/D):** Provides an overview description of the DSP and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control and status register descriptions for each subsystem
- ***DSP56300 Family Manual*** **(order number DSP56300FM/AD):** Provides a detailed description of the core processor including internal status and control registers and a detailed description of the family instruction set

Refer to these documents for detailed information about chip functionality and operation.

NOTE:

A detailed list of known chip errata is also provided with this kit. Refer to the *DSP56311 Chip Errata* document for information that has changed since the publication of the preceding reference documentation. The latest version can be obtained on the Motorola DSP World Wide Web site at the following URL:

http://www.mot.com/SPS/DSP/chiperrata/index.html

2.3 Memory

The DSP56311EVM includes the following external memory:

- 64K × 24-bit fast static RAM (FSRAM) for expansion memory
- 128K × 8-bit flash memory for stand-alone operation

Refer to Figure 2-1 for the location of the FSRAM and flash on the DSP56311EVM. Figure 2-2 shows a functional block diagram of the DSP56311EVM including the memory devices.

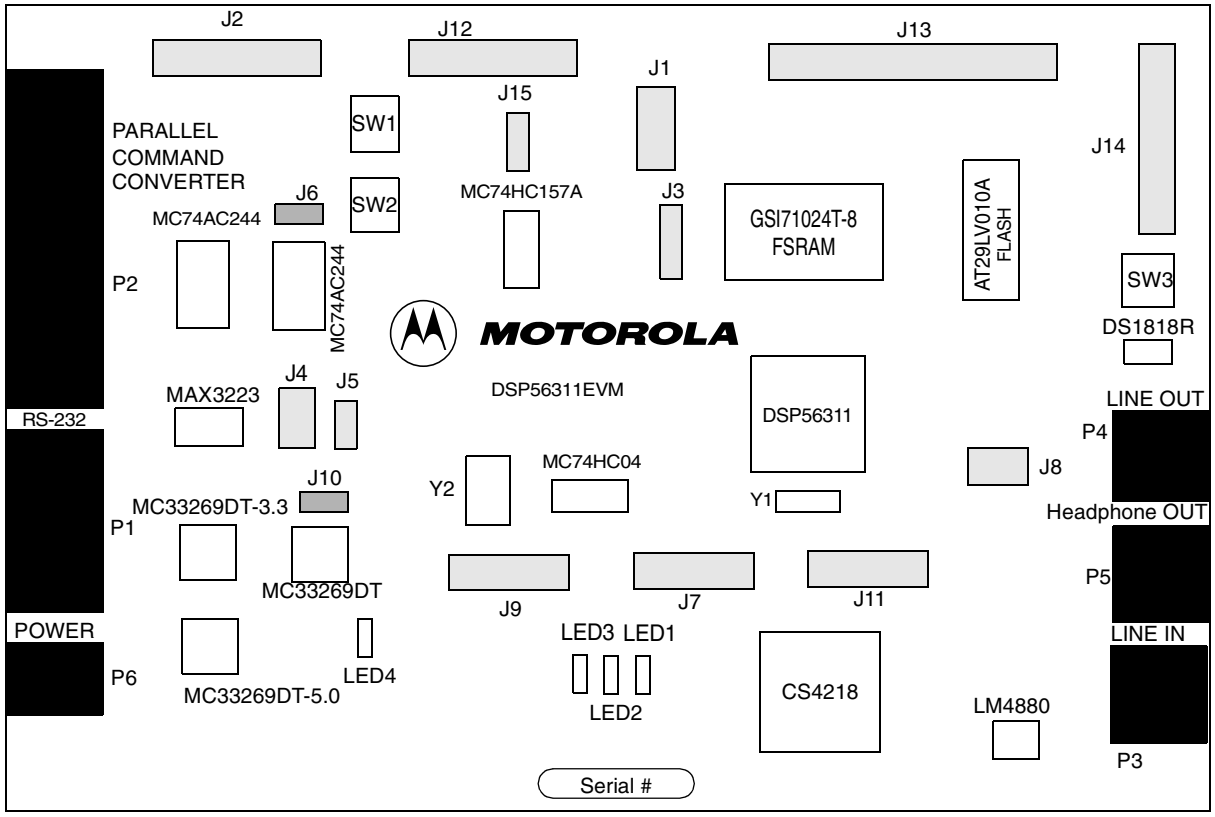

Figure 2-1. DSP56311EVM Component Layout

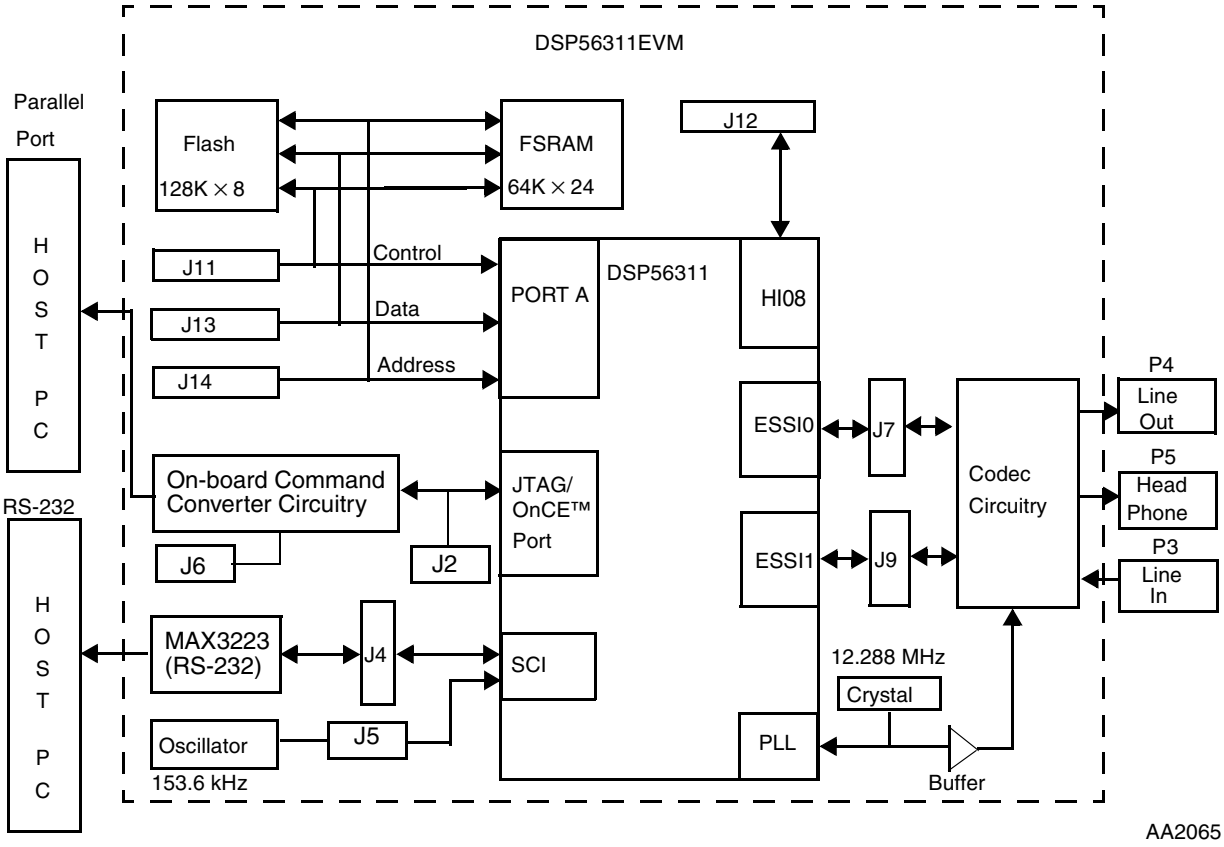

Figure 2-2. DSP56311EVM Functional Block Diagram

2.3.1 FSRAM

The DSP56311EVM uses one bank of 64K × 24-bit fast static RAM (GS71024T-8, labelled U2) for memory expansion. The GS71024T-8 uses a single 3.3 V power supply and has an access time of 8 ns. The following sections detail the operation of the FSRAM.

2.3.1.1 FSRAM Connections

The basic connection for the FSRAM is shown in Figure 2-3.

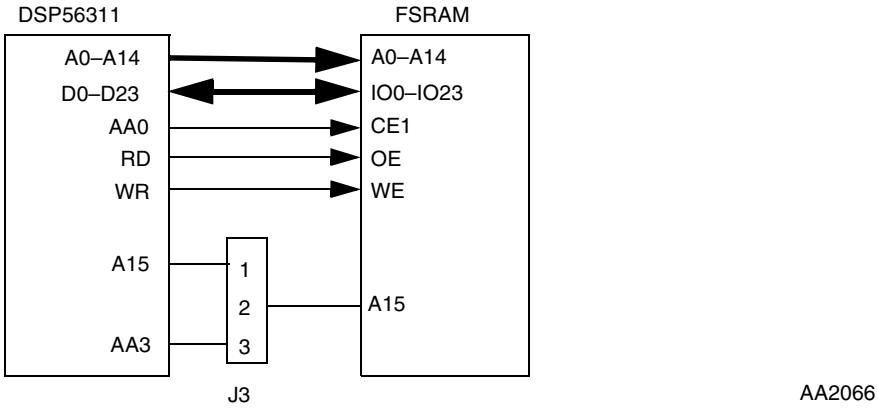

Figure 2-3. FSRAM Connections to the DSP56311

The data input/output pins IO0–IO23 for the FSRAM are connected to the DSP56311 D0–D23 pins. The FSRAM write enable ($\overline{WE}$) and output enable ($\overline{OE}$) lines are connected to the DSP56311 write enable ($\overline{WR}$) and read enable ($\overline{RD}$) lines, respectively. The FSRAM chip enable ($\overline{CE1}$) is generated by the DSP56311 address attribute 0 ($\overline{AA0}$). The FSRAM activity is controlled by AA0 and the corresponding address attribute register 0 ($\overline{AAR0}$). The FSRAM address input pins, A0–A14, are connected to the respective port A address pins of the DSP. Address bit A15 and address attribute 3 ($\overline{AA3}$) are connected to jumper J3 pin 1 and pin 3 respectively. Pin 2 of jumper J3 is then connected to address bit A15 of the FSRAM. This allows the external FSRAM to be configured as either unified or split memory map. Table 2-1 illustrates the FSRAM configurations selectable via jumper J3. The default board configuration selects a unified memory map of 64K words.

Table 2-1. J3 FSRAM Memory Configuration Options

J3	Memory Map Type
1–2	Unified Memory Map (Default)
2–3	Split Memory Map

When a unified memory map is selected, jumper shorting J3 pins 1 and 2, the 64K words of available external FSRAM are not partitioned into X data, Y data, and program memory. Thus, accesses to P:$1000, X:$1000, and Y:$1000 are treated as accesses to the same memory cell, and 48-bit long memory data moves are not possible to or from the external FSRAM.

Selecting the split memory map partitions the 64K of available FSRAM memory into two contiguous 32K memory blocks. This configuration allows for 48-bit long memory data moves from FSRAM. Thus, access to X:$1000 and Y:$1000 could access different memory cells in the partitioned external FSRAM. The split memory map utilizes address attribute pin 3 (AA3). Activity of the DSP56311 pin AA3 is controlled by the corresponding AAR3 register.

2.3.1.2 Example: Programming AAR0

As mentioned previously, the FSRAM activity is controlled by the DSP56311 pin AA0 and the corresponding AAR0. AAR0 controls the external access type, the memory type, and which external memory addresses access the FSRAM. Figure 2-4 shows the memory map that is attained with the AAR0 settings described in this example.

NOTE:

In this example, the memory switch bit in the operating mode register (OMR) is cleared, and the 16-bit compatibility bit in the status register is cleared.

In Figure 2-4, the FSRAM responds to the 64K of X and Y data memory addresses between $040000 and $04FFFF. However, with the unified memory map, accesses to the same external memory location are treated as accesses to the same memory cell.

A priority mechanism exists among the four AAR control registers. AAR3 has the highest priority and AAR0 has the lowest. Bit 14 of the OMR, the address priority disable (APD) bit, controls which AA pins are asserted when a selection conflict occurs (that is the external address matches the address and the space that is specified in more than one AAR). If the APD bit is cleared when a selection conflict occurs, only the highest priority AA pin is asserted. If the APD bit is set when a selection conflict occurs, the lower priority AA pins are asserted in addition to the higher priority AA pin. For this example, only one AA pin must be asserted, AA0. Thus, the APD bit can be cleared.

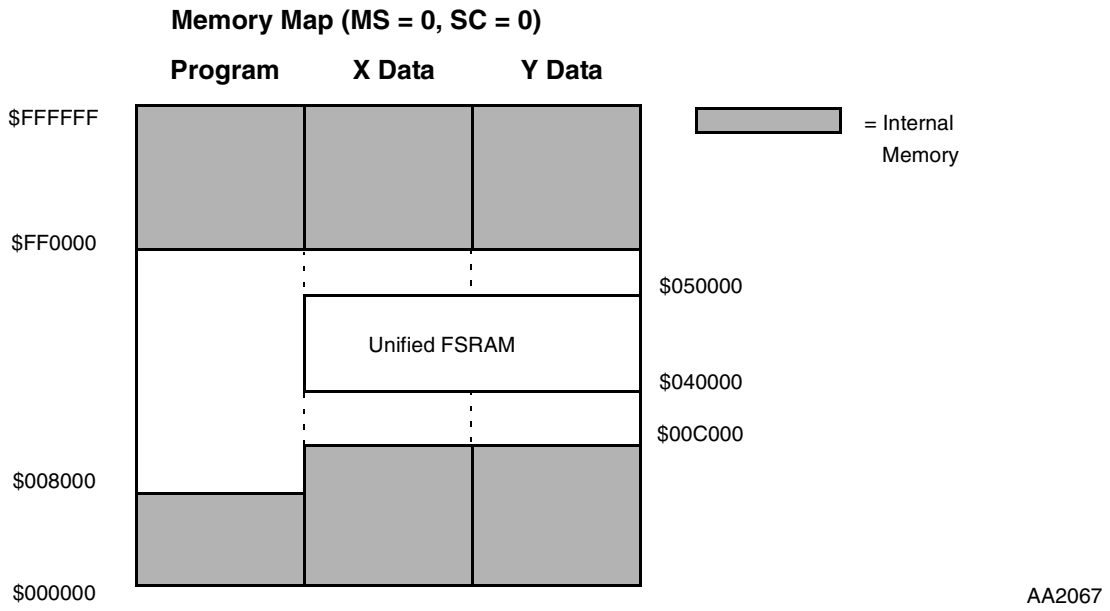

Figure 2-4. Example Memory Map with the Unified External Memory

Figure 2-5 shows the settings of AAR0 for this example. The external access type bits (BAT1 and BAT0) are set to 0 and 1, respectively, to denote FSRAM access. The address attribute polarity bit (BAAP) is cleared to define AA0 as active low. Bit 6 (BAM) of the AAR is reserved and should be written with 0 only. Packing is not needed with the FSRAM; thus, the packing enable bit (BPAC) is cleared to disable this option.

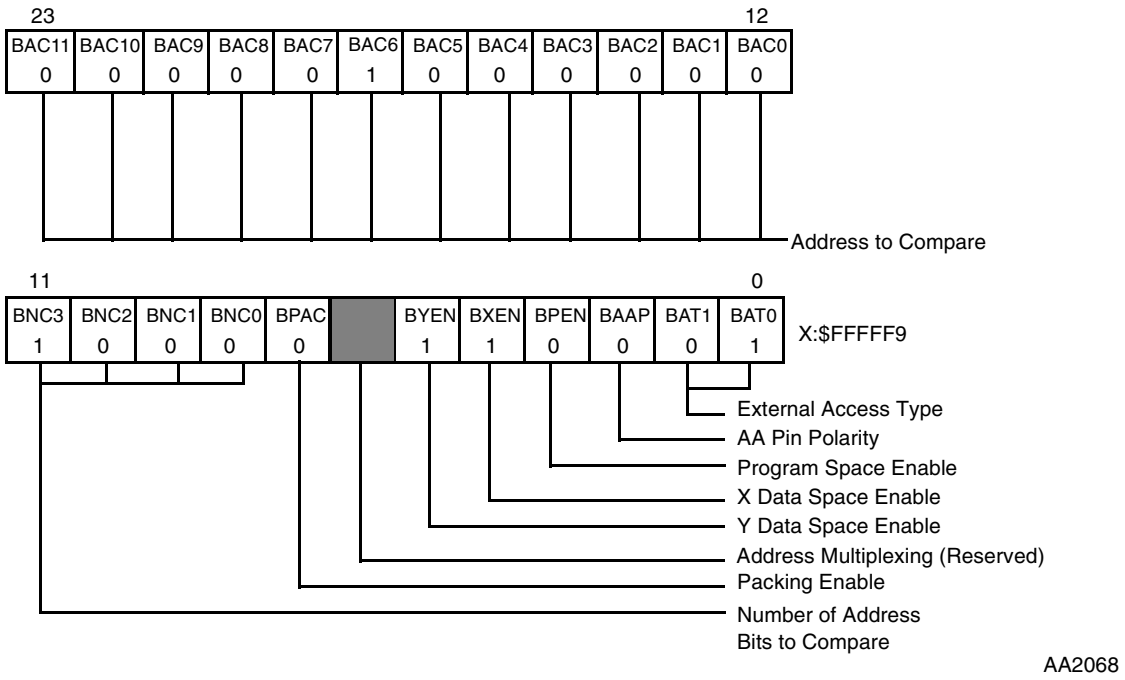

Figure 2-5. Address Attribute Register AAR0

The P, X data, and Y data space enable bits (BPEN, BXEN, and BYEN) define whether the FSRAM is activated during external P, X data, or Y data space accesses, respectively. For this example, the BXEN and BYEN bits are set, and BPEN is cleared to allow the FSRAM to respond to X and Y data memory accesses only.

The number of address-bits to compare, BNC(3:0), and the address-to-compare bits, BAC(11:0), determine which external memory addresses access the FSRAM. The BNC bits define the number of upper address bits that are compared between the BAC bits and the external address to determine if the FSRAM is accessed. For this example, the FSRAM is assigned to respond to addresses between $040000 and $04FFFF. Thus, the BNC bits are set to $8 and the BAC bits are set to $040. If the eight most significant bits of the external address are 00000100, the FSRAM is accessed.

2.3.2 Flash

The DSP56311EVM uses an Atmel AT29LV010A-20TC chip (U3) to provide a 128K × 8-bit CMOS flash for stand-alone operation (that is startup boot operation without accessing the DSP56311 through the JTAG/OnCE port). The AT29LV010 uses a 3.3 V power supply and has a read access time of 200 ns.

2.3.2.1 Flash Connections

The basic connection for the flash is shown in Figure 2-6.

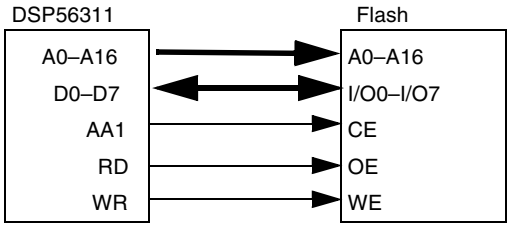

Figure 2-6. Flash Connections

The flash address pins (A0–A16) connect the respective port A address pins on the DSP. The flash data input/output pins I/O0–I/O7 are connected to the DSP56311 D0–D7 pins. The flash write enable ($\overline{WE}$) and output enable ($\overline{OE}$) lines connect the DSP56311 write ($\overline{WR}$) and read ($\overline{RD}$) enable lines, respectively. Address attribute 1 (AA1) generates the flash chip enable, $\overline{CE}$.

2.3.2.2 Programming for Stand-Alone Operation

The DSP56311 mode pins determine the chip operating mode and startup procedure when the DSP56311 exits the reset state. The switch at SW3 resets the DSP56311 by asserting and then clearing the $\overline{RESET}$ pin of the DSP56311. The mode pins MODA, MODB, MODC, and MODD are sampled as the DSP56311 exits the reset state. The mode pins for the DSP56311EVM are controlled by jumper block J1, shown in Figure 2-1 on page 2-2 and Table 2-2. The DSP56311 boots from the flash after reset if there are jumpers connecting pins 3 and 4 and pins 5 and 6 on J1 (Mode 1: MODA and MODD are set, and MODB and MODC are cleared). The DSP56311 moves the 8-bit data from the flash into internal SRAM and then executes it.

2.4 Mode Selector

Boot mode selection for the DSP56311 is made by jumper selections on header J1. Refer to Table 2-2 for header J1 jumper options.

Table 2-2. Boot Mode Selection Options

Mode Number	J1				Boot Mode Selected
	D 1–2	C 3–4	B 5–6	A 7–8	
8	OPEN	JUMP	JUMP	JUMP	Jump to program at $008000
9	OPEN	JUMP	JUMP	OPEN	Bootstrap from byte-wide memory
10	OPEN	JUMP	OPEN	JUMP	Bootstrap from SCI
12	OPEN	OPEN	JUMP	JUMP	HI08 bootstrap in ISA/DSP56300 mode
13	OPEN	OPEN	JUMP	OPEN	HI08 bootstrap in HC11 non-multiplexed bus mode

Table 2-2. Boot Mode Selection Options (Continued)

Mode Number	J1				Boot Mode Selected
	D 1–2	C 3–4	B 5–6	A 7–8	
14	OPEN	OPEN	OPEN	JUMP	HI08 bootstrap in 8051 multiplexed bus mode.
15	OPEN	OPEN	OPEN	OPEN	HI08 bootstrap in MC68302 bus mode.

2.5 Audio Codec

The DSP56311EVM analog section uses Crystal Semiconductor's CS4218-KQ for two channels of 16-bit A/D conversion and two channels of 16-bit D/A conversion. Refer to Figure 2-1 on page 2-2 for the location of the codec on the DSP56311EVM and to Figure 2-2 on page 2-3 for a functional diagram of the codec within the evaluation module. The CS4218 uses a 3.3 V digital power supply and a 5 V analog power supply.

The CS4218 is driven by a 12.288 MHz signal at the codec Master Clock (CLKIN) input pin. The crystal at Y1 creates a 12.288 MHz signal which is buffered and sent to the codec. Refer to the Crystal Semiconductor's *16-Bit Stereo Audio Codec (CS4218) Data Sheet* included with this kit for more information.

The CS4218 is very flexible, offering selectable sampling frequencies between 8 kHz and 48 kHz. The sampling frequency is selected using jumpers on jumper block J8. Table 2-3 shows jumper positions that select the possible sampling frequencies for the DSP56311EVM.

Table 2-3. CS4218 Sampling Frequency Selection

J8 Pins 1–2 (MF6)	J8 Pins 3–4 (MF7)	J8 Pins 5–6 (MF8)	Sampling Frequency (kHz)
Jumper	Jumper	Jumper	48.0
Jumper	Jumper	Open	32.0
Jumper	Open	Jumper	24.0
Jumper	Open	Open	19.2
Open	Jumper	Jumper	16.0
Open	Jumper	Open	12.0
Open	Open	Jumper	9.6
Open	Open	Open	8.0

The codec is connected to the DSP56311 ESSI0 through the shorting jumpers on J7 and to ESSI1 through the shorting jumpers on J9, shown in Figure 2-1 on page 2-2. Jumper block J9 connects the ESSI1 pins of the DSP56311 to the control pins of the CS4218. Jumper block J7 connects the ESSI0 pins of the DSP56311 to the data pins of the CS4218. By removing these jumpers, the user has full access to the ESSI0 and ESSI1 pins of the DSP56311. The following sections describe the connections for the analog and digital sections of the codec.

2.5.1 Codec Analog Input/Output

The DSP56311EVM contains 1/8” stereo jacks for stereo input, output, and headphones. Figure 2-7 shows the analog circuitry of the codec.

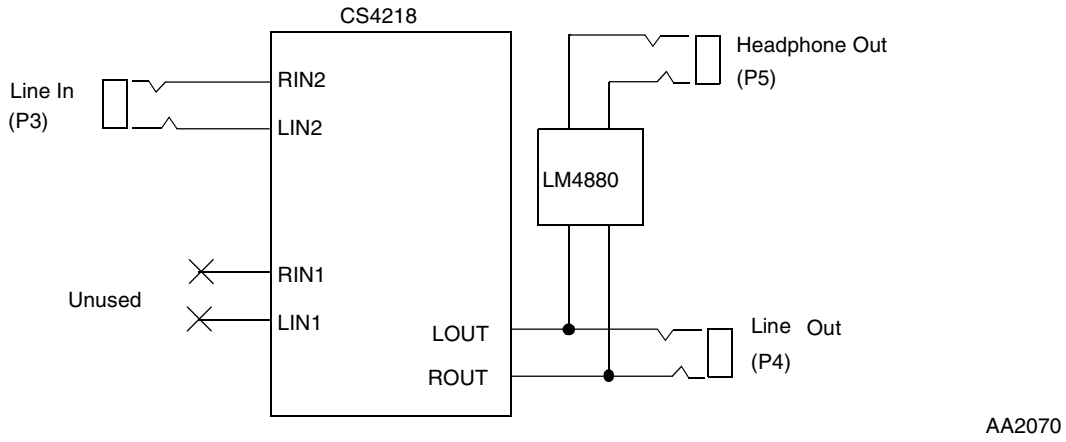

Figure 2-7. Codec Analog Input/Output Diagram

The stereo jack labelled Line In (P3) on the DSP56311EVM connects to the codec right and left input pins, RIN2 and LIN2. Standard line-level inputs are 2 $V_{PP,}$ but the codec requires that input levels be limited to 1 V_{PP}. Thus, a voltage divider forms a 6 dB attenuator between P3 and the CS4218.

The codec right and left channel output pins, ROUT and LOUT, provide their output analog signals through the stereo jack labelled Line Out (P4) on the DSP56311EVM. The outputs of the codec are also connected to the stereo jack labelled Headphone Out (P5) on the DSP56311EVM through National Semiconductor’s LM4880 dual-audio power amplifier at U8. The headphone stereo jack permits the direct connection of stereo headphones to the DSP56311EVM.

2.5.2 Codec Digital Interface

Figure 2-8 shows the digital interface to the codec. Table 2-4 and Table 2-5 show the jumper selections to enable/disable the codec’s digital signals.

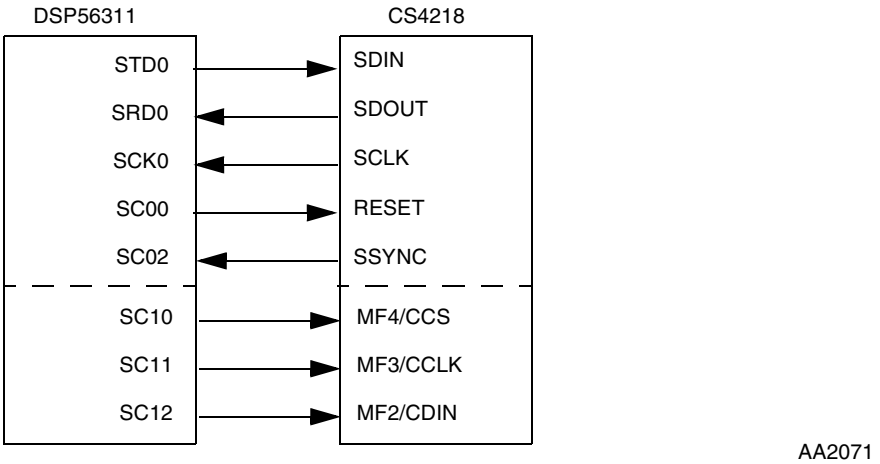

Figure 2-8. Codec Digital Interface Connections

Table 2-4. J7 Jumper Block Options

J7 Pin Number	DSP Signal Name	J7 Pin Number	Codec Signal Name
1	SCK0	2	SCLK
3	SC00	4	RESET
5	STD0	6	SDIN
7	SRD0	8	SDOUT
9	SC01	10	—
11	SC02	12	SSYNC

Table 2-5. J9 Jumper Block Options

J9 Pin Number	DSP Signal Name	J9 Pin Number	Codec Signal Name
1	SCK1	2	—
3	SC10	4	CCS
5	STD1	6	—
7	SRD1	8	—
9	SC12	10	CDIN
11	SC11	12	CCLK

The serial interface of the codec transfers digital audio data and control data into and out of the device. The codec communicates with the DSP56311 through the ESSI0 for the data information and through the ESSI1 for the control information. The codec has three modes of serial operation that are selected by the serial mode select SMODE1, SMODE2, and SMODE3 pins. The SMODE pins on the DSP56311EVM are set to enable serial mode 4, which separates the audio data from the control data. The SMODE pins are also set to enable the master sub-mode with 32-bit frames, the first 16 bits being the left channel, and the second 16 bits being the right channel.

The DSP56311 ESSI0 transfers the data information to and from the codec. The DSP56311 serial transmit data (STD0) pin transmits data to the codec. The DSP56311 serial receive data (SRD0) pin receives data from the codec. These two pins are connected to the codec serial port data in (SDIN) and serial port data out (SDOUT) pins, respectively. In master sub-mode, the codec serial port clock (SCLK) pin provides the serial bit rate clock for the ESSI0 interface. It is connected to the DSP56311 bidirectional serial clock (SCK0) pin. The DSP56311 serial control 0 (SC00) pin is programmed to control the codec reset signal $\overline{\text{RESET}}$. The serial control 2 (SC02) pin is connected to the codec serial port sync (SSYNC) signal. A rising edge on SSYNC indicates that a new frame is about to start.

The DSP56311 ESSI1 pins are used as general purpose I/O (GPIO) signals to transfer the control data to the codec. The control data needs to be transferred only when it changes. The DSP56311 serial control 0 (SC10) pin is programmed to control the codec multi-function pin 4 or the control data chip select pin, MF4/$\overline{\text{CCS}}$. This pin must be low for entering control data. The serial control 1 (SC11) pin connects to the codec multi-function pin 3 or the control data clock pin, MF3/CCLK. The control data is inputted on the rising edge of CCLK. The serial control 2 (SC12) pin is connected to the codec multi-function pin 2 or the control data input pin, MF2/CDIN. This pin contains the control data for the codec.

2.6 Command Converter

The DSP56311EVM provides an on-board command converter for use with Motorola's DSP56300 Debugger. The on-board command converter communicates with the host PC through a parallel DB25 connector and the PC's parallel printer port. The command converter receives commands from the host PC. The set of commands may include read data, write data, reset OnCE module, reset DSP56311, request JTAG interface, or release OnCE module. The command conversion is performed in software within the Motorola DSP56300 Debugger on the host PC. This software interprets the commands and sends a sequence of instructions to the DSP56311's JTAG/OnCE port. The DSP56311 may then continue to receive data or it may transmit data back to the host PC. The on-board command converter circuitry is enabled by leaving the shorting jumper J6 open. Table 2-6 shows the JTAG enable/disable options. Refer to Figure 2-1 on page 2-2 for the location of J6 on the DSP56311EVM and to Figure 2-2 on page 2-3 for a functional diagram. Figure 2-9 is a block diagram of the parallel port command converter interface. Table 2-8 shows the DB25 connector pinout.

Table 2-6. On-Board JTAG Enable/Disable Option

J6	Option Selected
1–2	On-Board Command Converter Disabled
OPEN	On-Board Command Converter Enabled

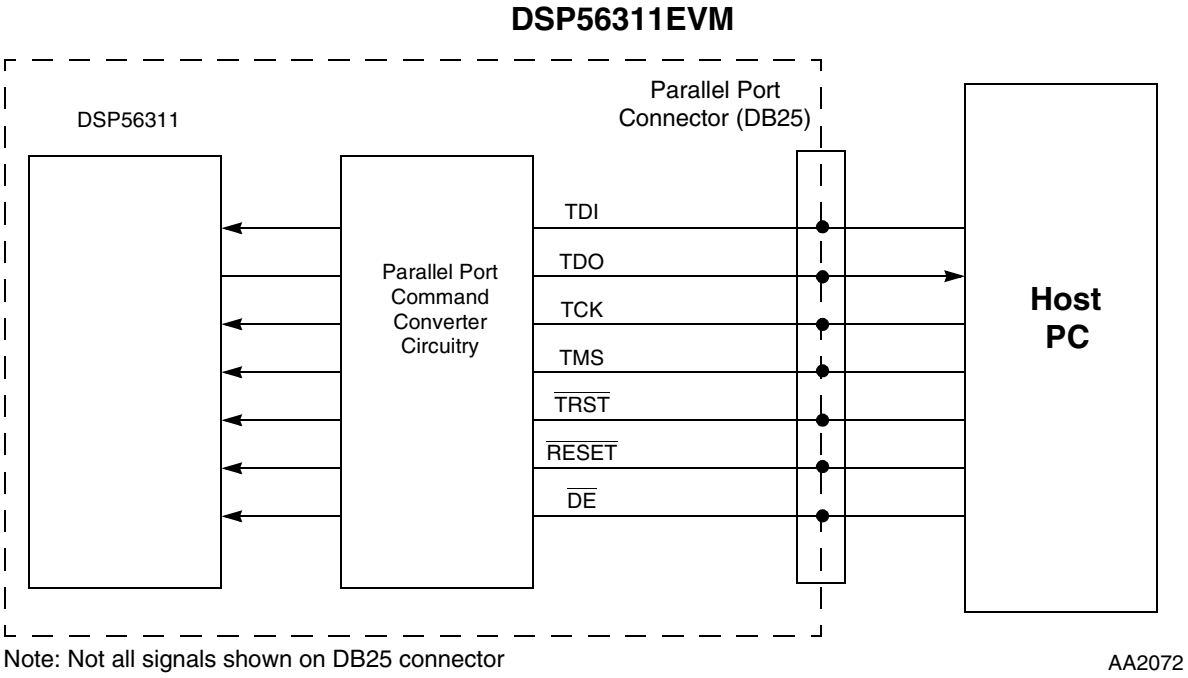

Figure 2-9. Parallel Port Interface

As an alternative to the on-board command converter, the DSP56311EVM 14-pin JTAG/OnCE connector at J2 allows the user to connect an external JTAG command converter board directly to the DSP56311EVM. Jumper J6 must be shorted to enable this option. Pin 8 has been removed from J2 so that the cable cannot be connected to the DSP56311EVM incorrectly. Table 2-7 shows the JTAG/OnCE (J2) connector pinout. The JTAG cable from the external JTAG command converter is similarly keyed so that the cable cannot be connected to the DSP56311EVM incorrectly.

Table 2-7. JTAG/OnCE™ (J2) Connector Pinout

Pin Number	DSP Signal Name	Pin Number	DSP Signal Name
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	—	8	KEY-PIN
9	RESET	10	TMS
11	+3.3 V	12	—
13	DE	14	TRST

Table 2-8. Command Converter Connector (P2) Pinout

Pin Number	Signal Name	Pin Number	Signal Name
1	—	14	—
2	RESET	15	IDENT
3	TMS	16	—
4	TCK	17	—
5	TDI	18	GND
6	TRST	19	GND
7	DE	20	GND
8	IDENT	21	GND
9	PORT_VCC	22	GND
10	—	23	GND
11	TDO	24	GND
12	—	25	GND
13	OUT_VCC		

2.7 Off-Board Interfaces

The DSP56311EVM provides interfaces with off-board devices via its on-chip peripheral ports. Most of the DSP ports are connected to headers on the EVM to facilitate direct access to these pins by using connectors or jumpers.

2.7.1 Serial Communication Interface Port (SCI)

Connection to the DSP's SCI port can be made at J4. Refer to Table 2-9 for pinout information. The signals at J4 are +3.3 V signals. Refer to Table 2-10 to route the DSP's SCI signals through an RS-232 level converter to P1. The pinout of P1 is shown in Table 2-11.

By installing a jumper at J5, the SCI port will be clocked by the on-board 153.6 kHz oscillator instead of being clocked externally via the SCI Header J4, pin 4.

Table 2-9. SCI Header (J4) Pinout

Pin Number	RS-232 Signal Name	Pin Number	DSP Signal Name
1	RxD	2	RxD
3	—	4	SCLK
5	TxD	6	TxD
7	—	8	RESET

Table 2-10. J4 Jumper Options

J7	DSP Signal Name
1–2	RxD
3–4	SCLK
5–6	TxD
7–8	RESET

Table 2-11. DSP Serial Port (P1) Connector Pinout

Pin Number	DSP Signal Name	Pin Number	DSP Signal Name
1	—	6	—
2	TxD	7	—
3	RxD	8	—
4	RESET	9	—
5	GND		

2.7.2 Enhanced Synchronous Serial Port 0 (ESSI0)

Connection to the DSP's ESSI0 port can be made at J7. Refer to Table 2-12 for the header's pinout.

Table 2-12. ESSI0 Header (J7) Pinout

Pin Number	DSP Signal Name	Pin Number	Codec Signal Name
1	SCK0	2	SCLK
3	SC00	4	RESET
5	STD0	6	SDIN
7	SRD0	8	SDOUT
9	SC01	10	—
11	SC02	12	SSYNC

2.7.3 Enhanced Synchronous Serial Port 1 (ESSI1)

Connection to the DSP's ESSI1 port can be made at J9. Refer to Table 2-13 for the header's pinout.

Table 2-13. ESSI0 Header (J9) Pinout

Pin Number	DSP Signal Name	Pin Number	Codec Signal Name
1	SCK1	2	MF4
3	SC10	4	—
5	STD1	6	—
7	SRD1	8	—
9	SC12	10	MF2
11	SC11	12	MF3

2.7.4 Host Port (HI08)

Connection to the DSP's HI08 port can be made at J12. Refer to Table 2-14 for the header's pinout.

Table 2-14. HI08 Header (J12) Pinout

Pin Number	DSP Signal Name	Pin Number	DSP Signal Name
1	H0	2	H1
3	H2	4	H3
5	H4	6	H5
7	H6	8	H7

Table 2-14. HI08 Header (J12) Pinout (Continued)

Pin Number	DSP Signal Name	Pin Number	DSP Signal Name
9	HA0	10	HA1
11	HA2	12	HCS
13	HDS	14	HACK
15	HREQ	16	HRW
17	RESET	18	GND
19	+3.3V	20	GND

2.7.5 Control Bus

Connection to the DSP's control bus control signals can be made at J11. Refer to Table 2-15 for the header's pinout.

Table 2-15. Control Bus Signal Header (J11) Pinout

Pin Number	DSP Signal Name	Pin Number	DSP Signal Name
1	WR	2	RD
3	BB	4	BG
5	TA	6	BR
7	—	8	—
9	—	10	CAS
11	AA0	12	AA1
13	AA3	14	AA2
15	+3.3V	16	GND

2.7.6 Address Bus

Connection to the DSP's address bus signals can be made at J14. Refer to Table 2-16 for the header's pinout.

Table 2-16. Address Bus Signal Header (J14) Pinout

Pin Number	Signal Name	Pin Number	Signal Name
1	DAB0	2	DAB1
3	DAB2	4	DAB3
5	DAB4	6	DAB5
7	DAB6	8	DAB7

Table 2-16. Address Bus Signal Header (J14) Pinout (Continued)

Pin Number	Signal Name	Pin Number	Signal Name
9	DAB8	10	DAB9
11	DAB10	12	DAB11
13	DAB12	14	DAB13
15	DAB14	16	DAB15
17	DAB16	18	DAB17
19	GND	20	GND
21	+3.3V	22	+3.3V

2.7.7 Data Bus

Connection to the DSP's data bus signals can be made at J13. Refer to Table 2-17 for header's pinout.

Table 2-17. Data Bus Signal Header (J13) Pinout

Pin Number	Signal Name	Pin Number	Signal Name
1	DDB0	2	DDB1
3	DDB2	4	DDB3
5	DDB4	6	DDB5
7	DDB6	8	DDB7
9	DDB8	10	DDB9
11	DDB10	12	DDB11
13	DDB12	14	DDB13
15	DDB14	16	DDB15
17	DDB16	18	DDB17
19	DDB18	20	DDB19
21	DDB20	22	DDB21
23	DDB22	24	DDB23
25	GND	26	GND
27	+3.3V	28	+3.3V

2.8 Power Supplies

The main power input to the DSP56311EVM, 7–12V AC/DC at 500 mA, is through a 2.1mm coax power jack. The DSP56311EVM provides +3.3VDC voltage regulation for the DSP, FSRAM memory, flash memory, codec, parallel JTAG interface, and supporting logic. Power applied to the DSP56311EVM is indicated with a Power-on LED, LED4. The DSP56311EVM also provides +5.0VDC voltage regulation for use by the codec and oscillator Y2. Additionally, the DSP56311EVM provides +1.8VDC for use by the DSP core. Jumper J10, the Core Measurement Jumper connects the +1.8VDC supply to the DSP core. This jumper provides a convenient point where the average current being consumed by the DSP core can be measured, which facilitates calculation of the DSP core's average power consumption.

2.9 Test Points

The following sections discuss the different types of test points on the DSP56311EVM.

2.9.1 Ground Test Points

Three on-board digital grounds (GND) and one analog ground (AGND) are provided to facilitate reference measurements. These are located near the corners of the PCB to allow easy access for oscilloscope probe ground straps.

2.9.2 Timer Output Test Points

Test points are provided for the three timer output pins of the DSP56311. Table 2-18 provides a list of the connections. These test points are located near the center of the board above the ESSI0 connector.

Table 2-18. Timer Output Test Points (TIO1–TIO3)

Test Point	DSP Pin Function
TIO0	Timer 0 output pin
TIO1	Timer 1 output pin
TIO2	Timer 2 output pin

2.9.3 External Interrupts–Test Points

Test points are provided for the DSP56311's external interrupt input pins at jumper J15. Table 2-19 provides the pinout of J15. Switch SW1 is connected to IRQD while SW2 is connected to IRQA.

Table 2-19. Interrupt Request Test Points (J15)

Pin	Test Point	DSP Pin Function
1	IRQD	DSP Interrupt Request D
2	IRQC	DSP Interrupt Request C
3	IRQB	DSP Interrupt Request B
4	IRQA	DSP Interrupt Request A
5	NMI	DSP Non Maskable Interrupt

2.10 Debug LED's

Three on-board Light-Emitting Diodes (LED's) are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging. LED1 is controlled by the timer output pin TIO0. LED2 is controlled by the timer output pin TIO1 and LED3 is controlled by TIO2. The TIO pins are data outputs when GPIO mode is enabled for the timers and the DIR bit is set in the Timer Control/Status Register (TCSR). Setting the DO bit to a logic 1 will turn on the associated LED. Table 2-20 outlines which LED is associated with which timer output pin.

Table 2-20. LED Indicators (LED1, LED2, and LED3)

LED	Associated Timer Output Pin
LED1	Timer Output 0 (TIO0)
LED2	Timer Output 1 (TIO1)
LED3	Timer Output 2 (TIO2)

2.11 Reset

The DSP56311EVM provides a power-on reset function (Dallas Semiconductor DS1818R, designated U14) for a clean and dependable RESET signal. A reset of the DSP can be generated from the JTAG connector, the Parallel JTAG Interface, and the user RESET push-button (SW3).

2.12 Clock Source

The DSP56311EVM uses a 12.288 MHz crystal, Y1, connected to the DSP's External Crystal Inputs, EXTAL and XTAL. The DSP56311 PLL can be programmed to multiply the input frequency to achieve the desired operating speed. The 12.288 MHz crystal is buffered and used by the codec for its clock source.

Appendix A
DSP56311EVM Schematics

This section provides the schematic drawings for the DSP56311 Evaluation Module.

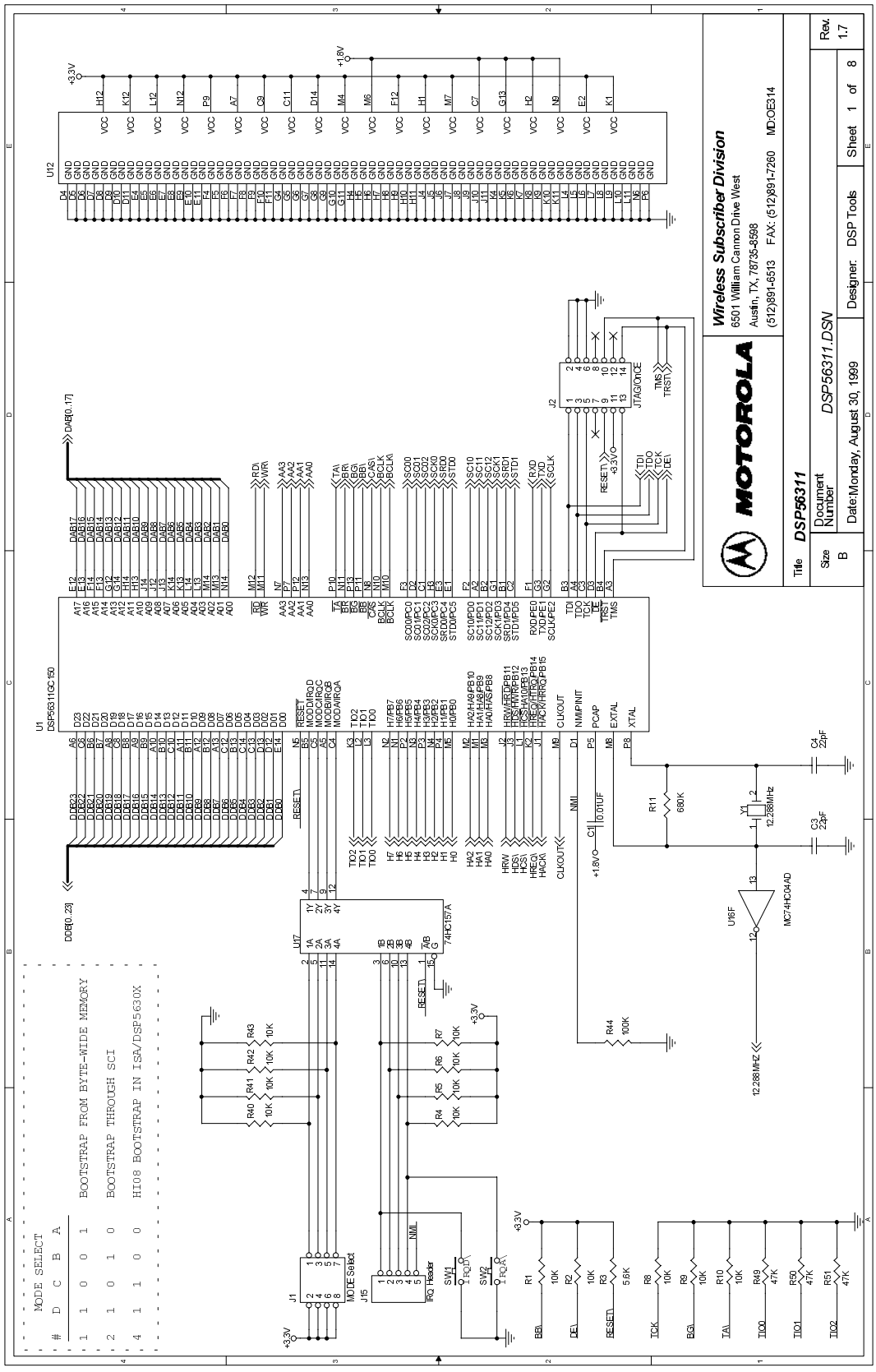

Figure A-1. DSP56311

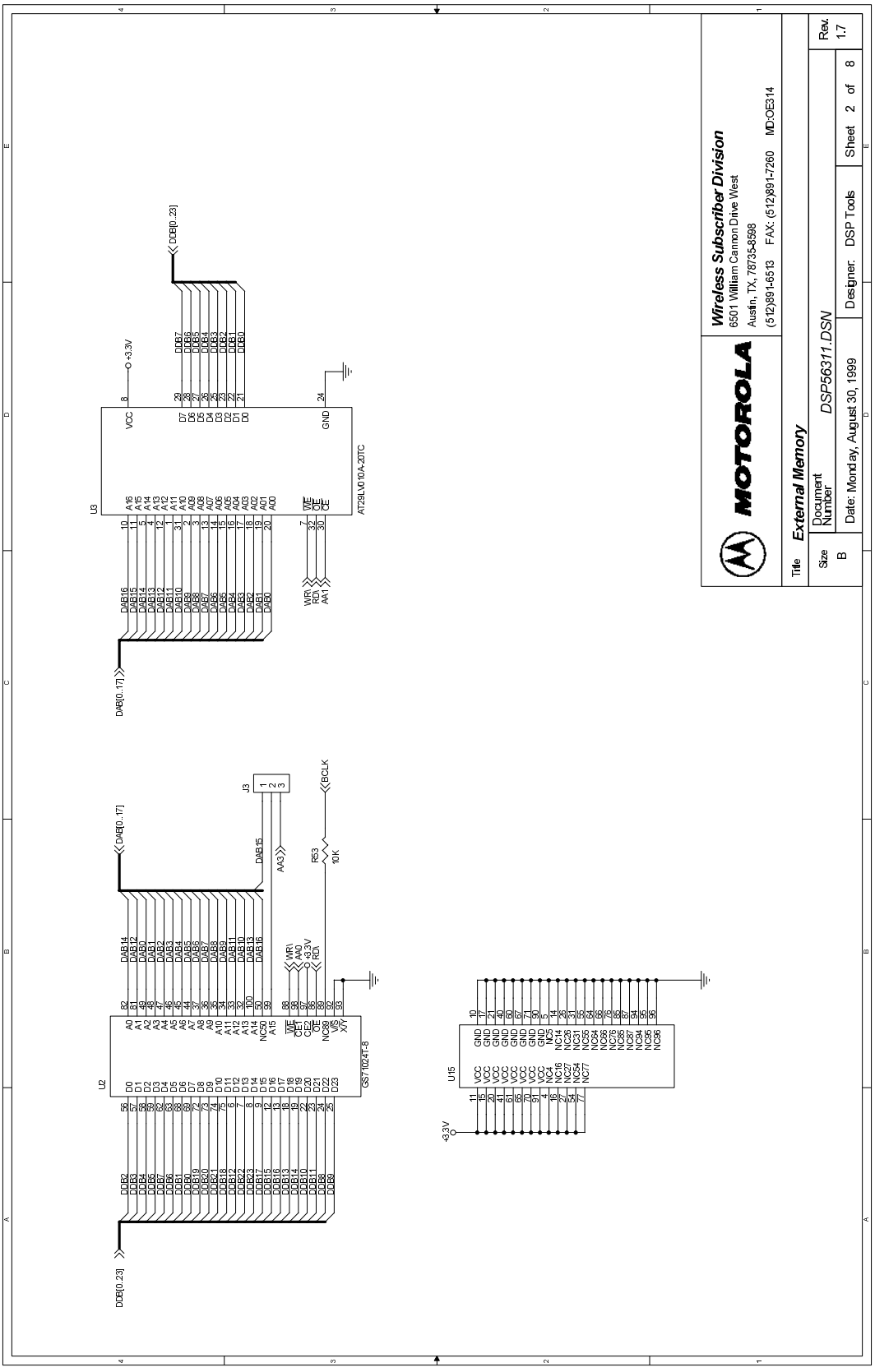

Figure A-2. External Memory

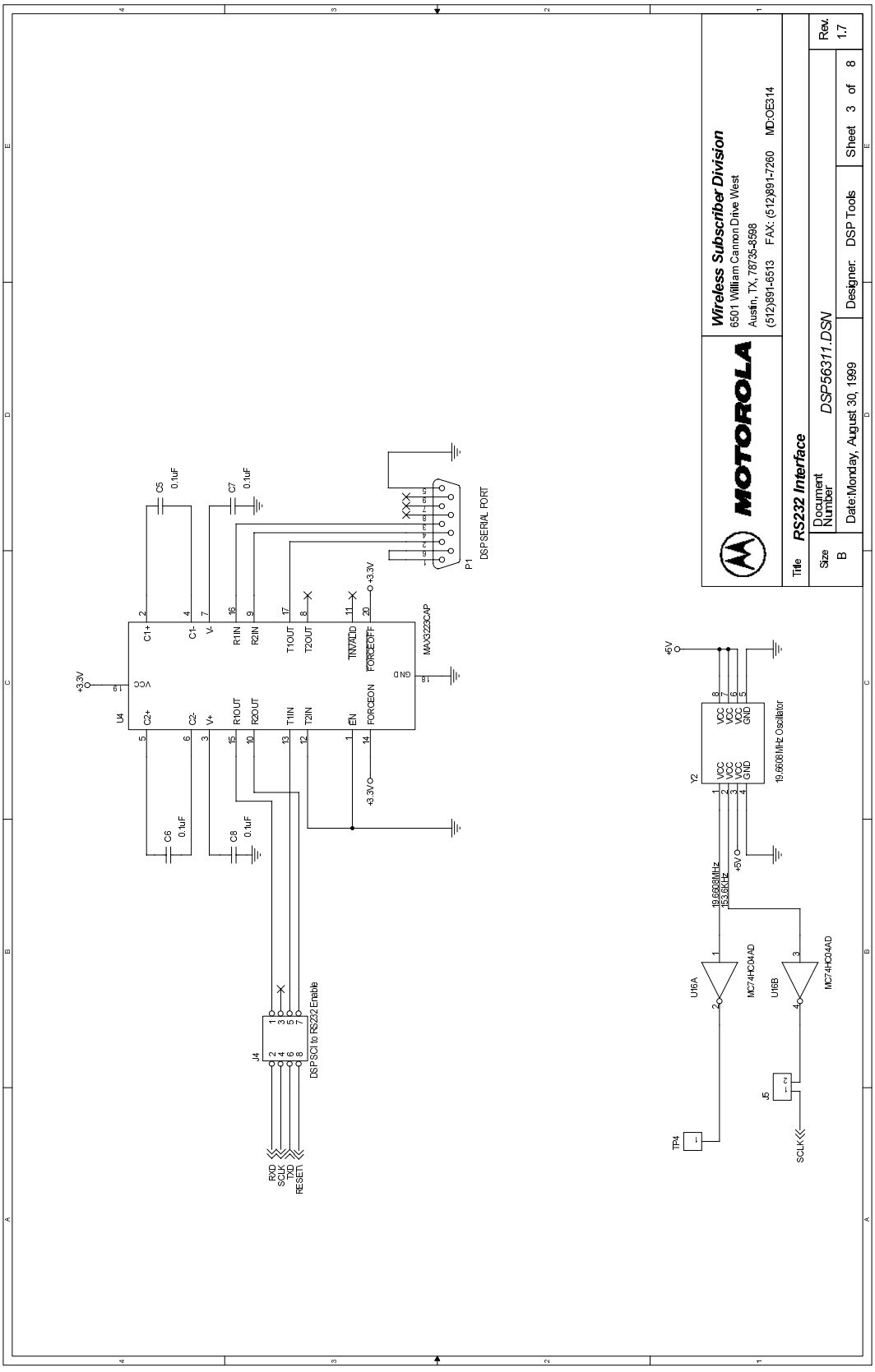

Figure A-3. RS232 Interface

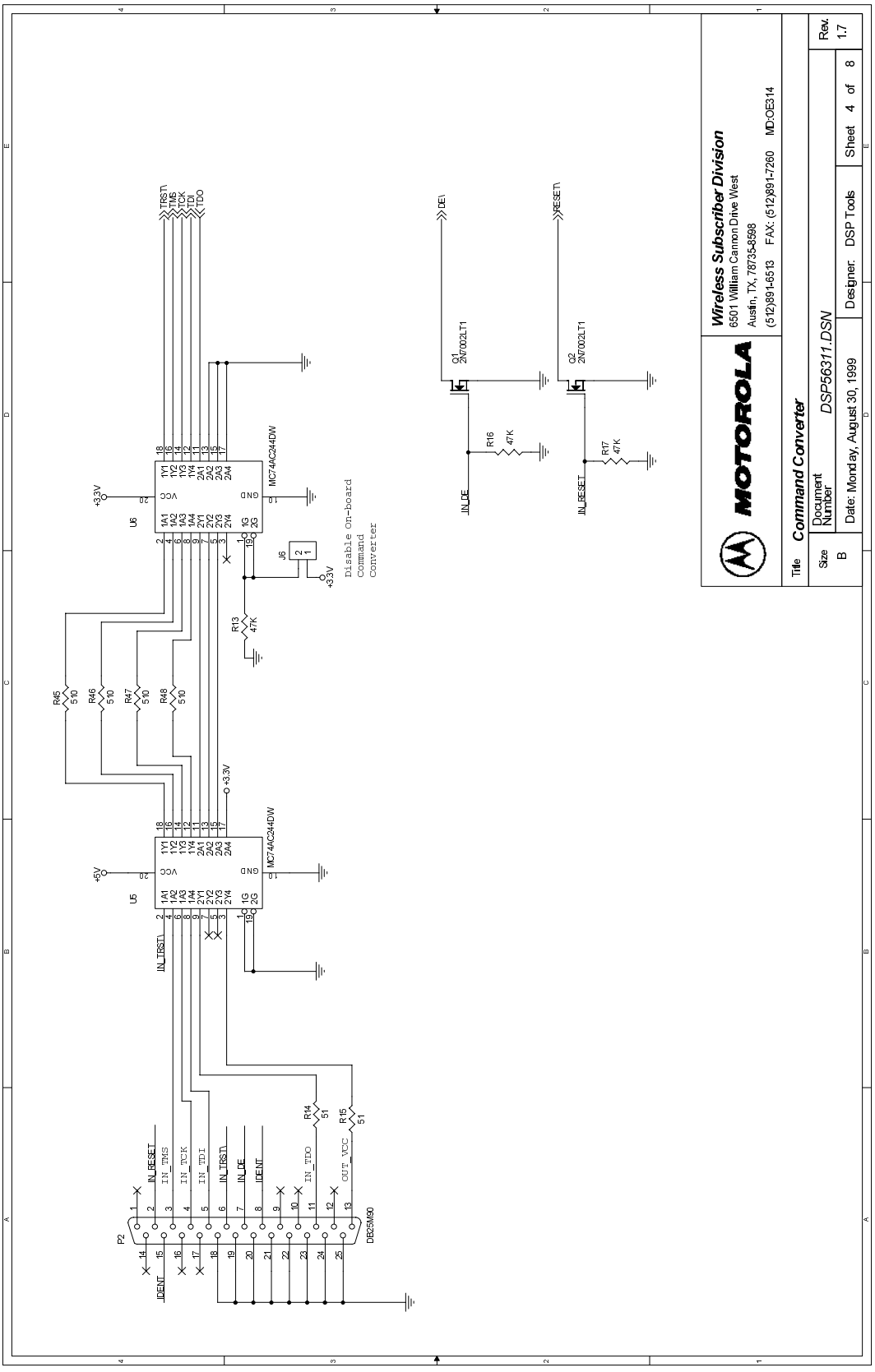

Figure A-4. Command Converter

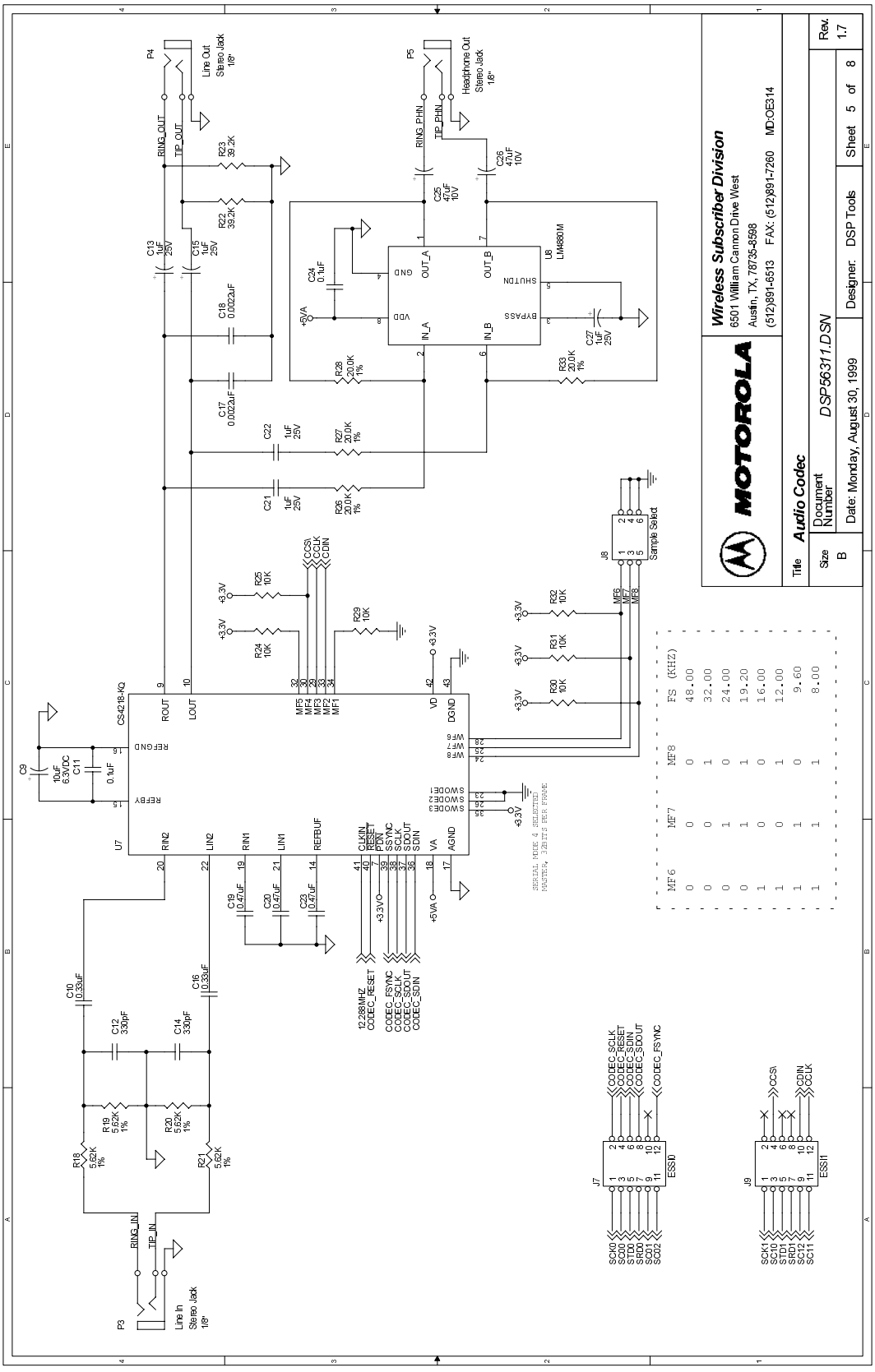

Figure A-5. Audio Codec

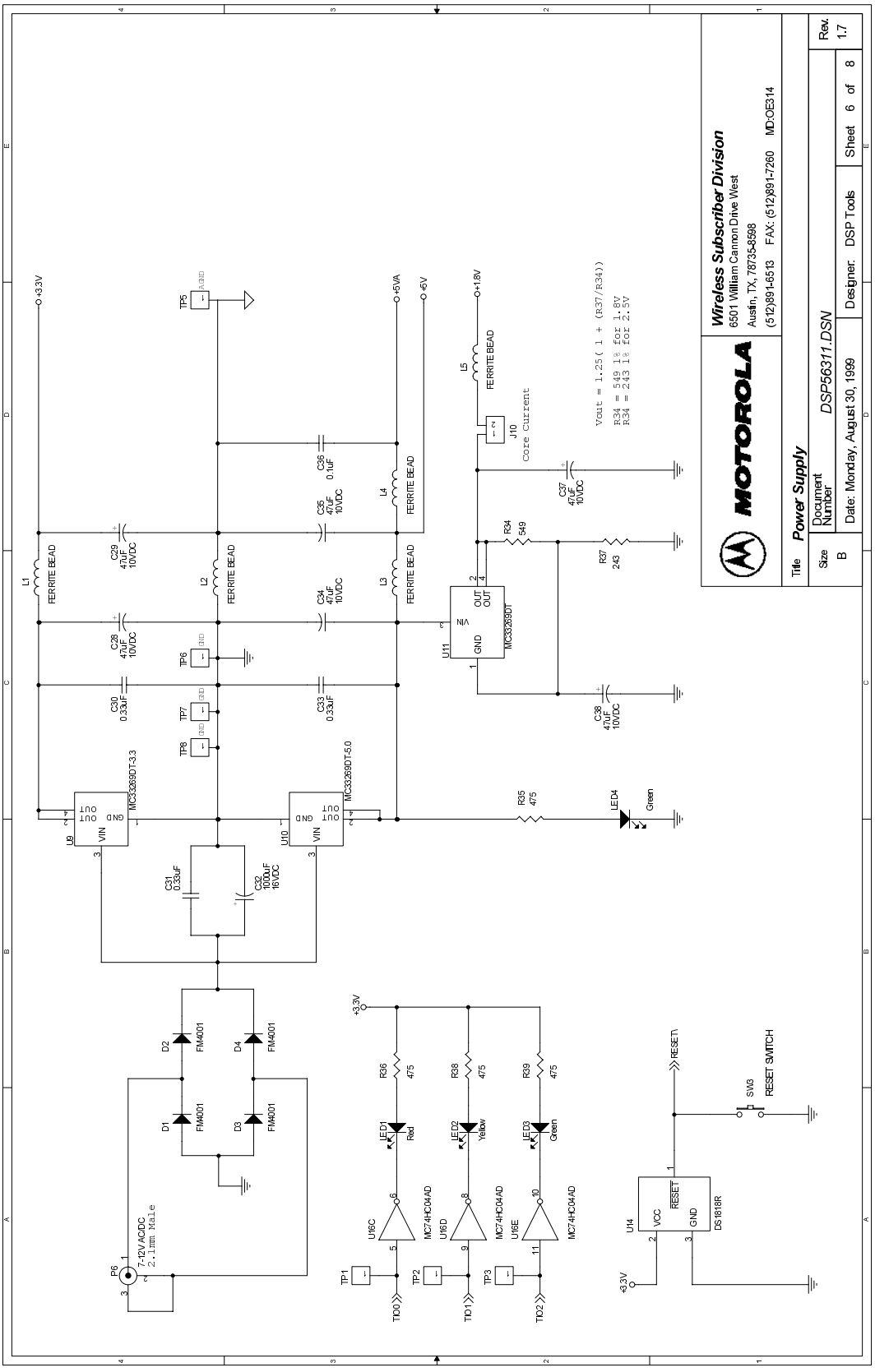

Figure A-6. Power Supply

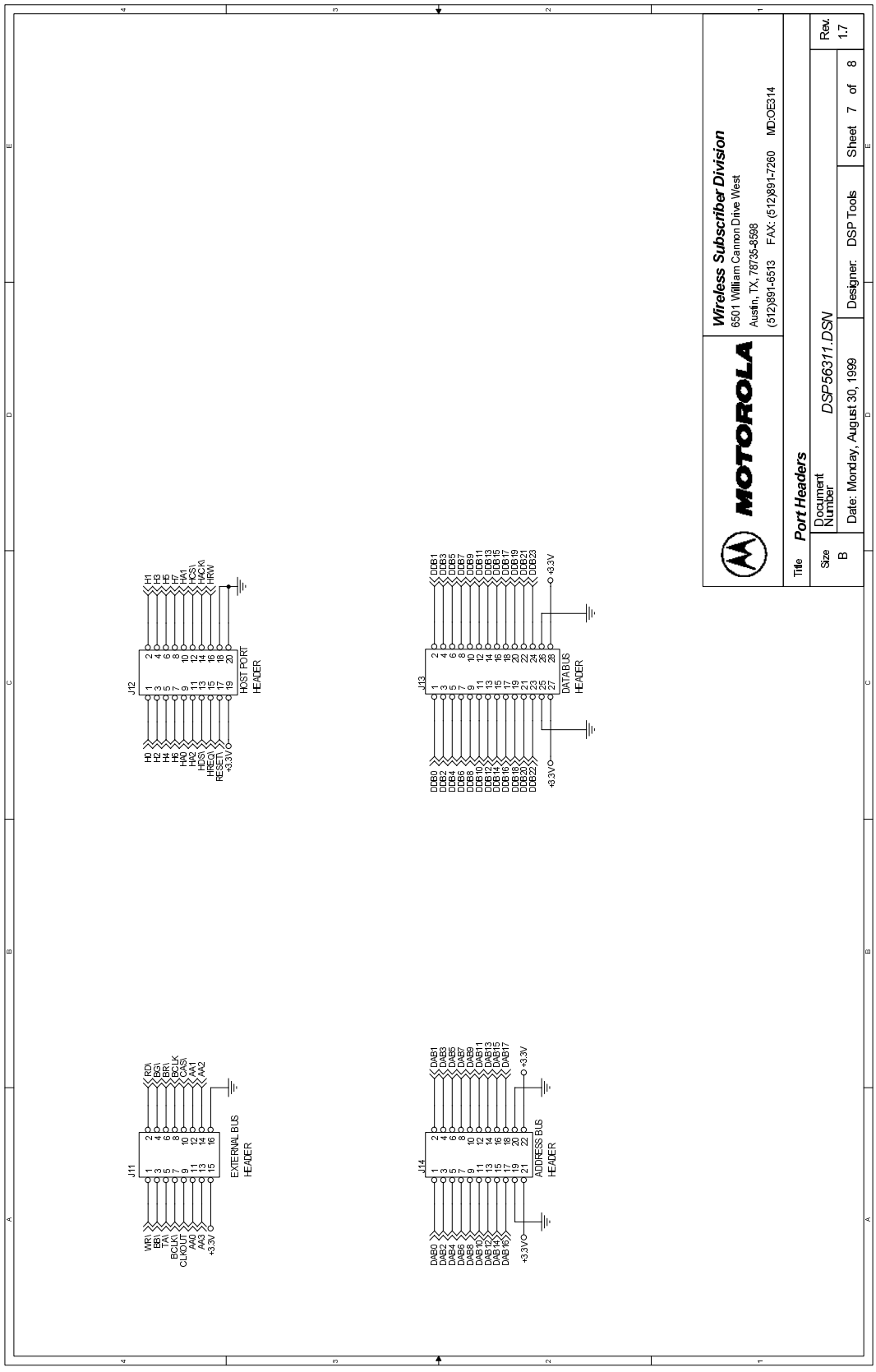

Figure A-7. Port Headers

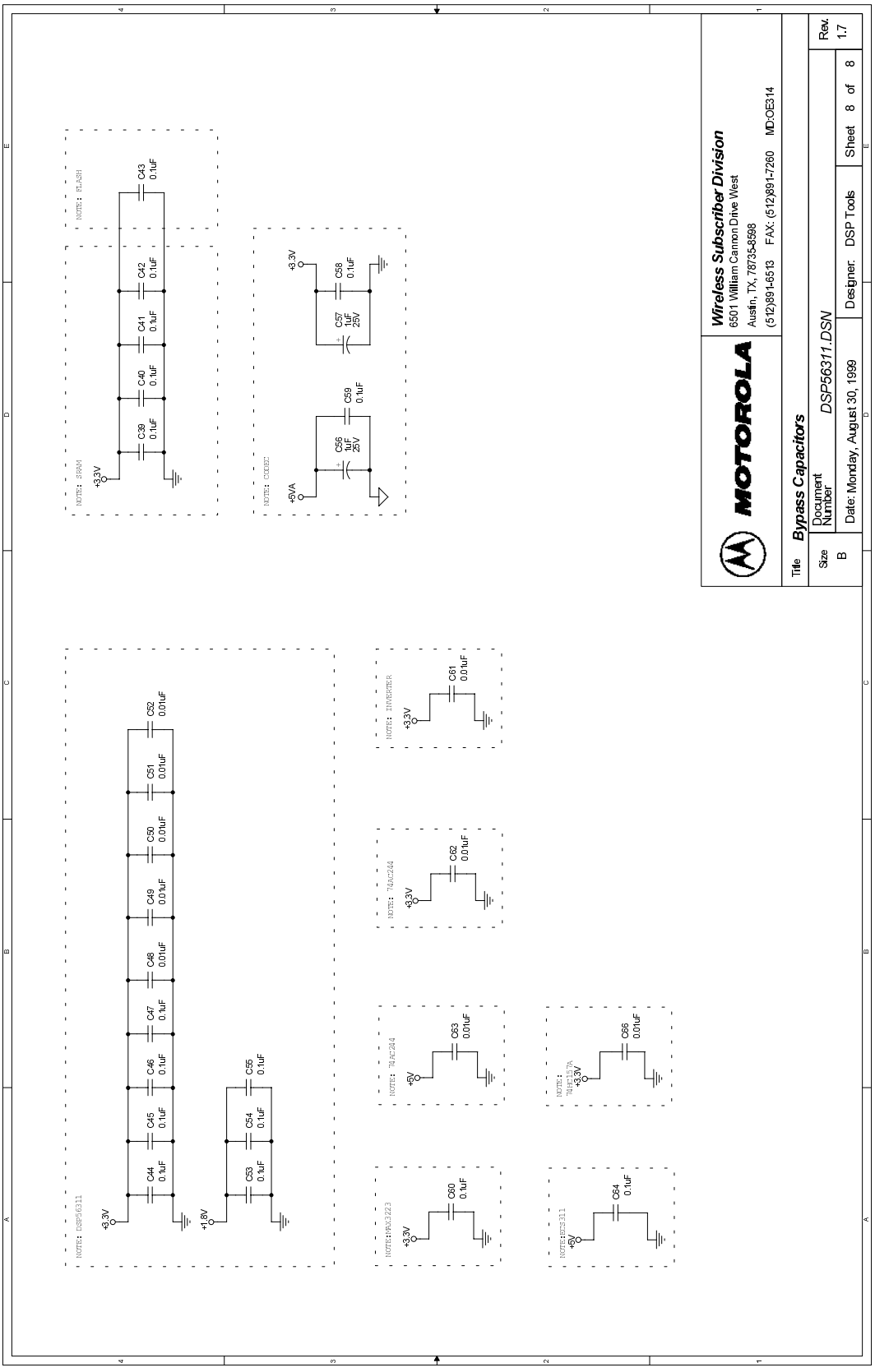

Figure A-8. Bypass Capacitors

Appendix B
DSP56311EVM Parts List

The following table contains information on the parts and devices on the DSP56311EVM.

Table B-1. DSP56311EVM Parts List

Qty	Designator	Manufacturer	Part Number	Description
ICs				
1	U1	Motorola	DSP56311GC150	DSP
1	U2	GSI	GS71024T-8	FSRAM
1	U3	Atmel	AT29LV010A-20TC	Flash
1	U4	Maxim	MAX3223CAP	RS-232 Transceiver
2	U5, U6	Motorola	MC74AC244DW	Octal Buffer
1	U7	Crystal Semiconductor	CS4218-KQ	Audio Codec
1	U8	National	LM4880M	Audio Amplifier
1	U9	Motorola	MC33269DT-3.3	3.3V Regulator
1	U10	Motorola	MC33269DT-5.0	5V Regulator
1	U11	Motorola	MC33269DT	Adj Regulator
1	U14	Dallas Semiconductor	DS1818R	Power-On-Reset
1	U16	Motorola	MC74HC04AD	Hex Inverter
1	U17	Motorola	MC74HC157AD	Multiplexer
Transistors				
2	Q1, Q2	Motorola	2N7002LT1	Transistor
Diodes				
4	D1, D2, D3, D4	Rectron	FM4001	IN4001 Diode
LEDs				
1	LED1	Hewlett Packard	HSMS-C650	Red LED
1	LED2	Hewlett Packard	HSMY-C650	Yellow LED

Table B-1. DSP56311EVM Parts List (Continued)

Qty	Designator	Manufacturer	Part Number	Description
2	LED3, LED4	Hewlett Packard	HSMG-C650	Green LED
Crystals				
1	Y1	ECS	ECS-122.8-S-4	12.288 MHz Crystal
1	Y2	ECS	OECS-196.6-3-C3X1A	19.6608 MHz /153.6 KHz Oscillator
Switches				
3	SW1, SW2, SW3	Panasonic	EVQ-QS205K	6 mm Switch
Connectors				
1	P1	Amphenol	617-C009S-AJ120	DB-9 Female Connector
1	P2	Amphenol	617-A025P-AJ120	DB-25 Female Connector
3	P3, P4, P5	Switchcraft	35RAPC4BHN2	3.5 mm Miniature Stereo Jack
1	P6	Switchcraft	RAPC-722	2.1 mm DC Power Jack
Connector Blocks				
2	J1, J4	Samtec	TSW-104-07-L-D	Header 8 pin double row
1	J2	Samtec	TSW-107-07-L-D	Header 14 pin double row
2	J3, J17	Samtec	TSW-103-07-L-S	Header 3 pin single row
1	J8	Samtec	TSW-106-07-L-S	Header 6 pin double row
3	J5, J6, J10	Samtec	TSW-102-07-L-S	Header 2 pin single row
2	J7, J9	Samtec	TSW-106-07-L-D	Header 12 pin double row
1	J11	Samtec	TSW-108-07-L-D	Header 16 pin double row
1	J12	Samtec	TSW-110-07-L-D	Header 20 pin double row
1	J13	Samtec	TSW-114-07-L-D	Header 28 pin double row
1	J14	Samtec	TSW-111-07-L-D	Header 22 pin double row
1	J15	Samtec	TSW-104-07-L-S	Header 4 pin single row
Test Points				
4	GND, AGND	Samtec	TSW-101-07-L-S	Header 1 pin single row
Capacitors				
1	C9	NIC	NTC-T106M16TRA	10 µF Capacitor, 16VDC Tantalum

Table B-1. DSP56311EVM Parts List (Continued)

Qty	Designator	Manufacturer	Part Number	Description
7	C13, C15, C21, C22, C27, C56, C57	SMEC	MCCE105M3NV-T1	1.0 μF Capacitor, 50VDC Ceramic
23	C5, C6, C7, C8, C11, C24, C36, C39, C40, C41, C42, C43, C44, C45, C46, C47, C53, C54, C55, C58, C59, C60, C64	SMEC	MCCE104M2NR-T1	0.1 μF Capacitor, 50VDC Ceramic
10	C1, C48, C49, C50, C51, C52, C61, C62, C63, C66	SMEC	MCCE103K2NR-T1	0.01 μF Capacitor, 50VDC Ceramic
2	C3, C4	SMEC	MCCE220J2NO-T1	22 pF Capacitor, 50VDC Ceramic
1	C2	NIC	NTC-T475M10TRA	4.7 μF Capacitor, 10VDC Tantalum
5	C10, C16, C30, C31, C33	SMEC	MCCE334J3NU-T1	0.33 μF Capacitor, 50VDC Ceramic
3	C19, C20, C23	SMEC	MCCE476M3NR-T1	0.47 μF Capacitor, 50VDC Ceramic
2	C12, C14	SMEC	MCCE331J2NR-T1	330 pF Capacitor, 50VDC Ceramic
2	C17, C18	SMEC	MCCE222J2NR-T1	2200 pF Capacitor, 50VDC Ceramic
8	C25, C26, C28, C29, C34, C35, C37, C38	NIC	NTC-L476M16TRD	47 μF Capacitor, 16VDC Tantalum
1	C32	Xicon	XAL16V1000	1000 μF Capacitor, 16VDC Electrolytic
Inductors				
5	L1, L2, L3, L4, L5	Murata	BL01RN1-A62	Ferrite Bead
Resistors				
1	R44	SMEC	RC73A2A100KOHMJT	100 KW, 5% Resistor
20	R1, R2, R4, R5, R6, R7, R8, R9, R10, R24, R25, R29, R30, R31, R32, R40, R41, R42, R43, R53	SMEC	RC73A2A10KOHMJT	10 KW, 5% Resistor
4	R26, R27, R28, R33	SMEC	RC73A2A20KOHMJT	20 KΩ, 5% Resistor
2	R22, R23	SMEC	RC73A2A39.2KOHMfT	39.2 KΩ, 1% Resistor

Table B-1. DSP56311EVM Parts List (Continued)

Qty	Designator	Manufacturer	Part Number	Description
	R13, R16, R17, R49, R50, R51	SMEC	RC73A2A47.5KOHMJT	47 KΩ, 5% Resistor
6	R3, R12, R18, R19, R20, R21	SMEC	RC73A2A5.6KOHMFT	5.62 KΩ, 1% Resistor
1	R11	SMEC	RC73A2A681KOHMJT	680 kΩ, 5% Resistor
1	R34	SMEC	RC73A2A243OHMFT	549 Ω, 1% Resistor
1	R37	SMEC	RC73A2A549OHMFT	243 Ω, 1% Resistor
4	R35, R36, R38, R39	SMEC	RC73A2A475OHMFT	475 Ω, 1% Resistor
4	R45, R46, R47, R48	SMEC	RC73A2A510OHMFT	510 Ω, 1% Resistor
2	R14, R15	SMEC	RC73A2A51OHMFT	51 Ω, 1% Resistor

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