

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Datasheet.Live

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### MOS FIELD EFFECT TRANSISTOR NP80N04MLG, NP80N04NLG, NP80N04PLG

#### SWITCHING N-CHANNEL POWER MOS FET

#### DESCRIPTION

The NP80N04MLG, NP80N04NLG, and NP80N04PLG are N-channel MOS Field Effect Transistors designed for high current switching applications.

#### ORDERING INFORMATION

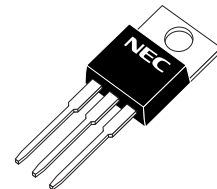
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP80N04MLG-S18-AY <sup>Note</sup>	Pure Sn (Tin)	Tube	TO-220 (MP-25K) typ. 1.9 g
NP80N04NLG-S18-AY <sup>Note</sup>		50 p/tube	TO-262 (MP-25SK) typ. 1.8 g
NP80N04PLG-E1B-AY <sup>Note</sup>		Tape	TO-263 (MP-25ZP) typ. 1.5 g
NP80N04PLG-E2B-AY <sup>Note</sup>		1000 p/reel	

**Note** Pb-free (This product does not contain Pb in the external electrode.)

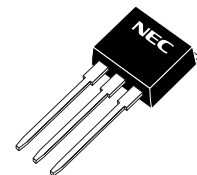
#### FEATURES

- Logic level
- Built-in gate protection diode
- Super low on-state resistance
  - NP80N04MLG, NP80N04NLG
    - $R_{DS(on)1} = 4.8 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 40 \text{ A)}$
    - $R_{DS(on)2} = 9.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 35 \text{ A)}$
  - NP80N04PLG
    - $R_{DS(on)1} = 4.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 40 \text{ A)}$
    - $R_{DS(on)2} = 8.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 35 \text{ A)}$
- High current rating
  - $I_{D(DC)} = \pm 80 \text{ A}$
- Low input capacitance
  - $C_{iss} = 4600 \text{ pF TYP.}$
- Designed for automotive application and AEC-Q101 qualified

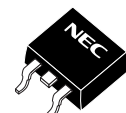
(TO-220)



(TO-262)



(TO-263)



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**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>bs</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±80	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±300	A
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	115	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current <sup>Note2</sup>	I <sub>AR</sub>	37	A
Repetitive Avalanche Energy <sup>Note2</sup>	E <sub>AR</sub>	137	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** T<sub>ch</sub> ≤ 150°C, R<sub>G</sub> = 25 Ω

**THERMAL RESISTANCE**

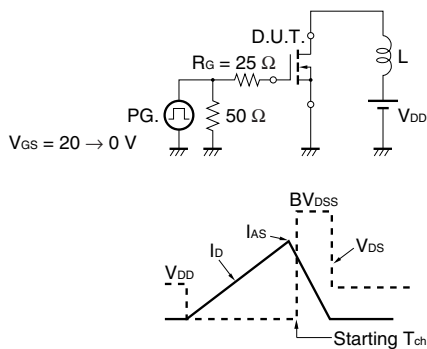
Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	1.30	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

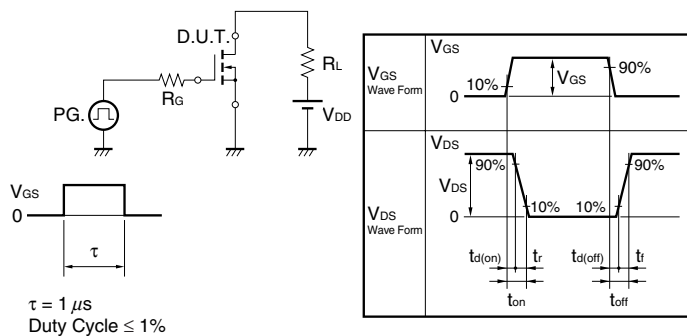
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.4		2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 35 A	25	64		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>Ds(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A NP80N04MLG, NP80N04NLG		3.8	4.8	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A NP80N04PLG		3.3	4.5	mΩ
	R <sub>Ds(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 35 A NP80N04MLG, NP80N04NLG		4.9	9.0	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 35 A NP80N04PLG		4.6	8.7	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V,		4600	6900	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		480	720	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		310	560	pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 40 A,		17	37	ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V,		18	45	ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		74	148	ns
Fall Time	t <sub>f</sub>			8	20	ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 32 V,		90	135	nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V,		13		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 80 A		26		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V		0.95	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 80 A, V <sub>GS</sub> = 0 V,		39		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		39		nC

**Note** Pulsed test

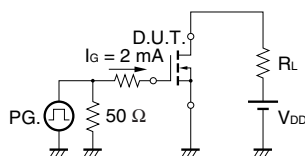
TEST CIRCUIT 1 AVALANCHE CAPABILITY



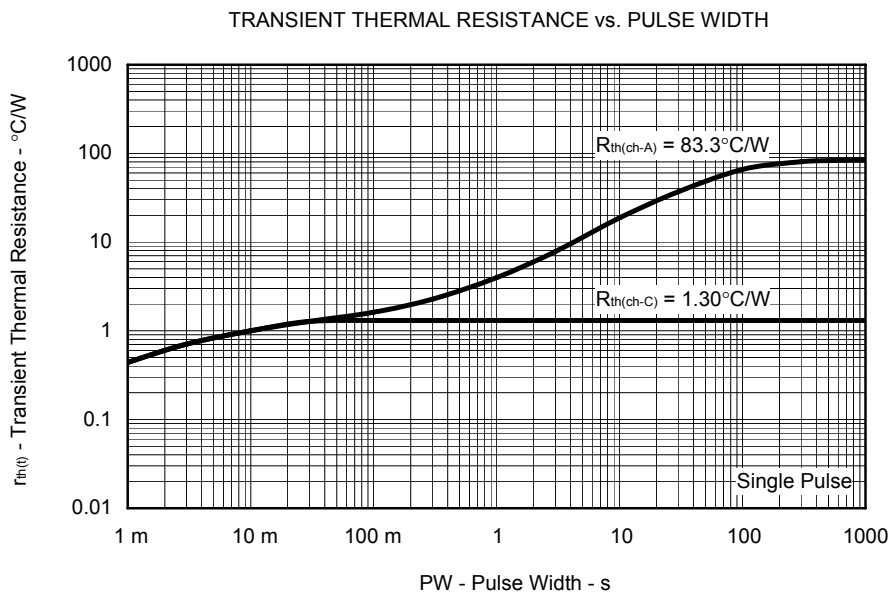
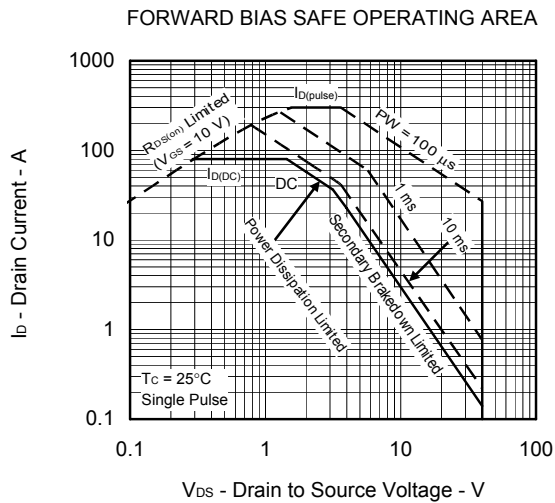
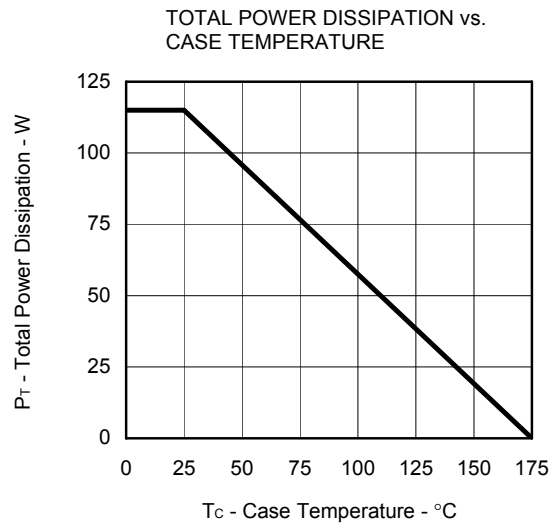
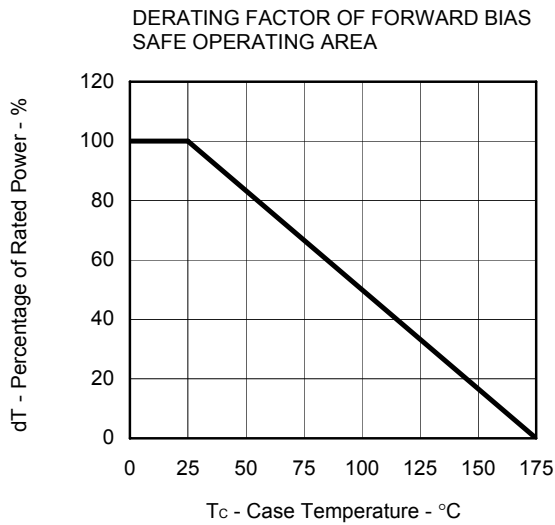
TEST CIRCUIT 2 SWITCHING TIME



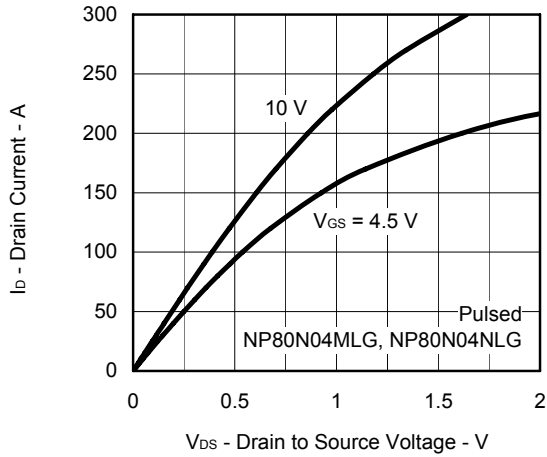
TEST CIRCUIT 3 GATE CHARGE



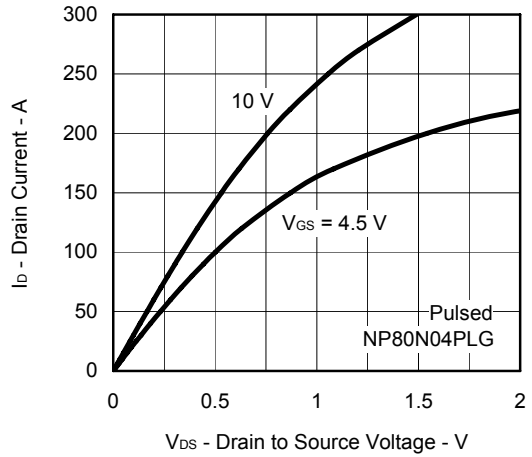
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



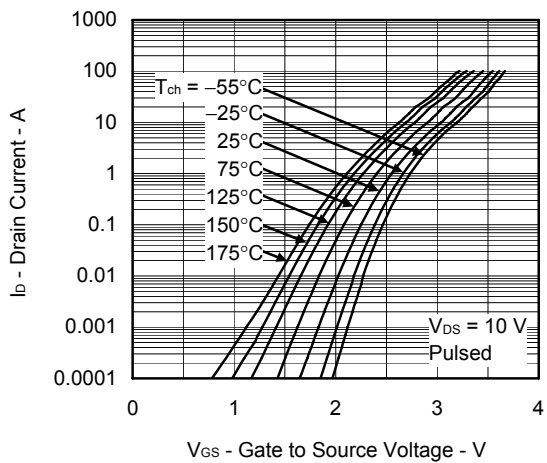
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



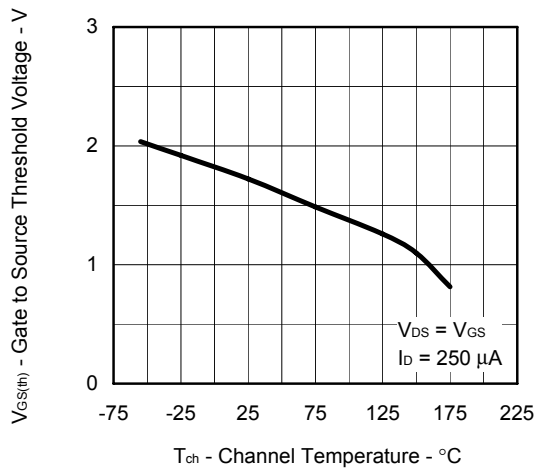
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



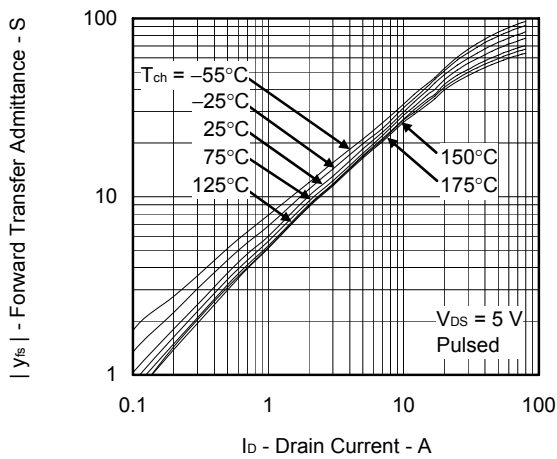
FORWARD TRANSFER CHARACTERISTICS

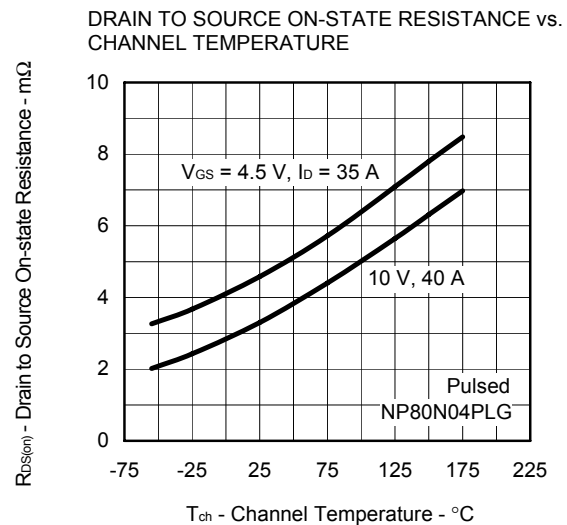
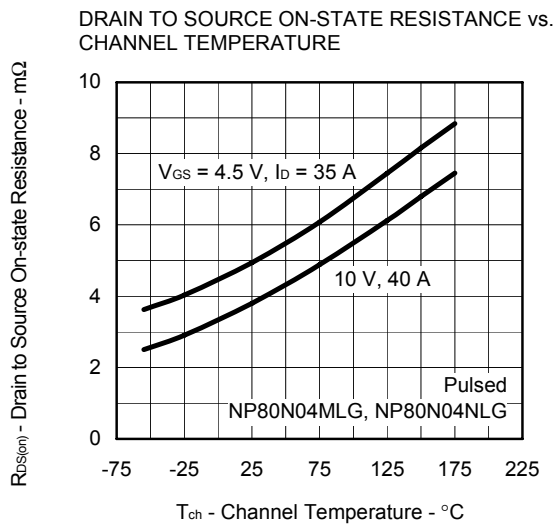
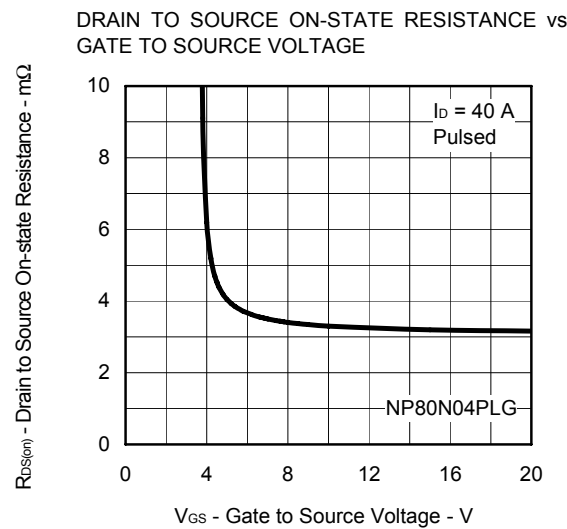
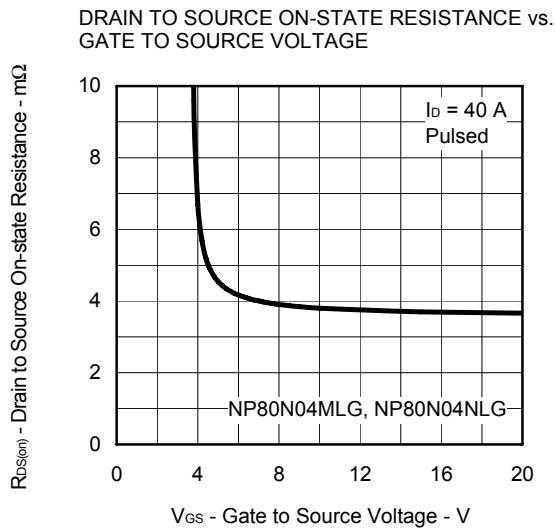
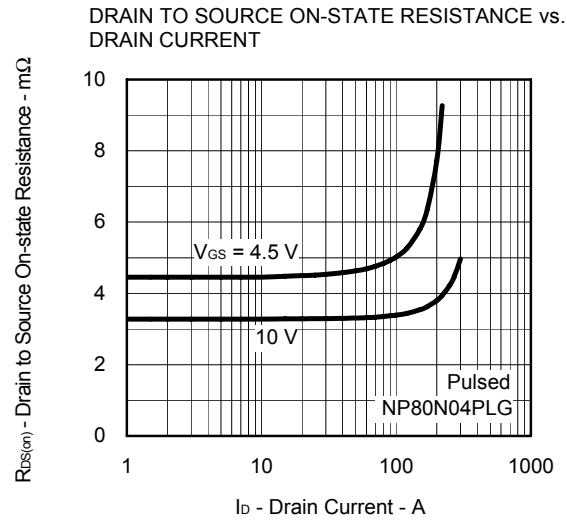
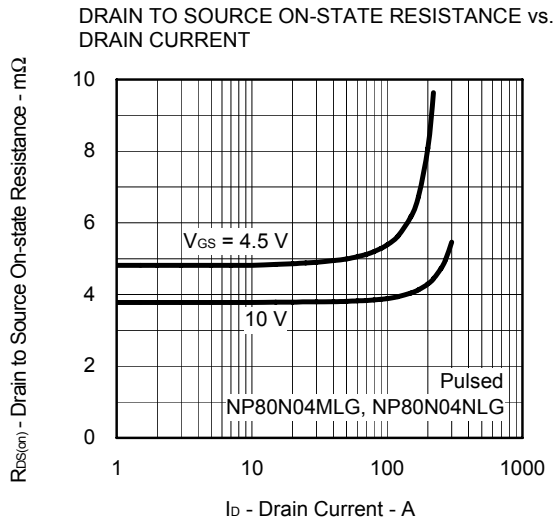


GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



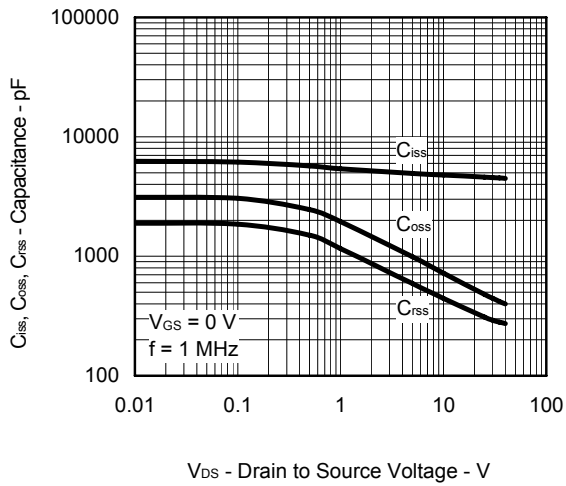
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



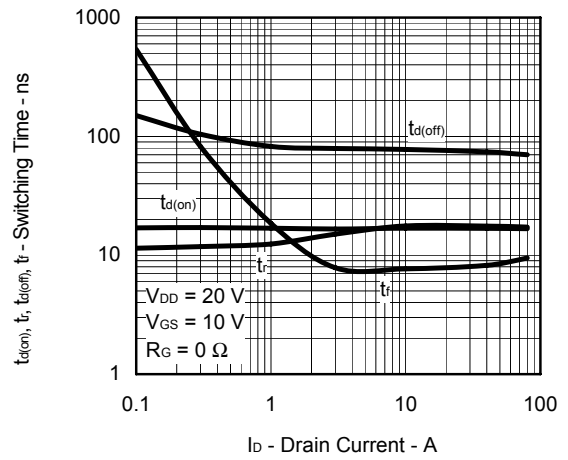




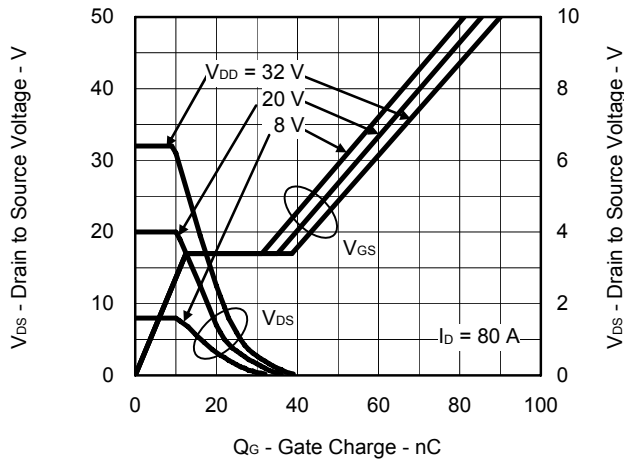
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



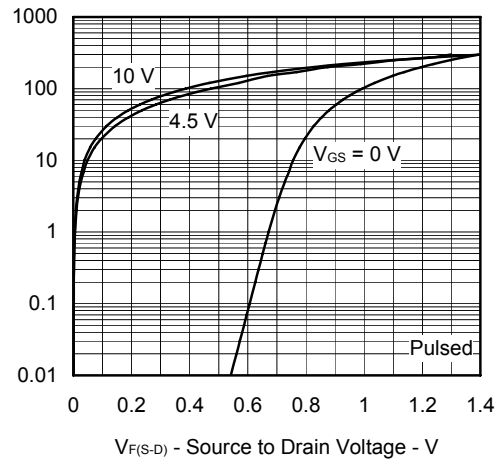
SWITCHING CHARACTERISTICS



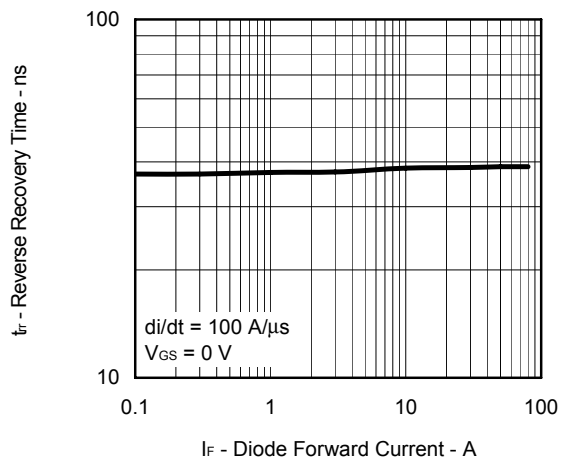
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

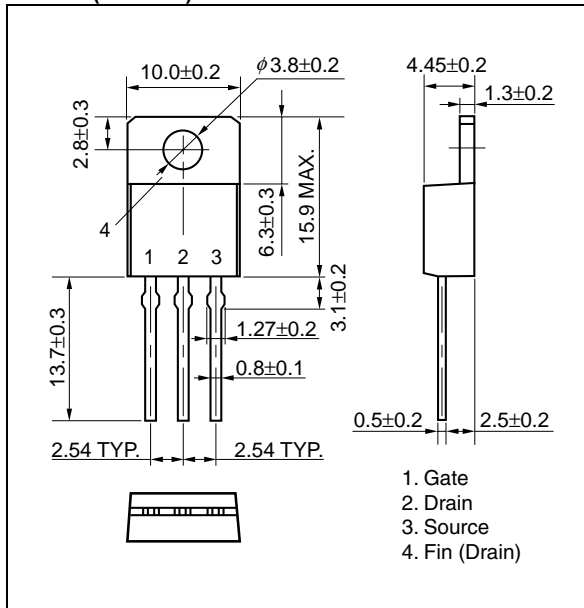


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

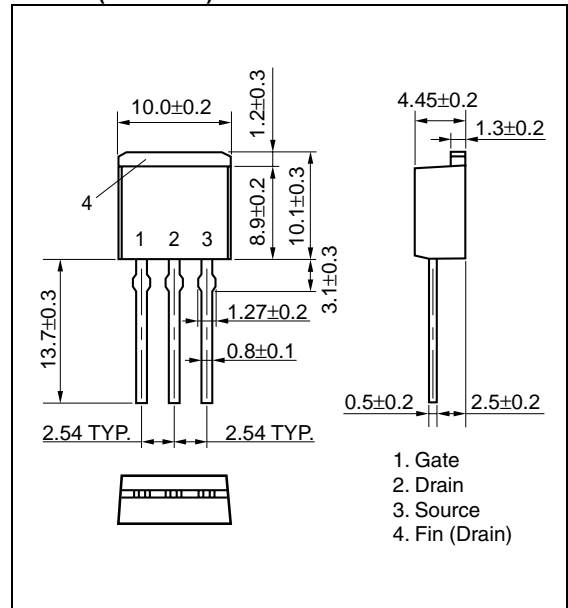


PACKAGE DRAWINGS (Unit: mm)

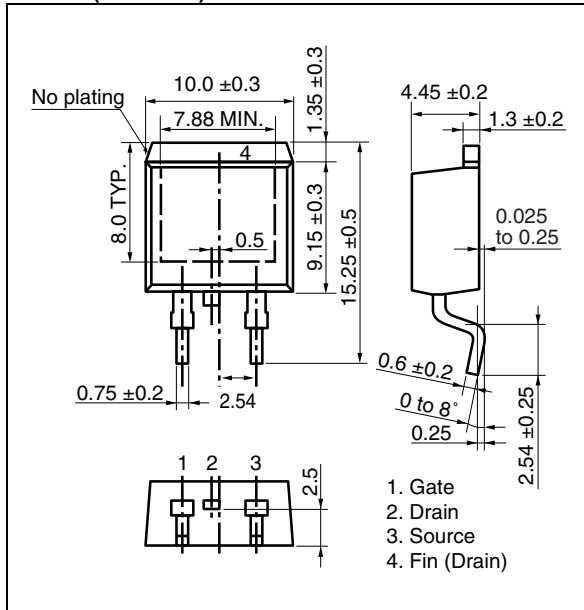
TO-220 (MP-25K)



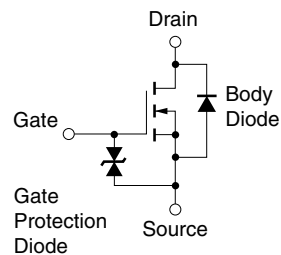
TO-262 (MP-25SK)



TO-263 (MP-25ZP)



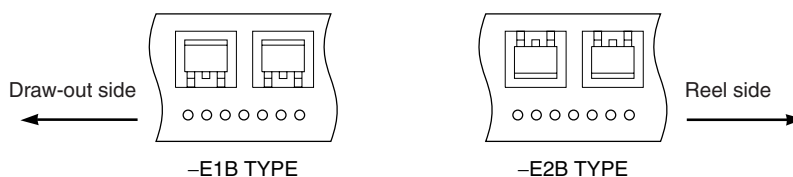
EQUIVALENT CIRCUIT



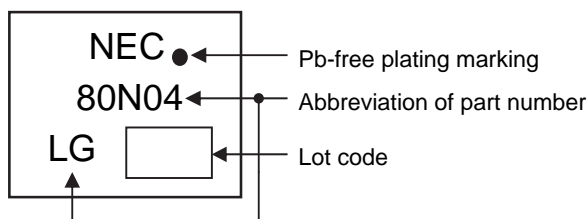
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

**TAPE INFORMATION (NP80N04PLG)**

There are two types (-E1B, -E2B) of taping depending on the direction of the device.



**MARKING INFORMATION**



**RECOMMENDED SOLDERING CONDITIONS**

These products should be soldered and mounted under the following recommended conditions.

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Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow NP80N04PLG	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Wave soldering NP80N04MLG, NP80N04NLG	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating NP80N04MLG, NP80N04NLG, NP80N04PLG	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

**Caution Do not use different soldering methods together (except for partial heating).**

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