

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

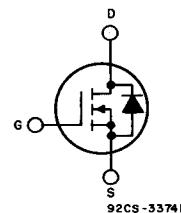
25 A and 30 A, 150 V - 200 V
 $r_{DS(on)} = 0.085 \Omega$ and 0.120Ω

Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

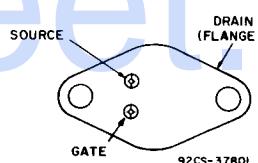
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N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-3780I

JEDEC TO-204AE

The IRF250, IRF251, IRF252 and IRF253 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

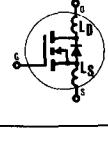
The IRF-types are supplied in the JEDEC TO-204AE metal package.

Absolute Maximum Ratings

Parameter	IRF250	IRF251	IRF252	IRF253	Units
V_{DS} Drain - Source Voltage ①	200	150	200	150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) ①	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	30	30	25	25	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	19	19	16	16	A
I_{DM} Pulsed Drain Current ③	120	120	100	100	A
V_{GS} Gate - Source Voltage			± 20		V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation		150	(See Fig. 14)		W
Linear Derating Factor		1.2	(See Fig. 14)		W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	120	120	100	100	A
<i>(See Fig. 15 and 16) L = 100 μH</i>					
T_J T_{stg} Operating Junction and Storage Temperature Range		-55 to 150			$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

IRF250, IRF251, IRF252, IRF253

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
V_{BDSS} Drain - Source Breakdown Voltage	IRF250 IRF252	200	—	—	V	$V_{GS} = 0\text{V}$	
	IRF251 IRF253	150	—	—	V	$I_D = 250\mu\text{A}$	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20\text{V}$	
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20\text{V}$	
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0\text{V}$	
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	
$I_{D(on)}$ On-State Drain Current ②	IRF250 IRF251	30	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, V_{GS} = 10\text{V}$	
	IRF252 IRF253	25	—	—	A		
$R_{DS(on)}$ Static Drain-Source On-State Resistance ②	IRF250 IRF251	—	0.07	0.085	Ω	$V_{GS} = 10\text{V}, I_D = 16\text{A}$	
	IRF252 IRF253	—	0.09	0.120	Ω		
g_{fs} Forward Transconductance ②	ALL	8.0	14	—	S (Ω)	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, I_D = 16\text{A}$	
C_{iss} Input Capacitance	ALL	—	2000	—	pF	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{ MHz}$ See Fig. 10	
C_{oss} Output Capacitance	ALL	—	800	—	pF		
C_{rss} Reverse Transfer Capacitance	ALL	—	300	—	pF		
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	35	ns	$V_{DD} = 95\text{V}, I_D = 16\text{A}, Z_0 = 4.7\Omega$	
t_r Rise Time	ALL	—	—	100	ns	See Fig. 17	
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	125	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t_f Fall Time	ALL	—	—	100	ns		
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	$V_{GS} = 10\text{V}, I_D = 38\text{A}, V_{DS} = 0.8\text{ Max. Rating.}$ See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q_{gs} Gate-Source Charge	ALL	—	37	56	nC		
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	42	63	nC		
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.	Modified MOSFET symbol showing the internal device inductances. 
L_S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.	

Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	0.83	$^\circ\text{C/W}$	
R_{thCS} Case-to-Sink	ALL	—	0.1	—	$^\circ\text{C/W}$	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	30	$^\circ\text{C/W}$	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRF250 IRF251	—	—	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRF252 IRF253	—	—	25	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRF250 IRF251	—	—	120	A	
	IRF252 IRF253	—	—	100	A	
V_{SD} Diode Forward Voltage ②	IRF250 IRF251	—	—	2.0	V	$T_C = 25^\circ\text{C}, I_S = 30\text{A}, V_{GS} = 0\text{V}$
	IRF252 IRF253	—	—	1.8	V	$T_C = 25^\circ\text{C}, I_S = 25\text{A}, V_{GS} = 0\text{V}$
t_{rr} Reverse Recovery Time	ALL	—	750	—	ns	$T_J = 150^\circ\text{C}, I_F = 30\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR} Reverse Recovered Charge	ALL	—	4.7	—	μC	$T_J = 150^\circ\text{C}, I_F = 30\text{A}, dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C .② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited

by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRF250, IRF251, IRF252, IRF253

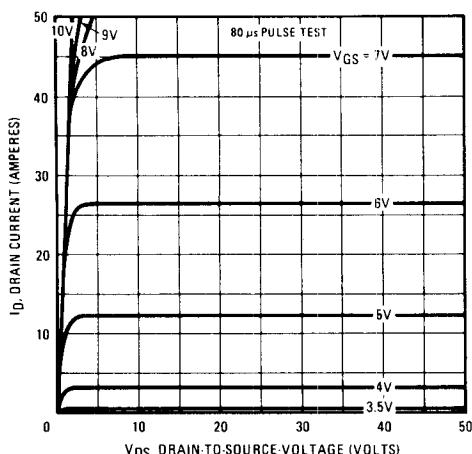


Fig. 1 – Typical Output Characteristics

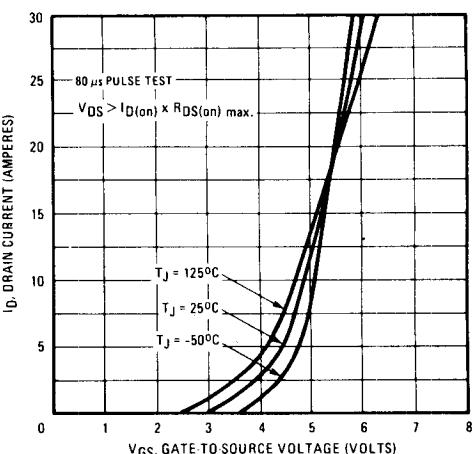


Fig. 2 – Typical Transfer Characteristics

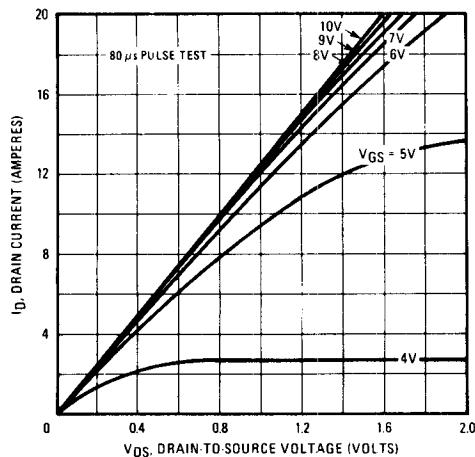


Fig. 3 – Typical Saturation Characteristics

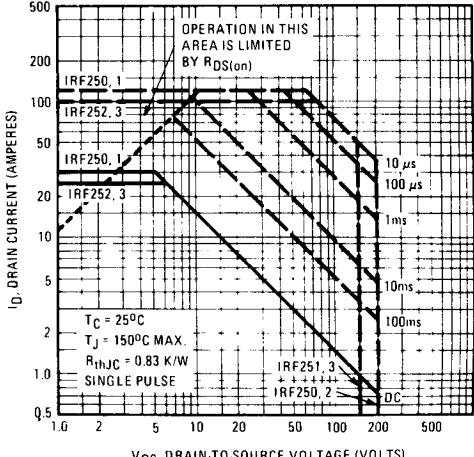


Fig. 4 – Maximum Safe Operating Area

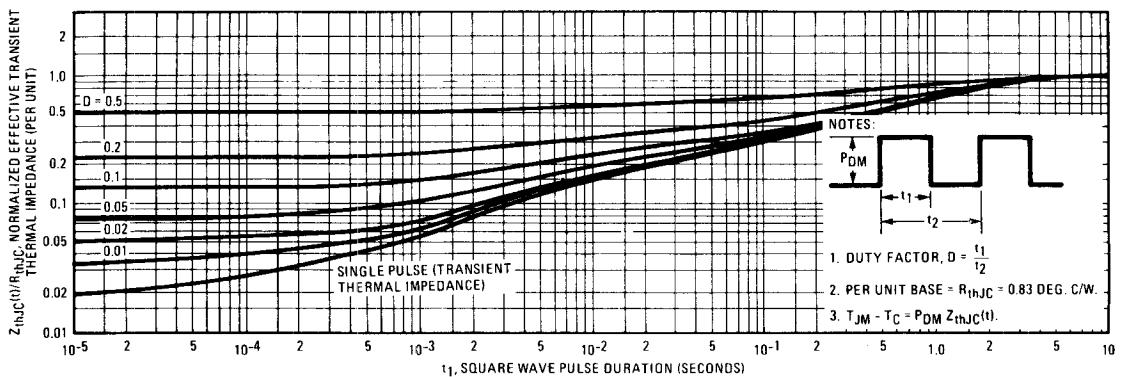


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF250, IRF251, IRF252, IRF253

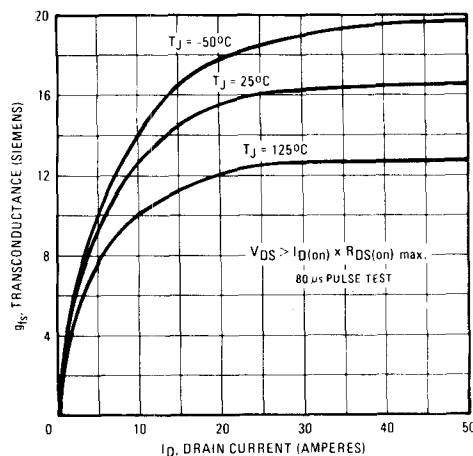


Fig. 6 – Typical Transconductance Vs. Drain Current

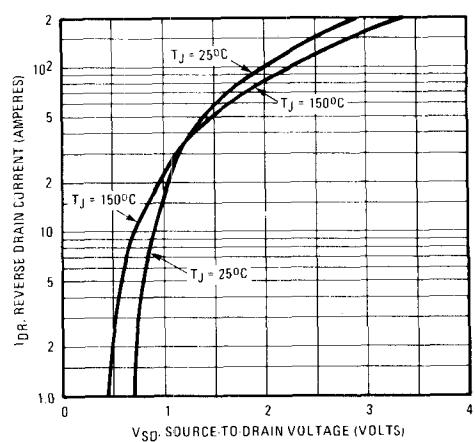


Fig. 7 – Typical Source-Drain Diode Forward Voltage

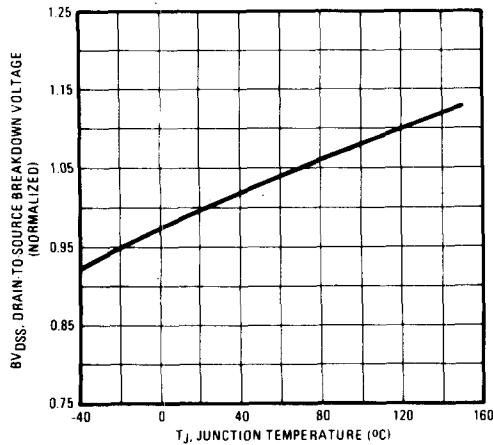


Fig. 8 – Breakdown Voltage Vs. Temperature

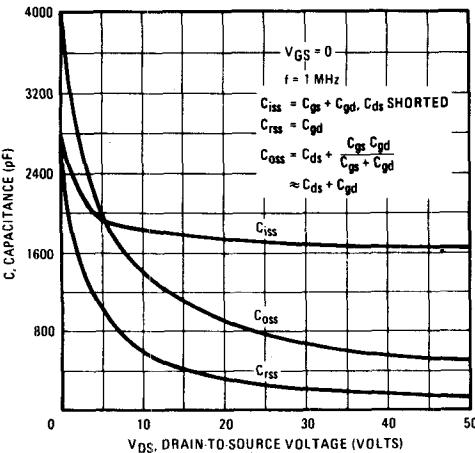


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

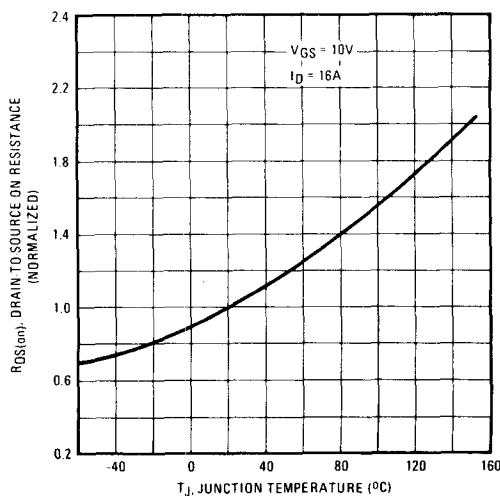


Fig. 9 – Normalized On-Resistance Vs. Temperature

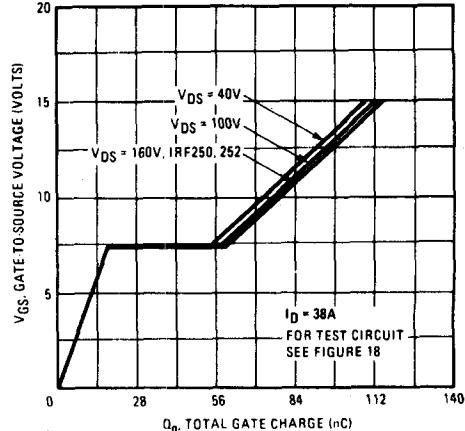


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

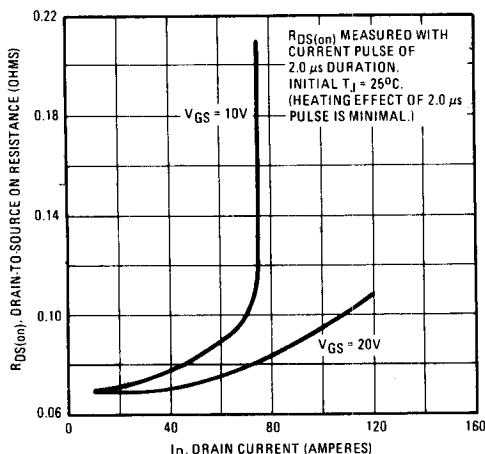
IRF250, IRF251, IRF252, IRF253

Fig. 12 – Typical On-Resistance Vs. Drain Current

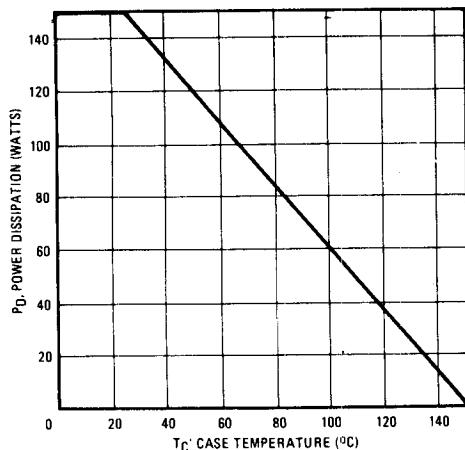


Fig. 14 – Power Vs. Temperature Derating Curve

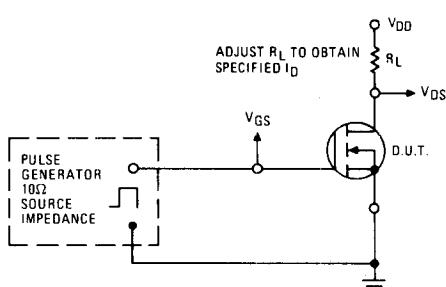


Fig. 17 – Switching Time Test Circuit

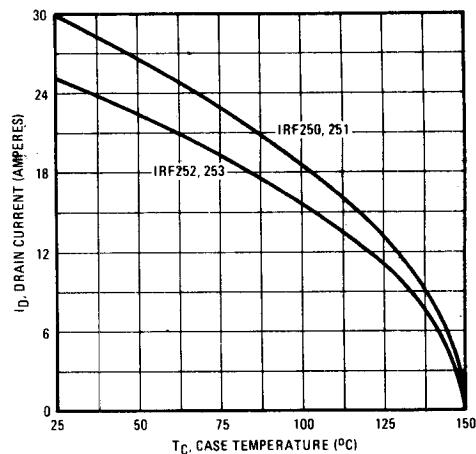


Fig. 13 – Maximum Drain Current Vs. Case Temperature

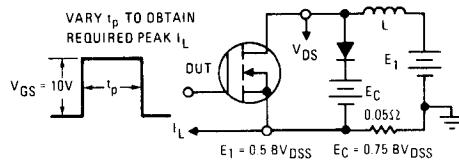


Fig. 15 – Clamped Inductive Test Circuit

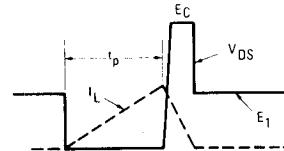


Fig. 16 – Clamped Inductive Waveforms

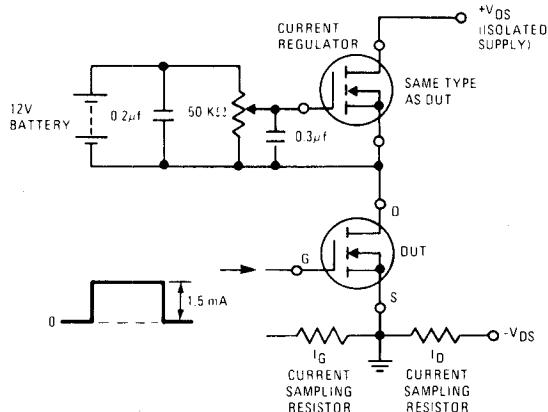


Fig. 18 – Gate Charge Test Circuit