Dual-Output or Two-Phase Synchronous Buck Controller with PMBus

Check for Samples: TPS40422

FEATURES

- **Single Supply Operation: 4.5 V to 20 V**
- **Output Voltage from 0.6 V to 5.6 V**
- **Dual or Two-Phase Synchronous Buck Controller**
- **PMBus Capability**
  - **Margining Up/Down with 2-mV Step**
  - **Programmable Fault Limit and Response**
  - **Output Voltage, Output Current Monitoring**
  - **External Temperature Monitoring with 2N3904**
  - **Programmable UVLO on/off Thresholds**
  - **Programmable Soft Start Time and Turn On/Off Delay**
- **On-Chip Non-volatile Memory (NVM) to Store Custom Configurations**
- **180° Out-of-Phase to Reduce Input Ripple**
- **600-mV Reference Voltage with ±0.5% Accuracy from 0°C to 70°C**
- **Inductor DCR Current Sensing**
- **Programmable Switching Frequency from 200 kHz to 1 MHz**
- **Voltage Mode Control with Input Feed Forward**
- **Current Sharing for Multiphase Operation**
- **Supports Pre-biased Output**
- **Differential Remote Sensing**
- **External SYNC**
- **BPEXT Pin Boosts Efficiency by Supporting External Bias Power**
- **OC/OV/UV/OT Fault Protection**
- **40-Pin, 6 mm × 6 mm, QFN Package**

APPLICATIONS

- **Multiple Rail Systems**
- **Telecom Base Station**
- **Switcher/Router Networking**
- **Server and Storage System**

DESCRIPTION

The TPS40422 is a dual-output PMBus synchronous buck controller. It can be configured also for a single, two-phase output.

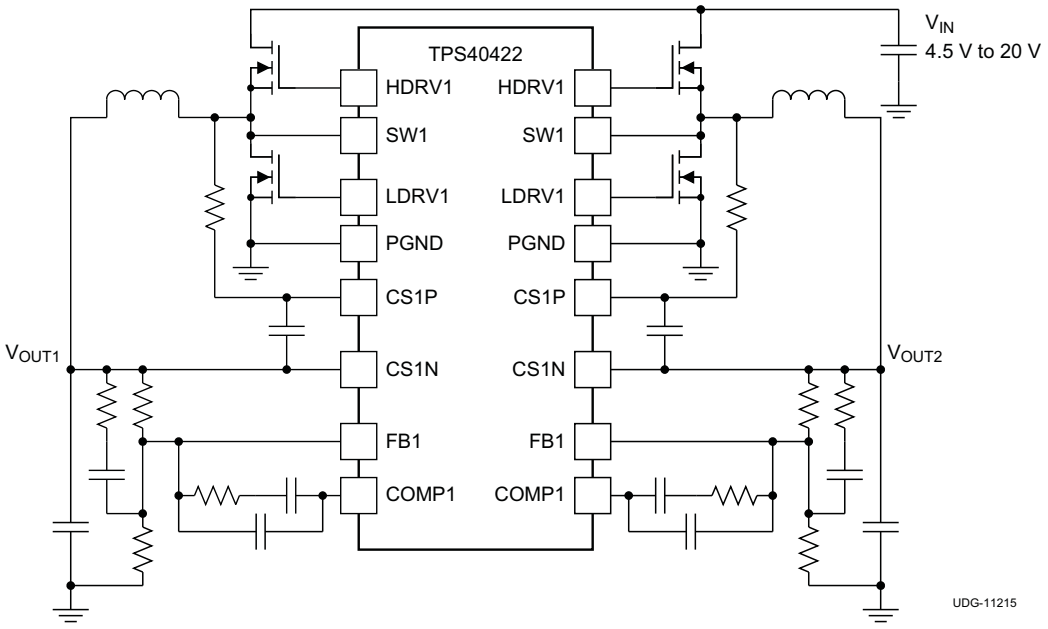
Its wide input range can support 5-V and 12-V intermediate buses. The accurate reference voltage satisfies the need of precision voltage to the modern ASICs and potentially reduces the output capacitance. Voltage mode control is implemented to reduce noise sensitivity and also ensures low duty ratio conversion.

Using the PMBus protocol, the TPS40422 margining function, reference voltage, fault limit, UVLO threshold, soft start time and turn on/off delay can be programmed.

In addition, an accurate measurement system is implemented to monitor the output voltages, currents and temperatures for each channel.

PRODUCT PREVIEW

SIMPLIFIED APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCT PREVIEW

ORDERING INFORMATION

TEMPERATUREE RANGE	PACKAGE	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ORDERABLE DEVICE NUMBER
–40°C to 125°C	QFN	40	Tape and Reel	2000	TPS40422RHAR
			Tube	90	TPS40422RHAT

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
Input voltage range(2)	VDD	–0.3	20	V
	BOOT1	–0.3	30	
	BOOT1 - SW1, BOOT2 - SW2	–0.3	7	
	CLK, DATA, CNTL1, CNTL2, SYNC	–0.3	3.6	
	FB1, FB2, VSNS1, VSNS2, BPEXT	–0.3	7	
Output voltage range(3)	LDRV1, LDRV2, BP6	–0.3	7	V
	SW1, SW2	–1	30	
	COMP1, COMP2, DIFFO1, $\overline{\text{SMBALRT}}$, PG1, PG2, TSNS1, TSNS2	–0.3	7	
	ADDR0, ADDR1, BP3, RT	–0.3	3.6	
Electrostatic discharge	Human Body Model (HBM)	2		kV
	Charged Device Model (CDM)	1.5		
Storage junction temperature, T_J		–40	150	°C
Operating junction temperature, T_{stg}		–55	155	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
VDD	Input operating voltage		4.5	20	V
T_J	Operating junction temperature		–40	125	°C
	Electrostatic discharge (ESD) ratings	Human Body Model (HBM)	2000		V
		Charge Device Model (CDM)	1500		

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ELECTRICAL CHARACTERISTICS(1)

T_J = –40°C to 125°C, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input supply voltage range		4.5		18	V
V_{VIN}	Power stage voltage range		0		18	V
I_{VDD}	Input operating current	Switching, no output load			20	mA
		Not switching			20	
UVLO						
$V_{IN(on)}$	Input turn on voltage(2)	Default settings	4.0	4.25	4.5	V
$V_{IN(off)}$	Input turn off voltage(2)	Default settings	3.8	4	4.2	V
$V_{INON(rng)}$	Programmable range for turn on voltage		4.25		16	V
$V_{INOFF(rng)}$	Programmable range for turn off voltage		4		15.75	V
ERROR AMPLIFIER						
V_{FB}	Feedback pin voltage	0°C ≤ T_J ≤ 70°C	597	600	603	mV
		–40°C ≤ T_J ≤ 125°C	594	600	606	
A_{OL}	Open-loop gain		80			dB
G_{BWP}	Gain bandwidth product		15			MHz
I_{FB}	FB pin bias current (out of pin)	V_{FB} = 0.6 V		TBD	50	nA
I_{COMP}	Sourcing	V_{FB} = 0 V	1			mA
	Sinking	V_{FB} = 1 V	1			
BP6 REGULATOR						
V_{BP6}	Output voltage	I_{BP6} = 10 mA	6.2	6.5	6.8	V
	Dropout voltage	V_{VIN} – V_{BP6}, V_{VDD} = 4.5 V, I_{BP6} = 25 mA			100	mV
I_{BP6}	Output current	VVDD = 12 V	120			mA
V_{BP6UV}	Regulator UVLO voltage		3.3	3.55	3.8	V
$V_{BP6UV(hyst)}$	Regulator UVLO voltage hysteresis		230	255	270	mV
BPEXT						
$V_{BPEXT(swover)}$	BPEXT switch-over voltage		4.6	4.7		V
$V_{hys(swover)}$	BPEXT switch-over hysteresis		100		200	mV
$V_{BPEXT(do)}$	BPEXT dropout voltage	V_{BPEXT}–V_{BP6}, V_{BPEXT} = 4.8 V, I_{BP6} = 25 mA			100	mV
BOOTSTRAP						
$V_{BOOT(drop)}$	Bootstrap voltage drop	I_{BOOT} = 5 mA			100	mV
BP3 REGULATOR						
V_{BP3}	Output voltage	V_{VDD} = 4.5 V, I_{BP3} ≤ 5 mA	3.1	3.3	3.5	V
OSCILLATOR						
f_{SW}	Adjustment range		200		1000	kHz
	Switching frequency	R_{RT} = 40 kΩ	450	500	550	kHz
V_{RMP}	Ramp peak-to-peak(3)			V_{VDD}/10		V
V_{VLY}	Valley voltage(3)		0.7	0.8	1.0	V
SYNCHRONIZATION						
V_{SYNCH}	SYNC high level threshold		2.0			V
V_{SYNCL}	SYNC low level threshold				0.8	V
t_{SYNC}	Minimum SYNC pulse width(3)				100	ns
$f_{SYNC(max)}$	Maximum SYNC frequency		1000			kHz
$f_{SYNC(min)}$	Minimum SYNC frequency				200	
	SYNC frequency range (increase from nominal oscillator frequency)		–20%		20%	

(1) Thresholds selected by entering high side parameters for PGOOD_ON and PGOOD_OFF. Cannot select same threshold for PGOOD_ON & PGOOD_OFF
(2) By design, hysteresis of at least 150 mV is specified.
(3) Specified by design. Not production tested.

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ELECTRICAL CHARACTERISTICS(1) (continued)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM						
$t_{OFF(min)}$	Minimum off time		100			ns
$t_{ON(min)}$	Minimum pulse				50	ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on	15	25	30	ns
		LDRV off to HDRV on	15	25	30	
SOFT START						
t_{SS}	Soft-start time	Factory default settings		2.8		ms
	Programmable range(4)		0.6		9	ms
	Accuracy over range(4)		–10%		10%	
$t_{ON(delay)}$	Turn-on delay time	Factory default settings		0		ms
$t_{OFF(delay)}$	Turn-off delay time	Factory default settings		0		ms
REMOTE SENSE AMPLIFIER						
Gain	Differential gain		0.995	1.000	1.005	V/V
$V_{OS(rsa)}$	Input offset voltage		–2.00		2.00	mV
BW	Closed-loop bandwidth(4)		2			MHz
$V_{DIFFO(max)}$	Max DIFFO output voltage		V_{BP6}-0.2			V
I_{DIFFO}	Sourcing		1			mA
	Sinking		1			
DRIVERS						
$R_{HS(up)}$	High-side driver pull-up resistance	(V_{BOOT}–V_{SW}) = 6.5 V, I_{HS} = -40 mA	0.8	1.5	2.5	Ω
$R_{HS(dn)}$	High-side driver pull-down resistance	(V_{BOOT}–V_{SW}) = 6.5 V, I_{HS} = 40 mA	0.5	1.0	1.5	
$R_{LS(up)}$	Low-side driver pull-up resistance	I_{LS} = -40 mA	0.8	1.5	2.5	
$R_{LS(dn)}$	Low-side driver pull-down resistance	I_{LS} = 40 mA	0.35	0.60	1.20	
$t_{HS(rise)}$	High-side driver rise time	C_{LOAD} = 5 nF	8	15	25	ns
$t_{HS(fall)}$	High-side driver fall time	C_{LOAD} = 5 nF	8	12	25	
$t_{LS(rise)}$	Low-side driver rise time	C_{LOAD} = 5 nF	8	15	25	
$t_{LS(fall)}$	Low-side driver fall time	C_{LOAD} = 5 nF	8	10	25	
CURRENT SENSING AMPLIFIER						
$V_{CS(rng)}$	Differential input voltage range	V_{CSPx}-V_{CSNx}	-60		60	mV
$V_{CS(cmr)}$	Input common-mode range		0		V_{BP6}–0.2	V
$V_{CS(os)}$	Input offset voltage	V_{CSPx} = V_{CSNx} = 0 V	-3		3	mV
A_{CS}	Current sensing gain		14.85	15.00	15.15	V/V
$V_{CS(out)}$	Amplfier output H2	V_{CSPx}-V_{CSNx} = 20 mV	270	300	330	mV
f_{C0}	Closed-loop bandwidth(4)		3	5		MHz
$V_{CS(chch)}$	Amplifier output difference between CH1, CH2	(V_{CSP1}– V_{CSN1}) = (V_{CSP2}–V_{CSN2}) = 20 mV	-15		15	mV
CURRENT LIMIT						
$t_{OFF(oc)}$	Off-time between restart attempts	Hiccup mode		7×t_{SS}		ms
DCR	Inductor DCR current sensing calibration value	Factory default settings		0.488		mΩ
		Programmable range	0.240		15.500	
$I_{OC(flt)}$	Output current overcurrent fault threshold	Factory default settings		30		A
		Programmable range	3		50	
$I_{OC(warn)}$	Output current overcurrent warning threshold	Factory default settings		27		A
		Programmable range	2		49	
$I_{OC(tc)}$	Output current fault/warning temperature coefficient		3900	4000	4100	ppm/°C

(4) Specified by design. Not production tested.

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ELECTRICAL CHARACTERISTICS(1) (continued)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD (5)						
V_{FBPGH}	FB PGOOD high threshold	Factory default settings		675		mV
V_{FBPGL}	FB PGOOD low threshold	Factory default settings		525		mV
$V_{PG(acc)}$	PGOOD accuracy over range	4.5 V ≤ V_{VDD} ≤ 20 V, 468 mV ≤ V_{PGOOD} ≤ 675 mV	–3%		3%	
$V_{pg(hyst)}$	FB PGOOD hysteresis voltage		15		40	mV
R_{PGOOD}	PGOOD pulldown resistance	V_{FB} = 0, I_{PGOOD} = 5 mA		30	70	Ω
$I_{PGOOD(lk)}$	PGOOD pin leakage current	538 mV ≤ V_{FBx} ≤ 658 mV, V_{PGOOD} = 5 V			20	µA
OUTPUT OVERVOLTAGE/UNDERVOLTAGE						
V_{FBOV}	FB pin over voltage threshold	Factory default settings		700		mV
V_{FBUV}	FB pin under voltage threshold	Factory default settings		500		mV
$V_{UVOV(acc)}$	FB UV/OV accuracy over range	4.5 V ≤ V_{VDD} ≤ 20 V	–3%		3%	
$V_{UVOV(hyst)}$	FB UV/OV hysteresis voltage		15		40	mV
OUTPUT VOLTAGE TRIMMING AND MARGINING						
$V_{FBTM(step)}$	Resolution of FB steps with trim and margin			2		mV
$t_{FBTM(step)}$	Transition time per trim or margin step	After soft-start time		30		µs
$V_{FBTM(max)}$	Maximum FB voltage with trim or margin only			660		mV
$V_{FBTM(min)}$	Minimum FB voltage with trim or margin only			480		mV
$V_{FBTM(rng)}$	FB voltage range with trim and margin combined		420		660	mV
V_{FBMH}	Margin high FB pin voltage	Factory default settings		660		mV
V_{FBML}	Margin low FB pin voltage	Factory default settings		540		mV
TEMPERATURE SENSE AND THERMAL SHUTDOWN						
T_{SD}	Junction shutdown temperature(6)		135	145	155	°C
T_{HYST}	Thermal shutdown hysteresis(6)		15	20	25	
$I_{TSNS(ratio)}$	Ratio of bias current flowing out of TSNS pin, state 2 to state 1		9.7	10.0	10.3	µA
I_{TSNS}(6)	State 1 current out of TSNSx pin			10		µA
I_{TSNS}(6)	State 2 current out of TSNSx pin			100		µA
V_{TSNS}	Voltage range on TSNSx pin(6)		0		1.00	V
$T_{SNS(acc)}$	External temp sense accuracy(6)	-40°C ≤ T_J ≤ 165°C	–5		5	°C
$T_{OT(flt)}$	Overtemperature fault limit(6)	Factory default settings		145		°C
	OT fault limit range(6)		120		165	
$T_{OT(warn)}$	Overtemperature warning limit(6)	Factory default settings		125		°C
	OT warning limit range(6)		100		140	
$T_{OT(step)}$	OT fault/warning step			5		°C
$T_{OT(hys)}$	OT fault/warning hysteresis(6)		15	20	25	°C
MEASUREMENT SYSTEM						
$M_{VOUT(rng)}$	Output voltage measurement range		0.5		5.8	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy		–2.0%		2.0%	
$M_{IOUT(rng)}$	Output current measurement signal range	V_{CSPx}–V_{CSNx}	0		60	mV
$M_{IOUT(acc)}$	Output current measurement accuracy	I_{OUT} ≥ 20 A, DCR = 0.5 mΩ	–1.0		1.0	A
PMBus ADDRESSING						
I_{ADD}	Address pin bias current		8.23	9.75	11.21	µA

(5) Thresholds selected by entering high side parameters for PGOOD_ON and PGOOD_OFF. Cannot select same threshold for PGOOD_ON & PGOOD_OFF
(6) Specified by design. Not production tested.

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ELECTRICAL CHARACTERISTICS(1) (continued)

T_J = –40ºC to 125ºC, V_{IN} = V_{DD} = 12 V, RT set for 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PMBus INTERFACE						
V_{IH}	Input high voltage, CLK, DATA, CNTL		2.1			V
V_{IL}	Input low voltage, CLK, DATA, CNTL				0.8	
I_{IH}	Input high level current, CLK, DATA, CNTL		–10		10	µA
I_{IL}	Input low level current, CLK, DATA, CNTL		–10		10	
V_{OL}	Output low level voltage, DATA, $\overline{\text{SMBALRT}}$	4.5 V ≤ V_{VDD} ≤ 20 V, I_{OUT} = 4 mA			0.8	V
I_{OH}	Output high level open drain leakage current, DATA, $\overline{\text{SMBALRT}}$	V_{OUT} = 5.5 V	0		10	µA
C_{OUT}(7)	Pin capacitance, CLK, DATA				1	pF
F_{PMB}	PMBus operating frequency range	Slave mode	10		400	kHz
t_{BUF}	Bus free time between START and STOP		4.7			µs
$t_{HD:STA}$	Hold time after repeated START		4.0			µs
$t_{SU:STA}$	Repeated START setup time		4.7			µs
$t_{SU:STO}$	STOP setup time		4.0			µs
$t_{HD:DAT}$	Data hold time	Receive mode	0			ns
		Transmit mode	300			
$t_{SU:DAT}$	Data setup time		250			ns
$t_{TIMEOUT}$	Error signal/detect		25		35	µs
$t_{LOW:MEXT}$	Cumulative clock low master extend time				50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time				25	µs
t_{LOW}	Clock low time		4.7			µs
t_{HIGH}	Clock high time		4.0			µs
t_{FALL}	CLK/DATA fall time				300	µs
t_{RISE}	CLK/DATA rise time				1000	µs

(7) Specified by design. Not production tested.

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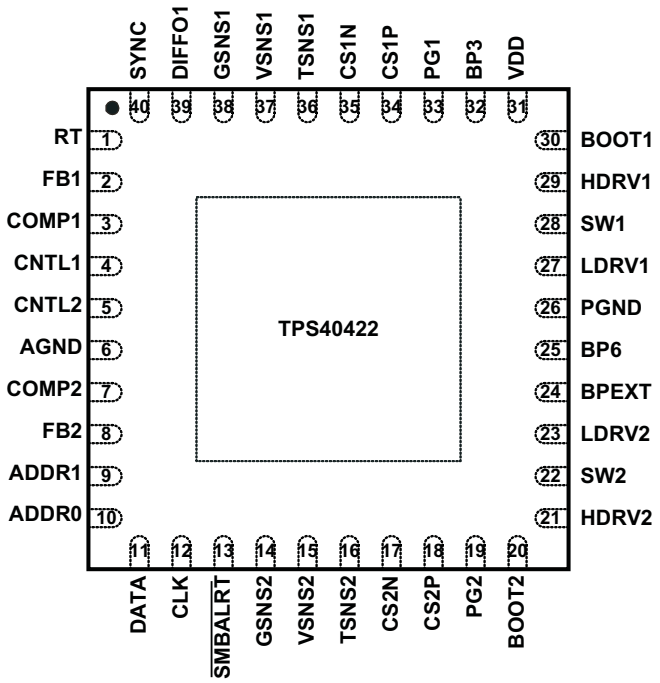
DEVICE INFORMATION



PIN FUNCTIONS

PIN	NO.	I/O	DESCRIPTION
ADDR0	10	I	Low-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to AGND to select the low-order octal digit in the PMBus address.
ADDR1	9	I	High-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to AGND to select the low-order octal digit in the PMBus address.
AGND	6	—	Low-noise ground connection to the controller. Connections should be arranged so that power level currents do not flow through the AGND path.
BOOT1	30	I	Bootstrapped supply for the high-side FET driver for channel 1 (CH1). Connect a capacitor (100 nF typical) from BOOT1 to SW1 pin.
BOOT2	20	I	Bootstrapped supply for the high-side FET driver for channel 2 (CH2). Connect a capacitor (100 nF typical) from BOOT2 to SW2 pin.
BP3	32	O	Output bypass for the internal 3.3-V regulator. Connect a 100 nF or larger capacitor from this pin to AGND.
BP6	25	O	Output bypass for the internal 6.5-V regulator. Connect a low ESR, 1 µF or larger ceramic capacitor from this pin to PGND.
BPEXT	24	I	External voltage input for BP6 switchover function. Connect a 100 nF or larger capacitor from this pin to PGND.
CLK	12	I	Clock input for the PMBus interface. Pull up to 3.3 V with a resistor.
CNTL1	4	I	Logic level input which controls startup and shutdown of CH1, determined by PMBus options.
CNTL2	5	I	Logic level input which controls startup and shutdown of CH2, determined by PMBus options.
COMP1	3	O	Output of the error amplifier for CH1 and connection node for loop feedback components.
COMP2	7	O	Output of the error amplifier for CH2 and connection node for loop feedback components. For two-phase operation, use COMP1 for loop feedback and connect COMP1 to COMP2.
CS1N	35	I	Negative terminal of current sense amplifier for CH1.
CS2N	17	I	Negative terminal of current sense amplifier for CH2.
CS1P	34	I	Positive terminal of current sense amplifier for CH1.
CS2P	18	I	Positive terminal of current sense amplifier for CH2.
DATA	11	I/O	Data input/output for the PMBus interface. Pull up to 3.3 V with a resistor.
DIFFO1	39	O	Output of the differential remote sense amplifier for CH1.

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PIN FUNCTIONS (continued)

PIN	NO.	I/O	DESCRIPTION
FB1	2	I	Inverting input of the error amplifier for CH1. Connect a voltage divider to FB1 between DIFFO1 and AGND to program the output voltage for CH1.
FB2	8	I	Inverting input of the error amplifier for CH2. Connect a voltage divider to FB2 between VSNS2 and GSNS2 to program the output voltage for CH2. For two-phase operation, use FB1 to program the output voltage and connect FB2 to BP6.
GSNS1	38	I	Negative terminal of the differential remote sense amplifier for CH1.
GSNS2	14	I	Negative terminal of the differential remote sense amplifier for CH2.
HDRV1	29	O	Bootstrapped gate drive output for the high-side N-channel MOSFET for CH1.
HDRV2	21	O	Bootstrapped gate drive output for the high-side N-channel MOSFET for CH2.
LDRV1	27	O	Gate drive output for the low side synchronous rectifier (SR) N-channel MOSFET for CH1.
LDRV2	23	O	Gate drive output for the low-side synchronous rectifier N-channel MOSFET for CH2.
PGND	26	—	Power GND.
PG1	33	O	Open drain power good indicator for CH1 output voltage.
PG2	19	O	Open drain power good indicator for CH2 output voltage.
RT	1	I	Frequency programming pin. Connect a resistor from this pin to AGND to set the oscillator frequency.
$\overline{\text{SMBALRT}}$	13	O	Alert output for the PMBus interface. Pull up to 3.3 V with a resistor.
SW1	28	I	Return of the high-side gate driver for CH1. Connect to the switched node for CH1.
SW2	22	I	Return of the high-side gate driver for CH2. Connect to the switched node for CH2.
SYNC	40	I	Logic level input for external clock synchronization. When an external clock is applied to this pin, the oscillator frequency sychronizes to one half of its frequency.
TSNS1	36	I	External temperature sense input for CH1.
TSNS2	16	I	External temperature sense input for CH2.
VDD	31	I	Power input to the controller. Connect a low ESR, 100 nF or larger ceramic capacitor from this pin to AGND.
VSNS1	37	I	Positive terminal of the differential remote sense amplifier for CH1.
VSNS2	15	I	Positive terminal of the differential remote sense amplifier for CH2.

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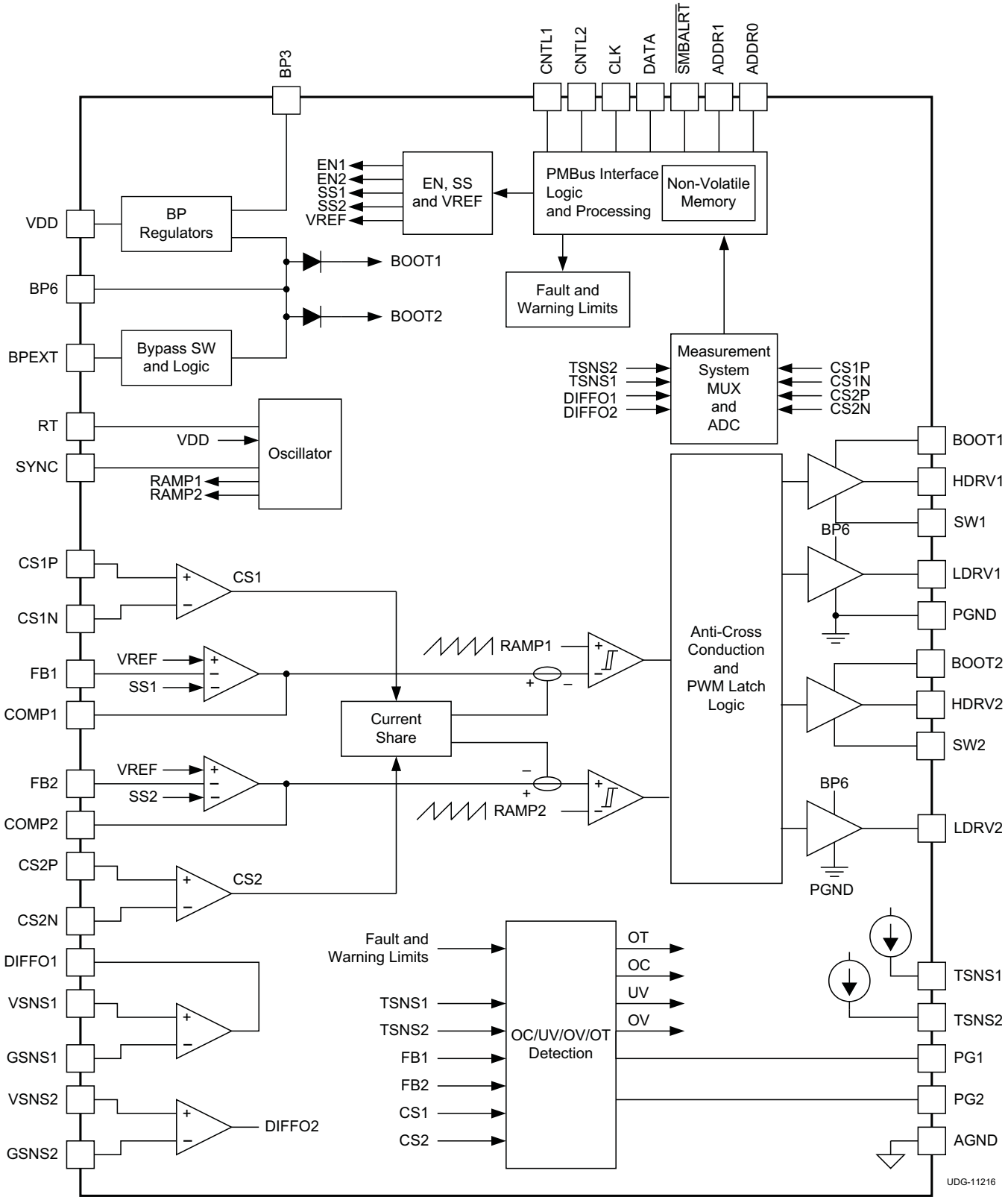
FUNCTIONAL BLOCK DIAGRAM



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS40422RHAR	PREVIEW	VQFN	RHA	40	3000	TBD	Call TI	Call TI	
TPS40422RHAT	PREVIEW	VQFN	RHA	40	250	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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