79S474
Evaluation Board

Hardware User's Manual

Version 1.0
September 1998

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Printed in U.S.A.

About the Manual

Notes

This manual provides a product description, installation instructions, theory of operation, design notes, and six schematic drawings for the 79S474 evaluation board.

Summary of Contents

Chapter 1, "79S474 Description and Installation Instructions," provides an overview on the 79S474 evaluation board features and includes a physical layout diagram, specification summary, and 64- or 32-bit system interface installation instructions. This chapter includes a section on getting started quickly.

Chapter 2, "Theory of Operation and Design Notes," discusses the functional operation of the 79S474 evaluation board. This chapter includes the jumper or switch settings for RC64474 or RC64475 CPU selection and a section that provides information on RC4700, RC64474, and RC64475 clock structure differences.

Chapter 3, "Schematics," includes six schematic drawings on the 79S474 evaluation board.

Important Notation: Although the part referenced on the schematics in Chapter 3 is the S440, these drawings apply to the S474 board. Note too that the processor number R4640 on the diagrams also applies to the RC64474.

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79S474 Description and Installation Instructions

Notes

Introduction

The IDT79S474 is an evaluation board. It is a small module that supports the RC64475 and the RC64474 on a single printed circuit board (PCB). The S474 allows the system designer to evaluate the performance of either CPU without modification to the existing design. The S474 plugs directly into the PGA socket of the R4700 in any board, including the 79S465 evaluation board. Figure 1.1 shows a block diagram of the 79S474. The board's physical layout is shown in Figure 1.2 on page 2.

Overview Of Features

Major features of the 79S474 include:

- *RC64475/RC64474 highly integrated RISController CPU support*
- *RC64474/RC64475 clock generation circuitry*
- *3.3V and 5V operation*
- *32-bit system interface support for RC64474 and RC64475*
- *64-bit system interface support for RC64475*

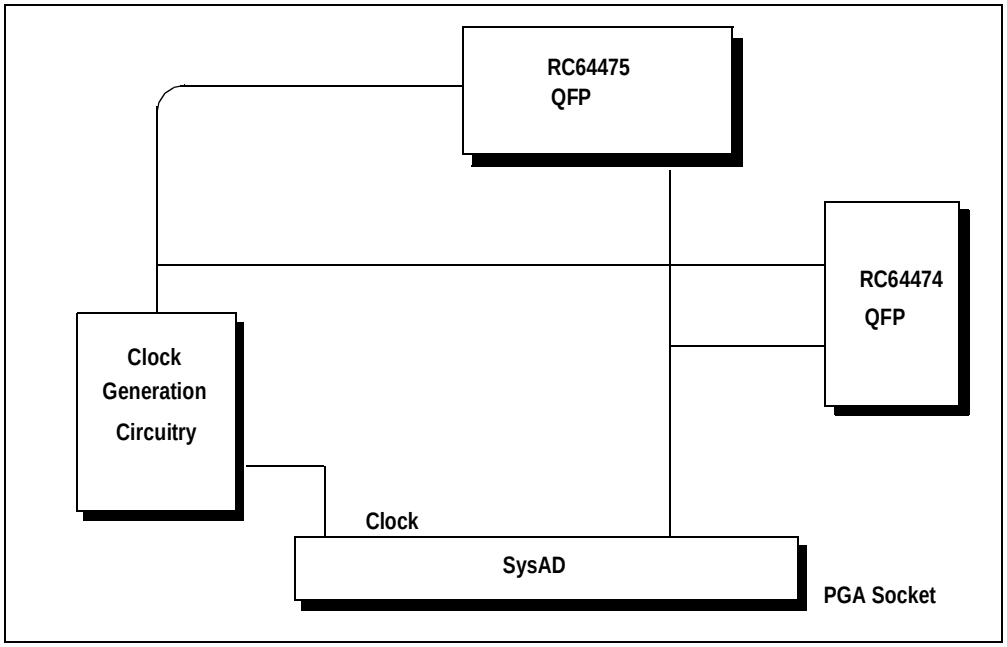

Figure 1.1 79S474 Block Diagram

Explanation of Features

The 79S474 is configured to plug directly into the 79S465 evaluation board. It supports the RC64475 QFP footprint as well as the QPF footprint of the RC64474. Selection between the two CPU options is accomplished through hardware jumpers that are not readable by software.

The 79S474 can be used to evaluate system performance of either the RC64475 or the RC64474. The S474 supports 32-bit system interface for the RC64474 and RC64475 as well as 64-bit system interface for the RC64475. The 79S474 draws power from the 79S465 evaluation board through the PGA socket it is plugged into and supports 5V operations.

Notes

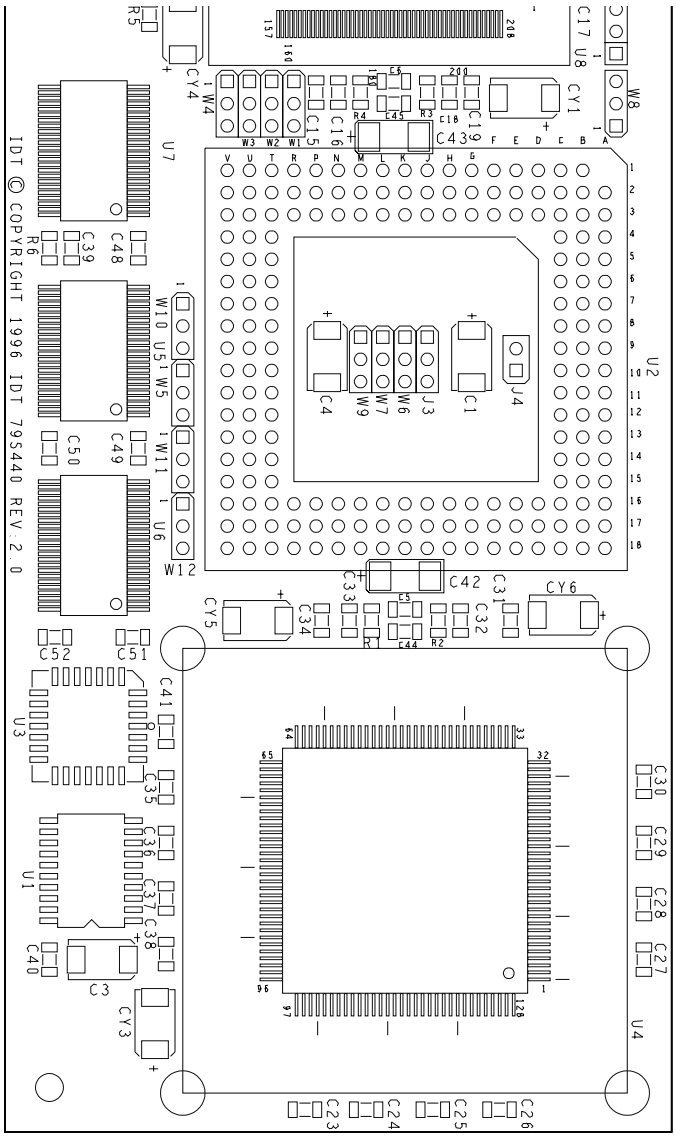

Figure 1.2 Physical Layout of 79S474

Notes

Specification Summary

Part Number

- *IDT79S474*

RISController

- *IDT79RC64474-250*
- *IDT79RC64475-250*

Physical Dimensions

- *Rectangular form factor: 6.5" x 3.0"*

Operating Temperature

- *0-50°C*

Relative Humidity

- *5% - 95%*

Power Supply

- *5.0V ± 5%, 10 Amps typical*

79S474 Installation_64-bit System Interface*

Note: When using the RC64475 in 64-bit mode, the 64-bit system interface must be used.

The S474 attachment board uses a 250 MHz RC64474/RC64475 CPU while the bus interface runs at 41.67 MHz. These settings are different from the default settings of the S465 evaluation board, which executes at 100/50 MHz.

The primary installation steps for the 64-bit system interface are as follows:

1. a. Plug the S474 attachment card into the PGA socket provided, replace the S465's crystal (U9) with a 41.67 MHz crystal, and change the default clock multiplier switch settings to x3 as follows:

Switch	Description
S2.3	Off
S1.2	On
S1.3	On

b. For the 64-bit system interface, memory size jumpers must be set to the 64-bit SRAM and DRAM size configurations that are listed in Table 1.1 and Table 1.2.

Notes

SRAM SIZE	
0 Mbytes	**4 Mbytes in 64 bit-mode**
S1.5 = OFF	S1.5 = OFF
S1.6 = OFF	S1.6 = OFF
S1.7 = OFF	S1.7 = ON
S1.8 = don't care	S1.8 = OFF
J1 = don't care	J1 = 2-3
J2 = don't care	J2 = 2-3
J3 = don't care	J3 = 2-3
J4 = don't care	J4 = 2-3
J5 = don't care	J5 = 2-3
J6 = don't care	J6 = 2-3

Table 1.1 SRAM Size Selections

DRAM SIZE	
0 Mbytes	**4 Mbytes in 64 bit-mode**
S1.5 = OFF	S1.5 = ON
S1.6 = OFF	S1.6 = ON
S1.7 = OFF	S1.7 = OFF
J9 = don't care	J9 = 1-2
J10 = don't care	J10 = 1-2
J11 = don't care	J11 = 1-2
J12 = don't care	J12 = 1-2
W1 = don't care	W1 = 1-2
W2 = don't care	W2 = 1-2
S1.8 = don't care	S1.8 = ON

Table 1.2 DRAM Size Selections

2. Power for the S474 is drawn from the S465 board through the connectors it is plugged into. For instructions on connecting the S465 board to a power source, see Chapter 2 of the *79S465 Evaluation Board Hardware User's Manual*.
3. The S474 board is shipped with the jumpers set—as shown in Table 1.6—to select the RC64475 CPU as the default configuration.

* The 79S465 board is initially configured for 64-bit system interface.

79S474 Installation_32-bit System Interface*

Note: When using the RC64474 or the RC64475 in 32-bit mode, the 79S465 board's 32-bit system interface must be used.

The S474 attachment board uses a 250 MHz RC64474/RC64475 CPU while the bus interface runs at 41.67 MHz. These settings are different from the default settings of the S465 evaluation board, which executes at 100/50 MHz.

Notes

The primary installation steps for 32-bit system interface are as follows:

1. a. Plug the S474 attachment card into the PGA socket provided, replace the S465's xtal (U9) with a 41.67 MHz crystal, and change the default clock multiplier switch settings to x3 as follows:

Switch	Description
S2.3	Off
S1.2	On
S1.3	On

b. For the 32-bit system interface option, modifications to the S465 evaluation board are required as follows:

- *Memory size jumpers must be changed according to the 32-bit SRAM and DRAM size configurations, as listed in Table 1.3 and Table 1.4.*

SRAM SIZE	
0 Mbytes	**2 Mbytes in 32 bit-mode**
S1.5 = OFF	S1.5 = OFF
S1.6 = OFF	S1.6 = OFF
S1.7 = OFF	S1.7 = ON
S1.8 = don't care	S1.8 = OFF
J1 = don't care	J1 = 2-3
J2 = don't care	J2 = 2-3
J3 = don't care	J3 = 1-2
J4 = don't care	J4 = 2-3
J5 = don't care	J5 = 2-3
J6 = don't care	J6 = 1-2

Table 1.3 SRAM Size Selections

Notes

DRAM SIZE	
0 Mbytes	**2 Mbytes in 32 bit-mode**
S1.5 = OFF	S1.5 = ON
S1.6 = OFF	S1.6 = ON
S1.7 = OFF	S1.7 = OFF
J9 = don't care	J9 = 2-3
J10 = don't care	J10- = 2-3
J11 = don't care	J11 = 2-3
J12 = don't care	J12 = 2-3
W1 = don't care	W1 = 2-3
W2 = don't care	W2 = 2-3
S1.8 = don't care	S1.8 = ON

Table 1.4 DRAM Size Selections

- *Switch S2.6 must be changed to the ON position as listed in Table 3.12.*
- *Existing controllers must be replaced with the 79S467 kit (EPLDs for 32-bit system support).*

1. Power to the S474 is drawn from the S465 board through the connectors it is plugged into. For instructions on connecting the S465 board to a power source, see Chapter 2 of the *79S465 Evaluation Board Hardware User's Manual*.
2. The S474 board is shipped with the jumpers set to select the RC64475 CPU as the default configuration. To select the RC64474 CPU, set the jumpers as shown in Table 1.6.

Jumper	RC64474
W5	2-3
W7	2-3
W8	1-2
W9	1-2
W10	2-3
W11	2-3
W12	2-3

Table 1.5 Switch Configurations for RC64474 CPU Selection

* The 79S465 board is initially configured for 64-bit system interface.

Getting Started Quickly

The 79S474 board is shipped ready to run with the RC64475 CPU selected. Prior to shipment, the jumpers are configured to the default settings listed in Table 1.6 and do not require further modification or setup.

Two basic requirements for the board to run are:

- *A power supply of +5V with at least 10 Amp of current*
- *A 79S465 evaluation board*

Table 1.6 lists the default jumper settings on the 79S474 attachment board.

Notes

Jumper or Switch	Default	Description
W1	2-3	5V supply
W2	2-3	5V supply
W3	2-3	5V supply
W4	2-3	5V supply
W7	1-2	RC64474 Off
W8	2-3	RC64475 On
W9	2-3	RC64475 On
W10	1-2	RC64475 On
W11	1-2	RC64475 On
W12	1-2	RC64474 Off
J3	2-3	Use buffered clock
W5	1-2	RC64474 Off

Table 1.6 79S474 Default Jumper Settings

Logic Analyzer Connections

A Corelis Logic Analyzer Pod, part #PI-RC64475-Q, can be mounted on the top of the RC64475 CPU, or part #PI-RC64474-Q can be mounted on top of the RC64474. Both parts can be used to connect to the HP Logic Analyzer, part #16500B.

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Theory of Operation and Design Notes

Notes

The following sections provide information on the functional operation of the 79S474 attachment board. For detailed schematics, refer to Chapter 3.

Jumper or Switch Settings

The 79S474 can be configured to work in different modes. As discussed in the following sections, changing CPUs, clocking schemes, SyncIn Paths, or CPU voltages can be accomplished through a combination of jumpers.

CPU Selections

The S474 can support different CPUs in different footprints, RC64475 or RC64474. The S474 is shipped with the RC64474 soldered on the board, the RC64475 is socketed to the board. Only one CPU can be activated at a time through different jumper selections, as listed in Table 2.1

Jumpers	RC64475 ON	Jumpers	RC64474 ON
W5	1-2	W5	2-3
W7	1-2	W7	2-3
W8	2-3	W8	1-2
W9	2-3	W9	1-2
W10	1-2	W10	2-3
W11	1-2	W11	2-3
W12	1-2	W12	2-3

Table 2.1 RC64475/RC64474 CPU Options

RC64474/RC64475 Master Clock Selection

The RC64474's master clock can be selected to be delayed by either 1 or 2 buffers, with respect to **TClock**. Enabling the desired buffer delay can be completed as shown in Table 2.2.

Jumper	Option	Description
W6	2-3	2 buffer delay
	1-2	3 buffer delay

Table 2.2 Master Clock/Buffer Delay Selections

Notes

RC64474/RC64475 Clock Selection

On the S474, it is possible to provide the input clock to the CPU through a copy of the **TClock** from the main board the S474 is plugged into, as shown in Table 2.3.

Jumper	Option	Description
J3	2-3	Use buffered clock for RC64474/RC64475 generated on S474
	1-2	Use copy of **TClock** from main board

Table 2.3 RC64474/RC64475 Clock Selections

Voltage Selection

The S474 board works only at 5V; however, voltage options on the board can be selected as shown in Table 2.4.

Jumper	Option	Description
W1	1-2	3.3V
	2-3	5V
W2	1-2	3.3V
	2-3	5V
W3	1-2	3.3V
	2-3	5V
W4	1-2	3.3V
	2-3	5V

Table 2.4 79S474 Voltage Selections

32-bit System Interface Selection

Both the RC64474 and the RC64475 can be configured to work in a 32-bit system bus interface. The RC64475 can also be configured to work in a 64-bit system interface. This configuration selection is made at reset time through the CPU mode bit. Because the S474 is designed to support either the 32- or 64-bit system bus interface, no special modifications are required.

However, because of its 64-bit bus interface default setting, modifications to the S465 evaluation board are necessary. To change the S465 eval board to a 32-bit system bus interface, a new set of EPLD controllers—part #79S467—must be installed. In addition, several of the S465's jumpers and switches must also be changed. For more information on changes to the jumpers and switches, refer to Chapter 3 of the *79S465 Evaluation Board Hardware User's Manual*.

Theory of Operation

The RC64474 and RC64475 are bus and upwardly software compatible to the 64-bit RISController CPU family. In the 64-bit bus mode, the RC64475 maintains the same bus protocol as the RC4700. In the 32-bit external bus, both the RC64474 and RC64475—when in 32-bit mode—maintain the RC4700's bus protocol, but it has been extended to accommodate the 32-bit bus width.

The external bus protocol refers to the handshaking between the CPU and the external logic as well as timing for the various bus transactions. System logic and ASICs designed to interface with the RC4700 must be modified to support the RC64474's or the RC64475's 32-bit bus interface. Similarly, the external clock structure of the RC64474 and the RC64475 is different from that of the RC4700, which provides greater flexibility to the system designer.

Notes

Clock Structure Differences

The RC4700, RC64474, and the RC64475 have different input and output clock structures but maintain the same bus protocol.

RC4700 Clocks

The RC4700 implements the same clock structure as the first generation 64-bit devices, such as the RC4000 and the RC4400. The RC4700 uses a single input clock—**MasterClock**—that is doubled internally by one PLL to generate the pipeline clock (PClk). A second PLL doubles **MasterClock** and then divides it by a constant number—from 2 to 8 as programmed during reset—to generate the output clocks—**RClock**, **TClock**, **MasterOut,** and **SyncOut**. These output clocks are used by the system logic to interface with the RC4700 during read and write operations.

Figure 2.1 illustrates the architecture of the RC4700's internal clock distribution tree. A more detailed explanation of these clocks is presented in the *IDT79RC4600 & IDT79RC4700 Processor Hardware User's Manual*.

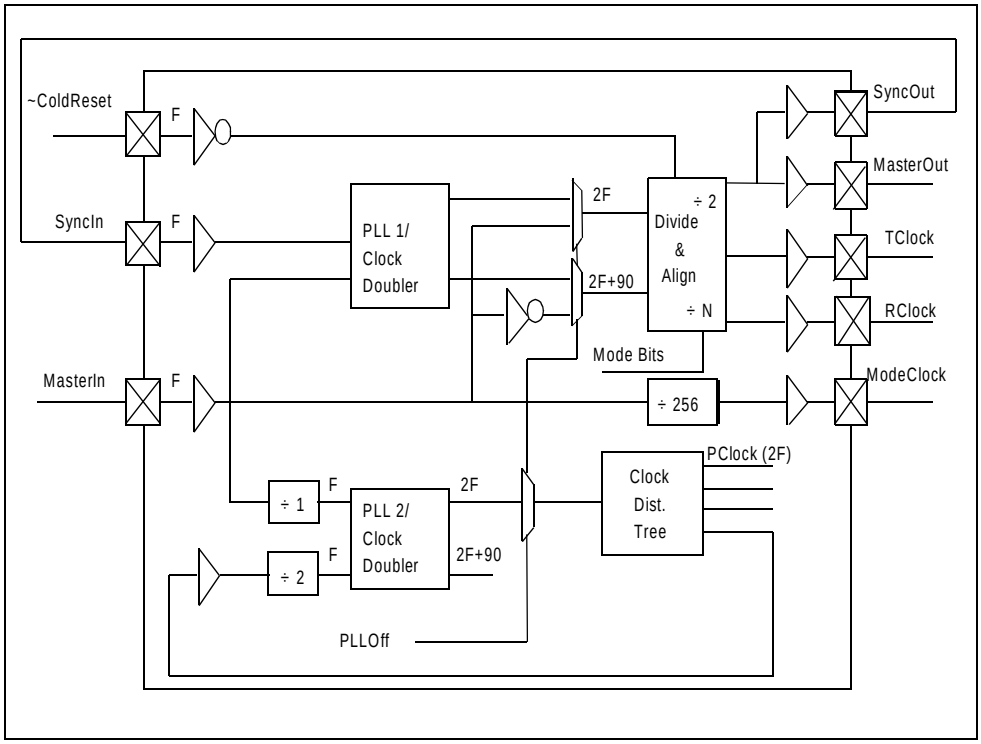


Figure 2.1 RC4700 Internal Clock Circuitry

RC64474 and RC64475 Clocks

The architecture for the internal clock distribution tree of the RC64474 and the RC64475 is different from that of the RC4700. Both the RC64474 and RC64475 use only a single input clock—**MasterClock**. **MasterClock** is multiplied internally using a single PLL by a constant number—from 2 to 8 as programmed during reset—to generate the pipeline clock (PClk). The RC64474 and the RC64475 do not generate an output clock. The **MasterClock** should be used as the system control logic clock. Both the RC64474 and RC64475 guarantee that the interface signals with the external system logic will be sampled using the rising edge of **MasterClock**.

An advantage of the RC64474 and the RC64475 is that the **MasterClock** frequency may be kept small. Similarly, the absence of output clocks from the RC64474 and RC64475 reduces the device's power consumption. This architecture allows several systems to synchronize using a single input clock at any frequency without being locked by the clocks provided by the CPU. This is an advantage for backplane applications where the input clock is provided from the backplane to several plugged-in cards.

Notes

Figure 2.2 illustrates the internal clock circuitry of the RC64474 and RC64475.

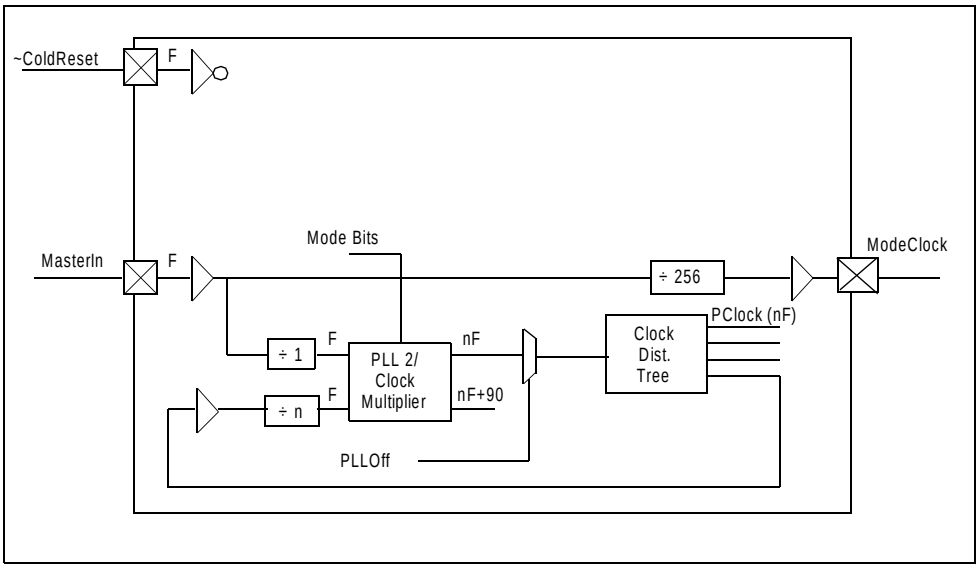


Figure 2.2 RC64474/RC64475 Internal Clock Circuitry

Generating RC4700-Compatible Clocks

Systems using the RC64475 in 64-bit system interface can use logic and ASIC previously developed to work with RC4700, without modifications.

With modifications, to support the 32-bit bus width interface of the RC64474 and the RC64475, systems using the RC64474 or RC64475 can also use the logic and ASIC previously developed to work with the RC4700. This mechanism requires the generation of **MasterOut**, **SyncOut**, **RClock,** and **TClock**, or alternatively, a subset of these according to the system requirements. More detail on these clocks is provided in the *IDT79RC4600 & IDT79RC4700 Processor Hardware User's Manual*.

The clock distribution tree must be implemented at the input of the RC64474 and RC64475. The RC4700's external clock generation is illustrated in Figure 2.3. In this case, a buffer is used to delay the input clock to RC64474 or RC64475. The output of the buffer is equivalent to **TClock**, **MasterOut,** and **SyncOut**. The input of the buffer is equivalent to **RClock**. For a tight delay between **RClock** and **TClock**, it is better to use a buffer that has a very narrow window for the minimum and the maximum input to output delays.

An example of this clock buffer type is the Motorola MC10H645 buffer, which guarantees a single nanosecond difference between the minimum and the maximum delays. In systems that use only the RC64474 or only the RC64475, the **SyncOut** to **SyncIn** path is irrelevant, since neither the RC64474 the RC64475 nor the system logic use these clocks. However, depending on the architecture of the system, the **MasterOut** could be relevant.

Notes

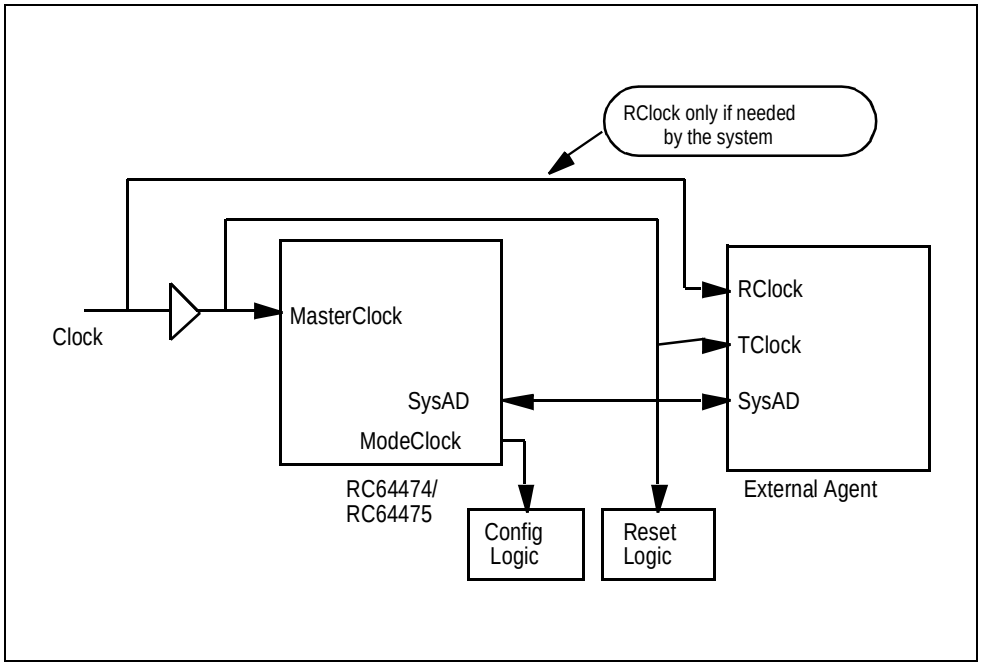


Figure 2.3 RC64474/RC64475 External Clock Generation Circuitry

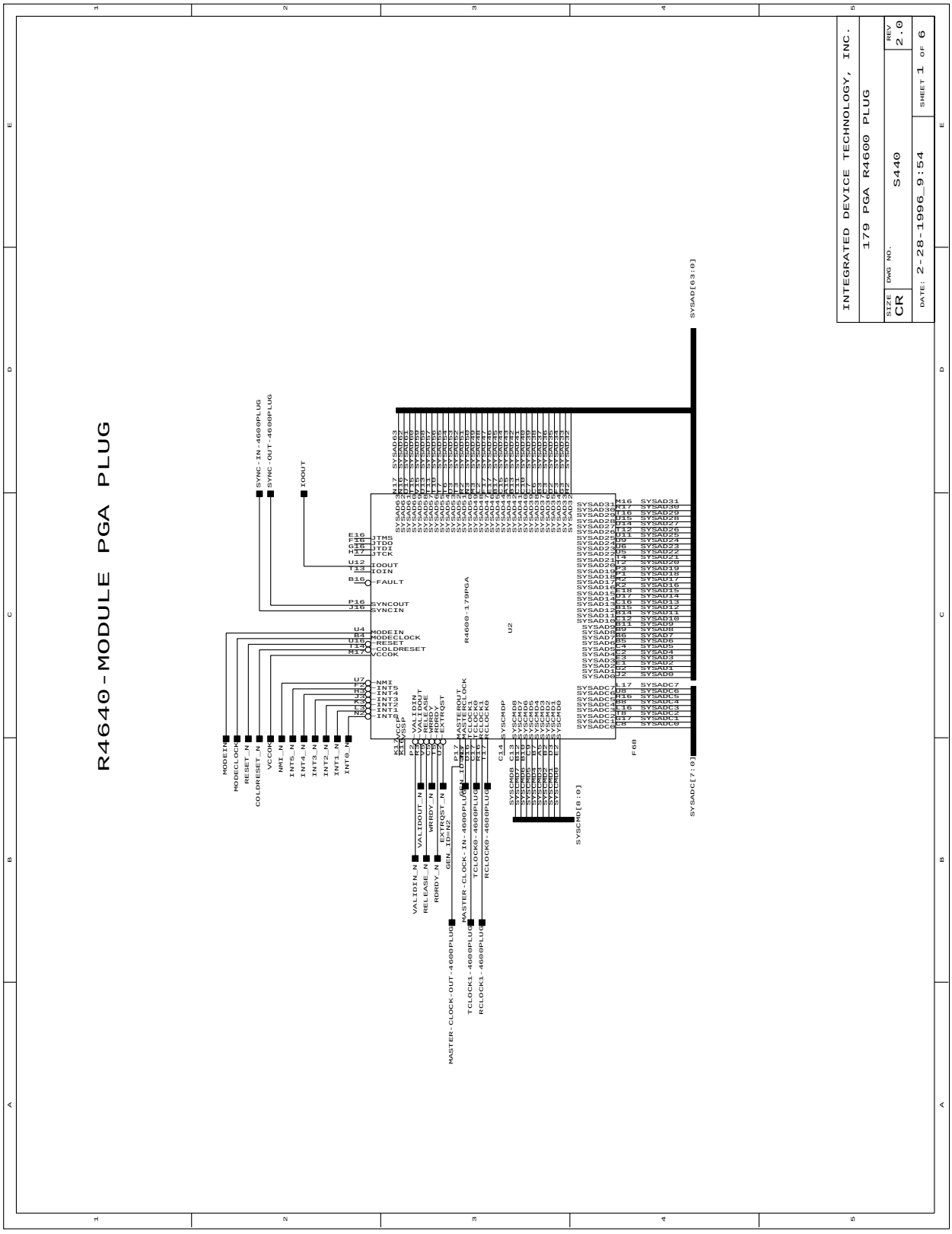
Notes

Schematics

Notes

Schematics

This chapter contains six schematic drawings for the 79S474 board.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DWG NO. S440
REV 2.0
DATE: 2-28-1996_9:54
SHEET 1 OF 6
R4600-179PGA
U2
SYSAD[63:0]
SYSADC[7:0]
SYSCMD[8:0]
MODEIN
MODECLOCK
RESET_N
COLDRESET_N
VCCOK
NMI_N
INT5_N
INT4_N
INT3_N
INT2_N
INT1_N
INT0_N
SYNC-IN-4600PLUG
SYNC-OUT-4600PLUG
IOOUT
JTMS
JTDO
JTDI
JTCK
IOOUT
IOIN
FAULT
SYNCOUT
SYNCIN
MODEIN
MODECLOCK
RESET
COLDRESET
VCCOK
NMI
INT5
INT4
INT3
INT2
INT1
INT0
VALIDIN
VALIDOUT
RELEASE
WRRDY
EXTRQST
MASTEROUT
MASTERCLOCK
TCLOCK0
TCLOCK1
RCLOCK0
RCLOCK1
SYSCMDP
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VALIDOUT_N
RELEASE_N
WRRDY_N
EXTRQST_N
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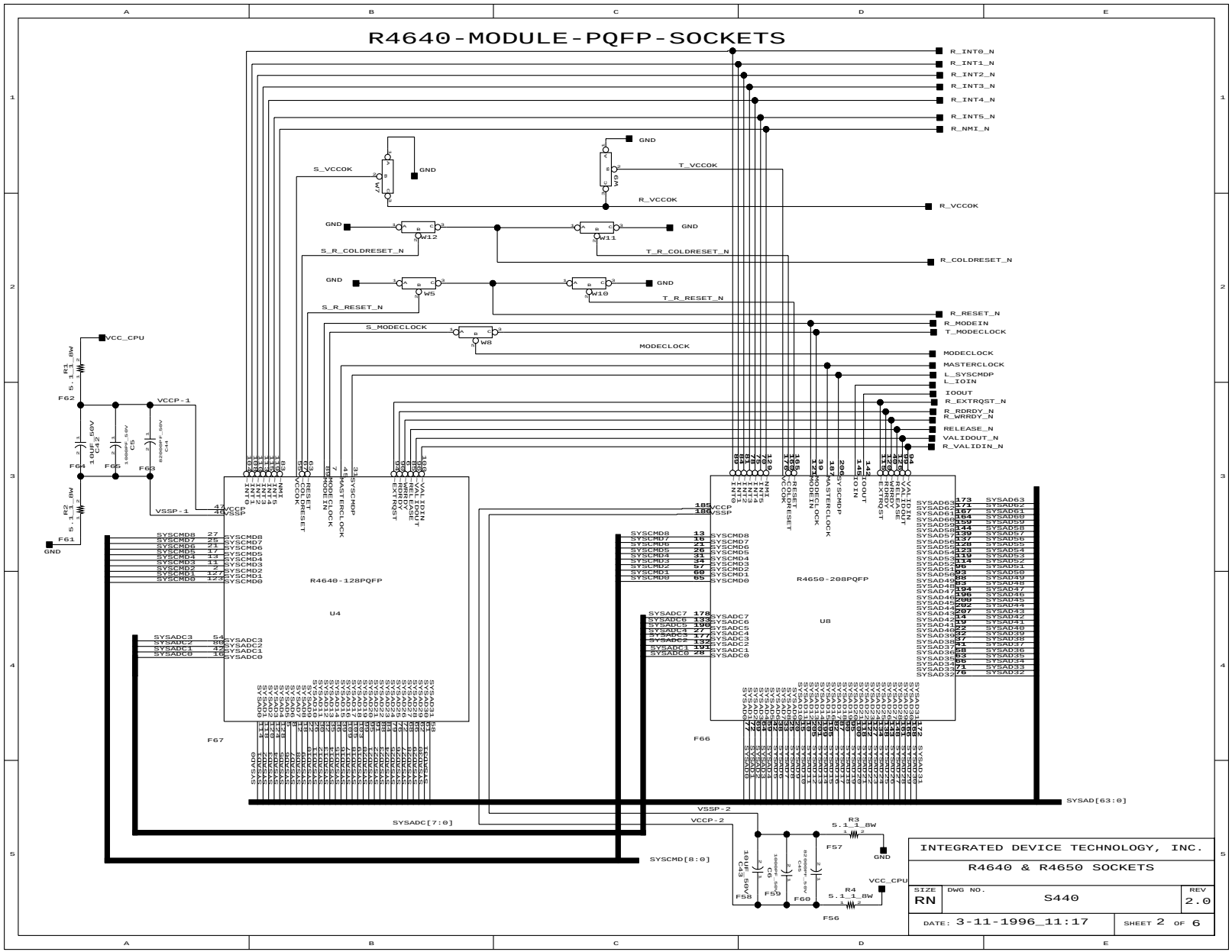
MASTER-CLOCK-IN-4600PLUG
TCLOCK0-4600PLUG
RCLOCK0-4600PLUG
TCLOCK1-4600PLUG
RCLOCK1-4600PLUG
MASTER-CLOCK-OUT-4600PLUG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R_INT1_N
R_INT2_N
R_INT3_N
R_INT4_N
R_INT5_N
R_NMI_N
R_VCCOK
R_COLDRESET_N
R_RESET_N
R_MODEIN
T_MODECLOCK
MODECLOCK
MASTERCLOCK
L_SYSCMDP
L_IOIN
IOOUT
R_EXTRQST_N
R_RDRDY_N
R_WRRDY_N
RELEASE_N
VALIDOUT_N
R_VALIDIN_N
S_VCCOK
T_VCCOK
S_R_COLDRESET_N
T_R_COLDRESET_N
S_R_RESET_N
T_R_RESET_N
S_MODECLOCK
MODECLOCK
VCC_CPU
VCCP-1
VSSP-1
R4640-128PQFP
U4
R4650-208PQFP
U8
F67
F66
SYSADC[7:0]
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VSSP-2
VCCP-2
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SIZE RN
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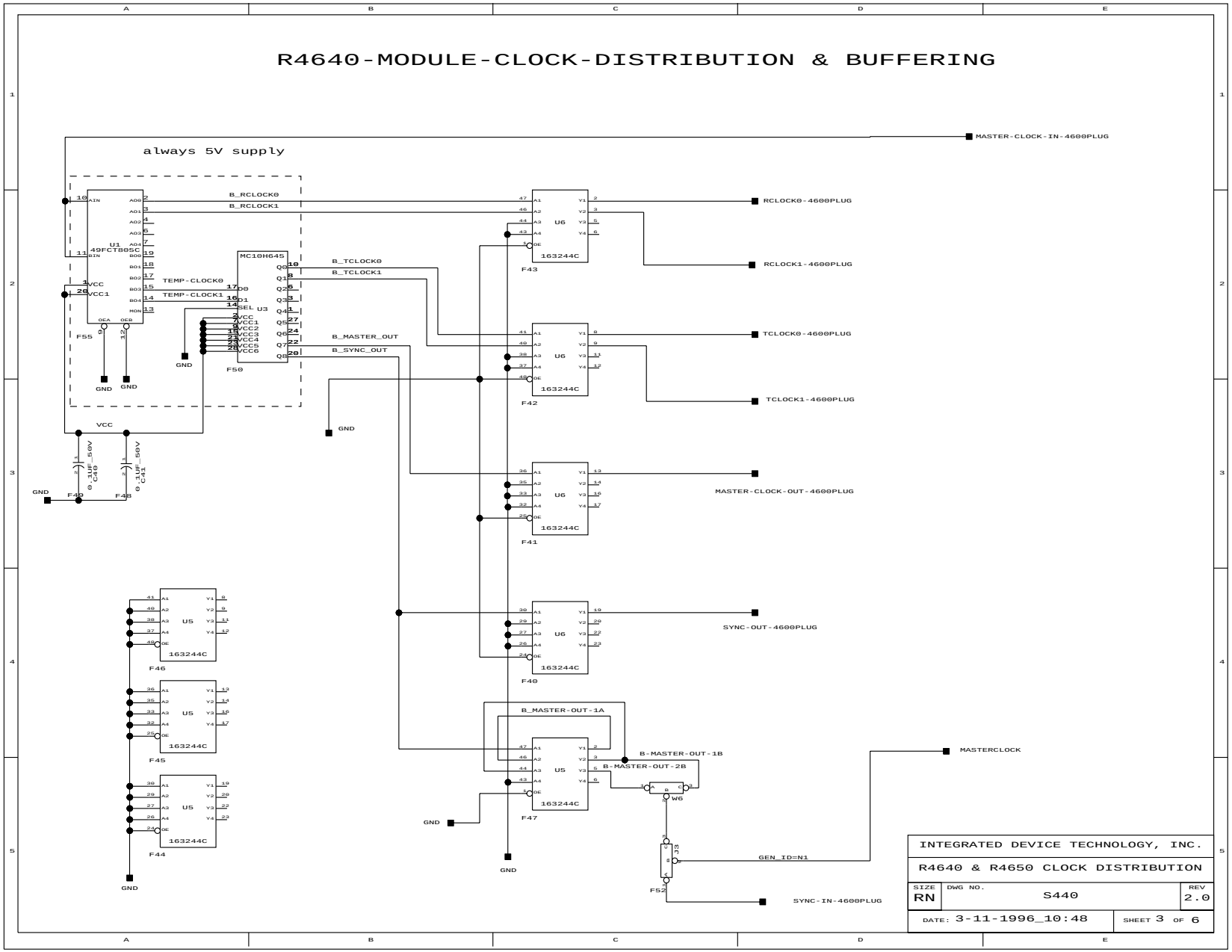
DATE: 3-11-1996_11:17
SHEET 2 OF 6

Schematics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always 5V supply
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B_RCLOCK0
B_RCLOCK1
RCLOCK0-4600PLUG
RCLOCK1-4600PLUG
TEMP-CLOCK0
TEMP-CLOCK1
B_TCLOCK0
B_TCLOCK1
TCLOCK0-4600PLUG
TCLOCK1-4600PLUG
B_MASTER_OUT
B_SYNC_OUT
MASTER-CLOCK-OUT-4600PLUG
SYNC-OUT-4600PLUG
B_MASTER-OUT-1A
B-MASTER-OUT-1B
B-MASTER-OUT-2B
MASTERCLOCK
GEN_ID=N1
SYNC-IN-4600PLUG
U1 49FCT805C
MC10H645
U3
U5
U6
163244C
F55
F50
F43
F42
F41
F40
F47
F46
F45
F44
F52
W6
C40 0.1UF_50V
C41 0.1UF_50V
VCC
GND
INTEGRATED DEVICE TECHNOLOGY, INC.
R4640 & R4650 CLOCK DISTRIBUTION
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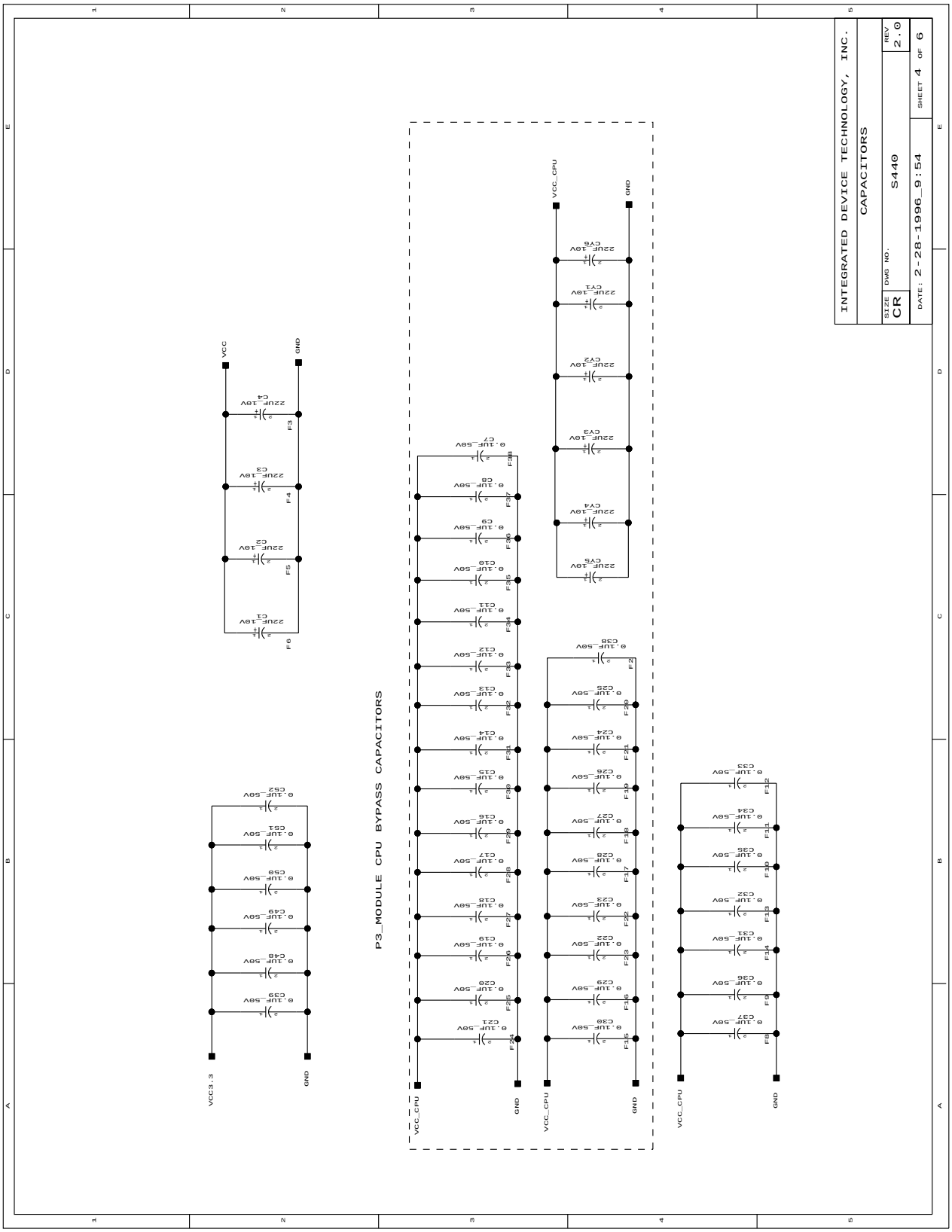
SHEET 3 OF 6

Schematics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CAPACITORS
SIZE CR
DWG NO. S440
REV 2.0
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SHEET 4 OF 6
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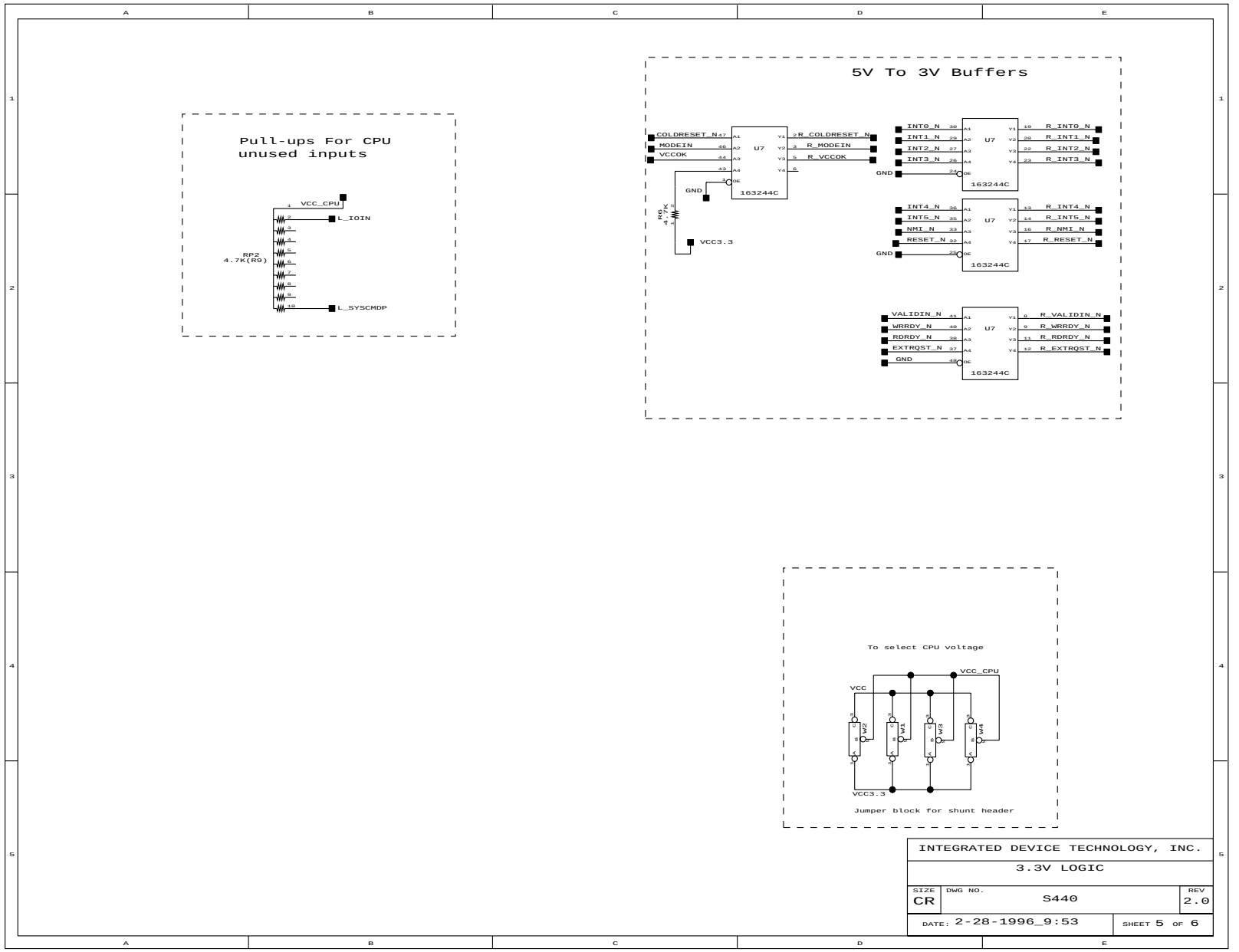
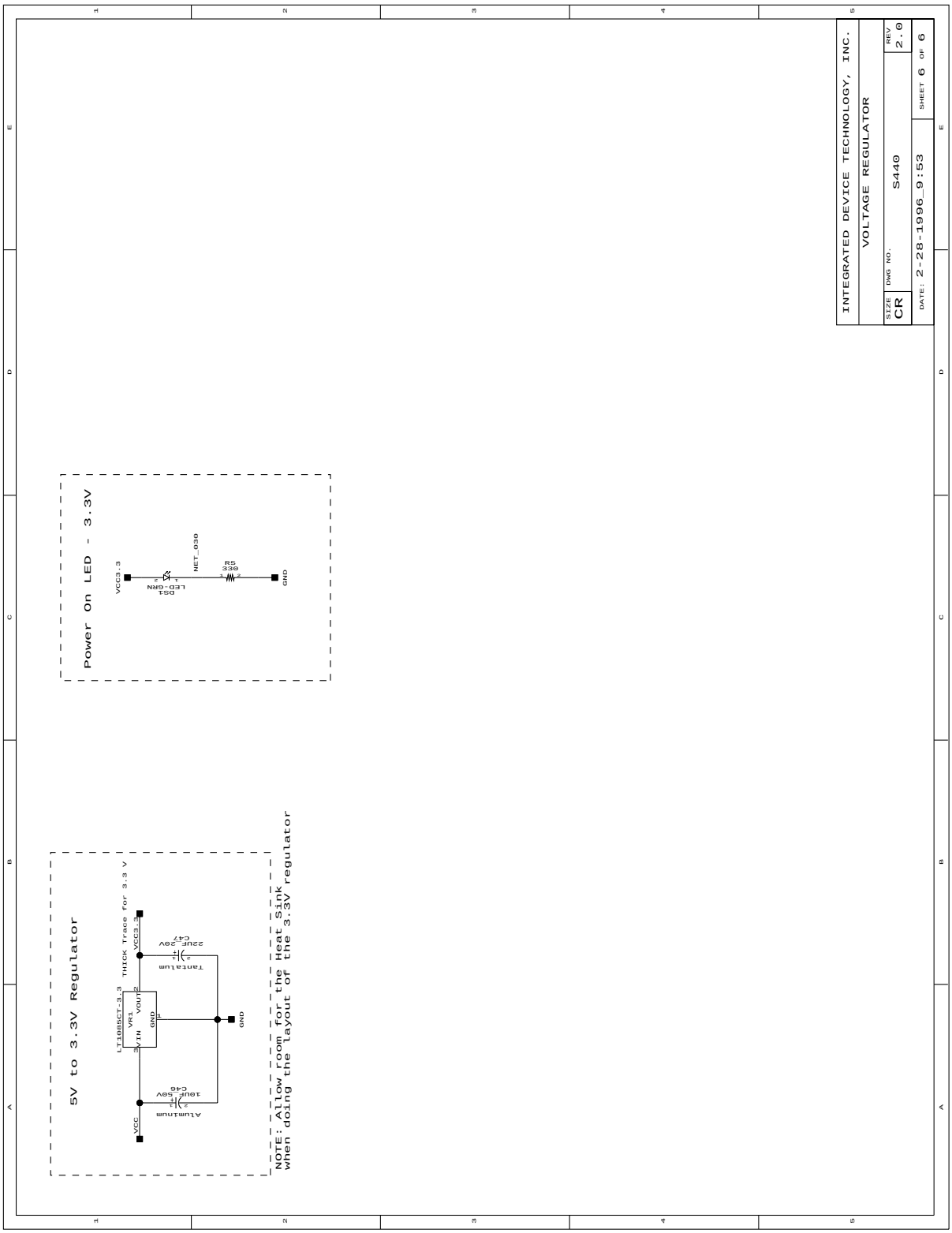
VCC
GND
VCC3.3
VCC_CPU
22UF_10V
0.1UF_50V


Pull-ups For CPU
unused inputs
VCC_CPU
L_IOIN
RP2
4.7K(R9)
L_SYSCMDP
5V To 3V Buffers
COLDRESET_N
MODEIN
VCCOK
GND
R9
4.7K
VCC3.3
U7
163244C
R_COLDRESET_N
R_MODEIN
R_VCCOK
INT0_N
INT1_N
INT2_N
INT3_N
R_INT0_N
R_INT1_N
R_INT2_N
R_INT3_N
INT4_N
INT5_N
NMI_N
RESET_N
R_INT4_N
R_INT5_N
R_NMI_N
R_RESET_N
VALIDIN_N
WRRDY_N
RDRDY_N
EXTRQST_N
R_VALIDIN_N
R_WRRDY_N
R_RDRDY_N
R_EXTRQST_N
To select CPU voltage
VCC
VCC_CPU
W2
W1
W3
W4
VCC3.3
Jumper block for shunt header
INTEGRATED DEVICE TECHNOLOGY, INC.
3.3V LOGIC
SIZE
CR
DWG NO.
S440
REV
2.0
DATE: 2-28-1996_9:53
SHEET 5 OF 6

Schematics


INTEGRATED DEVICE TECHNOLOGY, INC.
VOLTAGE REGULATOR
SIZE CR
DWG NO. S440
REV 2.0
DATE: 2-28-1996 9:53
SHEET 6 OF 6
Power On LED - 3.3V
VCC3.3
LED-GRN
D51
NET_030
RS
330
GND
5V to 3.3V Regulator
THICK Trace for 3.3 V
LT1085CT-3.3
VR1
VIN
VOUT
GND
VCC
VCC3.3
Aluminum
10uF 50V
C46
Tantalum
22uF 20V
C47
NOTE: Allow room for the Heat Sink
when doing the layout of the 3.3V regulator