

High-Speed CMOS Logic Presettable Synchronous 4-Bit Up/Down Counters

Features

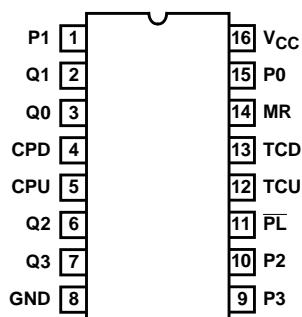
- **Synchronous Counting and Asynchronous Loading**
- **Two Outputs for N-Bit Cascading**
- **Look-Ahead Carry for High-Speed Counting**
- **Fanout (Over Temperature Range)**
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- **Wide Operating Temperature Range ... -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- **HCT Types**
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The 'HC192, 'HC193 and 'HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Pinout

**CD54HC192, CD54HC193, CD54HCT193 (CERDIP)
CD74HC192 (PDIP, SOP, TSSOP)
CD74HC193 (PDIP, SOIC)
CD74HCT193 (PDIP)**
TOP VIEW



Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (PL). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

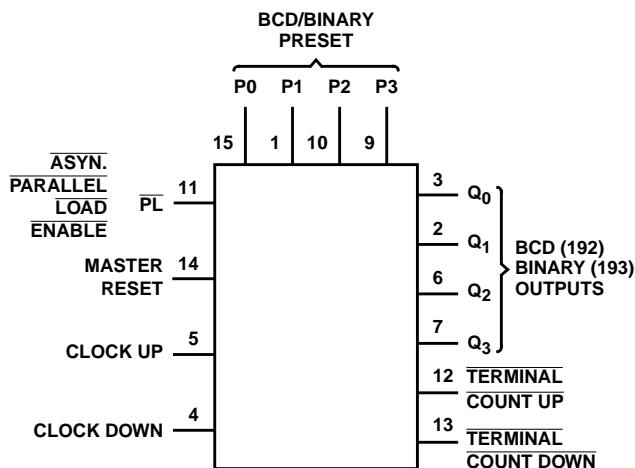
If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC192F3A	-55 to 125	16 Ld CERDIP
CD54HC193F3A	-55 to 125	16 Ld CERDIP
CD54HCT193F3A	-55 to 125	16 Ld CERDIP
CD74HC192E	-55 to 125	16 Ld PDIP
CD74HC192NSR	-55 to 125	16 Ld SOP
CD74HC192PW	-55 to 125	16 Ld TSSOP
CD74HC192PWR	-55 to 125	16 Ld TSSOP
CD74HC192PWT	-55 to 125	16 Ld TSSOP
CD74HC193E	-55 to 125	16 Ld PDIP
CD74HC193M	-55 to 125	16 Ld SOIC
CD74HC193MT	-55 to 125	16 Ld SOIC
CD74HC193M96	-55 to 125	16 Ld SOIC
CD74HCT193E	-55 to 125	16 Ld PDIP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Absolute Maximum Ratings

DC Supply Voltage, V _{CC}	-0.5V to 7V
DC Input Diode Current, I _{IK}		
For V _I < -0.5V or V _I > V _{CC} + 0.5V	±20mA
DC Output Diode Current, I _{OK}		
For V _O < -0.5V or V _O > V _{CC} + 0.5V	±20mA
DC Output Source or Sink Current per Output Pin, I _O		
For V _O > -0.5V or V _O < V _{CC} + 0.5V	±25mA
DC V _{CC} or Ground Current, I _{CC} or I _{GND}	±50mA

Thermal Information

Package Thermal Impedance, θ _{JA} (see Note 1):	
E (PDIP) Package
M (SOIC) Package
NS (SOP) Package
PW (TSSOP) Package
Maximum Junction Temperature 150°C
Maximum Storage Temperature Range -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) 300°C
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range (T _A)	-55°C to 125°C
Supply Voltage Range, V _{CC}		
HC Types2V to 6V
HCT Types45V to 5.5V
DC Input or Output Voltage, V _I , V _O	0V to V _{CC}
Input Rise and Fall Time		
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS		
		V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX			
HC TYPES														
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
High Level Output Voltage TTL Loads			-0.02	6	5.9	-	-	5.9	-	5.9	-	V		
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V		
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V		
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V		
			5.2	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA		
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	µA		

CD54/74HC192, CD54/74HC193, CD54/74HCT193

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)	V _{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	-	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
P0-P3	0.4
MR	1.45
PL	0.85
CPU, CPD	1.45

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Pulse Width CPU, CPD 192	t _W	2	115	-	-	145	-	175	-	ns
		4.5	23	-	-	29	-	35	-	ns
		6	20	-	-	25	-	30	-	ns
CPU, CPD 193	t _W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
PL	t _W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR	t _W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
Set-up Time Pn to PL	t _{SU}	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Hold Time Pn to PL	t _H	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Hold Time CPD to CPU or CPU to CPD	t _H	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Recovery Time PL to CPU, CPD	t _{REC}	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR to CPU, CPD	t _{REC}	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
Maximum Frequency CPU, CPD 192	f _{MAX}	2	5	-	-	4	-	3	-	MHz
		4.5	22	-	-	18	-	15	-	MHz
		6	24	-	-	21	-	18	-	MHz
CPU, CPD 193	f _{MAX}	2	5	-	-	4	-	3	-	MHz
		4.5	25	-	-	20	-	17	-	MHz
		6	29	-	-	24	-	20	-	MHz
HCT TYPES										
Pulse Width CPU, CPD 192	t _W	2	-	-	-	-	-	-	-	ns
		4.5	23	-	-	29	-	35	-	ns
		6	-	-	-	-	-	-	-	ns
CPU, CPD 193	t _W	2	-	-	-	-	-	-	-	ns
		4.5	23	-	-	29	-	35	-	ns
		6	-	-	-	-	-	-	-	ns

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
\bar{P}_L	t _W	2	-	-	-	-	-	-	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	-	-	-	-	-	-	-	ns
MR	t _W	2	-	-	-	-	-	-	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	-	-	-	-	-	-	-	ns
Set-up Time Pn to \bar{P}_L	t _{SU}	2	-	-	-	-	-	-	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	-	-	-	-	-	-	-	ns
Hold Time Pn to \bar{P}_L	t _H	2	-	-	-	-	-	-	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	-	-	-	-	-	-	-	ns
Hold Time CPD to CPU or CPU to CPD	t _H	2	-	-	-	-	-	-	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	-	-	-	-	-	-	-	ns
Recovery Time \bar{P}_L to CPU, CPD	t _{REC}	2	-	-	-	-	-	-	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	-	-	-	-	-	-	-	ns
MR to CPU, CPD	t _{REC}	2	-	-	-	-	-	-	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	-	-	-	-	-	-	-	ns
Maximum Frequency CPU, CPD 192	f _{MAX}	2	-	-	-	-	-	-	-	MHz
		4.5	22	-	-	18	-	15	-	MHz
		6	-	-	-	-	-	-	-	MHz
CPU, CPD 193	f _{MAX}	2	-	-	-	-	-	-	-	MHz
		4.5	22	-	-	18	-	15	-	MHz
		6	-	-	-	-	-	-	-	MHz

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CPU to \bar{T}_{CU}	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	125	-	155	-	190	ns
		C _L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C _L = 15pF	5	-	10	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	21	-	26	-	32	ns
CPD to \bar{T}_{CD}	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	125	-	155	-	190	ns
		C _L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C _L = 15pF	5	-	10	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	21	-	26	-	32	ns
CPU to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	220	-	270	-	325	ns
		C _L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	37	-	46	-	55	ns

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CPD to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	220	-	270	-	325	ns
		C _L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	37	-	46	-	55	ns
PL to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	220	-	275	-	330	ns
		C _L = 50pF	4.5	-	-	44	-	55	-	66	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	37	-	47	-	56	ns
MR to Q _n	t _{PHL}	C _L = 50pF	2	-	-	200	-	250	-	300	ns
		C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	34	-	43	-	51	ns
Transition Time Q, TCU, TCD	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
		C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C _L = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay CPU to \overline{TCU}	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C _L = 15pF	5	-	11	-	-	-	-	-	ns
CPU to \overline{TCD}	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C _L = 15pF	5	-	11	-	-	-	-	-	ns
CPU to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
CPD to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
PL to Q _n	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
MR to Q _n	t _{PHL}	C _L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C _L = 15pF	5	-	18	-	-	-	-	-	ns
Transition Time Q, TCU, TCD	t _{TLH} , t _{THL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C _L = 50pF	-	-	-	10	-	10	-	10	pF
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C _{PD}	C _L = 15pF	5	-	50	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per gate.

4. $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

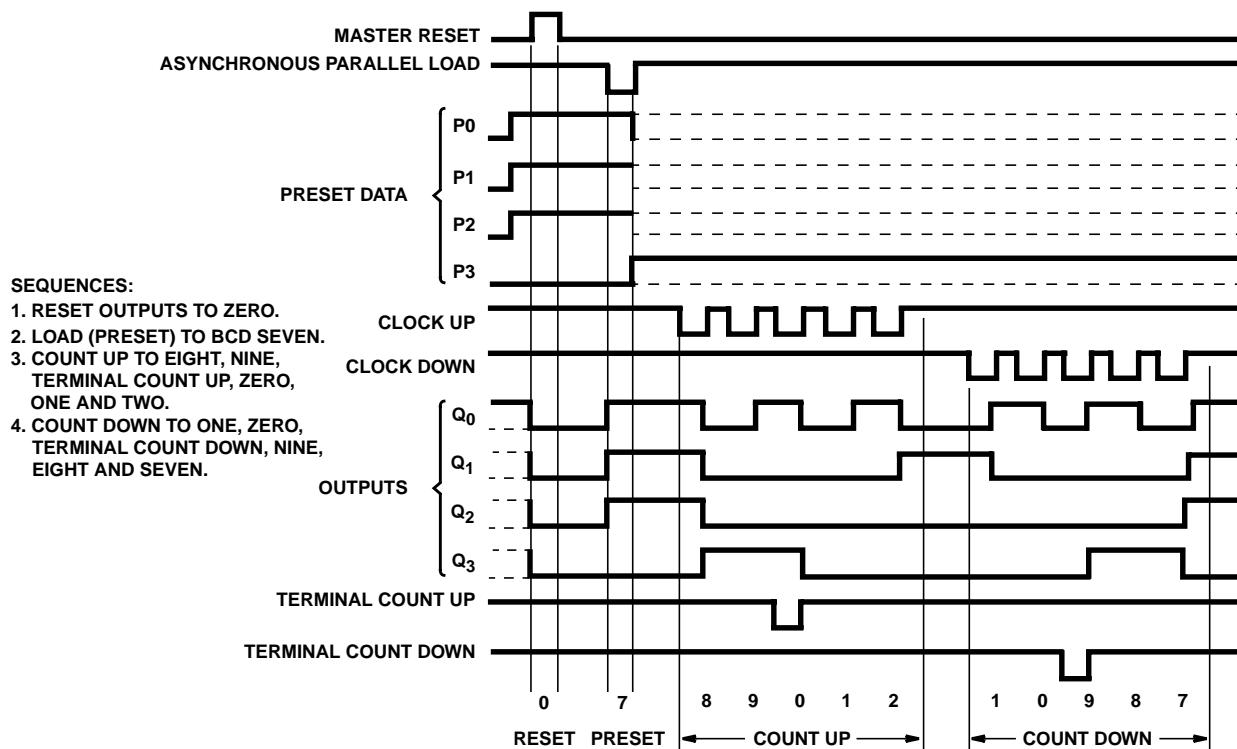


FIGURE 1. 'HC192 SYNCHRONOUS DECADE COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

Test Circuits and Waveforms (Continued)

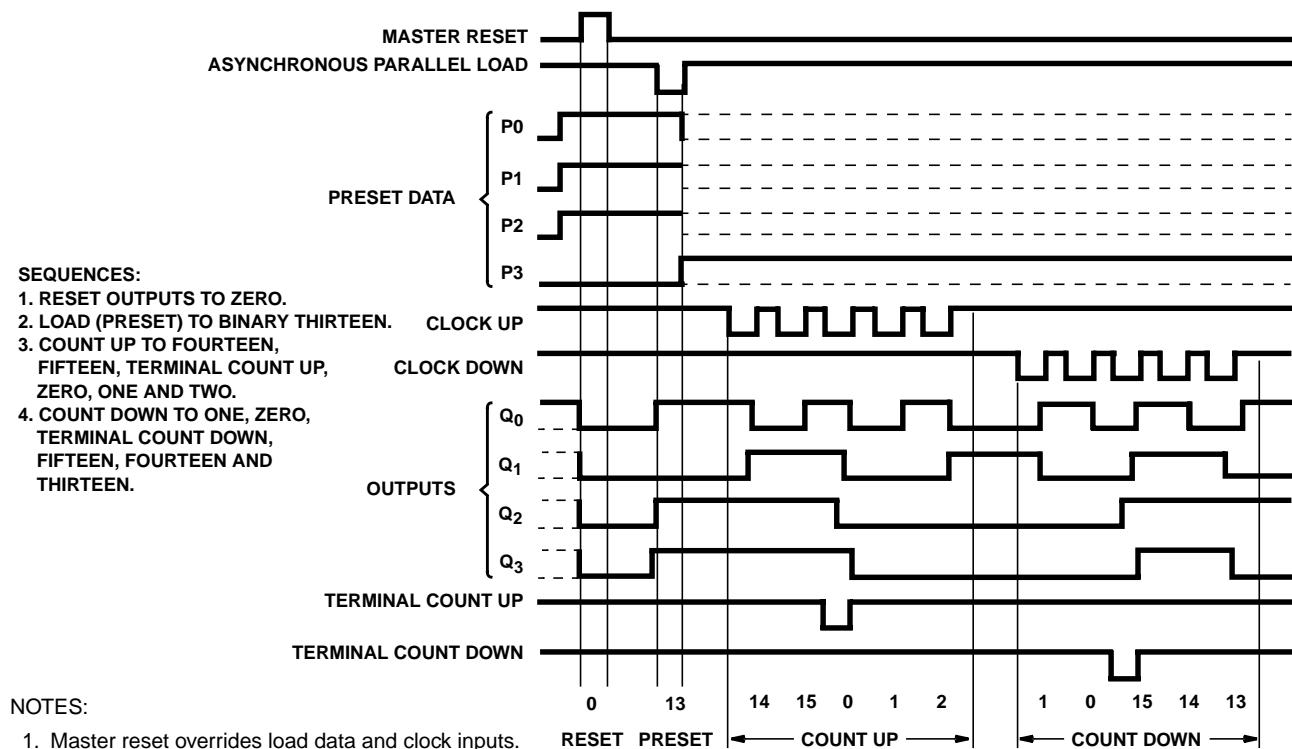


FIGURE 2. 'HC193 SYNCHRONOUS BINARY COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

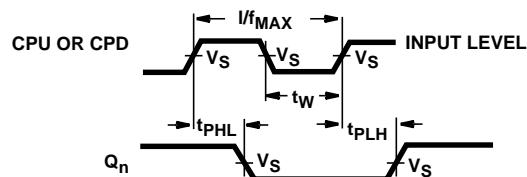


FIGURE 3. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

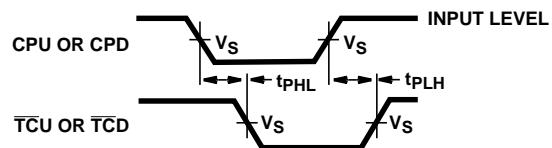


FIGURE 4. CLOCK TO TERMINAL COUNT DELAYS

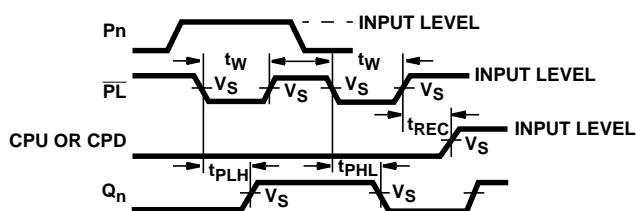


FIGURE 5. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME

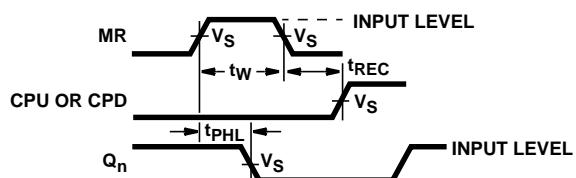


FIGURE 6. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

Test Circuits and Waveforms (Continued)

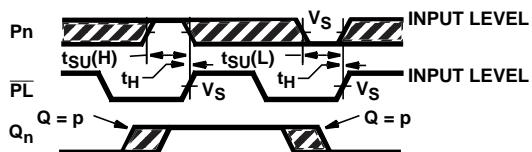


FIGURE 7. SET-UP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)

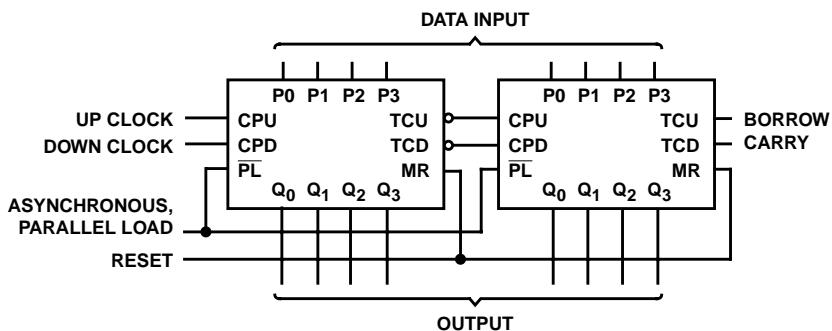
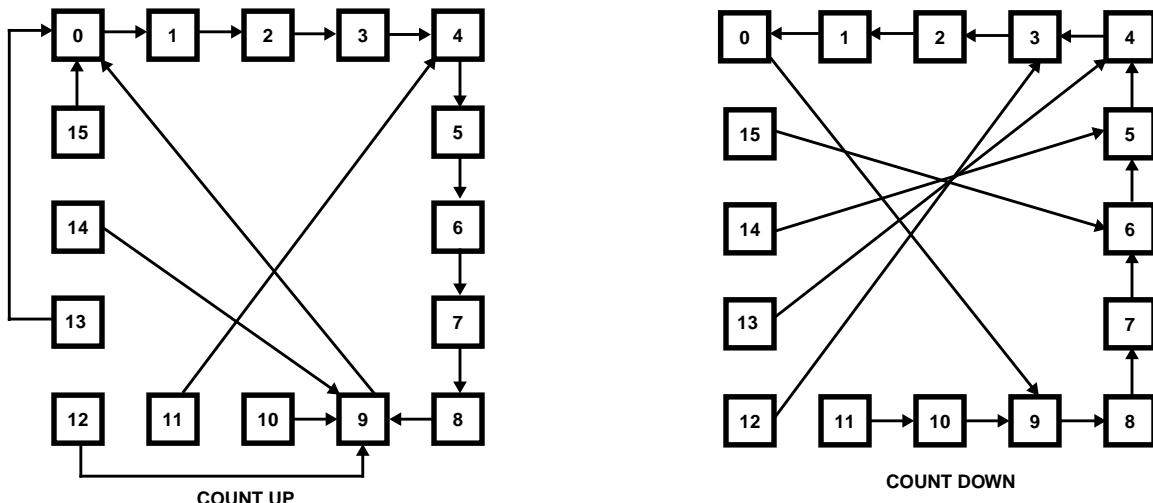


FIGURE 8. CASCDED UP/DOWN COUNTER WITH PARALLEL LOAD



NOTE: Illegal states in BCD counters corrected in one count.

NOTE: Illegal states in BCD counters corrected in one or two counts.

FIGURE 9. 'HC192, 'HCT193 STATE DIAGRAMS

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8780801EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9084801MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
9084801MEAS2035	OBsolete	CDIP	J	16		TBD	Call TI	Call TI
CD54HC192F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC193F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HCT193F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD74HC192E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC192EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC192NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC192PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC193E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC193EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC193M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC193M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC193M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC193ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC193MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC193MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT193E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT193EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

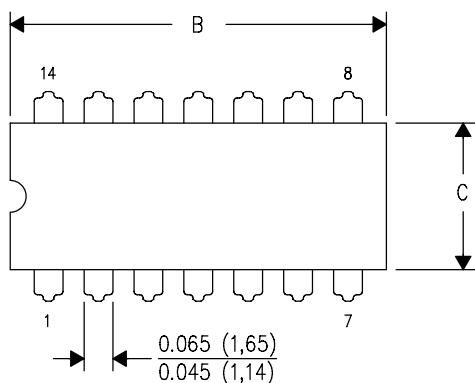
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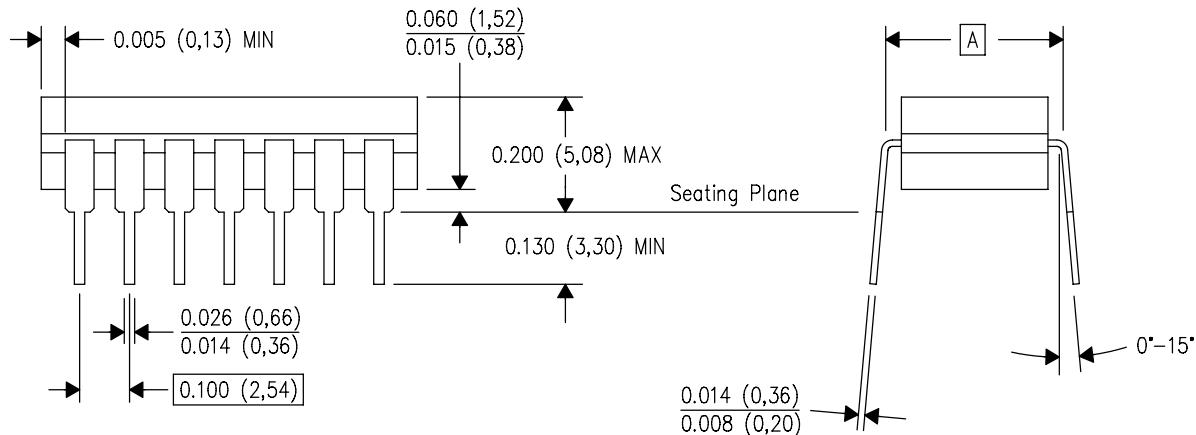
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



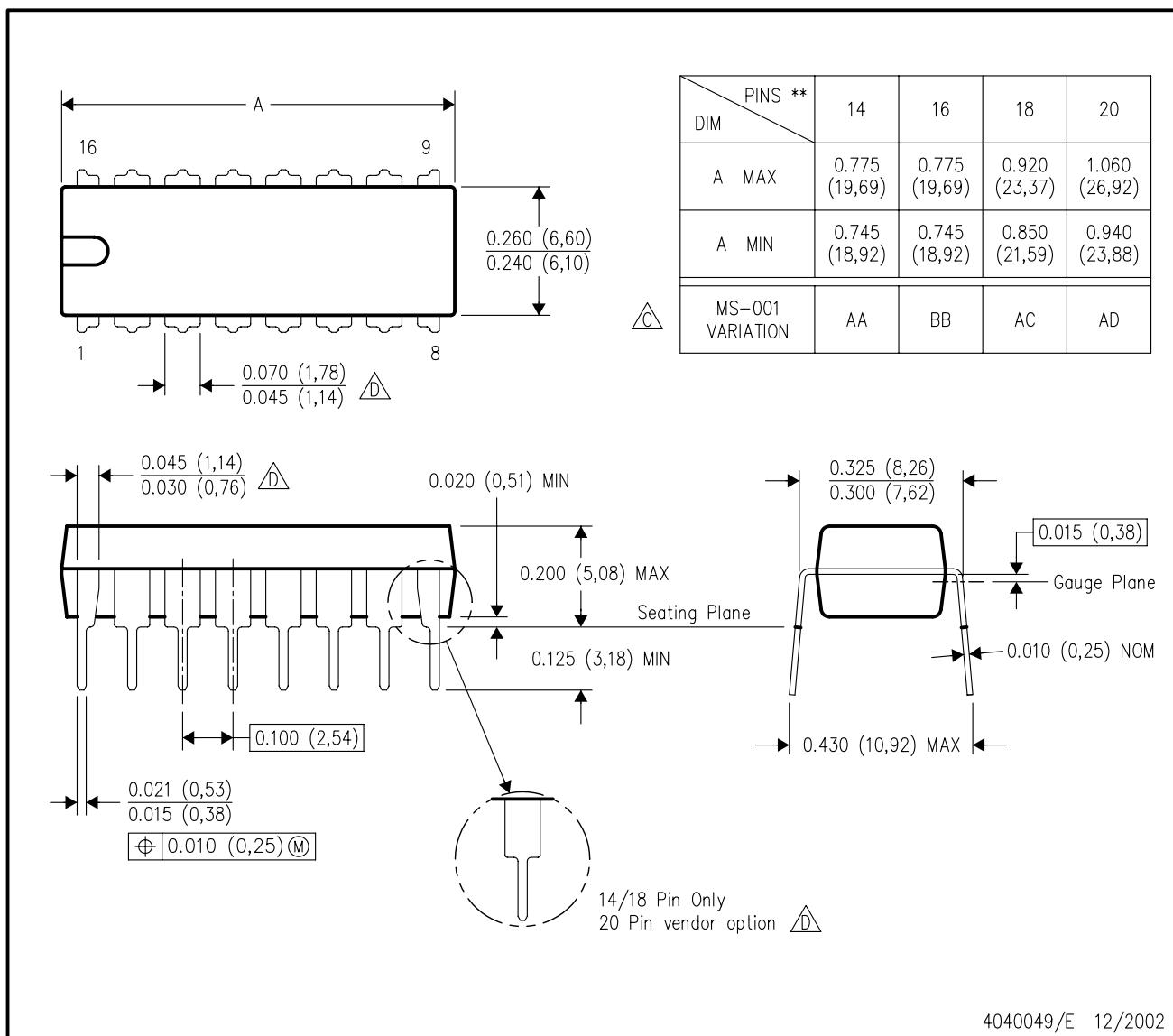
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



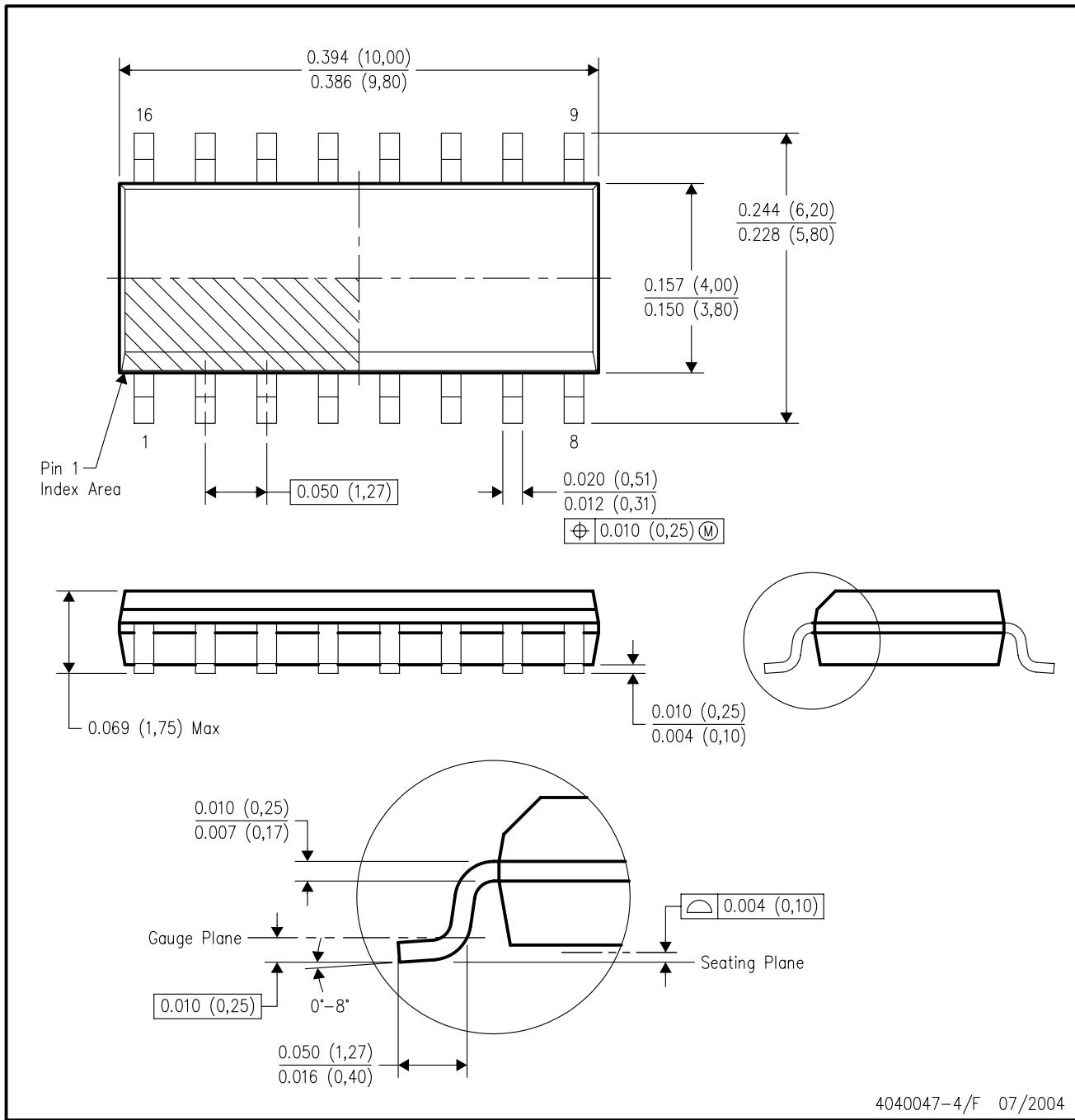
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

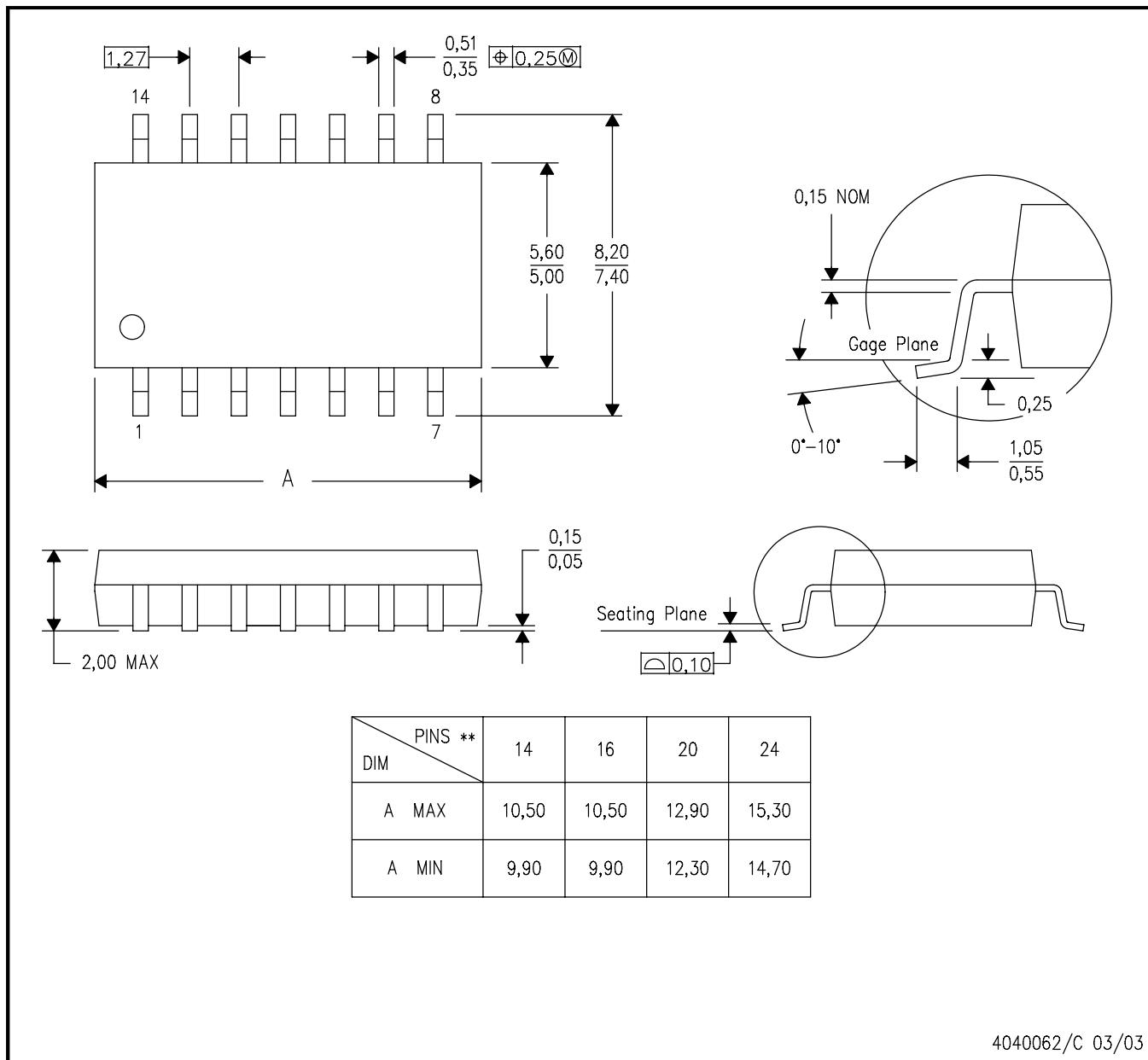
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

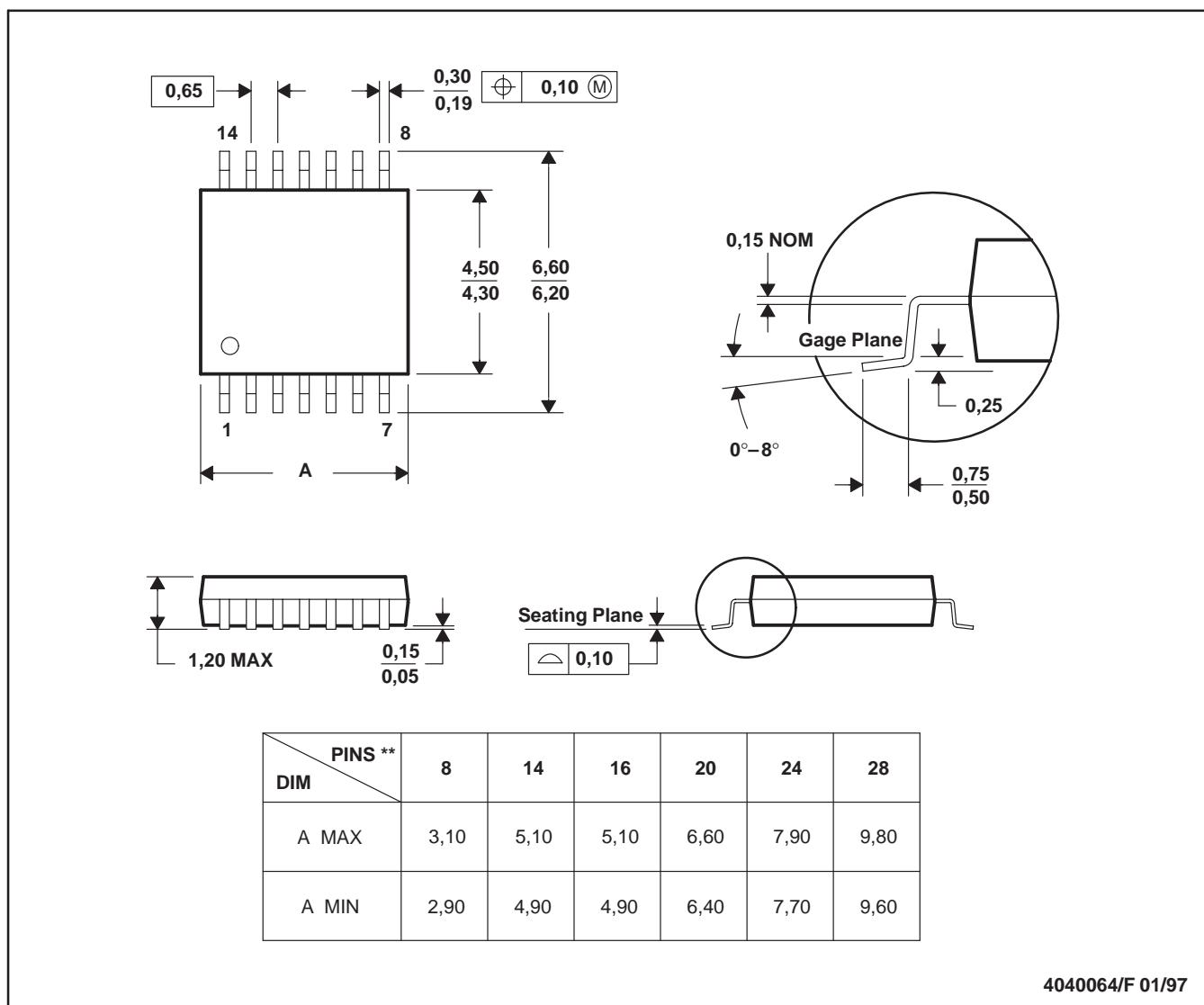


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - Falls within JEDEC MO-153

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		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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CD74HC192, Status: ACTIVE

High Speed CMOS Logic Presettable Synchronous BCD Decade Up/Down Counter with Asynchronous Reset

 View ROHS Compliant Devices

View RoHS Compliant Devices

 clear gif clear gif Features Quality & Pb-Free Data Related Products Tools & Software Samples Pricing/Packaging Inventory Symbols/Footprints Technical Documents Applications Notes Simulation Models Reference Designs Refine Your Selection

- Logic: Decade Counter

 Support

- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
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- Part Number Nomencla

 Datasheet H

CD54/74HC192, CD54/74HC193, CD54/74HCT193 (Rev. F) (cd74hc192.pdf, 368 KB)
13 Oct 2003 Download

	CD54HC192	CD74HC192
Voltage Nodes(V)	6, 5, 2	
	Samples	Samples
	Inventory	Inventory

 Product Information Features Save this to your personal library

Synchronous Counting and Asynchronous Loading

Two Outputs for N-Bit Cascading

Look-Ahead Carry for High-Speed Counting

Fanout (Over Temperature Range)

- Standard Outputs 10 LSTTL Loads
- Bus Driver Outputs 15 LSTTL Loads

Wide Operating Temperature Range . . . -55°C to 125°C

Balanced Propagation Delay and Transition Times

Significant Power Reduction Compared to LSTTL Logic ICs

HC Types

- 2V to 6V Operation
- High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$

HCT Types

- 4.5V to 5.5V Operation
- Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
- CMOS Input Compatibility, $I_L < 1\mu A$ at V_{OL}, V_{OH}

Data sheet acquired from Harris Semiconductor

 Description

The 'HC192, 'HC193 and 'HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input (PL). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is present to an illegal state or assumes an illegal state when power is applied, it will

return to the normal sequence in one count as shown in state diagram.

Pricing/Packaging/CAD Design Tools/Samples								
			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
CD74HC192E	ACTIVE	-55 to 125	0.37 1KU	PDIP (N) 16	View	25	<input type="checkbox"/>	Purchase Samples
CD74HC192EE4	ACTIVE	-55 to 125	0.37 1KU	PDIP (N) 16	View	25	<input type="checkbox"/>	Purchase Samples
CD74HC192NSR	ACTIVE	-55 to 125	0.33 1KU	SO (NS) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC192NSRE4	ACTIVE	-55 to 125	0.33 1KU	SO (NS) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC192PW	ACTIVE	-55 to 125	0.33 1KU	TSSOP (PW) 16	View	90	<input type="checkbox"/>	Purchase Samples
CD74HC192PWE4	ACTIVE	-55 to 125	0.33 1KU	TSSOP (PW) 16	View	90	<input type="checkbox"/>	Purchase Samples
CD74HC192PWR	ACTIVE	-55 to 125	0.33 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
CD74HC192PWRE4	ACTIVE	-55 to 125	0.33 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	Request Free Samples
CD74HC192PWT	ACTIVE	-55 to 125	0.39 1KU	TSSOP (PW) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC192PWTE4	ACTIVE	-55 to 125	0.39 1KU	TSSOP (PW) 16	View	250	<input type="checkbox"/>	Purchase Samples

Inventory								
TI Inventory Status				Reported Distributor Inventory				
CD74HC192E	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	1425*	24 2 Dec	10 Weeks	Americas	Avnet	474	<input type="checkbox"/>	
		25 5 Dec		Europe	EBV Elektronik	700	<input type="checkbox"/>	
		75 12 Dec			Spoerle	625	<input type="checkbox"/>	
		1526 19 Dec						
		>10k 16 Jan						
CD74HC192EE4	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	1425*	24 2 Dec	10 Weeks	None Reported				
		25 5 Dec		View Distributors				
		75 12 Dec						
		1526 19 Dec						
		>10k 16 Jan						
CD74HC192NSR	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	
	0*	831 28 Dec	10 Weeks	None Reported				
		537 3 Jan		View Distributors				
		97 9 Jan						
		792 16 Jan						
		684 23 Jan						
CD74HC192NSRE4	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005				
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase	

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	0*	831 28 Dec	10 Weeks	None Reported			-
		537 3 Jan					
		97 9 Jan					
		792 16 Jan					
		684 23 Jan					
CD74HC192PW	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported			
CD74HC192PWE4	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported			
CD74HC192PWR	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	Americas	DigiKey	>1k	
CD74HC192PWRE4	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported			
CD74HC192PWT	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported			
CD74HC192PWTE4	As of 9:51 AM GMT, 29 Nov 2005			As of 9:51 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported			

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** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred [TI Authorized Distributor](#) for additional information.

Quality & Lead (Pb)-Free Data

	Product Content					MTBF/FIT Rate
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details	
CD74HC192E <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View	
CD74HC192EE4 <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View	
CD74HC192NSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192NSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192PW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192PWE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192PWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192PWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192PWT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	
CD74HC192PWTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View	

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

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Datasheets

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Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)

29 Aug 2002 [Abstract](#)

Selecting the Right Texas Instruments Signal Switch (szza030.htm, 9 KB)

07 Sep 2001 [Abstract](#)

Implications of Slow or Floating CMOS Inputs (Rev. C) (scba004c.htm, 9 KB)

01 Feb 1998 [Abstract](#)

CMOS Power Consumption and CPD Calculation (Rev. B) (scaa035b.htm, 9 KB)

01 Jun 1997 [Abstract](#)

Designing With Logic (Rev. C) (sdya009c.htm, 9 KB)

01 Jun 1997 [Abstract](#)

Live Insertion (sdya012.htm, 9 KB)

01 Oct 1996 [Abstract](#)

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)

01 Oct 1996 [Abstract](#)

SN54/74HCT CMOS Logic Family Applications and Restrictions (scla011.htm, 9 KB)

01 May 1996 [Abstract](#)

Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (scla008.htm, 9 KB)

01 Apr 1996 [Abstract](#)

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User Guides

Signal Switch Data Book (Rev. A) (scdd003a.pdf, 19732 KB)

14 Nov 2003 [Download](#)

LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)

05 Dec 2002 [Download](#)

More Literature

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)

15 Mar 2005 [Download](#)

Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)

10 Aug 2004 [Download](#)

SN74HC4851/HC4852 Product Clip (Rev. B) (scyb019b.pdf, 501 KB)

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Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)

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