Application Note AN4105

Design Considerations for Switched Mode Power Supplies Using A Fairchild Power Switch (SPS) in a Flyback Converter

Introduction

Flyback switched mode power supplies (SMPS) are among the most frequently used power circuits in household and consumer electronics. The basic function of an SMPS is to supply regulated power to the load on the secondary, or output side. An SMPS typically incorporates a power transformer, secondary side rectifier diodes, switching semiconductor device with control IC, and peripheral circuitry. If the level of integration of the switching and control circuitry is not high enough, then additional, separate circuits will be required to accommodate all functions. Such additional components raise the overall SMPS cost and not uncommonly reduce reliability.

Fairchild Power Switch (SPS) is a range of highly integrated ICs for power supply applications. They combine a high voltage power MOSFET (SenseFET) and pulse width modulation (PWM) based control IC in one package. Moreover, they provide enhanced IC functionality, thereby minimizing the number of additional components needed in an SMPS. Fairchild Power Switch (SPS) ICs are widely used in the power circuits of a variety of equipment, such as color TVs, printers, PCs, monitors, battery chargers and ac adapters. They typically incorporate a variety of enhanced protection functions and permit much reduced power consumption in standby modes.

This application note considers the three major functional blocks of an SMPS: Fairchild Power Switch (SPS), flyback converter, and transformer. It discusses a variety of issues important to their design and use in the overall SMPS.

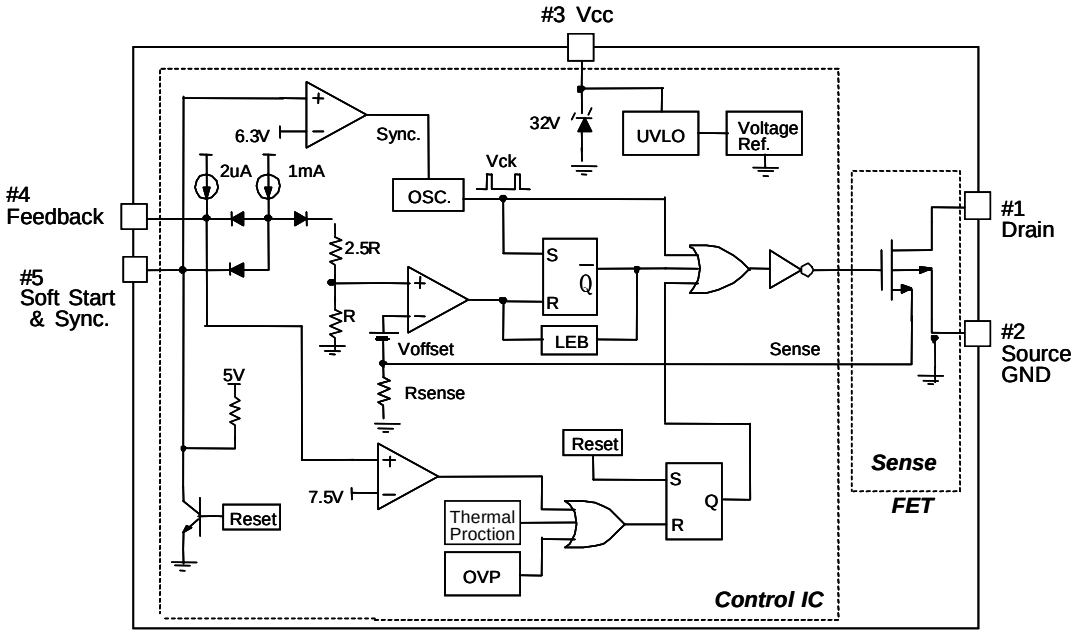


Figure1. Internal block diagram of a Fairchild Power Switch(SPS).

1. Block Diagram and Basic Operation of a Fairchild Power Switch(SPS)

1.1 Block diagram

Figure 1 presents a block diagram of a Fairchild Power Switch (SPS). It can be divided into several large, functional sections: under voltage lockout circuitry (UVLO); reference voltage; oscillator (OSC); pulse width modulation (PWM) block; protection circuits; and gate driving circuits.

1.2 Under voltage lockout (UVLO)

A Fairchild Power Switch (SPS) under voltage lockout (UVLO) circuitry (Figure 2) guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the value of V_{CC} (Figure 3). The tur off and turn on voltage thresholds are fixed internally at 10V and 15V, respectively. Therefore the UVLO circuitry turns off the control circuit when V_{CC} is lower than 10V and starts it when V_{CC} is higher than 15V. Once the control circuit starts operating, V_{CC} must drop below the 10V level for the UVLO to stop the circuit again. Before switching starts, the IC current is less than 300µA. IC operation starts when C_{CC} (Figure 2) charges to 15V. Because only a small current (<1 mA) is allowed to flow in through the resistor during normal operation this technique reduces the current dissipation in the SMPS start up resistor.

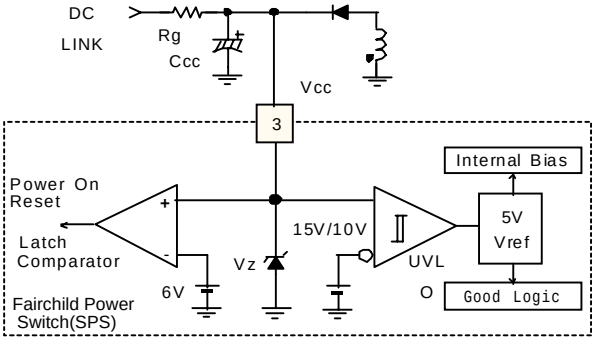


Figure 2. Detail of the undervoltage lockout (UVLO) circuitry in a Fairchild Power Switch. The gate operating circuit holds in a *low* state during UVLO, thereby maintaining the SenseFET at turnoff.

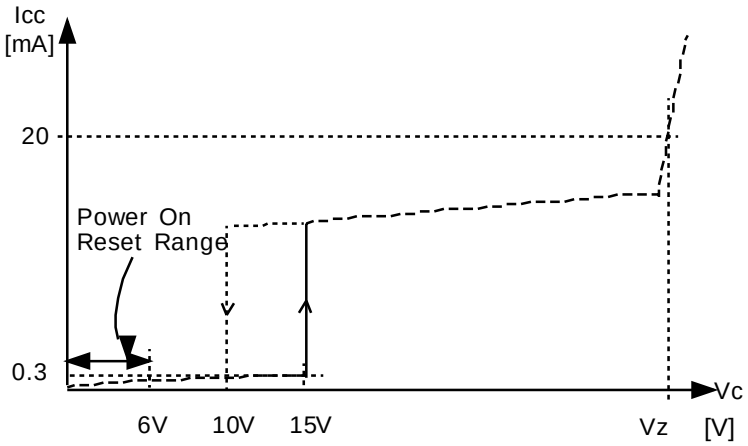


Figure 3. Fairchild Power Switch(SPS) control circuit status *vs.* V_{cc}.

1.3 Feedback control circuit

The Fairchild Power Switch(SPS) control IC uses a current mode PWM and operates such that MOSFET current is proportional to the feedback voltage V_{fb}. This limits the MOSFET current at every cycle. It also offers other advantages, such as a well regulated SMPS output voltage with input voltage changes. This method of control also works successfully in SMPSs used for monitors, which may have a broad range of synchronizing frequencies to deal with. As shown in Figure 4, the Fairchild Power Switch (SPS) oscillator turns on the MOSFET. The feedback comparator operates to turn it off again, when the MOSFET current reaches a set value proportional to V_{fb}. The MOSFET turn off operation is as follows:(1) the internal (R+2.5R) voltage divider sets the voltage fed back to one input of the feedback comparator at V_{fb} /3.5; (2) a current proportional to the drain current flows to the MOSFET sense terminal making V_{sense} proportional to the drain

current; and, (3) when V_{sense} becomes greater than V_{fb}, the output of the feedback comparator goes high, turning off the MOSFET. Figure 4 also shows that the circuit is designed to use an opto isolator in the feedback loop. This is appropriate for an off line design where input to output isolation is required. C_{fb} improves the noise characteristics. If the control IC incorporates an error amp however, as in Fairchild's KA3842B/3B/4B/5B current mode PWM controller ICs for SMPSs then a resistor and capacitor are required to provide the feedback to the error amp. This would provided the same functions as those provided by the circuit of Figure 4, e.g., fine control of the output voltage through Vfb. Similarly, other appropriate devices here are Fairchild's LM431/TL431/KA431 series of three terminal shunt regulators. These have a very sharp turn on characteristic much like a Zener diode and are widely used in SMPS secondary side error amplifiers.

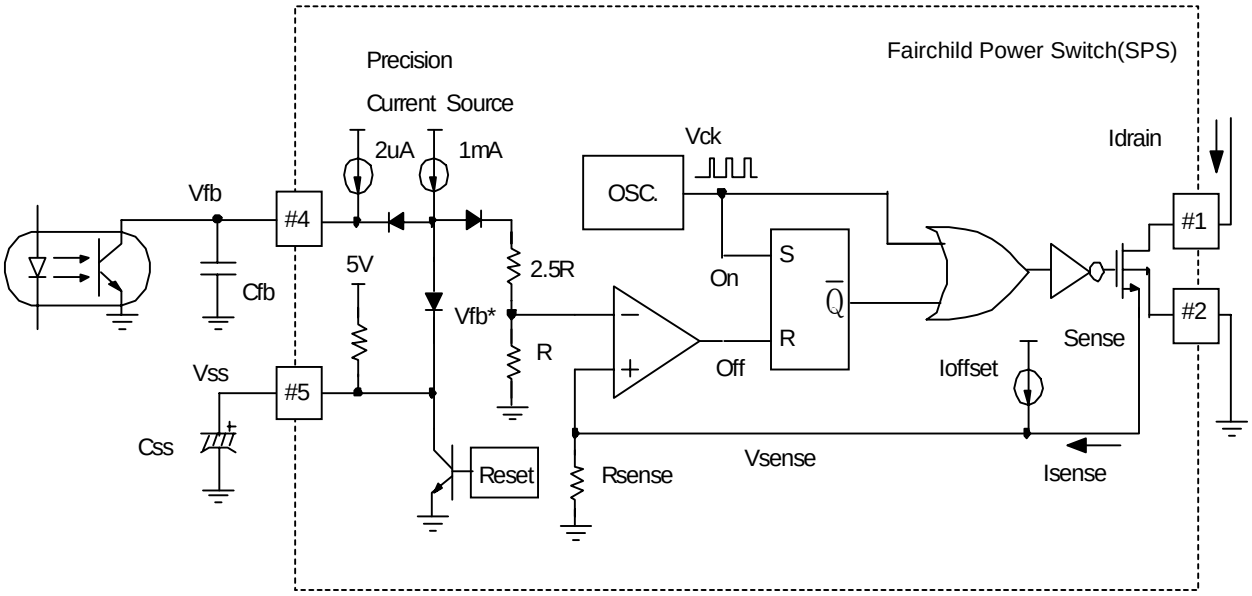
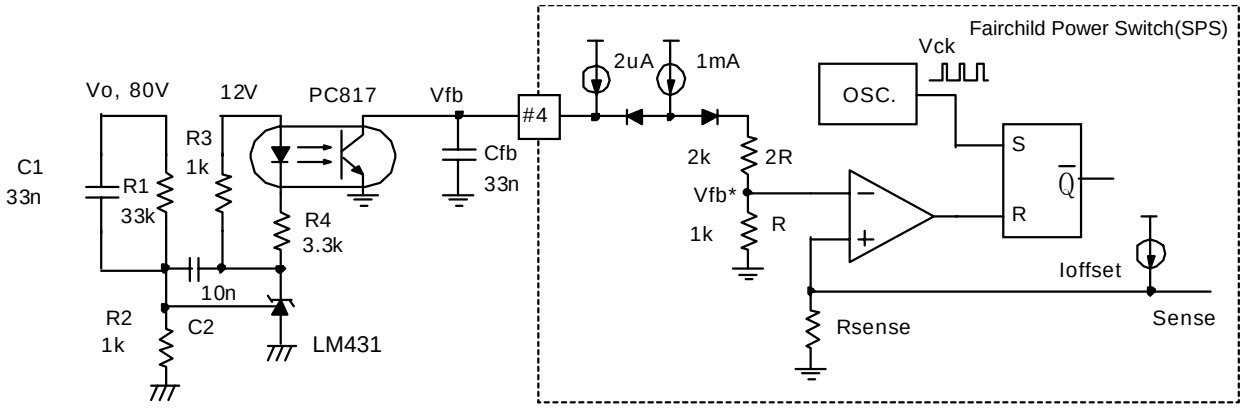


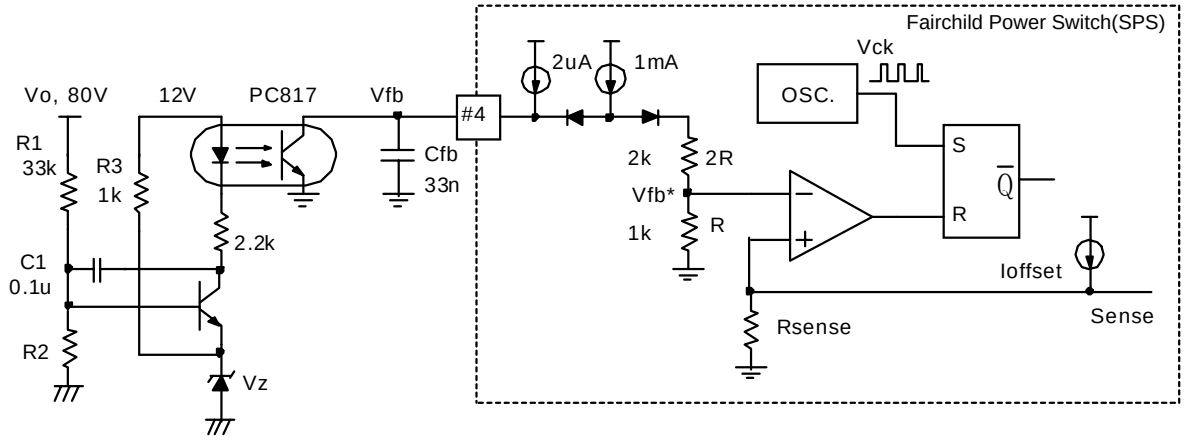
Figure 4. Fairchild Power Switch(SPS) feedback circuit appropriate for off line SMPS use (current mode PWM).

1.4 Example Fairchild Power Switch (SPS) control circuit

Figure 5 shows two approaches to controlling feedback in a Fairchild Power Switch (SPS). The design in Figure 5a uses the LM431 regulator, and that of Figure 5b uses a Zener diode. Although there are differences among Zeners, and their constant voltage characteristics are slightly poorer than shunt regulators', a design using a Zener diode has cost advantages. In Figure 5a, C1 together with R1 produce a zero point to compensate the pole formed by the Fairchild Power Switch (SPS)'s internal 3.5KΩ resistor and C_{fb}; There would be no safety problems if the zero did not exist, but it is added to improve dynamic response. If dynamic response is not a factor, C1 can be removed (as in fact was done in Figure 5b). C2 increases the loop gain enough at low frequencies to improve the output load regulation. R3, through the LM431's bias resistor, can set the photodiode current at almost zero. R4 limits the maximum current of the photodiode to 2.3mA [(12V - 2.5V - 2V) /3.3KΩ, where 2.5V is the LM431's saturation voltage and 2 V is the photodiode's voltage drop]. C_{fb} should be determined by considering the shutdown delay time (see Section 2.1). In Figure 5b, R3 sets a fixed current to the Zener diode to stabilize its voltage.



(a) Control Circuit using KA431(LM431) Control IC



(b) Control Circuit using a Zener Diode Control IC

Figure 5. Fairchild Power Switch(SPS) feedback control circuit.

1.5 Soft start operation

Normally, the SMPS output voltage increases from start up with a fixed time constant. This is due to the capacitive component of the load. At start up, therefore, the feedback signal applied to the PWM comparator's inverting input reaches its maximum value (1V), This is because the feedback loop is effectively open. Also at this time, the drain current is at its peak value (I_{peak}) and maximum allowable power is being delivered to the secondary load. With that said, note that when the SMPS pushes maximum power to the secondary side for this initial fixed time, the entire circuit is seriously stressed. Use of a soft start function avoids such stresses. Figure 6 shows how to implement a soft start for a Fairchild Power Switch(SPS). At turn on, the soft start capacitor C_S on pin 5 of the Fairchild Power Switch(SPS) starts to charge through the 1mA current source. When the voltage across C_S reaches 3V, diode D_S turns off. No more current flows to it from the 1mA current source. Cs then continues to charge to 5V through the 50kΩ resistor.

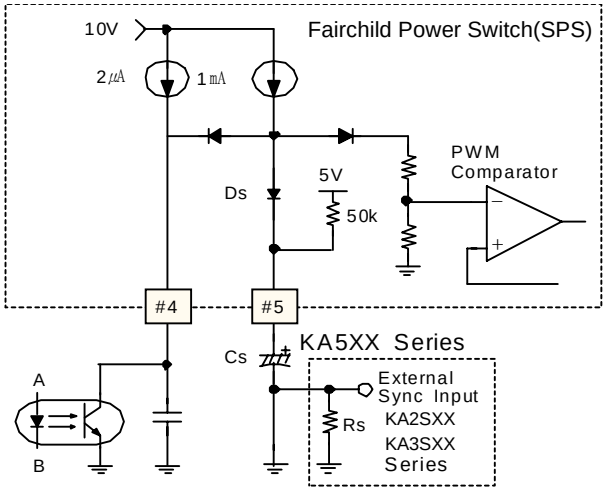


Figure 6. Soft start circuit.

Note that when the voltage across C_S exceeds 3V, The voltage at the comparator's inverting terminal no longer follows the voltage across C_S. Instead, it follows the output voltage feedback signal. In shutdown or protection circuit operation, capacitor C_S is discharged, to enable it to charge from 0V at restart.

1.6 Synchronization

In an SMPS intended for use with monitors, synchronization is handled differently than in a general purpose SMPS. For monitor use, it is necessary to prevent noise from appearing on the monitor display. To accomplish this, it is necessary to synchronize the SMPS switching frequency with the monitor's horizontal sync frequency. The monitor's horizontal scan flyback signal is commonly used as the external sync signal for the SMPS. By synchronizing the switching with the horizontal scan's flyback, the switching noise is positioned at the far left of the monitor display where it cannot be seen. Figure 7 shows how to implement the external synchronization scheme. The external sync signal, applied across resistor R_S, cannot drop below 0.6V because of diode D_{sync}. After the conclusion of the initial soft start, the voltage across C_S remains at 5V until the external sync signal is applied, at which point it looks like V_{Rs} of Figure 8. The sync comparator compares V_{Cs} against a 6.3V level and produces the comparator output waveform, V_{comp} of Figure 8. A Fairchild Power Switch (SPS) has an internal timing capacitor, C_t. Figure 8 shows that when the voltage on C_t, V_{Ct}, reaches an upper threshold, it begins to discharge; then, when it reaches a lower threshold, it again starts to charge. This operation is controlled by the internal oscillator. The oscillator output signal, V_{Ck} in Figure 8, which goes low

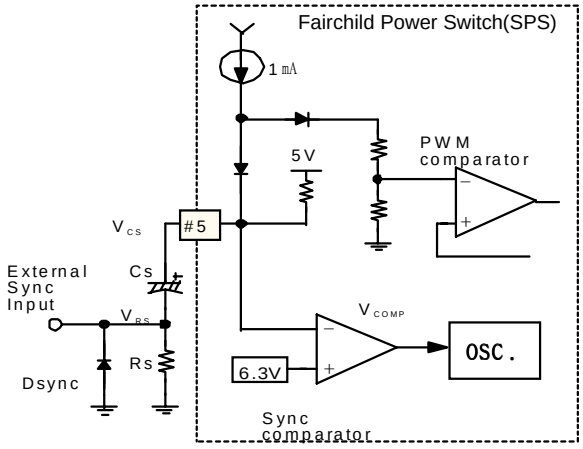


Figure 7. Synchronization circuit.

when C_t recharges and high when it discharges, is applied to the Fairchild Power Switch (SPS) S/R Latch Set terminal. In the absence of an external sync signal, the voltage across C_t oscillates at the basic frequency of 20kHz. In the presence of a sync signal, however, the Set signal goes high because V_{Ct} charges to the high threshold following the external sync signal, and, ultimately, the Set signal, which determines the switching frequency, synchronizes to the external sync signal. It is necessary to limit the Set signal's high duration to 5% or less of the full cycle. As the Set signal drops low the gate turns on. If the device were not synchronized to the horizontal scan of the monitor, noise would appear on the screen. When the Set signal goes high, the sync is synchronized with the horizontal scan flyback. Because the high duration is 5% (maximum) of the full cycle, the start of the horizontal scan (as the Set signal goes low) turns on the switch. The switch turn on noise, therefore, is hidden in the horizontal blanking period at the far left of the monitor display.

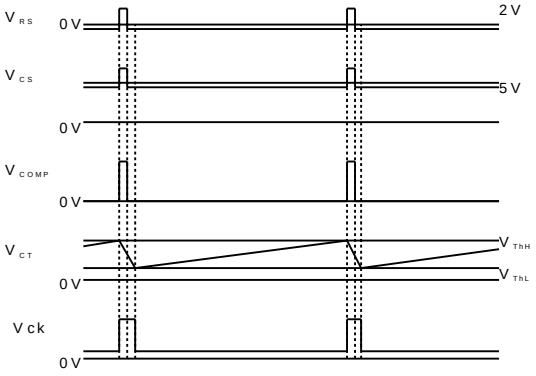


Figure 8. Synchronization circuit operation.

2. Fairchild Power Switch(SPS) Built In Protection Circuits

Since a Fairchild Power Switch (SPS)'s built in protection circuits do not require additional, external components, reliability is increased without increasing cost. Note that the protective circuitry can completely stop the SMPS operation (latch mode protection) until the power is turned off and on again, and can make the control voltage restart above the ULVO level should the latch be released below ULVO (Auto Restart Mode protection).

2.1 Output overload protection

An overload is any load greater than the load defined as normal for operation. This is not a short circuit. The Fairchild Power Switch (SPS) overload protection determines whether the overload is true or merely transient. Only a true overload will trigger the overload protection. When the Fairchild Power Switch (SPS) senses an overload, it waits for a specified time. If the overload is still present after this, it is considered a true overload and the device shuts down.

The Fairchild Power Switch (SPS) has a current control that prohibits current flow above a set maximum, which means the maximum input power is limited at any given voltage. Therefore, if the output load tries to draw more than this level, V_o (Figure 9) drops below the set voltage and LM431 can draw only a given minimum current. As a result, the opto coupler secondary current drops to almost zero. Almost the entire current flow at the node is from the Fairchild Power Switch (SPS) 1mA current source. Hence, the internal 3KΩ resistor (2.5R + R = 3KΩ) moves V_{fb} to 3V. From this point on, however, the 5μA current source starts to charge C_{fb}, and, because the opto coupler secondary current is almost zero, V_{fb} continues to increase. When V_{fb} reaches 7.5V, the Fairchild Power Switch (SPS) shuts down.

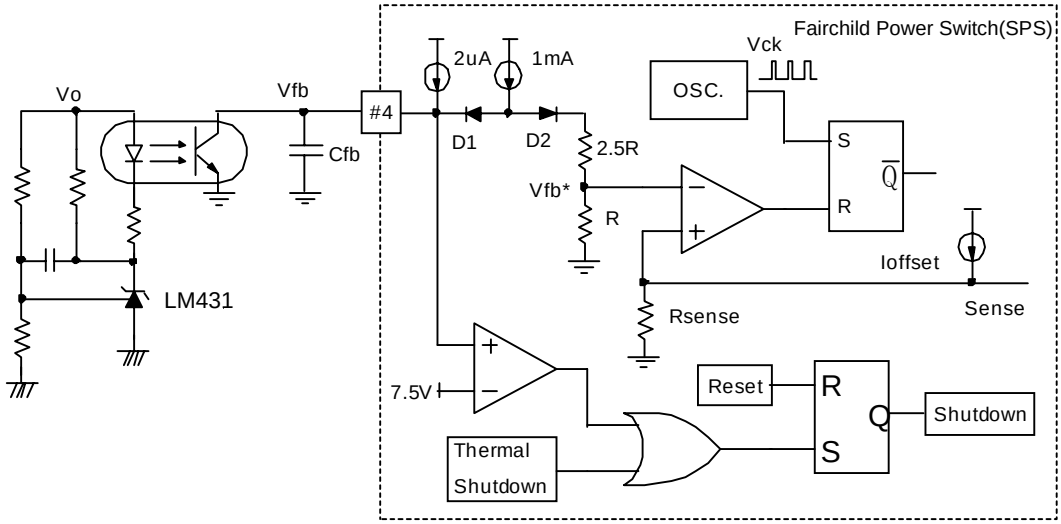


Figure 9. Fairchild Power Switch(SPS) overload protection circuit.

The shutdown delay interval is therefore determined by $C_{fb.}$ When C_{fb} is 10nF, the shutdown delay t2 (see Figure 10b) is about 9mS. With C_{fb} at 0.1μF, t2 is about 90mS. Such delay intervals do not allow the typical transients observed to shut down the Fairchild Power Switch (SPS). Note that, if a longer delay is needed, C_{fb} cannot be made arbitrarily large because it is important in determining the dynamic response of the SMPS. When a large value of C_{fb} is necessary, a series connected capacitor and Zener diode can be connected across C_{fb} as shown in Figure 10a. The combination works in this way: When V_{fb} is below 3V, the low valued C_{fb} allows the SMPS to have a good dynamic response. When V_{fb} is above 3.9V, the high valued C_d extends the delay time to the desired shutdown point. Of course, where transients are insignificant and good dynamic response is not required, then do without C_d and the Zener, thereby eliminating their added costs.

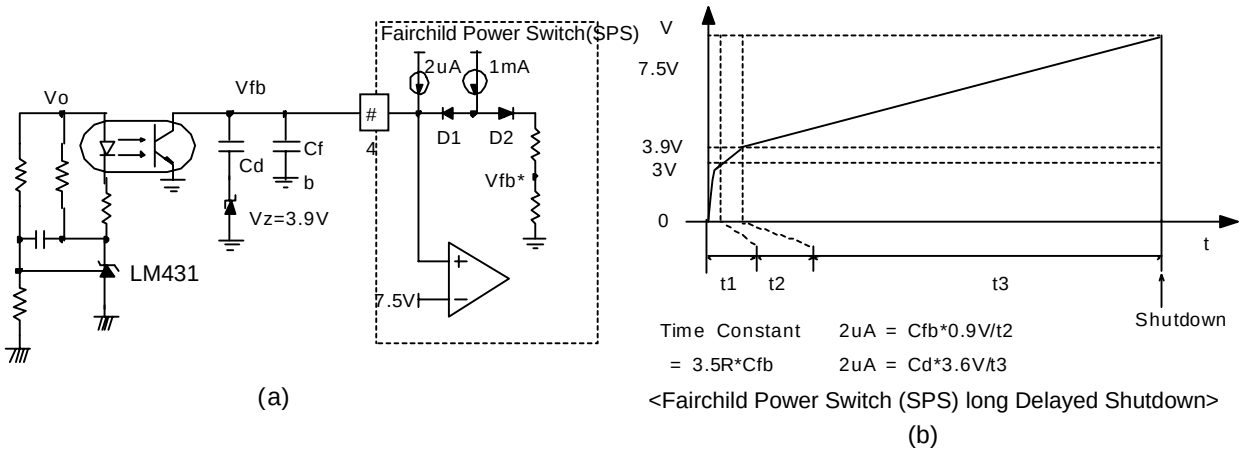


Figure 10. Long delay shutdown.

2.2 Output short circuit protection

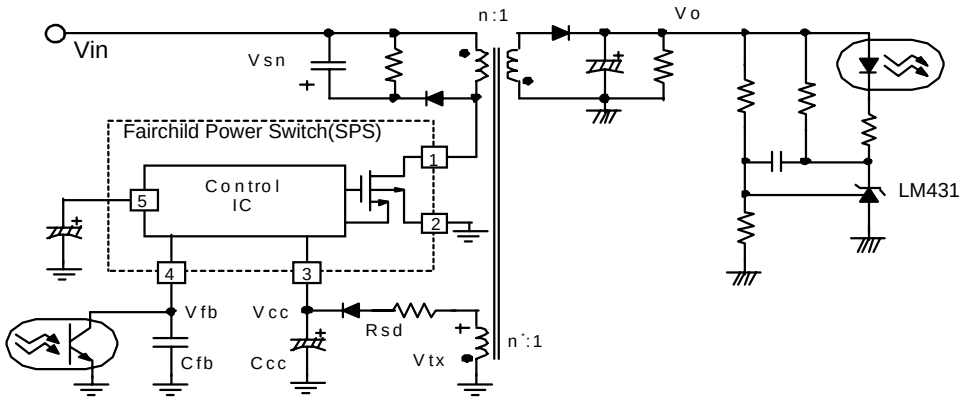
When the SMPS's output terminal is short circuited the input current is at maximum. The output power however, is not a maximum. This is because there can be no load voltage since the load is a short circuit. Under such conditions the output short circuit protection operates as follows.

When the output load short circuits a relatively large transformer winding in the SMPS, the Fairchild Power Switch(SPS)'s MOSFET current becomes much greater than I_{peak} because the inductor's magnetic core is unable to reset. This is due to low transformer coil voltage at turn off. This occurs because the current remaining in the inductor during the Fairchild Power Switch(SPS)'s minimum turn on time cannot decrease by that amount during the remaining turn off time. Even though it is a large current, it does not unduly stress the MOSFET but does greatly stress the transformer's secondary coils and the secondary side rectifiers.

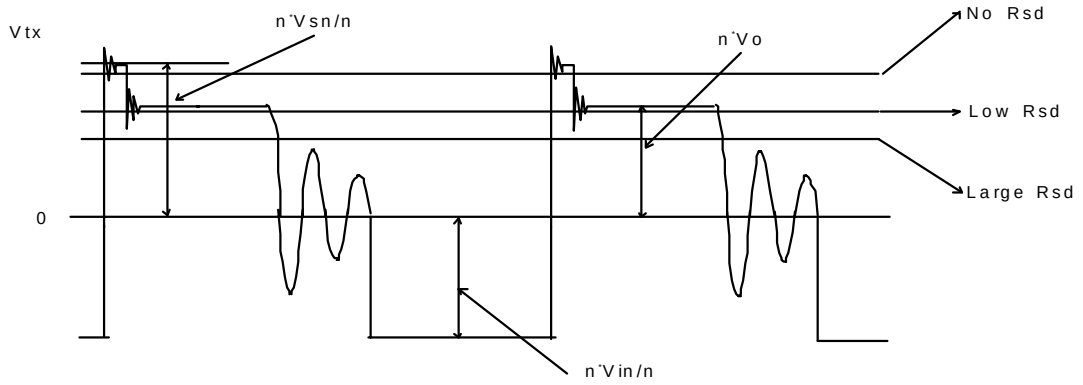
In most flyback or forward converters the controller gets its power from a small secondary bias winding in the transformer. Furthermore, this controller voltage is proportional to the output voltage (see circuit of Figure 11a). This is fairly straightforward because, for a flyback converter, the coil voltage when the switch turns off is proportional to the output voltage. For a forward converter, the transformer average voltage at turn off is proportional to the output voltage. For a flyback converter SMPS, the output short circuit protection circuit can be operated in either latch mode or auto restart mode.

The change in V_{cc} as a function of Rsd is shown in Figure 11b. Rsd is shown in Figure 11a. When R_{sd} is zero, V_{cc} reaches the maximum value of V_{tx} (see lower primary winding, Figure 11a), i.e., $n'V_{sn}/n$, which is proportional to the maximum transformer current. For this case, if the output short circuits, V_{cc} increases and, after a specified delay, the protection circuit operates, entering the latch mode.

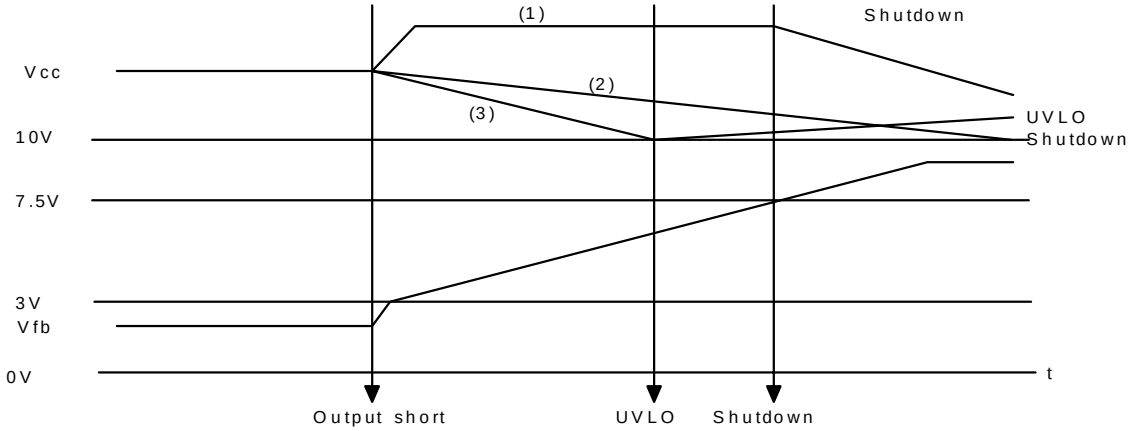
However, when R_{sd} is made sufficiently large, V_{cc} can become smaller than $n'V_o$. Therefore, if the output short circuits, V_{cc} drops, but, if C_{cc} (see Figure 11a) is sufficiently large, V_{cc} stays at a level higher than the UVLO's lower threshold voltage (10V) until V_{fb} reaches 7.5V (Figure 11c-2) and latch mode protection starts. In contrast, if C_{cc} is small enough V_{cc} approaches the UVLO's low threshold before V_{fb} reaches 7.5V (Figure 11c-3), and the UVLO operates instead of the protection circuit, stopping the device switching. In such a case, if V_{cc} exceeds the ULVO's upper threshold voltage (15V), auto restart operates again. R_{sd}, C_{cc}, and C_{fb} have affects even at start up and power down, so their values must be decided upon carefully. Our experiments have indicated that 10 - 20Ω is most appropriate for R_{sd}.



(a) Flyback converter



(b) The voltage Vtx ware form of N_B and V_{CC}(the rectified V_{NB}) depending on Rsd



(C) Vcc and Vfb waveforms depending on the relative size of Cvcc at output short

Figure 11. Operation of the SMPS flyback converter's output short circuit protection (latch mode).

2.3 Fast protection without delay

It was mentioned above that the Fairchild Power Switch(SPS) shutdown capability is associated with a delay, to allow normal transients to occur without shutting down the system. In effect, this restricts the protection range. If fast protection is required, then additional circuitry is called for. Figure 12 shows how it's done. A transistor is used to force the feedback photodiode current to increase causing the primary side V_{fb} to be forced below 0.3V. Therefore the Fairchild Power Switch (SPS) stops switching. Depending on the magnitude of the photodiode current, the protection can be made to operate sufficiently fast. In such a case, when the transistor is turned off, the protection shifts to auto restart mode for normal operation. It is also possible to use this circuit as an output enable circuit. Fast latch mode protection can be implemented by adding a photocoupler. Thus, when the output terminal latch mode transistor turns on, a large current flows through the photodiode PC2. *A* large current therefore flows through the primary phototransistor, which increases V_{fb} rapidly. This executes fast latch mode protection with no time delay.

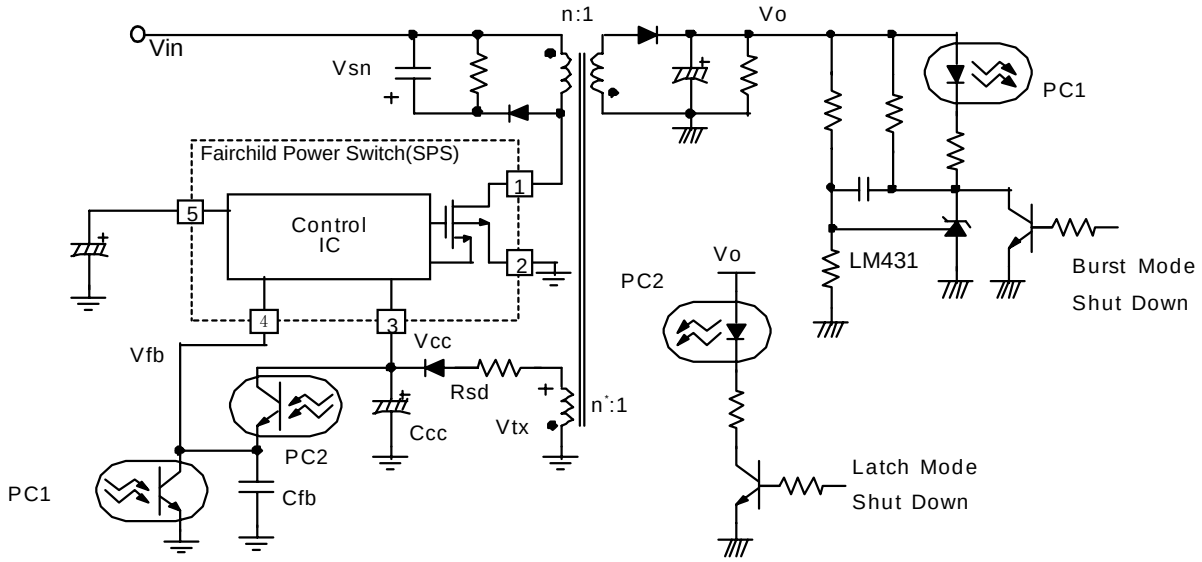


Figure 12. A fast protection circuit without a shutdown delay.

2.4 Overvoltage protection

The Fairchild Power Switch (SPS) has a self protection feature that operates even when faults exist in the feedback path. These could include an open or short circuit. On the primary side, if the feedback terminal is short circuited, then the voltage on it is zero and hence the Fairchild Power Switch (SPS) is unable to start switching. If the feedback path open circuits, the protection circuit operates as though a secondary overload is present. Further, if the feedback terminal looks open due say, to some fault in the primary feedback circuit, the primary side could switch at the set maximum current level until the protection circuit operates. This causes the secondary voltage to become much greater than the rated voltage. Note that in such a case if there were no protection circuit, the fuse could blow or, more serious, a fire could start. It is possible that, without a regulator, devices directly connected to the secondary output could be destroyed. Instead, however, the Fairchild Power Switch (SPS) over voltage protection circuit operates. Since V_{CC} is proportional to the output, in an over voltage situation it will also increase. In the Fairchild Power Switch (SPS), the protection circuit operates when V_{cc} exceeds 25V. Therefore in normal operation V_{cc} must be set below 25V.

3. Noise Considerations at switch Turn On

3.1 SMPS current sensing

Whether an SMPS is current mode or voltage mode controlled, or uses some form of non linear control, it requires the protection afforded by current sensing capabilities. Even though most current sensing is done using a sensing resistor or a current transformer, there are instances where a MOSFET is used by the SMPS to further reduce current sensing losses. The Fairchild Power Switch (SPS) switching element is a SenseFET. This minimises any power losses in the sense resistor, which is integrated onto the controller chip.

3.2 Current sensing waveform noise after turn on

A leading edge spike is present on the current sense line when the SMPS switching device turns on. It arises from three causes, as shown in Figure 13: (1) reverse recovery current; (2) charge/discharge current of the MOSFET shunt capacitance; and (3) MOSFET gate operating current.

(1) Reverse recovery current is generated when the SMPS operates in continuous conduction mode (CCM; see Section 4.1). If the MOSFET is turned on while the rectifier diode is conducting, the diode, during its reverse recovery time will act like a short circuit. Therefore a large current spike will flow in the MOSFET. There are three ways to reduce the magnitude of this (reverse recovery) current: use a fast recovery diode; reduce the MOSFET's gate operating current at turn on; or, increase the transformer leakage inductance.

(2) The total capacitance on the MOSFET's drain side includes the parasitic capacitor C_{ds} between the drain and the source terminals, the junction capacitance of the snubber diode, and the capacitance of the transformer windings. At turn on, the total equivalent capacitor discharges through the MOSFET.

(3) As shown in the diagram, the MOSFET gate operating current also flows through the current sensing resistor.

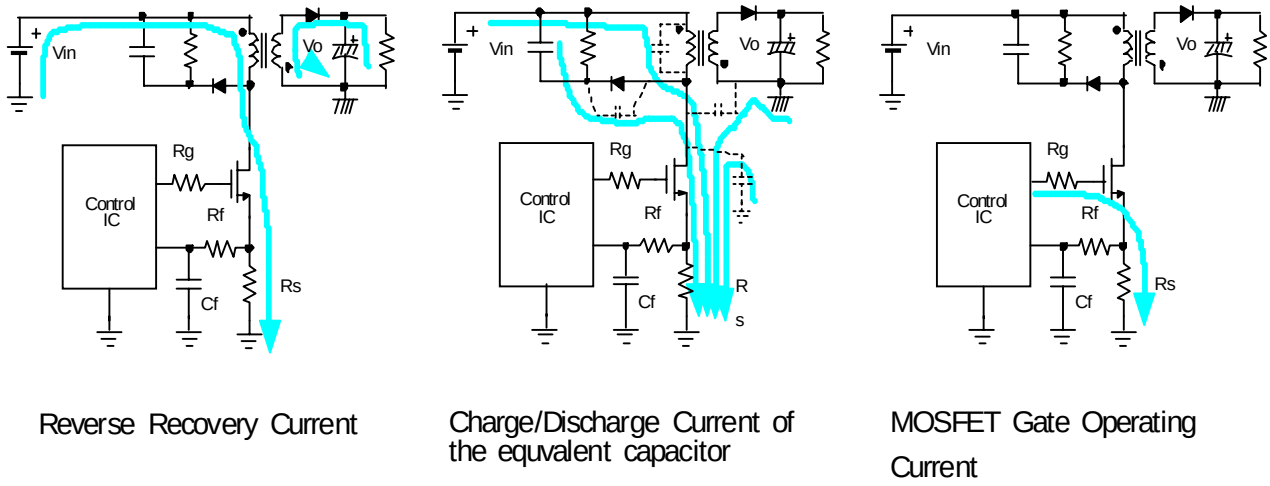


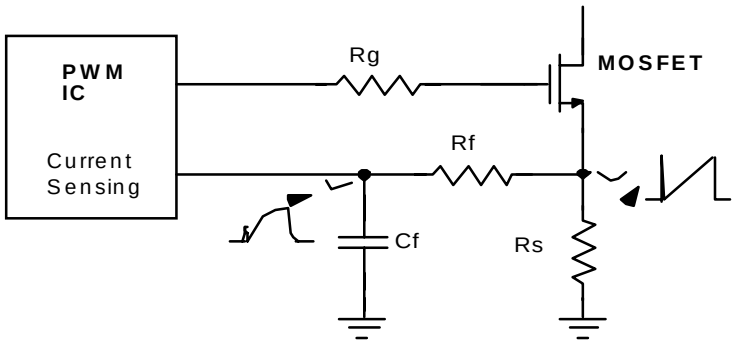
Figure 13. Current sensing waveform noise after turn on.

3.3 Dealing with leading edge noise

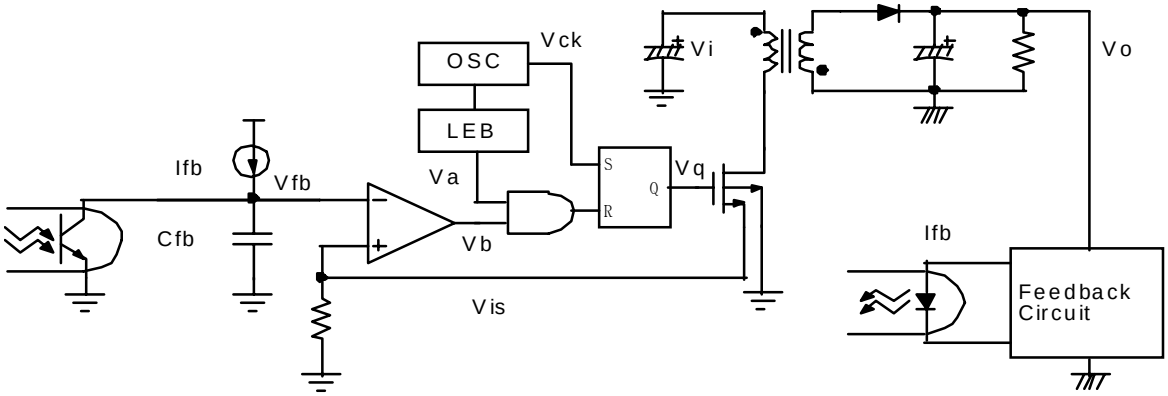
Among the measures taken to reduce leading edge noise, the most commonly used technique is the RC filter. As shown in Figure 14a the RC filter is effective against the noise, but it has the disadvantage that it distorts the current sensing signal so that accurate current sensing becomes difficult. Furthermore, a large RC value may be difficult to implement on an IC and may even require a bigger chip. The technique of leading edge blanking, as presented in Figure 14b and 14c, overcomes the distortion disadvantage of the RC technique and works as follows. Since the problem noise arises just after turn on, if a circuit is inserted that ignores the current sensing line for a fixed time just after turn on, operation can continue normally regardless of the noise. Whatever the details of the location and type of circuit used, the basic idea is to maintain a minimum turn on time i.e., to use the shortest turn on time that cannot be terminated once turn on starts. Duty ratio control with a minimum turn on time is implemented through a non linear control method having a very wide control range relative to a linear control. The non linear control operates such that if load conditions require a turn on time of 400ns when the minimum turn on time is set at 500ns, then one switching cycle will turn on at 800ns. The next cycle will be missed, ensuring that the average turn on time is 400nS. In this case every other cycle is missed. This is pulse skipping. In this case the switching frequency will be half that of a linearly controlled system, thereby improving SMPS efficiency at light loads. The input power is therefore minimised. The Fairchild KA34063 dc/dc converter is an example of a non linear control IC.

3.3.1 Burst mode operation

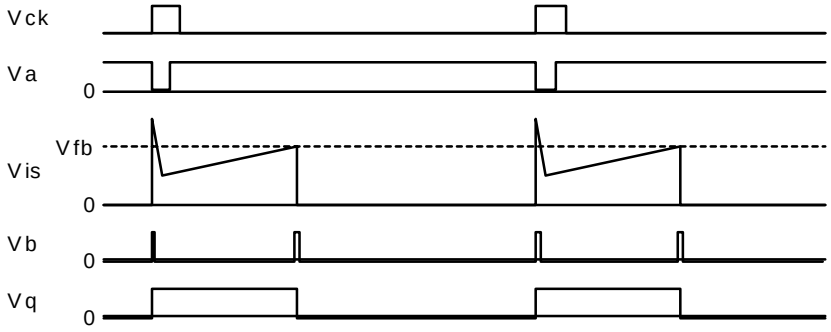
The aforementioned method can be viewed as an example of burst mode operation. Burst mode operation, by reducing the switching frequency, is one of the most useful ways to improve SMPS efficiency at light loads and to reduce the standby input power of household appliances, etc. Note that burst mode operation is not a burst oscillation (as in ringing choke conversion circuits), which can bring about reliability problems. There are mainly two types of true burst mode operation: one type lowers the switching frequency equally. The other switches at normal frequency for a fixed time and stops the control IC operation for a large number of cycles. Even though in the first method the control IC continues to consume power, the output voltage ripple is minimized. The second method can be a useful way to reduce the minimum input power at standby (since obviously the standby power is greatly reduced when the IC is stopped). Indeed, it is often used in cell phones to reduce the dc/dc converter’s power consumption in standby mode. However, it has the disadvantage of a larger output voltage ripple. Currently, Europe restricts a household appliance’s standby input power to less than 5W, and in time it will be required to be less than 3W. For such needs, burst mode operation will be a powerful method to satisfy the requirement for reduced standby input power.



(a) Noise elimination using RC filter



(b) Internal block diagram for noise elimination using LEB



(c) Noise elimination and waveforms in LEB

Figure 14. Leading edge blanking.

4. Flyback Converter Operation

4.1 Operation in continuous conduction mode (CCM)

Figure 15 shows a typical flyback converter. When the current through the converter's inductor is always greater than zero within a switching cycle, the converter is said to operating in the continuous conduction mode (CCM). Figure 16 shows the waveforms of CCM operation, which operates as follows.

4.1.1 For $t_0 \sim t_1 = T_{ON}$

At t_0 the MOSFET turns on. Immediately before t_0, the inductor current was flowing through diode D, but when the MOSFET turns on, D turns off thereby isolating the output terminal from the input terminal. At MOSFET turn on, its V_{DS} goes to zero, hence V_D becomes (V_o + V_i/n). During the interval after MOSFET turn on (i.e., from t_0 on), V_i is applied to L_m, so I_{Lm} increases linearly with a slope as shown by the following equation:

$$\text{Slope} = \frac{V_i}{L_m}$$

When the energy flow is examined, it is seen that the input power source supplies energy to L_m while the MOSFET is on. However, since the energy in L_m continues to increase while the output terminal is isolated from the input terminal, it is C_o that has to supply the output current during this interval.

4.1.2 For $t_1 \sim t_2 = T_{OFF}$

At t_1 the MOSFET turns off. At the instant of turn off, the inductor current that had been flowing through the MOSFET starts to flow through diode D. When D turns on, V_{DS} becomes (V_i +nV_o). During this interval the voltage nV_o is applied to L_m so that I_{Lm} decreases in a straight line with the following slope:

$$\text{Slope} = \frac{nV_O}{L_m}$$

When the energy flow during this interval is examined, it is seen that the inductor energy is delivered to the output. The energy in L_m is reduced by the amount of energy it delivers to the output. When the MOSFET turns on again, at t_2, one switching cycle will end.

4.1.3 Relationship between input and output

As shown in Figure 16, the colored areas A and B of the waveform V_{Lm} (the voltage applied to the inductor) must be equal because the average voltage of the inductor or transformer in steady state is always zero. Therefore:

$$V_i T_{ON} = nV_O T_{OFF}$$

$$\frac{nV_O}{V_i} = \frac{T_{ON}}{T_{OFF}} = \frac{D}{D-1}$$

The input and output currents become:

$$I_i = DI_{Lm,\,AVG}$$

$$I_O = n(1-D)I_{Lm,\,AVG}$$

Hence the input and output powers are equal. An ideal waveform is shown here because the effect of leakage inductance has been ignored. In reality leakage inductance will cause ringing.

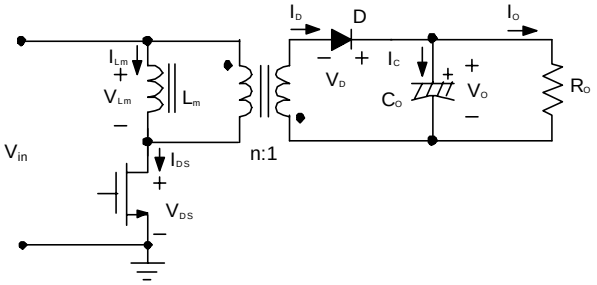


Figure 15. A typical flyback converter.

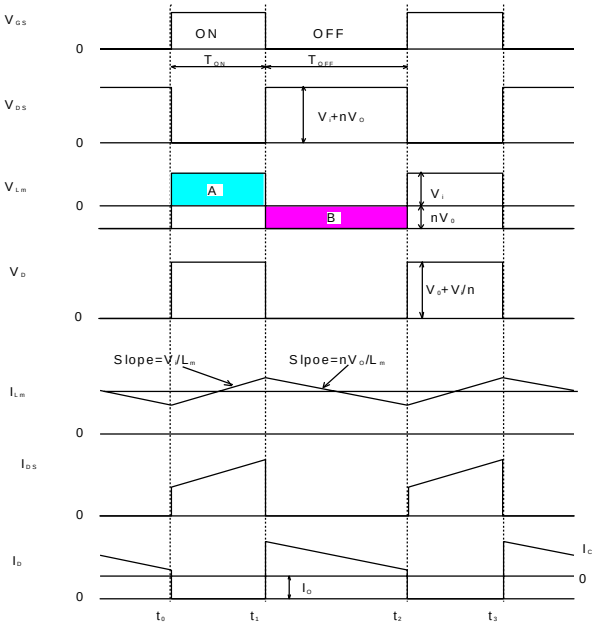


Figure 16. Flyback converter operating waveforms in continuous current mode (CCM).

4.2 Discontinuous conduction mode (DCM)

The appearance of an interval in which the inductor current becomes zero during a switching cycle marks flyback converter operation as discontinuous conduction mode (DCM). As shown in Figure 17, the voltage waveform applied to the inductor, V_{Lm}, becomes more complex in DCM. Hence, to avoid difficulties in computation T_{OFF} is not used. Instead, three input and output relationships of a converter are derived by using T_{OFF} * , the time when the output rectifier diode is actually conducting.

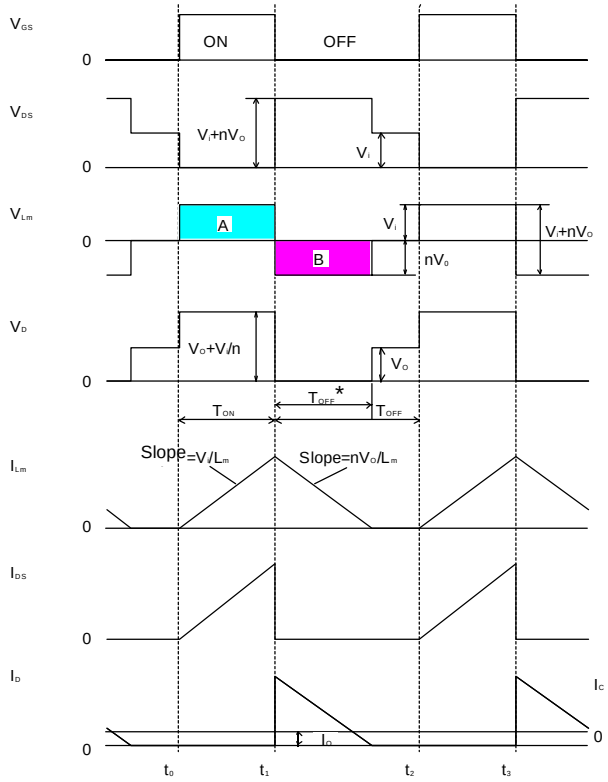


Figure 17. Flyback converter operating waveforms in discontinuous current mode (DCM).

The boundary condition between DCM and CCM is:

$$I_i + I_O = \frac{V_i}{2L_m} T_{ON}$$

The following input output relationship in DCM is derived by using the fact that the colored areas A and B of V_{Lm} in Figure 17 must always be equal because, in steady state, the average inductor (or transformer) voltage is always zero.

.

$$V_i T_{ON} = nV_O T^*_{OFF}$$

$$\frac{V_O}{V_i} = \frac{T_{ON}}{T^*_{OFF}} = \frac{D^*}{1-D^*}$$

Deriving the above equation again, using I_o and the fact that the input and output powers are equal, V_o is obtained as:

$$V_O = \frac{(V_i T_{ON})^2}{2\frac{I_O}{n} L_m (T_{ON} + T_{OFF}) + V_i}$$

The following equation represents the input power:

$$P_{IN} = \frac{1}{2} L_m I^2_{Lm,(peak)} fsw$$

where f_{sw} is the switching frequency.

4.3 Flyback converter design

4.3.1 Turns ratio considerations

The turns ratio of an SMPS's flyback converter transformer is an important variable. It affects the voltage and current levels associated with the primary side switching device and the secondary side rectifier, as well as the number of turns on the transformer and the current through it. A frequently discussed design concept suggests operating at maximum duty ratio when the input voltage is a minimum. For simplified calculations, here it is assumed that operating conditions change as listed immediately below.

- V_{ac} input: 85 ~ 265V_{ac}
- V_{dc} (rectified voltage): 100 ~ 400V_{dc}
- Output voltage: 50V_{dc}
- Inductor current: Continuous conduction mode (CCM) operation assumed.

The input power taken by the dc source is the product of the dc voltage and average input current. Using a wide duty cycle to deliver equal average current reduces efficiency. A narrow duty cycle increases the effective current on the primary side, increasing the operating temperature of the primary winding and the MOSFET. Also, it is best to decide on a turns ratio, n, based on the device used. If the voltage on the primary side MOSFET is relatively low (e.g., 600V), make n small; if it is on the high side (e.g., 800V), make n large. As the value of n increases, the primary side switching

device current and the secondary side rectifier diode voltage decreases Hence, with high output voltage and multiple secondary side outputs, it is advantageous to increase n.

4.3.2 Deciding on the operating current mode

As discussed in Sections 4.1 and 4.2, there are two different operating current modes possible in a flyback converter: the continuous conduction mode (CCM); and the discontinuous conduction mode (DCM). Here the advantages and disadvantages of each are reviewed, to help the designer make a proper choice between them.

4.3.2.1 Characteristics of the discontinuous conduction mode

In a flyback converter design, if discontinuous conduction occurs just at minimum input voltage and maximum output power, then discontinuous conduction must be considered to be the case for all input conditions. The flyback converter's input power in discontinuous conduction mode can be expressed as:

$$P_I = \frac{1}{2} L_m I_P^2 f_{sw}$$

Regardless of any changes in input voltage, the power equation indicates that the input current is limited by the peak value of the current flowing through the MOSFET in the transformer primary. A Fairchild Power Switch (SPS) has an integrated overcurrent protection feature (see Section 2.1, above). This feature does not require external components and operates across the range of input current. However, the fixed operating current of DCM, tends somewhat to offset the effect of the larger effective primary side current. The gain is at the low frequency end where core loss is not a problem since only a minimum number of turns need be wound. Also, turn on loss is not a serious problem due to the low input current. Other losses such as eddy current, skin effect, proximity effect, etc., are not significant. A more clearly defined advantage of DCM operation is that it permits the use of a slow and hence, low cost secondary rectifier diode. In contrast to the continuous conduction mode, in the discontinuous conduction mode the effective current is higher, requiring the use of heavier wire and hence thicker coils. Therefore DCM does not bring an advantage insofar as transformer construction is concerned. Moreover, DCM causes the MOSFET operating temperature to increase because of the large effective primary side current, as was described above (Section 4.3.1).

4.3.2.2 Characteristics of the continuous conduction mode

Since the coils' effective current is decreased CCM brings the advantage of lighter wire. The smaller effective current also reduces MOSFET heating. This is a definite advantage for average input current. On the other hand, CCM operation brings with it a need to consider the rectifier diode's reverse recovery current. Depending on the diode's reverse recovery time (t_{rr}), the reverse recovery current may stress the diode and increase the loss at its end terminals. It is therefore necessary to use a diode with the minimum t_{rr} possible within the allowable cost range.

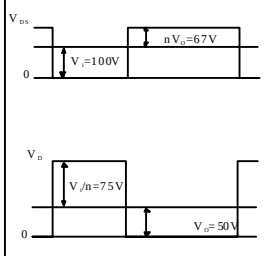
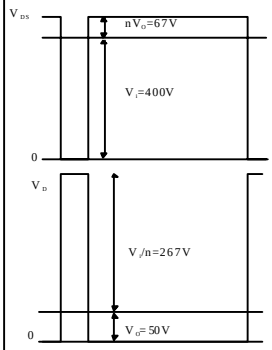
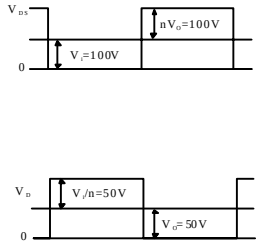
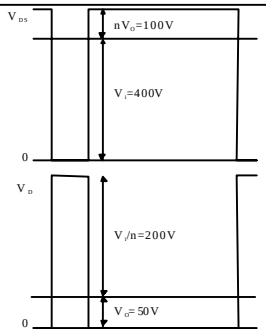
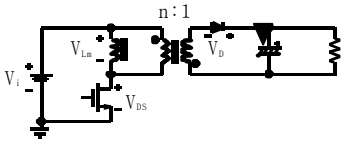
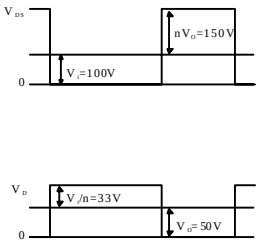
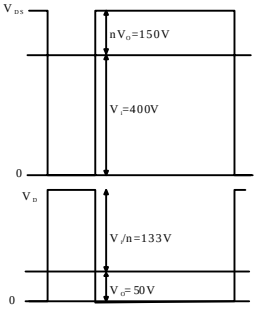
n	V_i=100V	V_i=400V	Merits & demerits
1	 V_{DS}=167V V_D=125V	 V_{DS}=467V V_D=317V	-Voltage applied to switch device is low -Effective current in switching device and primary winding is low -Voltage applied to rectifier diode is high -Output voltage ripple is small -Control must be done through short turn-on time
2	 V_{DS}=200V V_D=100V	 V_{DS}=500V V_D=250V	 -Intermediate Design Method
3	 V_{DS}=250V V_D=83V	 V_{DS}=550V V_D=183V	-Voltage applied to switch device is high -Effective current in switching device and primary winding is high -Voltage applied to rectifier diode is low -Output voltage ripple is large -Control must be done through long turn-on time

Figure 18. The current and voltage ratings required on the primary side switching device and the secondary side rectifier diode depend on the turns ratio (n) selected.

4.3.2.3 Designer's choice

As is clear from the above discussion, DCM operation can be advantageous, in terms of cost and efficiency, if the input is small and it is required to precisely control the input power through the primary side switch (MOSFET) current. On the other hand, for large inputs and where switching turn on loss could be a major problem, a CCM design would be more advantageous. In conclusion, therefore, the system designer must decide between the two modes according to which mode best fits the characteristics of the system being designed.

5. The Transformer

5.1 Why a transformer is needed

There are three reasons for needing a transformer in a power conversion circuit. The first reason is safety. A transformer affords electrical isolation between the primary and secondary sides, as shown in Figure 19a. In addition, a true ground on the output side helps prevent electric shock. The second reason is for voltage conversion. For example, if a dc/dc converter (such as the buck converter shown in Figure 19b) switching at 50kHz is used to obtain 5V from 100V. The duty cycle would only be 5%. Using a 50kHz switching frequency, the control circuit may have only about 1µs to act, which is not an easy task. Even if this were possible, the internal voltage and current for each element would be very large reducing efficiency. The problem is aggravated at high output current. In the above example, using a transformer to lower the voltage to 10V would then allowing an on time of about 10µs. This is an advantageous strategy for lowering cost and raising efficiency. The third reason to use a transformer has to do with high voltages and voltage fluctuations. For example, even though all control for a 1000V supply is done at the 5V power source on the GND side, a transformer is necessary if power is needed for current sensing at the 1000V output terminal or for other control. If the isolation voltage between the transformer windings is sufficient, a 1000V potential difference can be safely maintained between the primary and secondary windings and power can be delivered. Further, a transformer is also required when the power GND has a sudden potential fluctuation as in a half bridge converter, gate drive power source.

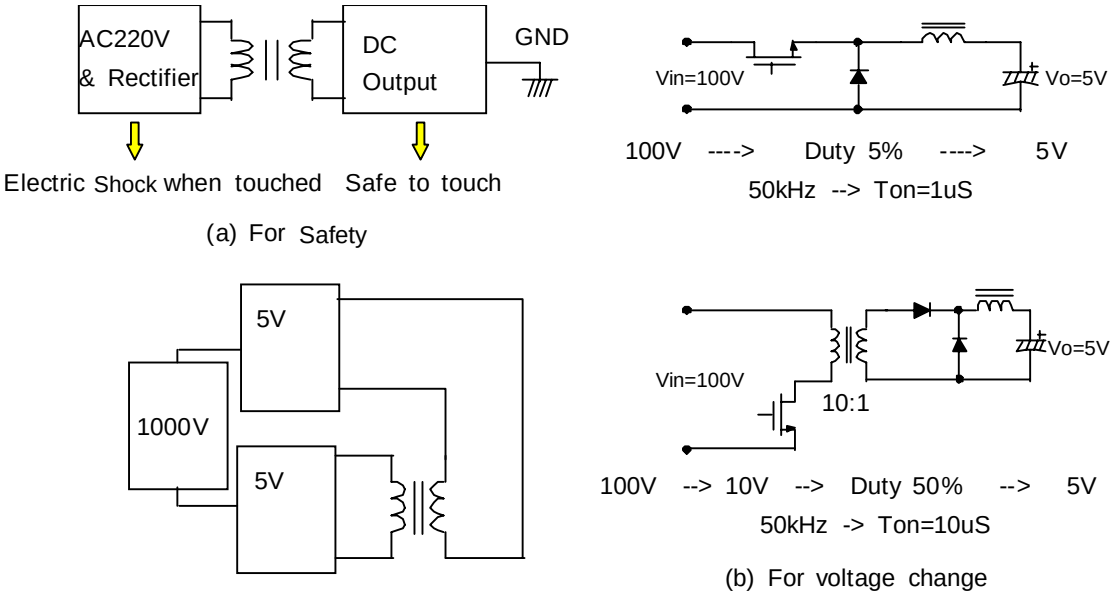
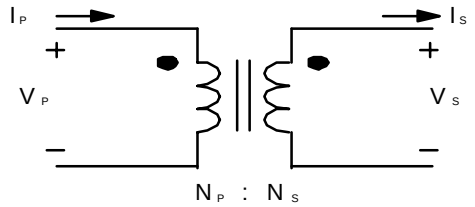


Figure 19. Why a transformer is needed.

5.2 The ideal transformer

The transformer is a device that uses inductive coupling between its windings to deliver power or signals from one winding to the another. This is usually from the primary winding to the secondary winding. The voltages across the windings can be raised or lowered with respect to each other, and, if necessary, the primary and secondary sides can be isolated from each other. Figure 20 shows an ideal transformer, a simplistic model useful in describing the transformer concept. An ideal transformer which is actually a fictional concept must satisfy the following three conditions:

1. The coupling coefficient between the windings is unity (i.e., the leakage flux is zero);
2. The coil loss is zero (the device has no losses).
3. The inductance of each coil is infinite.



$V_P : V_S = N_P : N_S$

$I_P : I_S = N_S : N_P$

Figure 20. Ideal transformer.

The input to output voltage ratio of an ideal transformer is directly proportional to the turns ratio. This is the ratio of the number of turns on the primary winding to the turns on the secondary. The polarity is represented schematically by the placement of a dot on each winding. Since $n = V_p/V_s$, and an ideal transformer has no loss, the current ratio is inversely proportional to the turns ratio. The current direction is such that it enters on one side and leaves at another. Thus the sum of all the nI that flow into the dot is zero. The dot, indicating the winding polarity, is placed to make the flux direction in the transformer core uniform when current flows into the dot. Furthermore, in the case of an ideal transformer, if the path on the secondary side windings is opened, there is no secondary current flow, and the current on the primary side also goes to zero.

5.3 The Real transformer

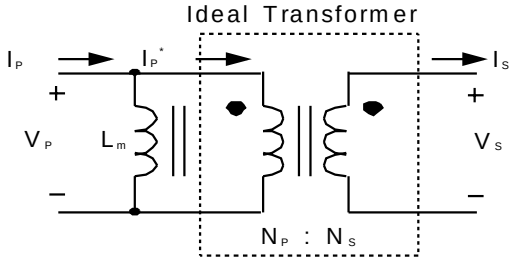
Significant differences exist between an ideal transformer and a real one. In a real transformer:

1. The coupling coefficient between each coil is finite, and when a gap is placed in the core as is done in many power transformers, the coupling coefficient becomes still smaller (i.e., there is leakage flux);

2. There are losses, such as iron (hysteresis) loss, eddy current loss, coil resistance loss, etc.; and,

3. The inductance of each coil is finite. When a gap is placed in the core the inductance becomes still smaller.

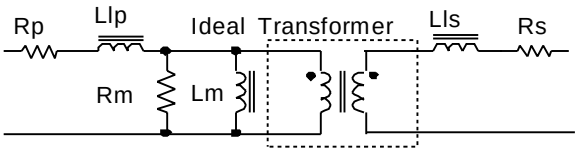
In a real transformer, should the secondary side be opened current would continue to flow in the primary (as in 3, above). So, while energy cannot be stored in the ideal transformer, it is stored in a real transformer. The so-called magnetizing inductance accounts for this energy storage phenomenon. The circuit of Figure 21 is a simplistic view of an actual transformer and shows the magnetizing inductance. Figure 22 presents a more complete equivalent circuit of a real transformer, showing inductances and loss resistances.



$V_P : V_S = N_P : N_S$

$I_P^* : I_S = N_S : N_P$

Figure 21. A model of an actual transformer showing the magnetizing inductance L_m, which accounts for energy storage.



- Rp:Primary side winding resistance
- Rs:Secondary side winding resistance
- Llp:Primary side leakage inductance
- Lls:Secondary side leakage inductance
- Lm:Magnetizing inductance
- Rm:Transformer core loss resistance

Figure 22. A more complete equivalent circuit of an actual transformer, showing inductances and loss resistances.

6. Transformer Design

6.1 Core selection

The maximum power that a transformer core can deliver and the maximum energy a transformer inductor can store depends on the shape and size of the core. In general, as the effective cross sectional area (Ae) increases, more power can be delivered. Also, as the window area (Aw) on which the coils are wound increases, more and thicker windings can be used, allowing a further increase in the power that can be delivered. The product of Aw and Ae is called the area product, AP, and the maximum power a transformer can deliver is proportional to an exponential power of AP. Indeed, recent transformer theory shows designs depending almost entirely on AP. In the broader view, a flyback converter transformer can be viewed as a coupled inductor, so

it's common to design a flyback transformer using inductor design methods. The two equations below, (a) and (b), represent two ways to calculate AP. Equation (a) below, is a method based on whether or not the core is saturated, is appropriate at low operating frequencies. Equation (b), limited by core loss, is appropriate at high frequencies. For any given design, it is necessary to calculate AP using both equations, and the equation that gives the higher value is the one that must be considered correct. Equation (a) assumes that all losses are wire losses and ignores the core (iron) loss.

$$AP = \left(\frac{LI_P I_{RMS} 10^4}{420 K B_{MAX}}\right)^{1.31} [cm^2] \qquad a)$$

L = Inductance of Transformer
Ip = Operating peak current
Bmax = MAximum operating flux density
Irms = RMS current

L and B_{MAX} are in Henries and Tesla units, respectively, and K is listed in Table 1, below. From the above equation the current density (J) per unit area of wire is obtained from the current by the relationship below, which assumes that the temperature of the inductor's "hot spot" is 30°C above ambient.

$$J_{30} = 420\ AP^{-0.24}\ [A/cm^2]$$

At any operating frequency high enough so that the core losses become large, the following equation should be used. Specifically, it assumes that the total transformer losses are split equally (50/50) between the wire and the core.

$$AP = \left(\frac{L\Delta I_m I_{RMS} 10^4}{130K}\right)^{1.58} (K_H f_{SW} + K_E (f_{sw})^2)^{0.66} [cm^2] \qquad b)$$

L = Inductance of Transformer
Ip = Operating peak current
Irms = RMS current

In equation (b), K_H is the hysteresis coefficient (typically 4×10^{-5} for ferrite cores) and K_E is the eddy current coefficient (typically 4×10^{-10} for ferrite cores). The current density relationship here, represented by the equation for J_{30}, below, assumes a hot spot temperature of 15°C above ambient, with the iron loss adding on an additional 15°C (again, a total of 30°C above ambient).

$$J_{30} = 297 AP^{-0.24}\ [A/cm^2]$$

The parameter K in equation (a) is the product of the window utilization factor K_U with the primary area factor K_P. (See Table 1.) K_U is the ratio of the cross sectional area of the winding's copper to the entire window area, and it is significant in setting the isolation between the primary and secondary sides. Because it is related to the transformer shape and winding method, the designer should know the value of K_U for the transformer usually used. The value of K_U can vary greatly, depending particularly on how closely the isolation safety standards (re isolation) are followed; the K_U of Table 1 assumes a general bobbin is used. K_P is the ratio of the area of the primary winding to that of the total winding. In Table 1, it is unity for the inductors because a buck boost inductor has no secondary windings. For the flyback transformer coupled inductor, K_P is usually 0.5, as Table 1 shows; such an inductor has the highest efficiency when the primary and secondary winding areas are equal. When there are more secondary windings, however, the K_P for a flyback transformer coupled inductor can be lower than 0.5. Note that the ease and speed of obtaining an accurate AP from equations (a) and (b) depends on the designer's experience. A reasonably good knowledge of the probable values of the three parameters K_U, K_P, and J for the flyback transformer being designed will reduce the number of trial and error attempts necessary.

Table 1. K_U, K_P, and *K*

	K_U	K_P	$K = K_U K_P$
CCM Buck, Boost Inductor	0.7	1.0	0.7
DCM Buck, Boost Inductor	0.7	1.0	0.7
CCM Flyback Transformer	0.4	0.5	0.2
DCM Flyback Transformer	0.4	0.5	0.2

6.2 Determination of the number of turns

Although the equation for the minimum number of flyback transformer turns can be determined using applied voltage and maximum turn on time, the equations used here are derived from the relationship between L and I_P. For an AP determined from equation (a), above, calculate N_{MIN} using the following equations:

$$N_{MIN} = \frac{LI_P}{B_{MAX}A_C}10^4$$

L = Inductance of Transformer
Ip = Operating peak current
Bmax = Maximum operating flux density
Ae = Effective cross-sectional area of core

For an AP determined from equation (b), above, calculate N_{MIN} using the following equations:

$$N_{MIN} = \frac{L\Delta I_m}{\Delta B_m A_C}10^4$$

L = Inductance of Transformer
Ip = Operating peak current
Bmax = Maximum operating flux density
Ae = Effective cross-sectional area of core

6.3 The windings

The cross sectional area of the winding must be obtained from the calculated effective current and the current density (from the appropriate equation above), factoring in the number of turns (as determined from a calculation of NMIN). If eddy current loss is not a serious problem simply divide the effective current by the current density, thereby determining the coil cross sectional area. Be aware, however, that as the coil becomes thicker, the problem of eddy current loss will arise. Using twisted thin coil strands (Litz wire), instead of a single heavy wire, can reduce the eddy current loss, but K_U will become smaller.

6.4 Determination of the gap

It is not easy to precisely calculate the required gap. However, the gap can be calculated from the following equation. It is based on the fringing effect of the surrounding flux. Note that the calculated value of L is usually larger than required.

$$l_g = \frac{u_O u_r N^2 A_C}{L}10^{-2}[cm]$$

Uo = Permeability of free space
Ur = Relative permeability

Therefore, the gap must be changed to obtain the required value of L.

References

1. Transformer and Inductor Design Handbook. 2nd ed. Col. Wm. T. McLyman. Marcel Dekker, Inc., 1988.

2. Switch Mode Power Supply Handbook. Keith H. Billings. McGraw-Hill, Inc., 1989.