

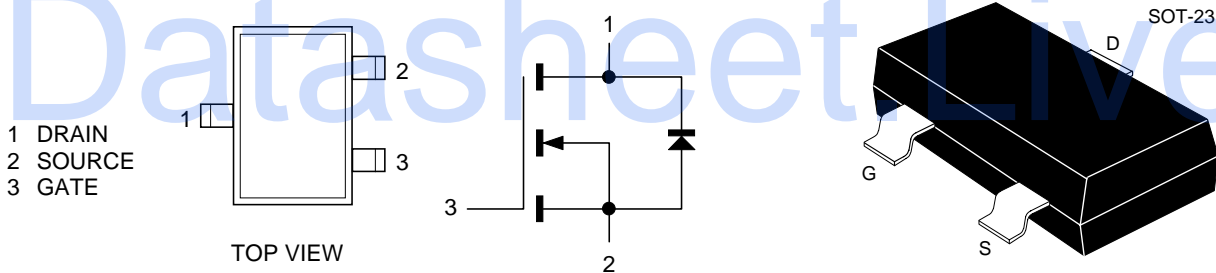
DESCRIPTION

Calogic's 2N7002 device type is a vertical DMOS FET transistor housed in a surface mount SOT-23 for micro-assembly applications. The device is an excellent choice for switching applications where breakdown (B_V) and low on-resistance are important.

ORDERING INFORMATION

Part	Package	Temperature Range
2N7002	Plastic SOT-23 Package	-55°C to +150°C
X2N7002	Sorted Chips in Carriers	-55°C to +150°C

PIN CONFIGURATION



CD5

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	7.5	0.115

PRODUCT MARKING	
2N7002	V02

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETERS	LIMITS	UNITS	TEST CONDITIONS
V_{DS}	Drain-Source Voltage	60	V	
V_{GS}	Gate-Source Voltage	± 40		
I_D	Continuous Drain Current	0.115	A	$T_A = 25^\circ\text{C}$
		0.073		$T_A = 100^\circ\text{C}$
I_{DM}	Pulsed Drain Current ¹	0.8		
P_D	Power Dissipation	200	mW	$T_A = 25^\circ\text{C}$
		80		$T_A = 100^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$	
T_{stg}	Storage Temperature Range	-55 to 150		
T_L	Lead Temperature (1/16" from case for 10 sec.)	300		

THERMAL RESISTANCE RATINGS

SYMBOL	THERMAL RESISTANCE	LIMITS	UNITS
R_{thJA}	Junction-to-Ambient	625	K/W

NOTE: 1. Pulse width limited by maximum junction temperature.

SPECIFICATIONS¹

SYMBOL	PARAMETER	MIN	TYP ²	MAX	UNIT	TEST CONDITIONS	
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	70		V	$I_D = 10\mu\text{A}$, $V_{GS} = 0\text{V}$	
$V_{GS(th)}$	Gate-Threshold Voltage	1	1.9	2.5		$V_{DS} = V_{GS}$, $I_D = 0.25\text{mA}$	
I_{GSS}	Gate-Body Leakage			± 100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	
I_{DSS}	Zero Gate Voltage Drain Current			1	μA	$V_{DS} = 60\text{V}$, $V_{GS} = 0\text{V}$ $T_C = 125^\circ\text{C}$	
				500			
$I_{D(ON)}$	On-State Drain Current ³	500	1000		mA	$V_{DS} = \geq 2V_{DS(ON)}$, $V_{GS} = 10\text{V}$	
$r_{DS(ON)}$	Drain-Source On-Resistance ³		5	7.5	Ω	$V_{GS} = 5\text{V}$, $I_D = 50\text{mA}$ $T_C = 125^\circ\text{C}$	
				9			13.5
			2.5	7.5			$V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ $T_C = 125^\circ\text{C}$
$V_{DS(ON)}$	Drain-Source On-Voltage ³		0.25	0.375	V	$V_{GS} = 5\text{V}$, $I_D = 50\text{mA}$ $V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$ $T_C = 125^\circ\text{C}$ ⁴	
				1.25			3.75
				2.2			6.75
g_{FS}	Forward Transconductance ³	80	170		mS	$V_{DS} = 10\text{V}$, $I_D = 0.2\text{A}$	
g_{OS}	Common Source Output Conductance ^{3,4}		500		μS	$V_{DS} = 5\text{V}$, $I_D = 50\text{mA}$	
DYNAMIC							
C_{iss}	Input Capacitance		16	50	pF	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	
C_{oss}	Output Capacitance ⁴		11	25			
C_{rss}	Reverse Transfer Capacitance		2	5			
SWITCHING							
t_{ON}	Turn-On Time		7	20	nS	$V_{DD} = 30\text{V}$, $R_L = 150\Omega$, $I_D = 0.2\text{A}$ $V_{GEN} = 10\text{V}$, $R_G = 25\Omega$ (Switching time is essentially independent of operating temperature)	
t_{OFF}	Turn-Off Time		7	20			

- NOTES: 1. $T_A = 25^\circ\text{C}$ unless otherwise specified.
 2. For design aid only, not subject to production testing.
 3. Pulse test; $PW = \leq 80\mu\text{s}$, duty cycle $\leq 1\%$.
 4. This parameter not registered with JEDEC.