



IP Core Generator: Constant

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Variable Width of Output Vectors
- Constant Value
- Binary, Octal, Decimal or Hexadecimal Radix Value

Constant

A Constant can be generated with the specified values. Note that this generator has to be run with the “Hard Macro” option deselected, since constants should be implemented as soft macros so that the mapper can “fold” them in with other logic in the design.

Parameters

Parameter	Value	Explanation
Width	Integer > 0	Width of output vector
Constant Value	Integer ≥ 0	Value of the constant
Radix	Binary	Constant value is specified using binary representation
	Octal	Value is octal
	Decimal	Value is decimal
	Hex	Value is hexadecimal

Pins

Type	Name	Option	Explanation
Out	RESULT[Width - 1:0]	No	Constant value, if Width is not large enough, least significant bits of value will be used

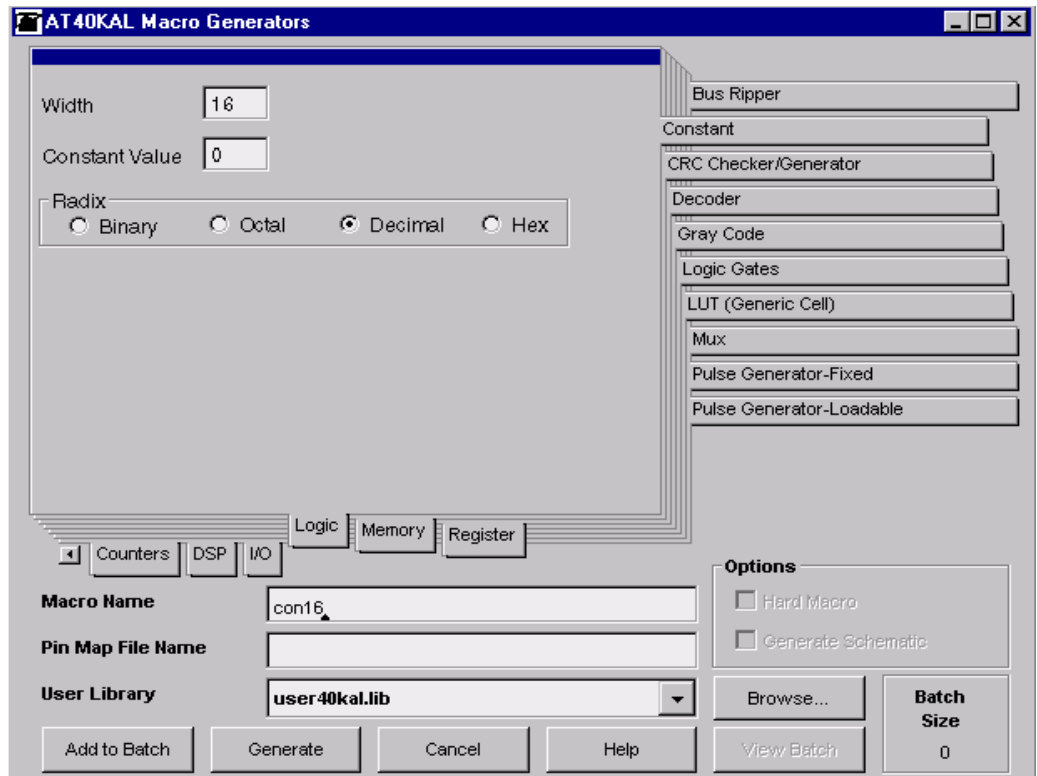
Figure 1 shows an example of the con16 macro options.

Programmable
SLI
AT40K
AT40KAL
AT94K

Application
Note



Figure 1. Constant Generator





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