
EM78468

**8-Bit
Microcontroller**

Product Specification

DOC. VERSION 1.3

ELAN MICROELECTRONICS CORP.


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Specification Revision History

| Doc. Version | Revision Description | Date |
|--------------|---|------------|
| 1.0 | Initial version | 2005/03/02 |
| 1.1 | 1. Added 64-pin LQFP Package | 2005/04/11 |
| 1.2 | 1. Modified the General Description, Features and Pin Assignment. 2. Modified the Functional Block Diagram. 3. Added Appendix C Quality Assurance and Reliability 4. Deleted the 64- pin QFP package | 2007/01/24 |
| 1.3 | 1. Working Voltage adjusted from 2.1V to 1.9V | 2007/08/30 |

1 General Description

The EM78468 is an 8-bit RISC type microprocessor designed and developed with low-power and high-speed CMOS technology. Integrated onto a single chip are on-chip Watchdog Timer (WDT), Data RAM, ROM, programmable real time clock counter, internal/external interrupt, power-down mode, LCD driver, infrared transmitter function, and tri-state I/O. Seven Code option bits are available to meet user's requirements.

2 Features

- CPU configuration
 - 4K×13 bits Mask-ROM
 - 144 bytes general purpose register
 - 128 bytes on-chip data RAM
 - 272 bytes SRAM
 - 8 level stacks for subroutine nesting
 - I/O port configuration
 - Typically, 12 bi-directional tri-state I/O ports.
 - 16 bi-directional tri-state I/O ports shared with LCD segment output pin.
 - Up to 28 bi-directional tri-state I/O ports
 - Operating voltage and temperature range:
 - Commercial: 1.9V ~ 5.5 V (at 0°C~+70°C)
 - Operating mode:
 - Normal mode: CPU is operated on main oscillator frequency (Fm)
 - Green mode: The CPU is operated on sub-oscillator frequency (Fs) and main oscillator (Fm) is stopped
 - Idle mode: CPU idle, LCD display remains working
 - Sleep mode: The whole chip stops working
 - ◆ Input port wake-up function (Port 6, Port 8). Works on Idle and Sleep mode.
 - ◆ Operation speed: DC ~ 10MHz clock input
 - ◆ Dual clock operation
 - Oscillation mode
 - High frequency oscillator can select among Crystal, RC, or PLL (phase-locked loop)
 - Low frequency oscillator can select between Crystal or RC mode
 - Peripheral configuration
 - 8-bit real time clock/counter (TCC)
 - One infrared transmitter / PWM generator function
 - Four sets of 8 bits auto reload down-count timer can be used as interrupt sources
 - ◆ Counter 1: independent down-count timer
 - ◆ Counter 2, High Pulse Width Timer (HPWT), and Low Pulse Width Timer (LPWT) shared with IR function.
 - ◆ Programmable free running on-chip watchdog timer (WDT). This function can operate on Normal, Green and Idle modes.
 - Eight interrupt sources: three external and five internal
 - Internal interrupt source: TCC; Counters 1, 2; High/Low pulse width timer.
 - External interrupt source: INT0, INT1 and Pin change wake-up (Port 6 and Port 8)
 - LCD Circuit
 - Common driver pins: 4
 - Segment driver pins: 32
 - LCD Bias: 1/3, 1/2 bias
 - LCD Duty: 1/4, 1/3, 1/2 duty
 - Package type:
 - Dice form: 59 pins
 - LQFP-64 pin: EM78468AQS/J (Body 7mm × 7mm)
 - LQFP-44 pin: EM78468BQS/J (Body 10mm × 10mm)
- Note:** Green products do not contain hazardous substances

3 Pin Assignment

(1) 44-Pin LQFP

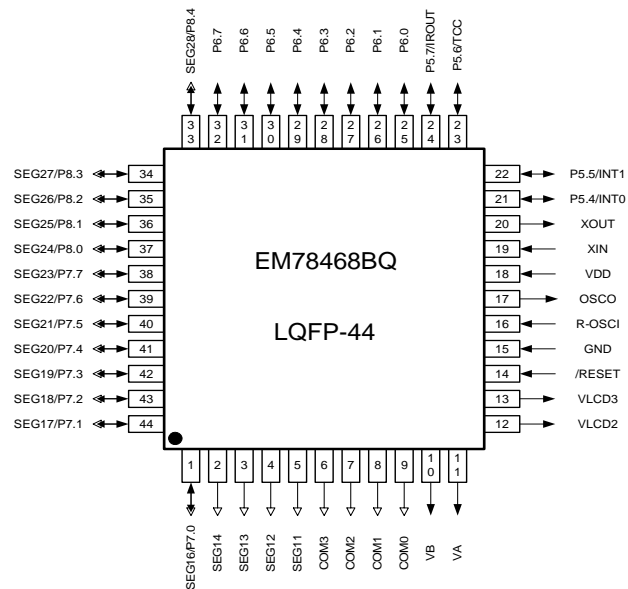


Fig. 3-1 44-pin LQFP

(2) 64-Pin LQFP

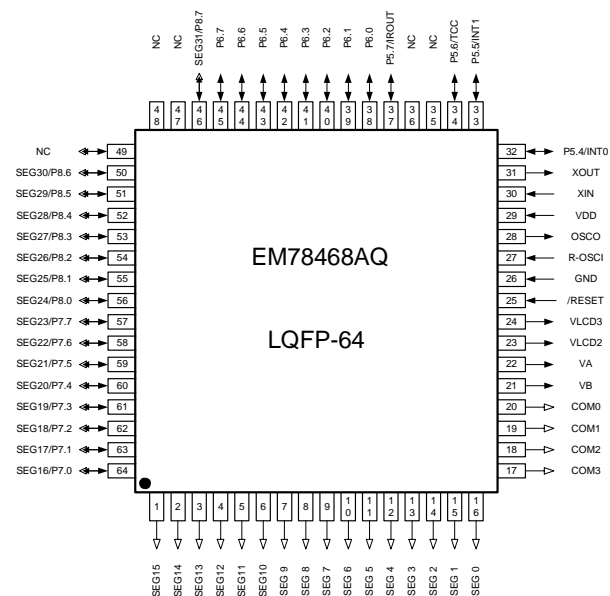
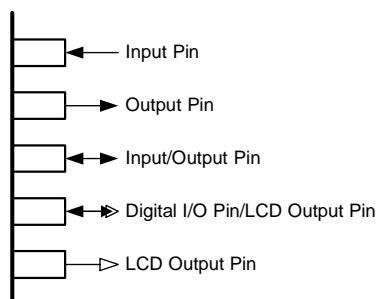


Fig. 3-2 64-pin LQFP



4 Block Diagram

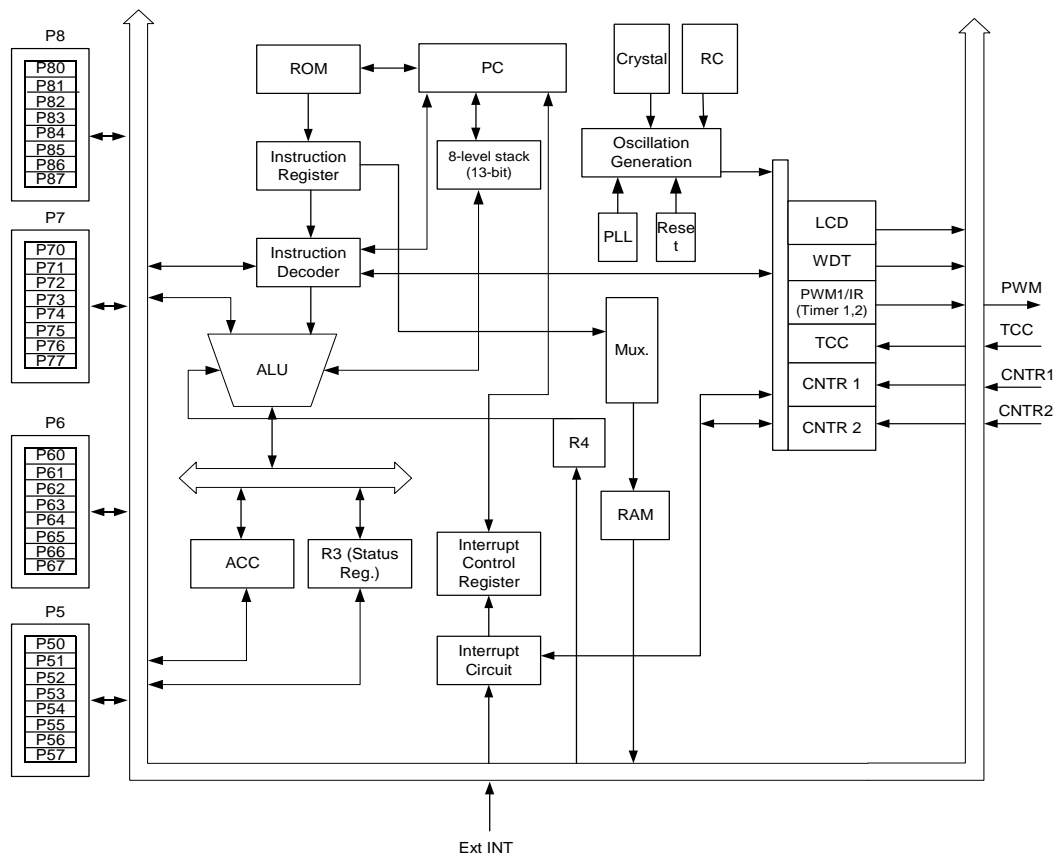


Fig. 4-1 System Block Diagram

5 Pin Description

Table 1 (a) Pin Description for Package of LQFP64

| Symbol | Pin No. | Type | Function |
|---|---------------------|---------|---|
| P5.4/INT0 | 32 | I/O | 1-bit General purpose input/output pin/external interrupt. INT0 interrupt source can be set to falling or rising edge by IOC71 register Bit 7 (INT_EDGE). Wakes up from sleep mode and idle mode when the pin status changes. |
| P5.5/INT1 | 33 | I/O | 1-bit General purpose input/output pin/external interrupt. Interrupt source is a falling edge signal. Wakes up from sleep mode and idle mode when the pin status changes. |
| P5.6/TCC | 34 | I/O | 1-bit General purpose input/output pin/external counter input. This pin works in normal/green/idle mode. |
| P5.7/IROUT | 37 | I/O | 1-bit General purpose input/output pin/IR/PWM mode output pin. This pin is capable of sinking 20mA/5V. |
| P6.0~P6.7 | 38~45 | I/O | 8-bit General purpose input/output pins. Pull-high, pull-low and open drain function supported. All pins can wake up from sleep and idle modes when the pin status changes |
| COM3~0 | 17~20 | O | LCD common output pin. |
| SEG0~SEG15 | 16~1 | O | LCD segment output pin. |
| SEG16/P7.0 ~ SEG23/P7.7 | 64 ~ 57 | O/(I/O) | LCD segment output pin. Can be shared with general purpose I/O pin |
| SEG24/P8.0 ~ SEG30/P8.6 SEG31/P8.7 | 56 ~ 50 46 | O/(I/O) | LCD segment output pin. Can be shared with general I/O pin. For general purpose I/O use, can wake up from sleep mode and idle mode when the pin status changes. For general purpose I/O use, supports pull-high function. |
| VB | 21 | O | Connect capacitors for LCD bias voltage. |
| VA | 22 | O | Connect capacitors for LCD bias voltage. |
| VLCD2 | 23 | O | One of LCD bias voltage. |
| VLCD3 | 24 | O | One of LCD bias voltage. |
| /RESET | 25 | I | General-purpose Input only Low active. If it remains at logic low, the device will be reset. |
| R-OSCI | 27 | I | In Crystal mode: crystal input In RC mode: pull-highresistor In PLL mode: connect 0.01μF capacitance to GND Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not use |
| OSCO | 28 | O | In Crystal mode: crystal input In RC mode: instruction clock output |
| Xin | 30 | I | In Crystal mode: Input pin for sub-oscillator. Connect to a 32.768kHz crystal. |
| Xout | 31 | o | In Crystal mode: Connect to a 32.768kHz crystal. In RC mode: instruction clock output |
| NC | 35~36 47~49 | | No connection |
| VDD | 29 | I | Power supply |
| GND | 26 | I | System ground pin |

Table 1 (b) Pin Description for Package of LQFP44

| Symbol | Pin No. | Type | Function |
|---|--------------------|---------|---|
| P5.4/INT0 | 21 | I/O | 1-bit General purpose input/output pin/external interrupt. The INT0 interrupt source can be set to falling or rising edge by IOC71 register Bit 7 (INT_EDGE). Wakes up from sleep mode and idle mode when the pin status changes. |
| P5.5/INT1 | 22 | I/O | 1-bit General purpose input/output pin/external interrupt. The Interrupt source is a falling edge signal. Wakes up from sleep mode and idle mode when the pin status changes. |
| P5.6/TCC | 23 | I/O | 1-bit General purpose input/output pin/external counter input. This pin works in normal/green/idle mode. |
| P5.7/IROUT | 24 | I/O | 1-bit General purpose input/output pin/IR/PWM mode output pin This pin is capable of sinking 18mA/5V. |
| P6.0~P6.7 | 25~32 | I/O | 8-bit General purpose input/output pins Pull-high, pull-low and open drain function supported. All pins can wake up from sleep and idle modes when the pin status changes. |
| COM3~0 | 6~9 | O | LCD common output pin. |
| SEG11~SEG14 | 5~2 | O | LCD segment output pin. |
| SEG16/P7.0 SEG17/P7.1 ~ SEG23/P7.7 | 1 44 ~ 38 | O/(I/O) | LCD segment output pin. Can be shared with general purpose I/O pin |
| SEG24/P8.0 ~ SEG31/P8.4 | 37 ~ 33 | O/(I/O) | LCD segment output pin. Can be shared with general I/O pin For general purpose I/O use, can wake up from sleep mode and idle mode when the pin status changes. For general purposes I/O use, supports pull-high function. |
| VB | 10 | O | Connect capacitors for LCD bias voltage. |
| VA | 11 | O | Connect capacitors for LCD bias voltage. |
| VLCD2 | 12 | O | One of LCD bias voltage. |
| VLCD3 | 13 | O | One of LCD bias voltage. |
| /RESET | 14 | I | General-purpose Input only Low active. If it remains at logic low, the device will be reset. |
| R-OSCI | 16 | I | In Crystal mode: crystal input In RC mode: pull-high resistor In PLL mode: connect 0.01μF capacitance to GND Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not use |
| OSCO | 17 | O | In Crystal mode: crystal input In RC mode: instruction clock output |
| Xin | 19 | I | In Crystal mode: Input pin for sub-oscillator. Connect to a 32.768kHz crystal. |
| Xout | 20 | O | In Crystal mode: Connect to a 32.768kHz crystal. In RC mode: instruction clock output |
| VDD | 18 | I | Power supply |
| GND | 15 | I | System ground pin |

6 Function Description

6.1 Operational Registers

6.1.1 R0/IAR (*Indirect Addressing Register*)

(Address: 00h)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a register, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1/TCC (*Timer Clock Counter*)

(Address: 01h)

Incremented by an external signal edge applied to TCC, or by the instruction cycle clock.

Written and read by the program as any other register.

6.1.3 R2/PC (*Program Counter*)

(Address: 02h)

- The structure of R2 is depicted in Fig. 6-1, *Program Counter Organization*.
- The configuration structure generates 4K×13 bits on-chip ROM addresses to the relative programming instruction codes.
- The contents of R2 are all set to "0"s when a Reset condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to jump to any location within a page.
- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of the stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- The most significant bits (A10~A11) will be loaded with the content of PS0~PS1 in the Status register (R3) upon execution of a "JMP" or "CALL" instruction.

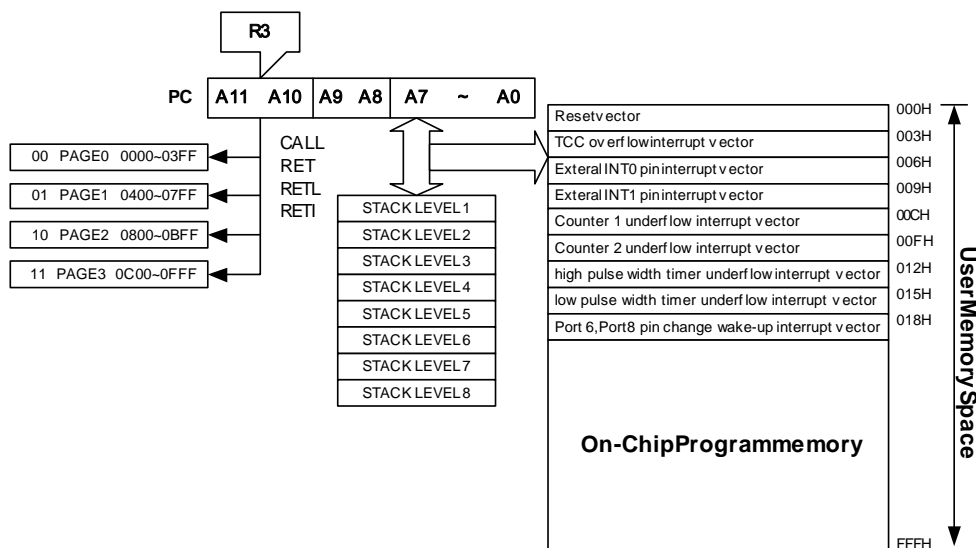


Fig. 6-1 Program Counter Organization

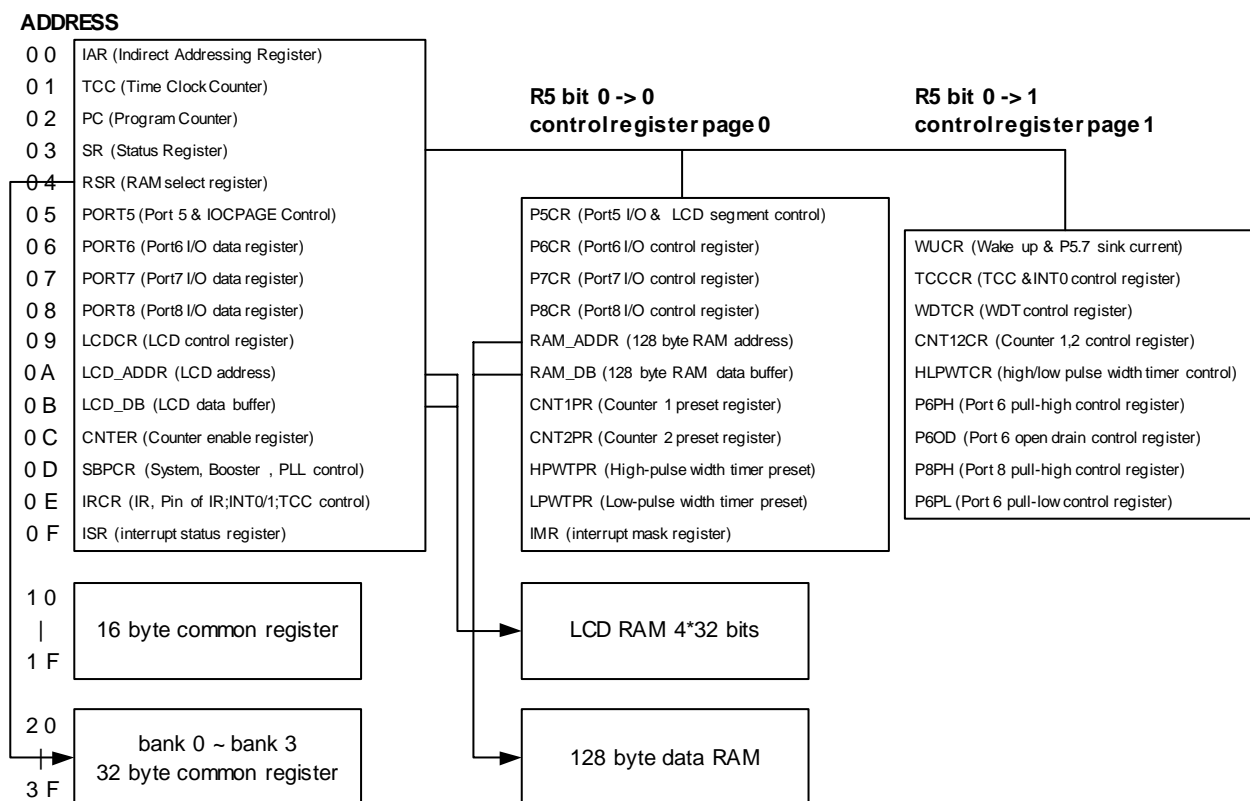


Fig. 6-2 Data Memory Configuration

6.1.4 R3/SR (Status Register)

(Address: 03h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | PS1 | PS0 | T | P | Z | DC | C |

Bit 7: Not used

Bits 6 ~ 5 (PS1 ~ 0): Page select bits

| PS1 | PS0 | ROM Page (Address) |
|-----|-----|----------------------|
| 0 | 0 | Page 0 (000H ~ 3FFH) |
| 0 | 1 | Page 1 (400H ~ 7FFH) |
| 1 | 0 | Page 2 (800H ~ BFFH) |
| 1 | 1 | Page 3 (C00H ~ FFFH) |

PS0~PS1 are used to select a ROM page. User can use the PAGE instruction (e.g. PAGE 1) or set PS1~PS0 bits to change the ROM page. When executing a "JMP", "CALL", or other instructions which causes the program counter to be changed (e.g. MOV R2, A), PS0~PS1 are loaded into the 11th and 12th bits of the program counter where it selects one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0~PS1 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power up and reset to 0 by WDT timeout.

| Event | T | P | Remark |
|-------------------------------|---|---|---------------|
| WDT wake up from sleep mode | 0 | 0 | – |
| WDT time out (not sleep mode) | 0 | 1 | – |
| /RESET wake up from sleep | 1 | 0 | – |
| Power up | 1 | 1 | – |
| Low pulse on /RESET | 1 | 1 | ×: don't care |

Bit 3 (P): Power down bit. Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4/RSR (RAM Select Register)

(Address: 04h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| RBS1 | RBS0 | RSR5 | RSR4 | RSR3 | RSR2 | RSR1 | RSR0 |

Bits 7 ~ 6 (RBS1 ~ RBS0): determine which bank is activated among the four banks.
 See the data memory configuration in Fig. 6-2. Use the BANK instruction (e.g. BABK 1) to change banks.

Bits 5 ~ 0 (RSR5 ~ RSR0): used to select up to 64 registers (Address: 00~3F) in indirect addressing mode. If no indirect addressing is used, the RSR can be used as an 8-bit general purpose read/writer register.

6.1.6 R5/Port 5 (Port 5 I/O Data and Page of Register Select)

(Address: 05h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|---------|
| R57 | R56 | R55 | R54 | – | – | – | IOCPAGE |

Bits 7~4: 4-bits I/O registers of Port 5

User can use the IOC50 register to define each bit either as input or output.

Bits 3~1: Not used

Bit 0 (IOCPAGE): change IOC5 ~ IOC F to another page

IOCPAGE = “0” : Page 0 (select register of IOC 50 to IOC F0)

IOCPAGE = “1” : Page 1 (select register of IOC 61 to IOC E1)

6.1.7 R6/Port 6 (Port 6 I/O Data Register)

(Address: 06h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R67 | R66 | R65 | R64 | R63 | R62 | R61 | R60 |

Bits 7~0: 8-bit I/O registers of Port 6

User can use the IOC60 register to define each bit either as input or output.

6.1.8 R7/Port 7 (Port 7 I/O Data Register)

(Address: 07h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R77 | R76 | R75 | R74 | R73 | R72 | R71 | R70 |

Bits 7~0: 8-bit I/O registers of Port 7

User can use the IOC70 register to define each bit either as input or output.

6.1.9 R8/Port 8 (Port 8 I/O Data Register)

(Address: 08h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R87 | R86 | R85 | R84 | R83 | R82 | R81 | R80 |

Bits 7~0: 8-bit I/O registers of Port 8

User can use IOC80 register to define each bit either as input or output.

6.1.10 R9/LCDCR (LCD Control Register)

(Address: 09h)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|----------|-------|-------|
| BS | DS1 | DS0 | LCDEN | -- | LCDDTYPE | LCDF1 | LCDF0 |

Bit 7 (BS): LCD bias select bit,

BS = "0": 1/2 bias

BS = "1": 1/3 bias

Bits 6 ~ 5 (DS1 ~ DS0): LCD duty select

| DS1 | DS0 | LCD Duty |
|-----|-----|----------|
| 0 | 0 | 1/2 duty |
| 0 | 1 | 1/3 duty |
| 1 | × | 1/4 duty |

Bit 4 (LCDEN): LCD enable bit

LCDEN = "0": LCD circuit disabled. All common/segment outputs are set to ground (GND) level.

LCDEN = "1": LCD circuit enabled.

Bit 3: Not used

Bit 2 (LCDDTYPE): LCD drive waveform type select bit

LCDDTYPE = "0" : A type waveform

LCDDTYPE = "1" : B type waveform

Bits 1 ~ 0 (LCDF1 ~ LCDF0): LCD frame frequency control bits

| LCDF1 | LCDF0 | LCD Frame Frequency (e.g. Fs=32.768kHz) | | |
|-------|-------|---|---------------------------|---------------------------|
| | | 1/2 Duty | 1/3 Duty | 1/4 Duty |
| 0 | 0 | $F_s/(256 \times 2)=64.0$ | $F_s/(172 \times 3)=63.5$ | $F_s/(128 \times 4)=64.0$ |
| 0 | 1 | $F_s/(280 \times 2)=58.5$ | $F_s/(188 \times 3)=58.0$ | $F_s/(140 \times 4)=58.5$ |
| 1 | 0 | $F_s/(304 \times 2)=53.9$ | $F_s/(204 \times 3)=53.5$ | $F_s/(152 \times 4)=53.9$ |
| 1 | 1 | $F_s/(232 \times 2)=70.6$ | $F_s/(156 \times 3)=70.0$ | $F_s/(116 \times 4)=70.6$ |

Note: Fs: sub-oscillator frequency

6.1.11 RA/LCD_ADDR (LCD Address)

(Address: 0Ah)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|--------|--------|--------|
| 0 | 0 | 0 | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |

Bits 7~5: Not used, fixed to "0"

Bits 4~0 (LCDA4 ~ LCDA0): LCD RAM addresses

| RA (LCD Address) | RB (LCD Data Buffer) | | | | | Segment |
|---------------------|----------------------|-------------------|-------------------|-------------------|-------------------|---------|
| | Bits 7 ~4 | Bit 3 (LCD_D3) | Bit 2 (LCD_D2) | Bit 1 (LCD_D1) | Bit 0 (LCD_D0) | |
| 00H | — | — | — | — | — | SEG0 |
| 01H | — | — | — | — | — | SEG1 |
| 02H | — | — | — | — | — | SEG2 |
| | | | | | | |
| 1DH | — | — | — | — | — | SEG29 |
| 1EH | — | — | — | — | — | SEG30 |
| 1FH | — | — | — | — | — | SEG31 |
| Common | X | COM3 | COM2 | COM1 | COM0 | |

6.1.12 RB/LCD_DB (LCD Data Buffer)

(Address: 0Bh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|--------|--------|
| — | — | — | — | LCD_D3 | LCD_D2 | LCD_D1 | LCD_D0 |

Bits 7~4: Not used

Bits 3~0 (LCD_D3 ~ LCD_D0) : LCD RAM data transfer register

6.1.13 RC/CNTER (Counter Enable Register)

(Address: 0Ch)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|--------|--------|
| — | — | — | — | LPWTEN | HPWTEN | CNT2EN | CNT1EN |

Bits 7, 5: Not used, must be fixed to "0"

Bits 6, 4: Not used

Bit 3 (LPWTEN): low pulse width timer enable bit

LPWTEN = "0" : Disable LPWT. Stop counting operation.

LPWTEN = "1" : Enable LPWT. Start counting operation.

Bit 2 (HPWTEN): high pulse width timer enable bit

HPWTEN = "0" : Disable HPWT. Stop counting operation.

HPWTEN = "1" : Enable HPWT. Start counting operation.

Bit 1 (CNT2EN): Counter 2 enable bit

CNT2EN = "0" : Disable Counter 2. Stop counting operation.

CNT2EN = "1" : Enable Counter 2. Start counting operation.

Bit 0 (CNT1EN): Counter 1 enable bit

CNT1EN = "0" : Disable Counter 1. Stop counting operation.

CNT1EN = "1" : Enable Counter 1. Start counting operation.

6.1.14 RD/SBPCR (System, Booster and PLL Control Register)

(Address: 0Dh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | CLK2 | CLK1 | CLK0 | IDLE | BF1 | BF0 | CPUS |

Bit 7: Not used

Bits 6 ~ 4 (CLK2 ~ CLK0): main clock selection bits for PLL mode (code option select)

| CLK2 | CLK1 | CLK0 | Main clock | Example Fs=32.768K |
|------|------|------|------------|--------------------|
| 0 | 0 | 0 | Fs×130 | 4.26 MHz |
| 0 | 0 | 1 | Fs×65 | 2.13 MHz |
| 0 | 1 | 0 | Fs×65/2 | 1.065 MHz |
| 0 | 1 | 1 | Fs×65/4 | 532 kHz |
| 1 | × | × | Fs×244 | 8 MHz |

Bit 3 (IDLE): Idle mode enable bit. This bit will determine the intended mode of the SLEEP instruction.

Idle="0"+SLEEP instruction → Sleep mode

Idle="1"+SLEEP instruction → Idle mode

*** NOP instruction must be added after SLEEP instruction.**

Example : Idle mode : Idle bit = "1" +SLEEP instruction + NOP instruction

Sleep mode : Idle bit = "0" +SLEEP instruction + NOP instruction

Bits 2, 1 (BF1, 0): LCD booster frequency select bit to adjust VLCD 2, 3 driving.

| BF1 | BF0 | Booster Frequency |
|-----|-----|-------------------|
| 0 | 0 | Fs |
| 0 | 1 | Fs/4 |
| 1 | 0 | Fs/8 |
| 1 | 1 | Fs/16 |

Bit 0 (CPUS): CPU oscillator source select, When CPUS=0, the CPU oscillator select sub-oscillator and the main oscillator is stopped.

CPUS = "0": sub-oscillator (Fs)

CPUS = "1": main oscillator (Fm)

CPU Operation Mode

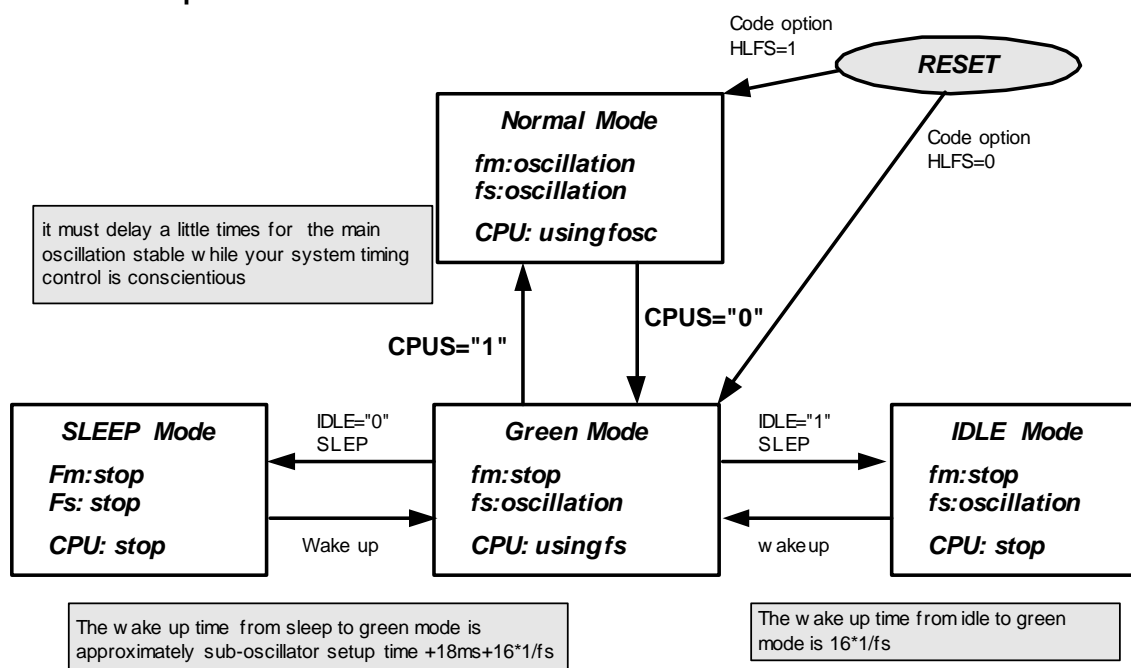


Fig. 6-3 CPU Operation Mode

6.1.15 RE/IRCR (IR and Port 5 Setting Control Register)

(Address: 0Eh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|-------|-------|-------|
| IRE | HF | LGP | — | IROUTE | TCCE | EINT1 | EINT0 |

Bit 7 (IRE): Infrared Remote Enable bit

IRE = "0" : Disable the IR/PWM function. The state of P5.7/IROUT pin is determined by Bit 7 of IOC 50 if it is for IROUT.

IRE = "1" : Enable IR or PWM function.

Bit 6 (HF): High carry frequency

HF = "0" : For PWM application, disable the H/W modulator function. The IROUT waveform is generated according to high-pulse and low-pulse time as determined by the respective high pulse and low pulse width timers. Counter 2 is an independent auto reload timer.

HF = "1" : For IR application mode, enable the H/W modulator function, the low time sections of the generated pulse is modulated with the Fcarrier frequency. The Fcarrier frequency is provided by Counter 2.

Bit 5 (LGP): IROUT for of low pulse width timer

LGP = "0" : The high-pulse width timer register and low-pulse width timer is valid.

LGP = "1" : The high-pulse width timer register is ignored. So the IROUT waveform is dependent on the low-pulse width timer register only.

Bit 4: Not used

Bit 3 (IROUTE): Define the function of P5.7/IROUT pin.

IROUTE = "0" : for bi-directional general I/O pin.

IROUTE = "1" : for IR or PWM output pin, the control bit of P5.7 (Bit 7 of IOC50) must be set to "0"

Bit 2 (TCCE): Define the function of P5.6/TCC pin.

TCCE = "0" : for bi-directional general I/O pin.

TCCE = "1" : for external input pin of TCC, the control bit of P5.6 (Bit 6 of IOC50) must be set to "1"

Bit 1 (EINT1): Define the function of P5.5/INT1 pin.

EINT1 = "0" : for bi-directional general I/O pin.

EINT1 = "1" : for external interrupt pin of INT1, the control bit of P5.5 (Bit 5 of IOC50) must be set to "1"

Bit 0 (EINT0): Define the function of P5.4/INT0 pin.

EINT0 = "0" : for bi-directional general I/O pin.

EINT0 = "1" : for external interrupt pin of INT0, the control bit of P5.4 (Bit 4 of IOC50) must be set to "1"

6.1.16 RF/ISR (Interrupt Status Register)

(Address: 0Fh)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ICIF | LPWTF | HPWTF | CNT2F | CNT1F | INT1F | INT0F | TCIF |

These bits are set to "1" when interrupt occurs respectively.

Bit 7 (ICIF): Port 6, Port 8, input status changed interrupt flag. Set when Port 6, Port 8 input changes.

Bit 6 (LPWTF): interrupt flag of the internal low-pulse width timer underflow.

Bit 5 (HPWTF): interrupt flag of the internal high-pulse width timer underflow.

Bit 4 (CNT2F): interrupt flag of the internal Counter 2 underflow.

Bit 3 (CNT1F): interrupt flag of the internal Counter 1 underflow.

Bit 2 (INT1F): external INT1 pin interrupt flag.

Bit 1 (INT0F): external INT0 pin interrupt flag.

Bit 0 (TCIF): TCC timer overflow interrupt flag. Set when TCC timer overflows.

6.1.17 Address: 10h~3Fh; R10~R3F (General Purpose Register)

R10~R31F and R20~R3F (Banks 0~3) are general purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

* Registers of IOC Page 0 (IOC50 ~ IOCF0, Bit 0 of R5 = "0")

6.2.2 IOC50/P5CR (Port 5 I/O and Ports 7, 8 for LCD Segment Control Register)

(Address: 05h, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC57 | IOC56 | IOC55 | IOC54 | P8HS | P8LS | P7HS | P7LS |

Bits 7~4 (IOC57~54): Port 5 I/O direction control register

IOC5x = "0": set the relative P5.x I/O pins as output

IOC5x = "1": set the relative P5.x I/O pin into high impedance (input pin)

Bit 3 (P8HS): Switch to high nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8.x pins.

P8HS = "0": select high nibble of Port 8 as normal P8.4~P8.7

P8HS = "1": select LCD segment output as SEG 28~SEG 31 output

Bit 2 (P8LS): Switch to low nibble I/O of Port 8 or to LCD segment output while sharing pins with SEGxx/P8.x pins

P8LS = "0": select low nibble of Port 8 as normal P8.0~P8.3

P8LS = "1": select LCD Segment output as SEG 24~SEG 27 output

Bit 1 (P7HS): Switch to high nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7.x pins

P7HS = "0": select high nibble of Port 7 as normal P7.4~P7.7

P7HS = "1": select LCD Segment output as SEG 20~SEG 23 output

Bit 0 (P7LS): Switch to low nibble I/O of Port 7 or to LCD segment output while sharing pins with SEGxx/P7.x pins

P7LS = "0": select low nibble of Port 7 as normal P7.0~P7.3

P7LS = "1": select LCD segment output as SEG 16~SEG 19 output

6.2.3 IOC60/P6CR (Port 6 I/O Control Register)

(Address: 06h, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC67 | IOC66 | IOC65 | IOC64 | IOC63 | IOC62 | IOC61 | IOC60 |

Bit 7 (IOC67)~Bit 0(IOC60): Port 6 I/O direction control register

IOC6x = "0": set the relative Port 6.x I/O pins as output

IOC6x = "1": set the relative Port 6.x I/O pin into high impedance (input pin)

6.2.4 IOC70/P7CR (Port 7 I/O Control Register)

(Address: 07h, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC77 | IOC76 | IOC75 | IOC74 | IOC73 | IOC72 | IOC71 | IOC70 |

Bit 7 (IOC77)~Bit 0 (IOC70): Port 7 I/O direction control register

IOC7x = "0": set the relative Port 7.x I/O pins as output

IOC7x = "1": set the relative Port 7.x I/O pin into high impedance (input pin)

6.2.5 IOC80/P8CR (Port 8 I/O Control Register)

(Address: 08h, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC87 | IOC86 | IOC85 | IOC84 | IOC83 | IOC82 | IOC81 | IOC80 |

Bit 7 (IOC 87)~Bit 0 (IOC 80): Port 8 I/O direction control register

IOC8x = "0": set the relative Port 8.x I/O pins as output

IOC8x = "1": set the relative Port 8.x I/O pin into high impedance (input pin)

6.2.6 IOC90/RAM_ADDR (128 Bytes RAM Address)

(Address: 09h, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--------|--------|--------|--------|--------|--------|--------|
| 0 | RAM_A6 | RAM_A5 | RAM_A4 | RAM_A3 | RAM_A2 | RAM_A1 | RAM_A0 |

Bit 7: Not used, fixed at "0"

Bits 6~0: 128 bytes RAM address

6.2.7 IOCA0/RAM_DB (128 Bytes RAM Data Buffer)

(Address: 0Ah, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| RAM_D7 | RAM_D6 | RAM_D5 | RAM_D4 | RAM_D3 | RAM_D2 | RAM_D1 | RAM_D0 |

Bits 7~0: 128 bytes RAM data transfer register

6.2.8 IOCB0/CNT1PR (Counter 1 Preset Register)

(Address: 0Bh, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Bit 7 ~ Bit 0: These are Counter 1 buffers which user can read and write. Counter 1 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by the IOC91 register. After an interrupt, it will auto reload the preset value.

6.2.9 IOCC0/CNT2PR (Counter 2 Preset Register)

(Address: 0Ch, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Bit 7 ~ Bit 0: These are Counter 2 buffers which user can read and write. Counter 2 is an 8-bit down-count timer with 8-bit prescaler used to preset the counter and read the preset value. The prescaler is set by IOC91 register. After an interrupt, it will reload the preset value.

When IR output is enabled, this control register can obtain carrier frequency output. If the Counter 2 clock source is equal to F_T , then

$$\text{Carrier frequency (F}_{\text{carrier}}) = \frac{F_T}{2 * (\text{preset_value} + 1) * \text{prescaler}}$$

6.2.10 IOCD0/HPWTPR (High-Pulse Width Timer Preset Register)

(Address: 0Dh, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Bit 7 ~ Bit 0: These are high-pulse width timer buffers which user can read and write. High-pulse width timer preset register is an eight-bit down-counter with 8-bit prescaler used as IOCD0 to preset the counter and read the preset value. The prescaler is set by the IOCA1 register. After an interrupt, it will reload the preset value.

For PWM or IR application, this control register is set as high pulse width.

If the high-pulse width timer source clock is F_T , then

$$\text{High pulse time} = \frac{\text{prescaler} * (\text{preset_value} + 1)}{F_T}$$

6.2.11 IOCE0/LPWTPR (Low-Pulse Width Timer Preset Register)

(Address: 0Eh, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |

Bit 7 ~ Bit 0: All are low-pulse width timer buffer that user can read and write.

Low-pulse width timer preset is an eight-bit down-counter with 8-bit prescaler that is used as IOCE0 to preset the counter and read preset value. The prescaler is set by IOCA1 register. After an interrupt, it will reload the preset value.

For PWM or IR application, this control register is set as low pulse width.

If the low-pulse width timer source clock is F_T , then

$$\text{Low pulse time} = \frac{\text{prescaler} * (\text{preset_value} + 1)}{F_T}$$

6.2.12 IOCF0/IMR (Interrupt Mask Register)

(Address: 0Fh, Bit 0 of R5 = "0")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ICIE | LPWTE | HPWTE | CNT2E | CNT1E | INT1E | INT0E | TCIE |

Bit 7~Bit 0: interrupt enable bit. Enable the respective interrupt source.

0: disable interrupt

1: enable interrupt

IOCF0 register is readable and writable.

* Registers of IOC Page 1 (IOC61 ~ IOCE1, Bit 0 of R5 = "1")

6.2.13 IOC61/WUCR (Wake up and Sink Current of P5.7/IROUT Control Register)

(Address: 06h, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|--------|--------|--------|
| IROCS | – | – | – | /WUE8H | /WUE8L | /WUE6H | /WUE6L |

Bit 7: IROCS: IROUT/Port 5.7 output sink current set

| IROCS | P5.7/IROUT Sink Current | |
|-------|-------------------------|--------|
| | VDD=5V | VDD=3V |
| 0 | 9 mA | 6 mA |
| 1 | 18 mA | 12 mA |

Bits 6, 5, 4: Not used

Bit 3 (/WUE8H): 0/1 → enable/disable P8.4~P8.7 pin change wake-up function

Bit 2 (WUE8L): 0/1 → enable/disable P8.0~P8.3 pin change wake-up function

Bit 1 (WUE6H): 0/1 → enable/disable P6.4~P6.7 pin change wake-up function

Bit 0 (WUE6L): 0/1 → enable/disable P6.0~P6.3 pin change wake-up function

*** Port 6 and Port 8 must not be set as input floating when wake-up function is enabled. The initial state of wake-up function is enabled.**

6.2.14 IOC71/TCCCR (TCC Control Register)

(Address: 07h, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|
| INT_EDGE | INT | TS | TE | PSRE | TCCP2 | TCCP1 | TCCP0 |

Bit 7 (INT_EDGE):

INT_EDGE = "0": Interrupt on rising edge of P5.4/INT0 pin

INT_EDGE = "1": Interrupt on falling edge of P5.4/INT0 pin

Bit 6 (INT): INT enable flag, this bit is read only

INT = "0": interrupt masked by DISI or hardware interrupt

INT = "1": interrupt enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

TS = "0": internal instruction cycle clock

TS = "1": transition on TCC pin, TCC period > internal instruction clock period

Bit 4 (TE): TCC signal edge

TE = "0": incremented by TCC pin rising edge

TE = "1": incremented by TCC pin falling edge

Bits 3~0 (PSRE, TCCP2 ~ TCCP0): TCC prescaler bits

| PSRE | TCCP2 | TCCP1 | TCCP0 | TCC Rate |
|------|-------|-------|-------|----------|
| 0 | × | × | × | 1:1 |
| 1 | 0 | 0 | 0 | 1:2 |
| 1 | 0 | 0 | 1 | 1:4 |
| 1 | 0 | 1 | 0 | 1:8 |
| 1 | 0 | 1 | 1 | 1:16 |
| 1 | 1 | 0 | 0 | 1:32 |
| 1 | 1 | 0 | 1 | 1:64 |
| 1 | 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1 | 1:256 |

6.2.15 IOC81/WDTCR (WDT Control Register)

(Address: 08h, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | – | – | – | WDTE | WDTP2 | WDTP1 | WDTP0 |

Bits 7 ~ 4: Not used

Bit 3 (WDTE): Watchdog timer enable. This control bit is used to enable the Watchdog timer,

WDTE = "0": Disable WDT function

WDTE = "1": enable WDT function

Bits 2 ~ 0 (WDTP2 ~ WDTP0): Watchdog Timer prescaler bits. The WDT source clock is sub-oscillation frequency.

| WDTP2 | WDTP1 | WDTP0 | WDT Rate |
|-------|-------|-------|----------|
| 0 | 0 | 0 | 1:1 |
| 0 | 0 | 1 | 1:2 |
| 0 | 1 | 0 | 1:4 |
| 0 | 1 | 1 | 1:8 |
| 1 | 0 | 0 | 1:16 |
| 1 | 0 | 1 | 1:32 |
| 1 | 1 | 0 | 1:64 |
| 1 | 1 | 1 | 1:128 |

6.2.16 IOC91/CNT12CR (Counters 1and 2 Control Register)

(Address: 09h, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--------|--------|--------|-------|--------|--------|--------|
| CNT2S | CNT2P2 | CNT2P1 | CNT2P0 | CNT1S | CNT1P2 | CNT1P1 | CNT1P0 |

Bit 7(CNT2S): Counter 2 clock source select 0/1 → Fs/ Fm*

(*Fs: sub-oscillator clock, Fm: main-oscillator clock)

Bits 6~4 (CNT2P2 ~ CNT2P 0): Counter 2 prescaler select bits

| CNT2P2 | CNT2P1 | CNT1P0 | Counter 2 Scale |
|--------|--------|--------|-----------------|
| 0 | 0 | 0 | 1:2 |
| 0 | 0 | 1 | 1:4 |
| 0 | 1 | 0 | 1:8 |
| 0 | 1 | 1 | 1:16 |
| 1 | 0 | 0 | 1:32 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

Bit 3 (CNT1S): Counter 1 clock source select 0/1 → Fs/ Fm*

Bits 2~0 (CNT1P2 ~ CNT1P0): Counter 1 prescaler select bits

| CNT1P2 | CNT1P1 | CNT1P0 | Counter 1 Scale |
|--------|--------|--------|-----------------|
| 0 | 0 | 0 | 1:2 |
| 0 | 0 | 1 | 1:4 |
| 0 | 1 | 0 | 1:8 |
| 0 | 1 | 1 | 1:16 |
| 1 | 0 | 0 | 1:32 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

6.2.17 IOCA1/HLPWTCR (High/Low Pulse Width Timer Control Register)

(Address: 0Ah, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--------|--------|--------|-------|--------|--------|--------|
| LPWTS | LPWTP2 | LPWTP1 | LPWTP0 | HPWTS | HPWTP2 | HPWTP1 | HPWTP0 |

Bit 7 (LPWTS): low-pulse width timer clock source select 0/1 → Fs/ Fm*

(*Fs: sub-oscillator clock, Fm: main-oscillator clock)

Bits 6~4 (LPWTP2~ LPWTP0): low-pulse width timer prescaler select bits

| LPWTP2 | LPWTP1 | LPWTP0 | Low-pulse Width Timer Scale |
|--------|--------|--------|-----------------------------|
| 0 | 0 | 0 | 1:2 |
| 0 | 0 | 1 | 1:4 |
| 0 | 1 | 0 | 1:8 |
| 0 | 1 | 1 | 1:16 |
| 1 | 0 | 0 | 1:32 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

Bit 3 (HPWTS): high-pulse width timer clock source select 0/1 → Fs/ Fm*

Bits 2~0 (HPWTP2~ HPWTP0): high-pulse width timer prescaler select bits

| HPWTP2 | HPWTP1 | HPWTP0 | High-pulse Width Timer Scale |
|--------|--------|--------|------------------------------|
| 0 | 0 | 0 | 1:2 |
| 0 | 0 | 1 | 1:4 |
| 0 | 1 | 0 | 1:8 |
| 0 | 1 | 1 | 1:16 |
| 1 | 0 | 0 | 1:32 |
| 1 | 0 | 1 | 1:64 |
| 1 | 1 | 0 | 1:128 |
| 1 | 1 | 1 | 1:256 |

6.2.18 IOCB1/P6PH (Port 6 Pull-high Control Register)

(Address: 0Bh, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PH67 | PH66 | PH65 | PH64 | PH63 | PH62 | PH61 | PH60 |

Bit 7 ~ Bit 0 (PH67 ~ PH60): enable bits of Port 6 pull-high function.

PH6x = "0": disable pin of P6.x internal pull-high resistor function

PH6x = "1": enable pin of P6.x internal pull-high resistor function

6.2.19 IOCC1/P6OD (Port 6 Open Drain Control Register)

(Address: 0Ch, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OP67 | OP66 | OP65 | OP64 | OP63 | OP62 | OP61 | OP60 |

Bit 7 ~ Bit 0: enable bits of Port 6 open drain function.

OP6x = "0": disable pin of P6.x open drain function

OP6x = "1": enable pin of P6.x open drain function

6.2.20 IOCD1/P8PH (Port 8 Pull-high Control Register)

(Address: 0Dh, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PH87 | PH86 | PH85 | PH84 | PH83 | PH82 | PH81 | PH80 |

Bit 7 ~ Bit 0: enable bits of Port 8 pull-high function.

PH8x = "0": disable pin of P8.x internal pull-high resistor function

PH8x = "1": enable pin of P8.x pull-high resistor function

6.2.21 IOCE1/P6PL (Port 6 Pull-low Control Register)

(Address: 0Eh, Bit 0 of R5 = "1")

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PL67 | PL66 | PL65 | PL64 | PL63 | PL62 | PL61 | PL60 |

Bit 7 ~ Bit 0: enable bits of Port 6 pull-low function.

PL6x = "0": disable pin of P6.x internal pull-low resistor function

PL6x = "1": enable pin of P6.x internal pull-low resistor function

6.3 TCC and WDT Prescaler

Two 8-bit counters are available as prescalers for the TCC (Time Clock Counter) and WDT (Watchdog Timer). The TCCP2~TCCP0 bits of the IOC71 register are used to determine the ratio of the TCC prescaler. Likewise, the WDTP2~WDTP0 bits of the IOC81 register are used to determine the WDT prescaler. The TCC prescaler (TCCP2~TCCP0) is cleared by the instructions each time they are written into TCC, while the WDT prescaler is cleared by the “WDTC” and “SLEP” instructions. Fig.7 depicts the circuit diagram of TCC and WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be selected by internal instruction clock or external signal input (edge selectable from the TCC control register). If the TCC signal source is from the internal instruction clock, the TCC will be incremented by 1 at every instruction cycle (without prescaler). If the TCC signal source is from an external clock input, the TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin.

The Watchdog Timer is a free running on sub-oscillator. The WDT will keep on running even after the oscillator driver has been turned off. During Normal mode, Green mode, or Idle mode operation, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the Normal mode and Green mode by software programming. Refer to WDTE bit of IOC81 register. The WDT time-out period is equal to $(\text{prescaler} \times 256 / (F_s/2))$.

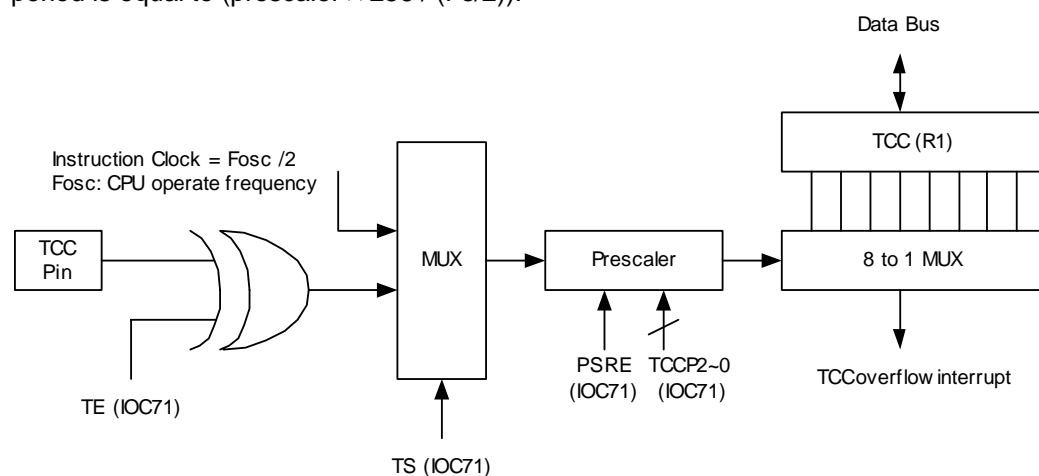


Fig. 6-4(a) Block Diagram of TCC

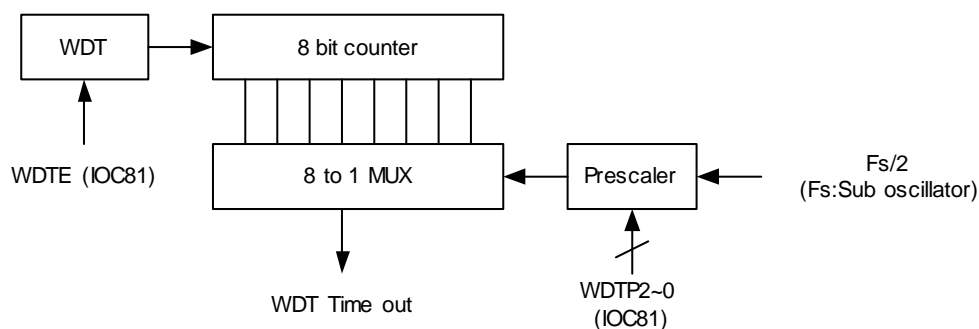
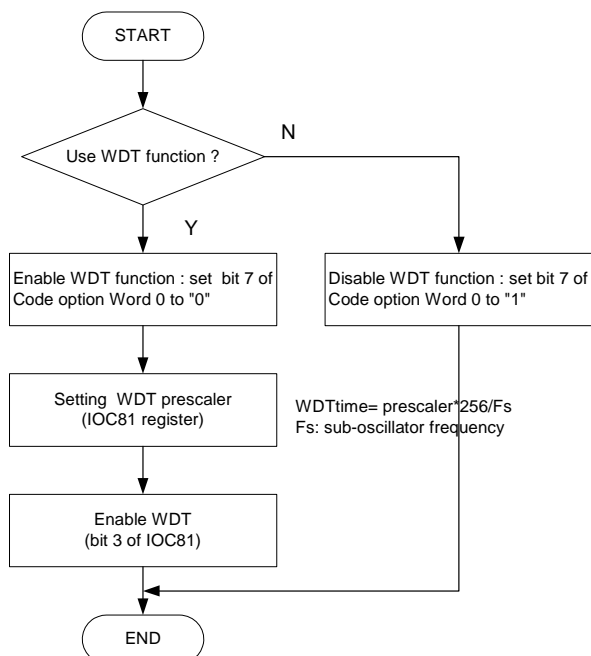
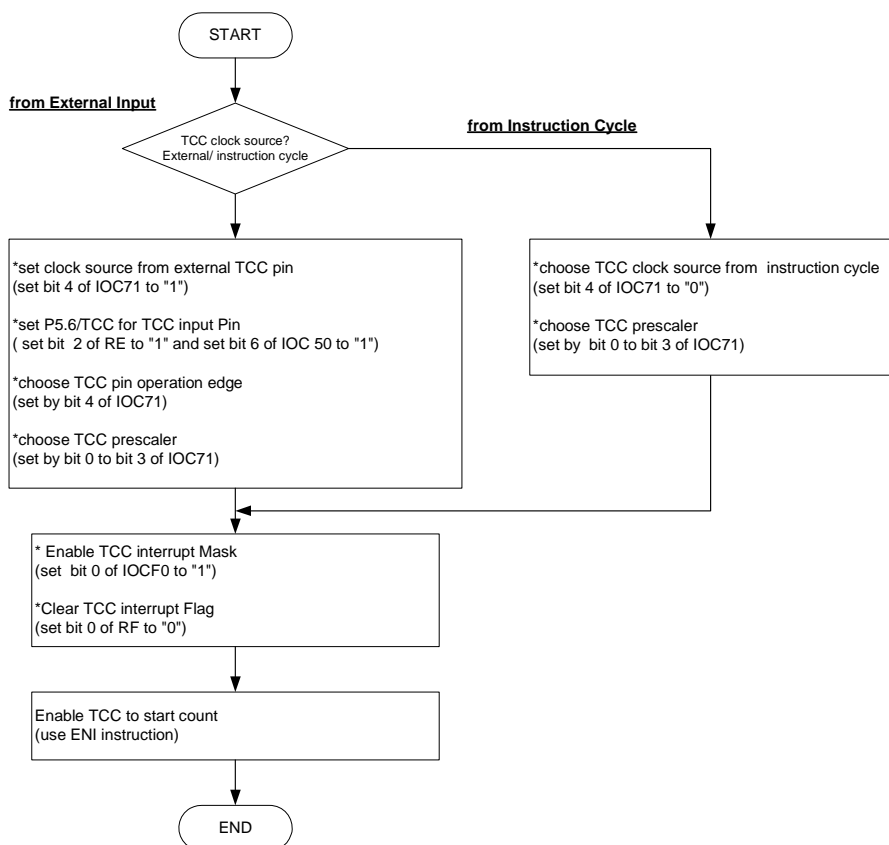


Fig. 6-4(b) Block Diagram of WDT

WDT Setting Flowchart

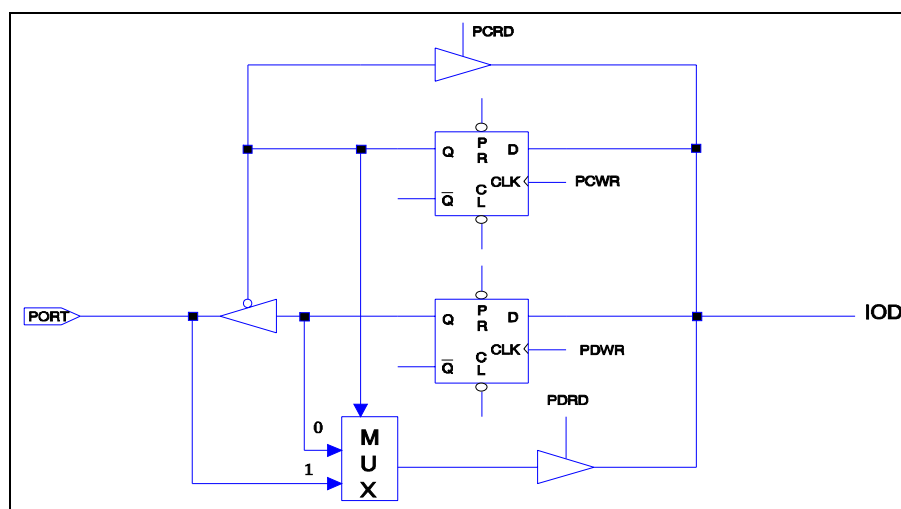


TCC Setting Flowchart



6.4 I/O Ports

The I/O registers, (Port 5, Port 6, Port 7 and Port 8), are bi-directional tri-state I/O ports. Port 6 and Port 8 are pulled-high internally by software; Port 6 is also pulled-low internally by software. Furthermore, Port 6 has its open-drain output also through software. Port 6 and Port 8 features an input status changed interrupt (or wake-up) function and is pulled-high by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC50 ~ IOC80). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits are shown in Fig. 6-5.



Note: Open-drain, pull-high, and pull down are not shown in the figure.

Fig. 6-5 The Circuit of I/O Port and I/O Control Register for Port 5 ~ 8

6.5 Reset and Wake-up

A reset can be activated by

- POR (Power-on Reset)
- WDT timeout. (if enabled)
- /RESET pin goes to low.

Note: The power-on reset circuit is always enabled. It will reset the CPU at 1.8V.

Once a reset occurs, the following functions are performed

- The oscillator is running, or will be started.
- The program counter (R2/PC) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The TCC/Watchdog timer and prescaler are cleared.
- When power is on, the Bits 5 and 6 of R3 and the upper two bits of R4 are cleared.
- Bits of the IOC71 register are set to all "1" except for Bit 6 (INT flag).
- For other registers, see Table 2.

Table 2 Summary of the Initialized Values for Registers

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|------------------|-------------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0x05 | IOC50 (P5CR) | Bit Name | IOC57 | IOC56 | IOC55 | IOC54 | P8HS | P8LS | P7HS | P7LS |
| | | Power-on | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | IOC60 (P6CR) | Bit Name | IOC67 | IOC66 | IOC65 | IOC64 | IOC63 | IOC62 | IOC61 | IOC60 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | IOC70 (P7CR) | Bit Name | IOC77 | IOC76 | IOC75 | IOC74 | IOC73 | IOC72 | IOC71 | IOC70 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | IOC80 (P8CR) | Bit Name | IOC87 | IOC86 | IOC85 | IOC84 | IOC83 | IOC82 | IOC81 | IOC80 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | IOC90 (RAM_ADDR) | Bit Name | X | RAM_A6 | RAM_A5 | RAM_A4 | RAM_A3 | RAM_A2 | RAM_A1 | RAM_A0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | IOCA0 (RAM_DB) | Bit Name | RAM_D7 | RAM_D6 | RAM_D5 | RAM_D4 | RAM_D3 | RAM_D2 | RAM_D1 | RAM_D0 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET & WDT | P | P | P | P | P | P | P | P |
| | | Wake-Up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | IOCB0 (CNT1PR) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | IOCC0 (CNT2PR) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0D | IOCD0 (HPWTPR) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0E | IOCE0 (LPWTPR) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0F | IOCF0 (IMR) | Bit Name | ICIE | LPWTE | HPWTE | CNT2E | CNT1E | INT1E | INT0E | TCIE |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x06 | IOC61 (WUCR) | Bit Name | IROCS | X | X | X | /WUE8H | /WUE8L | /WUE6H | /WUE6L |
| | | Power-on | 0 | U | U | U | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | U | U | U | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | U | U | U | P | P | P | P |



| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------------------|-------------------------|--|--------|--------|--------|-------|--------|--------|--------|
| 0x07 | IOC71 (TCCCR) | Bit Name | INT_EDGE | INT | TS | TE | PSRE | TCCP2 | TCCP1 | TCCP0 |
| | | Power-on | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | IOC81 (WDTCR) | Bit Name | X | X | X | X | WDTE | WDTP2 | WDTP1 | WDTP0 |
| | | Power-on | U | U | U | U | 0 | 1 | 1 | 1 |
| | | /RESET & WDT | U | U | U | U | 0 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | U | U | U | U | P | P | P | P |
| 0x09 | IOC91 (CNT12CR) | Bit Name | CNT2S | CNT2P2 | CNT2P1 | CNT2P0 | CNT1S | CNT1P2 | CNT1P1 | CNT1P0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0A | IOCA1 (HLPWTCR) | Bit Name | LPWTS | LPWTP2 | LPWTP1 | LPWTP0 | HPWTS | HPWTP2 | HPWTP1 | HPWTP0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0B | IOCB1 (P6PH) | Bit Name | PH67 | PH66 | PH65 | PH64 | PH63 | PH62 | PH61 | PH60 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0C | IOCC1 (P6OD) | Bit Name | OP67 | OP66 | OP65 | OP64 | OP63 | OP62 | OP61 | OP60 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0D | IOCD1 (P8PH) | Bit Name | PH87 | PH86 | PH85 | PH84 | PH83 | PH82 | PH81 | PH80 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x0E | IOCE1 (P6PL) | Bit Name | PL67 | PL66 | PL65 | PL64 | PL63 | PL62 | PL61 | PL60 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x00 | R0 (IAR) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET & WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x01 | R1 (TCC) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x02 | R2 (PC) | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | Jump to address 0x0018 or continue to execute next instruction | | | | | | | |
| 0x03 | R3 (SR) | Bit Name | X | PS1 | PS0 | T | P | Z | DC | C |
| | | Power-on | U | 0 | 0 | 1 | 1 | U | U | U |
| | | /RESET & WDT | U | 0 | 0 | t | t | P | P | P |
| | | Wake-up from Pin Change | U | P | P | t | t | P | P | P |
| 0x04 | R4 (RSR) | Bit Name | Bank 1 | Bank 0 | – | – | – | – | – | – |
| | | Power-on | 0 | 0 | U | U | U | U | U | U |
| | | /RESET & WDT | 0 | 0 | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

| Address | Name | Reset Type | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|------------------|-------------------------|-------|-------|-------|--------|---------|---------|---------|---------|
| 0x05 | R5 (Port 5) | Bit Name | R57 | R56 | R55 | R54 | X | X | X | IOCPAGE |
| | | Power-on | 1 | 1 | 1 | 1 | U | U | U | 0 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | U | U | U | 0 |
| | | Wake-up from Pin Change | P | P | P | P | U | U | U | P |
| 0x06 | R6 (Port 6) | Bit Name | R67 | R66 | R65 | R64 | R63 | R62 | R61 | R60 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x07 | R7 (Port 7) | Bit Name | R77 | R76 | R75 | R74 | R73 | R62 | R71 | R70 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x08 | R8 (Port 8) | Bit Name | R87 | R86 | R85 | R84 | R83 | R82 | R81 | R80 |
| | | Power-on | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | /RESET & WDT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0x09 | R9 (LCDCR) | Bit Name | BS | DS1 | DS0 | LCDEN | X | LCDTYPE | LCDF1 | LCDF0 |
| | | Power-on | 1 | 1 | 0 | 0 | U | 0 | 0 | 0 |
| | | /RESET & WDT | 1 | 1 | 0 | 0 | U | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | U | P | P | P |
| 0xA | RA (LCD_ADDR) | Bit Name | X | X | X | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |
| 0xB | RB (LCD_DB) | Bit Name | X | X | X | X | LCD_D 3 | LCD_D 2 | LCD_D 1 | LCD_D 0 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET & WDT | U | U | U | U | P | P | P | P |
| | | Wake-up from Pin Change | U | U | U | U | P | P | P | P |
| 0xC | RC (CNTER) | Bit Name | X | X | X | X | LPWTEN | HPWTEN | CNT2EN | CNT1EN |
| | | Power-on | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | 0 | P | P | P | P | P |
| 0xD | RD (SBPCR) | Bit Name | X | CLK2 | CLK1 | CLK0 | IDLE | BF1 | BF0 | CPUS |
| | | Power-on | U | 0 | 0 | 0 | 1 | 0 | 0 | *1 |
| | | /RESET & WDT | U | 0 | 0 | 0 | 1 | 0 | 0 | *1 |
| | | Wake-up from Pin Change | U | P | P | P | P | P | P | P |
| 0xE | RE (IRCR) | Bit Name | IRE | HF | LGP | X | IROUTE | TCCE | EINT1 | EINT0 |
| | | Power-on | 0 | 0 | 0 | U | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | U | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | P | P | P | U | P | P | P | P |
| 0xF | RF (ISR) | Bit Name | ICIF | LPWTF | HPWTF | CNT2F | CNT1F | INT1F | INT0F | TCIF |
| | | Power-on | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | /RESET & WDT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | Wake-up from Pin Change | N | P | P | P | P | P | P | P |
| 0x10 ~ 0x3F | R10~R3F | Bit Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | | Power-on | U | U | U | U | U | U | U | U |
| | | /RESET & WDT | P | P | P | P | P | P | P | P |
| | | Wake-up from Pin Change | P | P | P | P | P | P | P | P |

Note: This bit is equal to the Code Option HLFS bit data

Legend: “x” = not used

“P” = previous value before reset

“—” = Not defined

“t” = check R3 register explanation

“u” = unknown or don't care

“N” = Monitors interrupt operation status

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows:

| Wake-up Signal | Sleep Mode | Idle Mode | Green Mode | Normal Mode |
|--|--|--|------------|-------------|
| TCC time out IOCF0 Bit 0=1 | × | × | Interrupt | Interrupt |
| INT0 pin IOCF0 Bit 1=1 | Wake-up + interrupt + next instruction | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| INT1 pin IOCF0 Bit 2=1 | Wake-up + interrupt + next instruction | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| Counter 1 IOCF0 Bit 3=1 | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| Counter 2 IOCF0 Bit 4=1 | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| High-pulse timer IOCF0 Bit 5=1 | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| Low-pulse timer IOCF0 Bit 6=1 | × | Wake-up + interrupt + next instruction | Interrupt | Interrupt |
| Port 6, Port 8 (input status change wake-up) Bit 7 of IOCF0 = "0" | Wake-up + next instruction | Wake-up + next instruction | × | × |
| Port 6, Port 8 (input status change wake-up) Bit 7 of IOCF0 = "1" | Wake-up + interrupt + next instruction | Wake-up + interrupt + next instruction | × | × |
| WDT time out | × | RESET | RESET | RESET |

Note: *¹ Only an external TCC pin can wake up from Idle mode.

6.6 Oscillator

6.6.1 Oscillator Modes

The EM78468 can operate in three different oscillator modes i.e., a.) Main oscillator (R-OSCI, OSCO), such as RC oscillator with external resistor and Internal capacitor mode (ERIC); b.) Crystal oscillator mode; and c.) PLL operation mode (R-OSCI connected to 0.01 μ F capacitor to Ground). User can select which mode by programming FMMD1 and FMMD0 in the Code Options Register. The sub-oscillator can be operated in Crystal mode and ERIC mode. Table 3 below shows how these three modes are defined.

Table 3 Oscillator Modes as defined by FSMD, FMMD1, FMMD0

| FSMD | FMMD1 | FMMD0 | Main Clock | Sub-clock |
|------|-------|-------|----------------|----------------|
| 0 | 0 | 0 | RC type (ERIC) | RC type (ERIC) |
| 0 | 0 | 1 | Crystal type | RC type (ERIC) |
| 0 | 1 | × | PLL type | RC type (ERIC) |
| 1 | 0 | 0 | RC type (ERIC) | Crystal type |
| 1 | 0 | 1 | Crystal type | Crystal type |
| 1 | 1 | × | PLL type | Crystal type |

Table 4 Summary of maximum operating speeds

| Conditions | VDD | Fxt Max. (MHz) |
|------------|-----|----------------|
| Two clocks | 2.3 | 4 |
| | 3.0 | 8 |
| | 5.0 | 10 |

6.6.2 Phase-locked Loop (PLL Mode)

When operating in PLL mode, High frequency is determined by the sub-oscillator. The RD register can be chosen to change the high oscillator frequency. The relation between high frequency (Fm) and sub-oscillator is shown in the table.

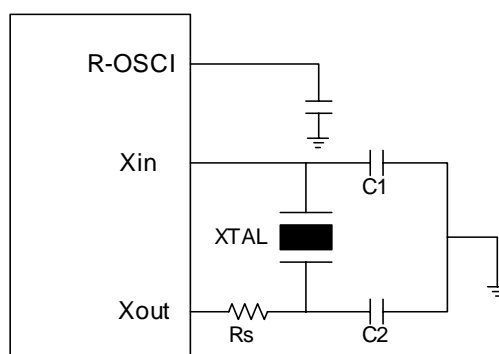


Fig. 6-6 PLL Mode Circuit

Bits 6~4 (CLK2~0) of RD: main clock selection bits for PLL mode (code option select)

| CLK2 | CLK1 | CLK0 | Main Clock | Example Fs=32.768kHz |
|------|------|------|------------|----------------------|
| 0 | 0 | 0 | Fs×130 | 4.26 MHz |
| 0 | 0 | 1 | Fs×65 | 2.13 MHz |
| 0 | 1 | 0 | Fs×65/2 | 1.065 MHz |
| 0 | 1 | 1 | Fs×65/4 | 532 kHz |
| 1 | × | × | Fs×244 | 8 MHz |

6.6.3 Crystal Oscillator/Ceramic Resonators (Crystal)

This LSI can be driven by an external clock signal through the R-OSCI pin as shown in Fig.6-7 below. In most applications, the R-OSCI pin and the OSCO pin can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 6-8 depicts such circuit. Table 5 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

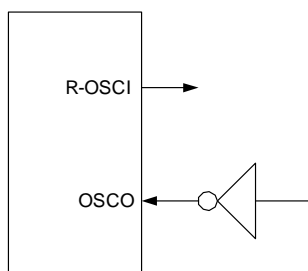


Fig. 6-7 External Clock Input Circuit

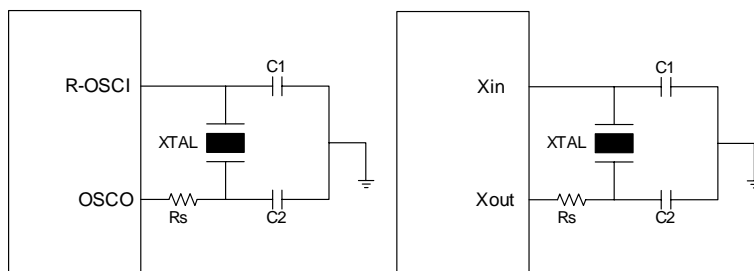


Fig. 6-8 Circuit for Crystal/Resonator

Table 5 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonators

| Oscillator Source | Oscillator Type | Frequency | C1 (pF) | C2 (pF) |
|-------------------|--------------------|-----------|---------|---------|
| Main oscillator | Ceramic Resonators | 455 kHz | 100~150 | 100~150 |
| | | 2.0 MHz | 20~40 | 20~40 |
| | | 4.0MHz | 10~30 | 10~30 |
| | Crystal Oscillator | 455kHz | 20~40 | 20~150 |
| | | 1.0MHz | 15~30 | 15~30 |
| | | 2.0MHz | 15 | 15 |
| Sub-oscillator | Crystal Oscillator | 4.0MHz | 15 | 15 |
| | | 32.768kHz | 25 | 25 |

6.6.4 RC Oscillator Mode with Internal Capacitor

If both precision and cost are taken into consideration, this LSI also offers a special oscillation mode, which has an on-chip internal capacitor and an external resistor connected to VDD. The internal capacitor functions as temperature compensator. In order to obtain more accurate frequency, a precise resistor is recommended.

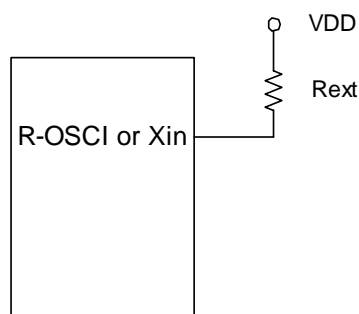


Fig. 6-9 Circuit for Internal C Oscillator Mode

Table 6 RC Oscillator Frequencies

| Pin | Rext | Average Fosc 5V, 25°C | Average Fosc 3V, 25°C |
|--------|------|-----------------------|-----------------------|
| R-OSCI | 51k | 2.2221 MHz | 2.1972 MHz |
| | 100k | 1.1345 MHz | 1.1203 MHz |
| | 300k | 381.36kHz | 374.77kHz |
| Xin | 2.2M | 32.768kHz | 32.768kHz |

Note: Measured from LQFP packages with frequency drift of about $\pm 30\%$.

Values are provided for design reference only.

6.7 Power-on Considerations

Any microcontroller (as with this LSI) is not warranted to start operating properly before the power supply stabilizes in a steady state. This LSI has an on-chip Power-on Reset (POR) with detection level range of 1.6V to 1.8V. The circuitry eliminates the extra external reset circuit but will work well only if the VDD rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.7.1 External Power-on Reset Circuit

This circuit implements an external RC to produce a reset pulse (see Fig. 6-10). The pulse width (time constant) should be kept long enough to allow VDD to reach minimum operation voltage. This circuit is used when the power supply rise time is slow. Because the current leakage from the /RESET pin is $\pm 5\mu\text{A}$, it is recommended that R should not be greater than 40K. In this way, the voltage at Pin /RESET is held below 0.2V. The diode (D) acts as a short circuit at power-down. The capacitor, C, is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

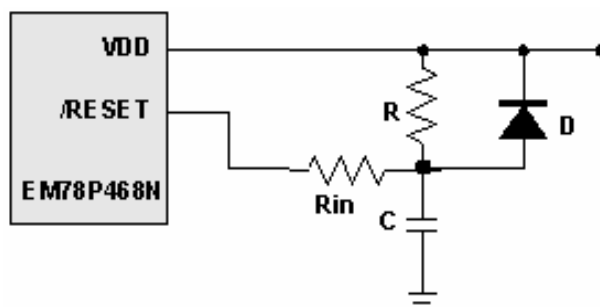


Fig. 6-10 External Power-on Reset Circuit

6.7.2 Residue-Voltage Protection

When battery is replaced, device power (VDD) is disconnected but residue-voltage remains. The residue-voltage may trips below minimum VDD, but above zero. This condition may cause poor power on reset. Fig. 6-11 and Fig. 6-12 show how to build a residue-voltage protection circuit

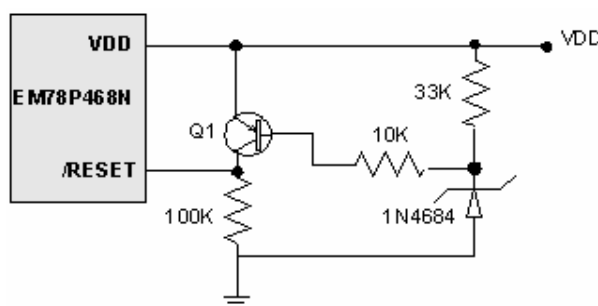


Fig. 6-11 Residue Voltage Protection Circuit 1

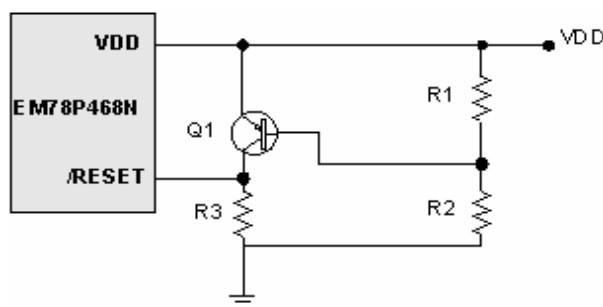


Fig. 6-12 Residue Voltage Protection Circuit 2

6.8 Interrupt

This LSI has eight interrupt sources as listed below:

- TCC overflow interrupt.
- External interrupt P5.4/INT0 pin
- External interrupt P5.5/INT1 pin
- Counter 1 underflow interrupt
- Counter 2 underflow interrupt
- High-pulse width timer underflow interrupt
- Low-pulse width timer underflow interrupt
- Port 6, Port 8 input status change wake-up

This IC has internal interrupts which are falling edge triggered or as follows:

- TCC timer overflow interrupt
- Four 8-bits down counter/timer underflow interrupt

If these interrupt sources change signal from high to low, the RF register will generate a "1" flag to the corresponding register if the IOCF0 register is enabled.

RF is the interrupt status register. It records the interrupt request in flag bit. IOCF0 is the interrupt mask register. Global interrupt is enabled by ENI instruction and disabled by DISI instruction. When one of the interrupts (when enabled) is generated, it will cause the next instruction to be fetch from address 0003H~0018H according to interrupt source.

With this LSI, each individual interrupt source has its own interrupt vector as depicted in Table 3. Before the interrupt subroutine is executed, the contents of the ACC and the R3 register are initially saved by the hardware. After the interrupt service routine is completed, the ACC and R3 are restored. The existing interrupt service routine does not allow other interrupt service routine to be executed. Hence, if other interrupts occur while an existing interrupt service routine is being executed, the hardware will save the later interrupts. Only after the existing interrupt service routine is completed that the next interrupt service routine is executed.

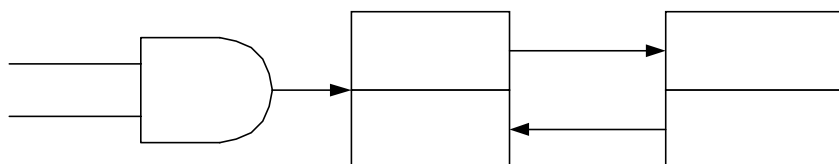


Fig. 6-15 Interrupt Back-up Diagram

Table 7 Interrupt Vector

| Interrupt Vector | Interrupt Status |
|------------------|--|
| 0003H | TCC overflow interrupt. |
| 0006H | External interrupt P5.4/INT0 pin |
| 0009H | External interrupt P5.5/INT1 pin |
| 000CH | Counter 1 underflow interrupt |
| 000FH | Counter 2 underflow interrupt |
| 0012H | High-pulse width timer underflow interrupt |
| 0015H | Low-pulse width timer underflow interrupt |
| 0018H | Port 6, Port 8 input status change wake up |

6.9 LCD Driver

This LSI can drive an LCD of up to 32 segments and 4 commons that can drive a total of 4×32 dots. The LCD block is made up of an LCD driver, display RAM, segment output pins, common output pins, and LCD operating power supply pins. This circuit works on normal mode, green mode and idle mode. The LCD duty; bias; the number of segment; the number of common and frame frequency are determined by the LCD controller register.

The basic structure contains a timing control that uses a subsystem clock to generate the proper timing for different duty and display accesses. The R9 register is a command register for the LCD driver which includes LCD enable/disable, bias (1/2 and 1/3), duty (1/2, 1/3, 1/4), and LCD frame frequency control. The register RA is an LCD contrast and LCD RAM address control register. The register RB is an LCD RAM data buffer. LCD booster circuit can change the operation frequency to improve VLCD2 and VLCD3 drive capability. The control register is described as follows.

6.9.1 R9/LCDCR (LCD Control Register)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|----------|-------|-------|
| BS | DS1 | DS0 | LCDEN | – | LCDDTYPE | LCDF1 | LCDF0 |

Bit 7 (BS): LCD bias select bit

“0”: 1/2 bias

“1”: 1/3 bias

Bits 6 ~ 5 (DS1 ~ DS0): LCD duty select

| DS1 | DS0 | LCD Duty |
|-----|-----|----------|
| 0 | 0 | 1/2 duty |
| 0 | 1 | 1/3 duty |
| 1 | × | 1/4 duty |

Bit 4 (LCDEN): LCD enable bit

“0”: disable the LCD circuit

“1”: enable the LCD circuit

When the LCD function is disabled, all common/segment output is set to ground (GND) level

Bit 3: Not used

Bit 2 (LCDTYPE): LCD drive waveform type select bit

LCDTYPE = "0": "A" type waveform

LCDTYPE = "1": "B" type waveform

Bits 1 ~ 0 (LCDF1 ~ LCDF0): LCD frame frequency control bits

| LCDF1 | LCDF0 | LCD Frame Frequency (e.g. Fs=32.768kHz) | | |
|-------|-------|---|-----------------|-----------------|
| | | 1/2 Duty | 1/3 Duty | 1/4 Duty |
| 0 | 0 | Fs/(256×2)=64.0 | Fs/(172×3)=63.5 | Fs/(128×4)=64.0 |
| 0 | 1 | Fs/(280×2)=58.5 | Fs/(188×3)=58.0 | Fs/(140×4)=58.5 |
| 1 | 0 | Fs/(304×2)=53.9 | Fs/(204×3)=53.5 | Fs/(152×4)=53.9 |
| 1 | 1 | Fs/(232×2)=70.6 | Fs/(156×3)=70.0 | Fs/(116×4)=70.6 |

Note: Fs: sub-oscillator frequency

6.9.2 RA/LCD_ADDR (LCD Address)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------|--------|--------|--------|--------|
| 0 | 0 | 0 | LCD_A4 | LCD_A3 | LCD_A2 | LCD_A1 | LCD_A0 |

Bits 7 ~ 5: Not used, fixed to "0"

Bits 4 ~ 0 (LCDA4 ~ LCDA0): LCD RAM address

| RA (LCD Address) | RB (LCD Data Buffer) | | | | | Segment |
|---------------------|----------------------|-------------------|-------------------|-------------------|-------------------|---------|
| | Bits 7 ~4 | Bit 3 (LCD_D3) | Bit 2 (LCD_D2) | Bit 1 (LCD_D1) | Bit 0 (LCD_D0) | |
| 00H | — | — | — | — | — | SEG0 |
| 01H | — | — | — | — | — | SEG1 |
| 02H | — | — | — | — | — | SEG2 |
| | | | | | | |
| 1DH | — | — | — | — | — | SEG29 |
| 1EH | — | — | — | — | — | SEG30 |
| 1FH | — | — | — | — | — | SEG31 |
| Common | X | COM3 | COM2 | COM1 | COM0 | |

6.9.3 RB/LCD_DB (LCD Data Buffer)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|---------|---------|---------|---------|
| — | — | — | — | LCD_D 3 | LCD_D 2 | LCD_D 1 | LCD_D 0 |

Bits 7 ~ 4: Not used

Bits 3 ~ 0 (LCD_D3 ~ LCD_D0): LCD RAM data transfer registers

6.9.4 RD/SBPCR (System, Booster and PLL Control Registers)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | CLK2 | CLK1 | CLK0 | IDLE | BF1 | BF0 | CPUS |

Bits 2 ~ 1 (BF1 ~ 0): LCD booster frequency select bits

| BF1 | BF0 | Booster Frequency |
|-----|-----|-------------------|
| 0 | 0 | Fs |
| 0 | 1 | Fs/4 |
| 1 | 0 | Fs/8 |
| 1 | 1 | Fs/16 |

The initial setting flowchart for LCD function

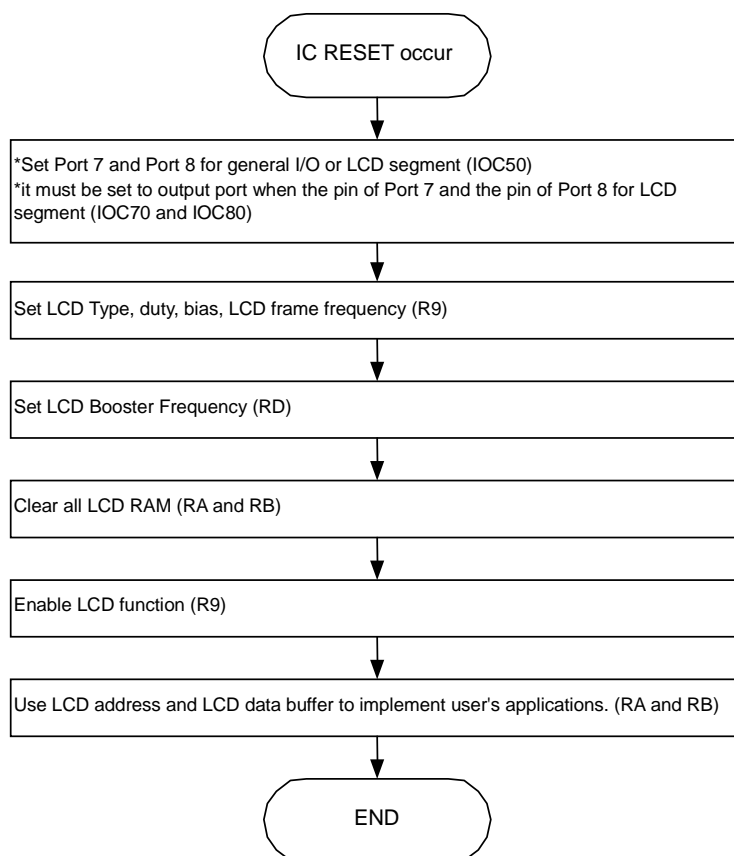
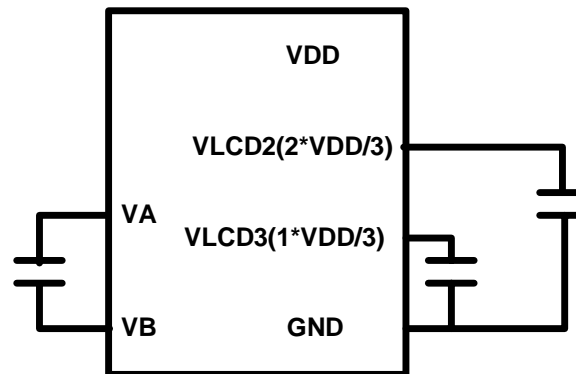
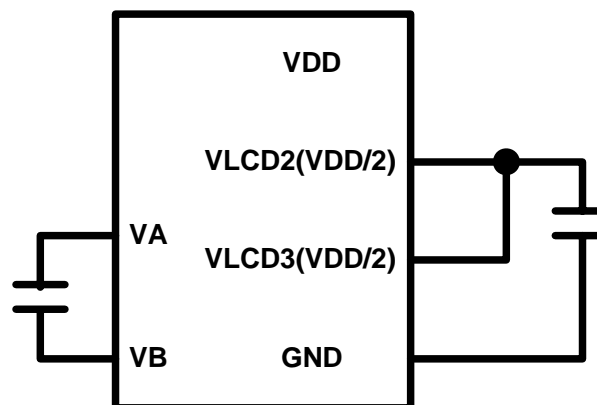


Fig. 6-14 The Initial Setting Flowchart for LCD Function

Boosting circuits connection for LCD voltage



External circuit for 1/3 Bias



External circuit for 1/2 Bias

Fig. 6-15 Charge Bump Circuit Connection ($C_{ext}=0.1\mu f$)

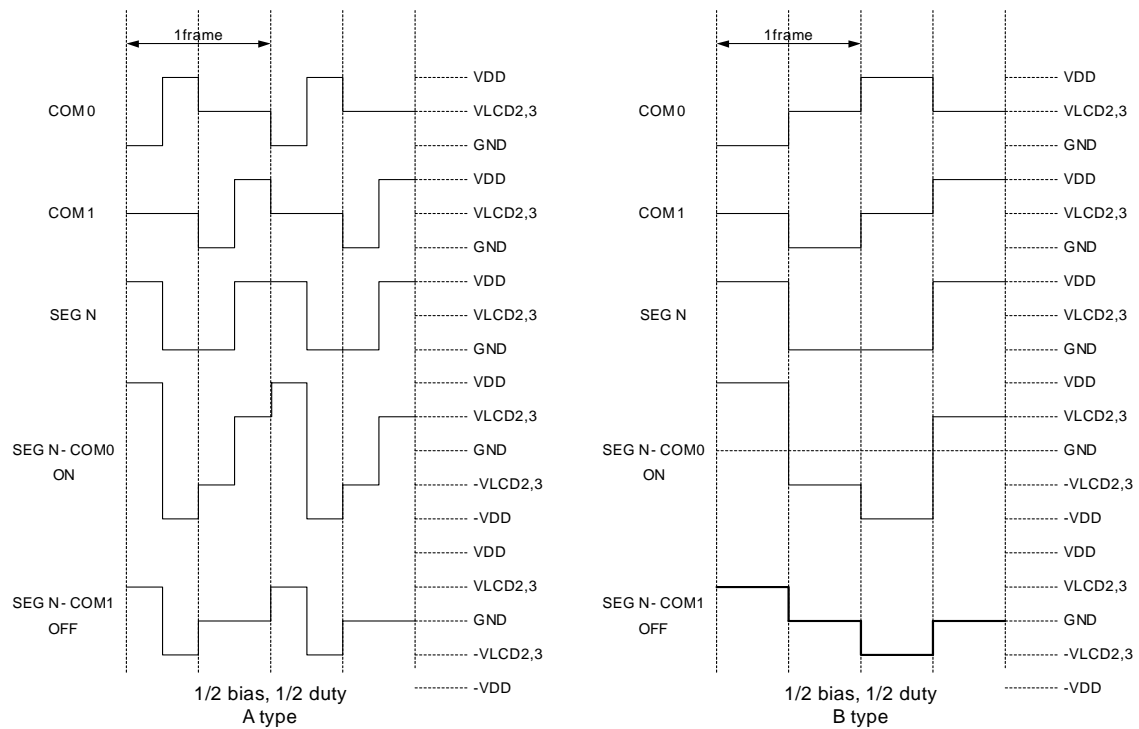


Fig. 6-16 LCD Waveform for 1/2 Bias, 1/2 Duty

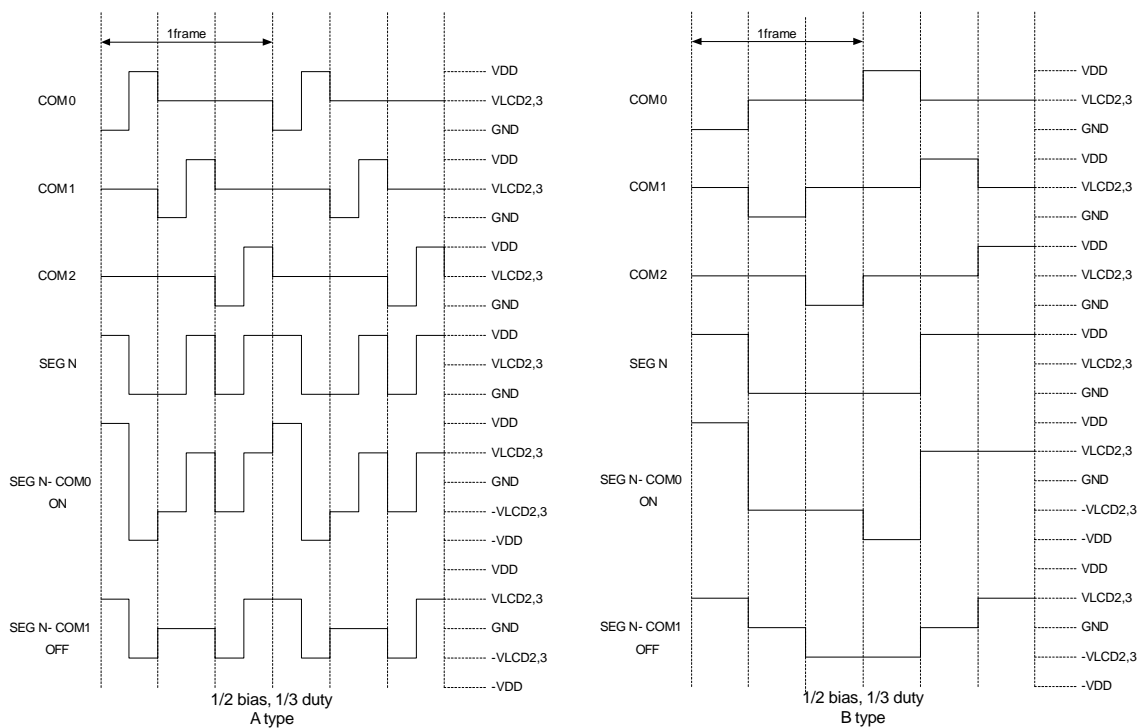


Fig. 6-17 LCD Waveform for 1/2 Bias, 1/3 Duty

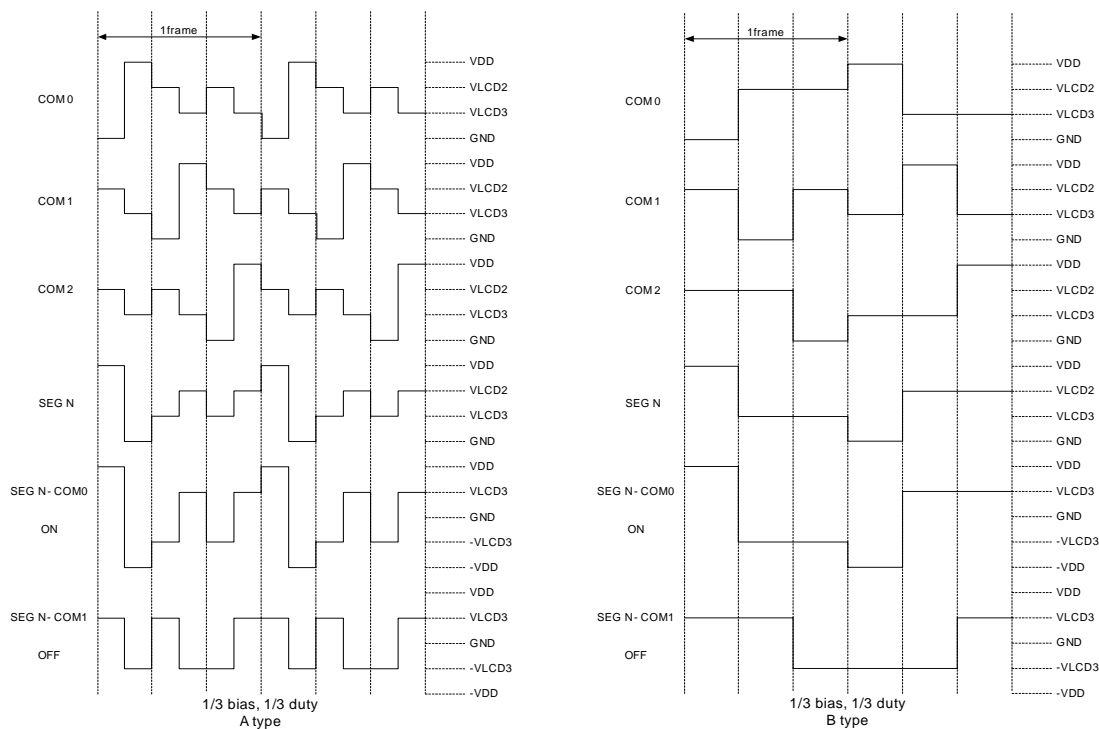


Fig. 6-18 LCD Waveform for 1/3 Bias, 1/3 Duty

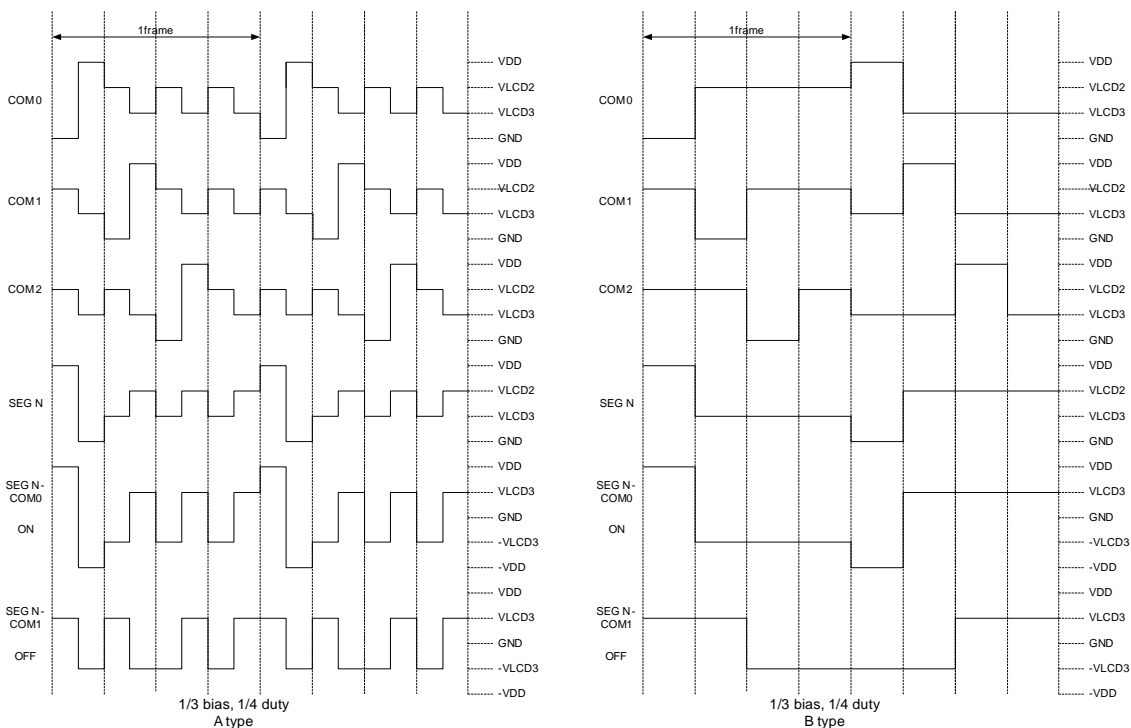


Fig. 6-19 LCD Waveform for 1/3 Bias, 1/4 Duty

6.10 Infrared Remote Control Application/PWM Waveform Generation

This LSI can output infrared carrier in user-friendly or in PWM standard waveform. The IR and PWM waveform generated functions include an 8-bit down count timer/counter, high-pulse width timer, low-pulse width timer, and IR control register. The IR system block diagram is shown in Fig. 6-20. The IROUT pin waveform is determined by IR control register (RE), IOC90 (Counters 1 and 2 control register), IOCA0 (high-pulse width timer, low-pulse width timer control register), IOCC0 (Counter 2 preset), IOCD0 (high-pulse width timer preset register), and IOCE0 (low-pulse width timer preset register). Details on $F_{carrier}$, high-pulse time, and low pulse time are explained as follows:

If Counter 2 clock source is F_T (this clock source can be set by IOC91);

$$F_{carrier} = \frac{F_T}{2 \times (1 + \text{decimal of Counter 2 preset value (IOCC 0)}) \times \text{prescaler}}$$

If high-pulse width timer source clock is F_T (this clock source can be set by IOCA1);

$$T_{high\ pulse\ time} = \frac{\text{prescaler} \times (1 + \text{decimal of high pulse width timer value (IOCD 0)})}{F_T}$$

If low-pulse width timer source clock is F_T (this clock source can be set by IOCA1);

$$T_{low\ pulse\ time} = \frac{\text{prescaler} \times (1 + \text{decimal of low pulse width timer value (IOCE 0)})}{F_T}$$

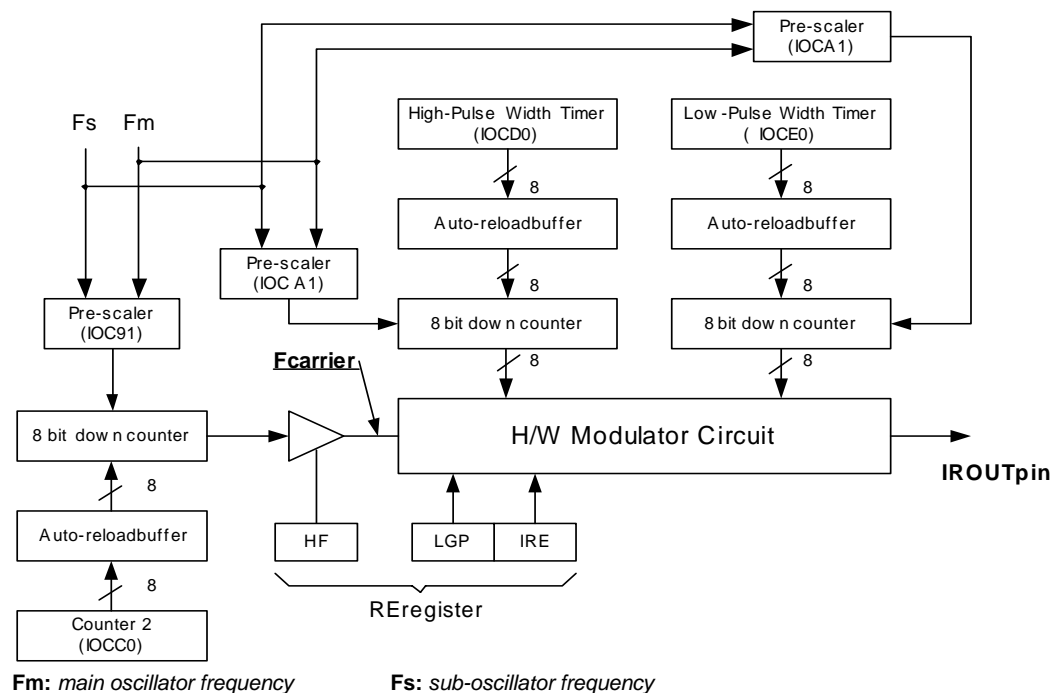


Fig. 6-20 IR/PWM System Block Diagram

The IROUT output waveform is further explained in the following figures:

Fig. 6-21 LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time.

Fig. 6-22 LGP=0, HF=0, the IROUT waveform cannot modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform.

Fig. 6-23 LGP=0, HF=1, the IROUT waveform can modulate Fcarrier waveform when in low-pulse width time. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting until high-pulse width timer interrupt occurs.

Fig. 6-24 LGP=0, HF=0, the IROUT waveform can not modulate Fcarrier waveform when in low-pulse width time. So IROUT waveform is determined by high-pulse time and low-pulse time. This mode can produce standard PWM waveform. When IRE goes from high to low, the output waveform of IROUT will keep on transmitting till high-pulse width timer interrupt occurs.

Fig. 6-25 LGP=1, when this bit is set to high level, the high-pulse width timer is ignored. So IROUT waveform output from low-pulse width timer is established.

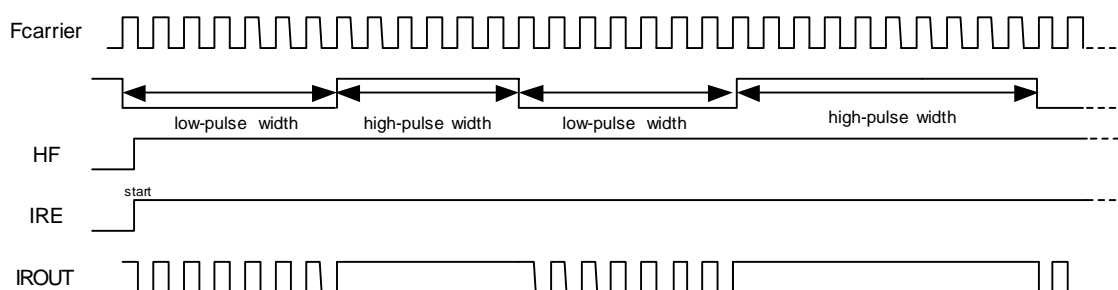


Fig. 6-21 LGP=0, IROUT Pin Output Waveform

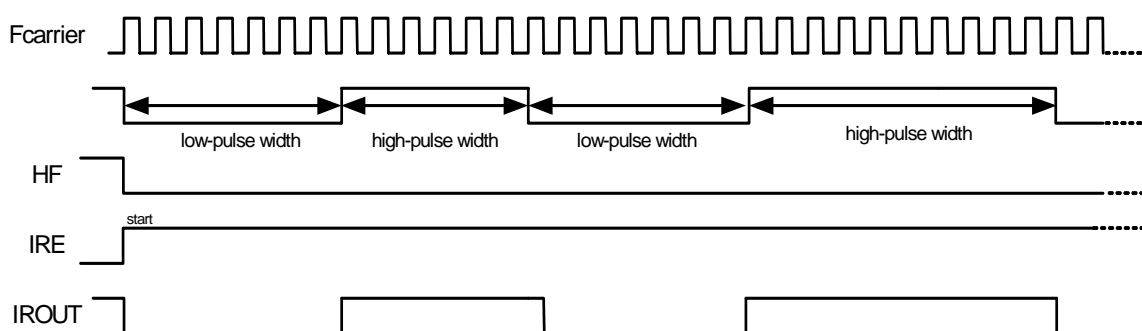


Fig. 6-22 LGP=0, IROUT Pin Output Waveform

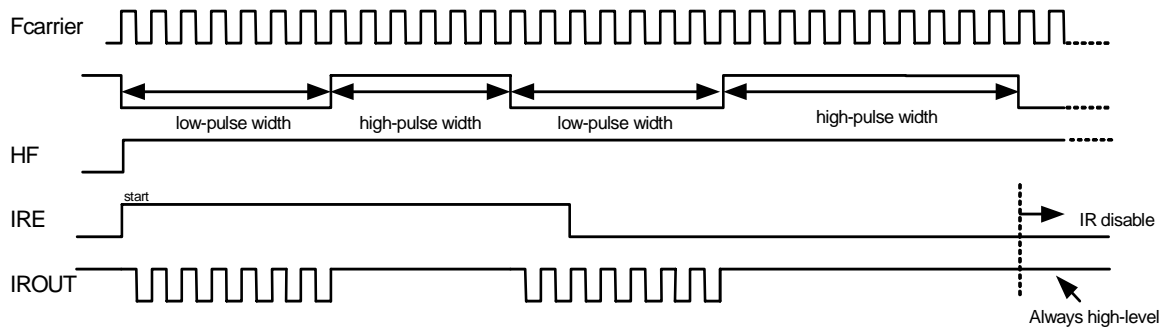


Fig. 6-23 LGP=0, IROUT Pin Output Waveform

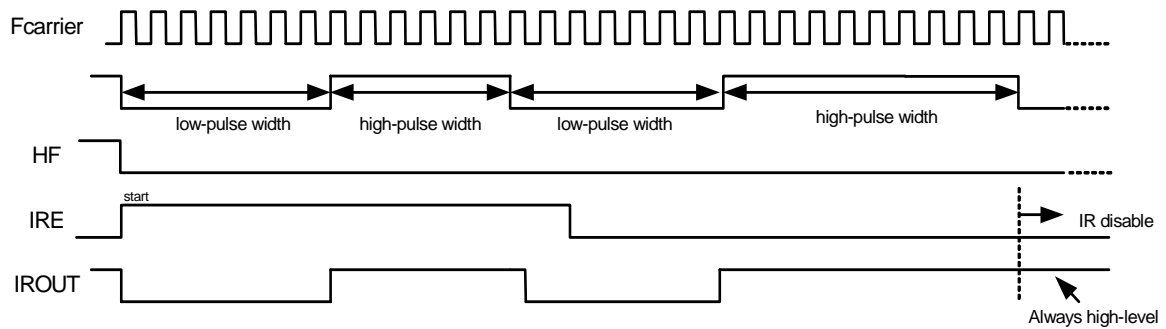


Fig. 6-24 LGP=0, IROUT Pin Output Waveform

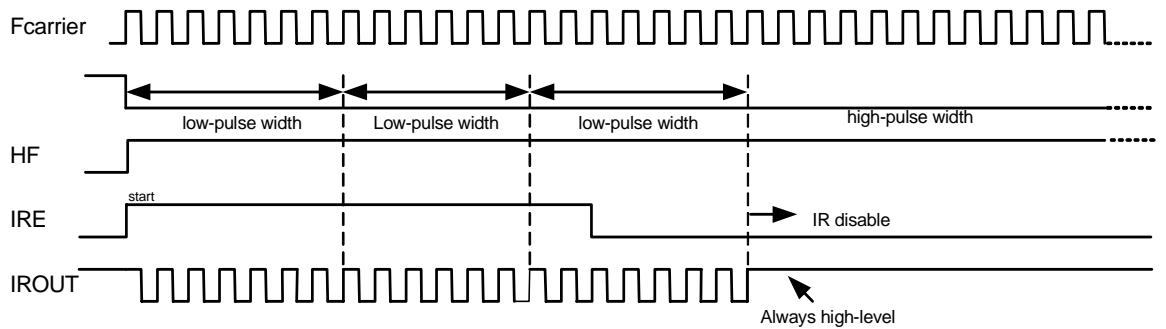


Fig. 6-25 LGP=1, IROUT Pin Output Waveform

IR/PWM Function Enable Flowchart

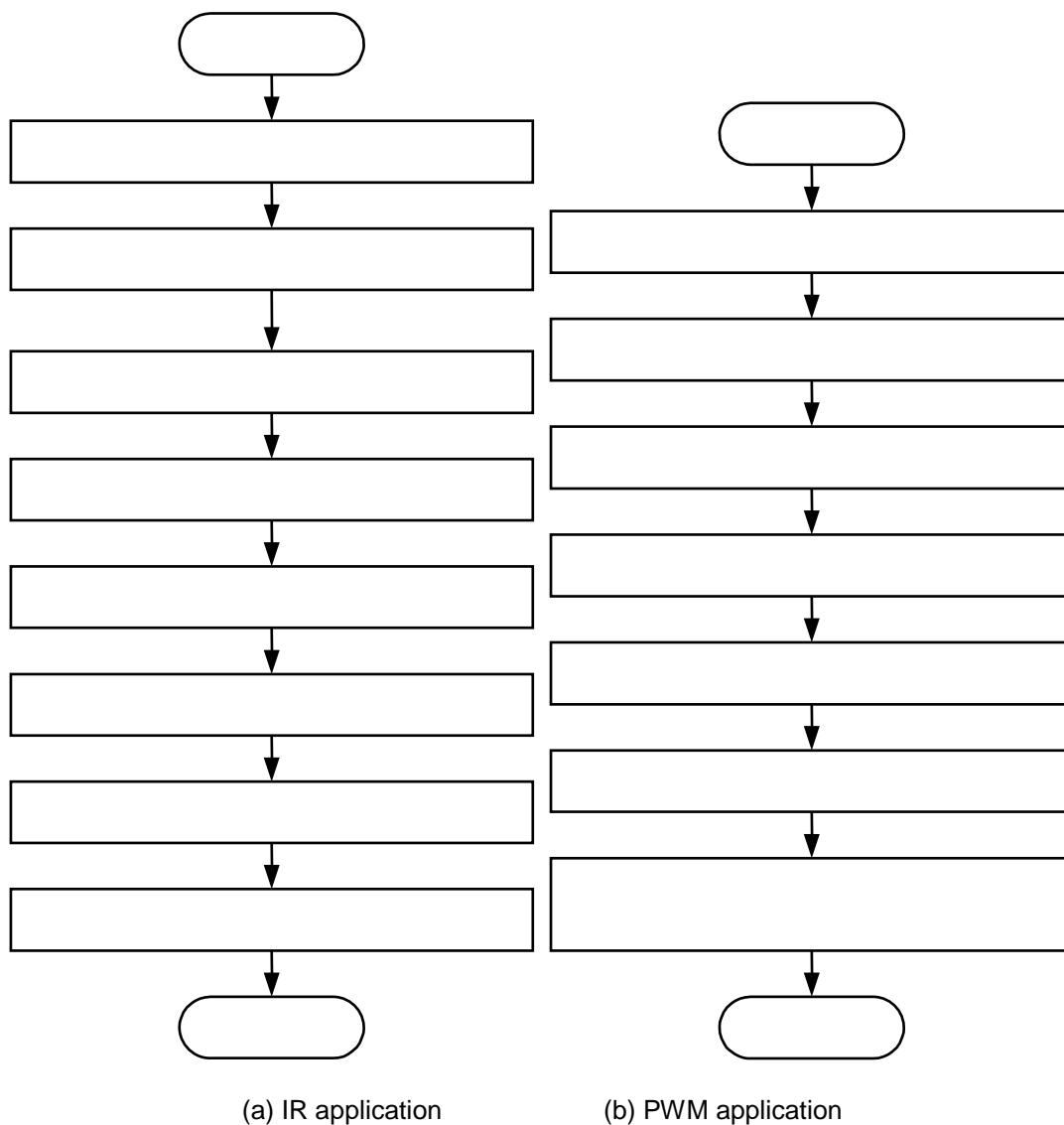


Fig. 6-26 IR/PWM Function Enable Flowchart

6.11 Code Options

The EM78468 has one Code Option word that is not a part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register (Word 0)

| Word 0 | | | | | | | | | | |
|-----------|-------|-------|--------|-------|-------|-------|-------|-------|-------|-------|
| Bits12~10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | CYES | HLFS | ENWDTB | FSMD | FMMD1 | FMMD0 | HLP | 0 | 0 | 0 |

Bits 12 ~ 10: Not used. These bits are set to “1” all the time.

Bit 9 (CYES): Cycle select for JMP and CALL instructions

CYES = “0”: only one instruction cycle (JMP or CALL) can be executed

CYES = “1”: two instructions cycles (JMP and CALL) can be executed

Bit 8 (HLFS): main or sub-oscillator select

HLFS = “0”: CPU is set to select sub-oscillator when a reset occurs.

HLFS = “1”: CPU is set to select main-oscillator when a reset occurs.

Bit 7 (ENWDTB): Watchdog timer enable/disable bit.

ENWDTB = “0”: Enable watchdog timer.

ENWDTB = “1”: Disable watchdog timer.

Bit 6 (FSMD): sub-oscillator type selection.

Bits 5, 4 (FMMD1, 0): main Oscillator type selection.

| FSMD | FMMD1 | FMMD0 | Main Oscillator Type | Sub Oscillator Type |
|------|-------|-------|----------------------|---------------------|
| 0 | 0 | 0 | RC type | RC type |
| 0 | 0 | 1 | Crystal type | RC type |
| 0 | 1 | × | PLL type | RC type |
| 1 | 0 | 0 | RC type | Crystal type |
| 1 | 0 | 1 | Crystal type | Crystal type |
| 1 | 1 | × | PLL type | Crystal type |

Bit 3 (HLP): Power consumption selection. If the system usually runs in green mode, it must be set to low power consumption to help support the energy saving issue. It is recommended that low power consumption mode is selected.

HLP = “0”: Low power consumption mode

HLP = “1”: High power consumption mode

Bits 2~0 (0): These bits are set to “0” all the time.

6.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2",). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

Execute within two instruction cycles the "JMP", "CALL", "RET", "RETL", & "RETI" instructions, or the conditional skip instructions ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") which were tested to be true. Also execute within two instruction cycles the instructions that are written to the program counter.

Additionally, the instruction set offers the following features:

- (1) Every bit of any register can be set, cleared, or tested directly.
- (2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

**Convention:**

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

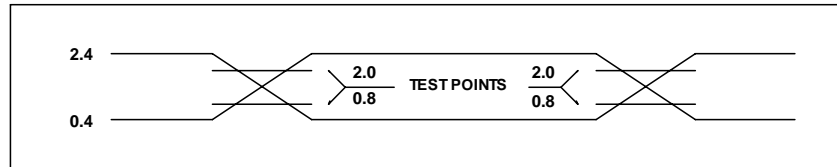
| Binary Instruction | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|----------|---------------------------------------|-------------------|
| 0 0000 0000 0000 | 0000 | NOP | No Operation | None |
| 0 0000 0000 0001 | 0001 | DAA | Decimal Adjust A | C |
| 0 0000 0000 0011 | 0003 | SLEP | 0 → WDT, Stop oscillator | T, P |
| 0 0000 0000 0100 | 0004 | WDTC | 0 → WDT | T, P |
| 0 0000 0000 rrrr | 000r | IOW R | A → IOCR | None [†] |
| 0 0000 0001 0000 | 0010 | ENI | Enable Interrupt | None |
| 0 0000 0001 0001 | 0011 | DISI | Disable Interrupt | None |
| 0 0000 0001 0010 | 0012 | RET | [Top of Stack] → PC | None |
| 0 0000 0001 0011 | 0013 | RETI | [Top of Stack] → PC, Enable Interrupt | None |
| 0 0000 0001 rrrr | 001r | IOR R | IOCR → A | None [†] |
| 0 0000 01rr rrrr | 00rr | MOV R, A | A → R | None |
| 0 0000 1000 0000 | 0080 | CLRA | 0 → A | Z |
| 0 0000 11rr rrrr | 00rr | CLR R | 0 → R | Z |
| 0 0001 00rr rrrr | 01rr | SUB A, R | R-A → A | Z,C,DC |
| 0 0001 01rr rrrr | 01rr | SUB R, A | R-A → R | Z,C,DC |
| 0 0001 10rr rrrr | 01rr | DECA R | R-1 → A | Z |
| 0 0001 11rr rrrr | 01rr | DEC R | R-1 → R | Z |
| 0 0010 00rr rrrr | 02rr | OR A, R | A ∨ R → A | Z |
| 0 0010 01rr rrrr | 02rr | OR R, A | A ∨ R → R | Z |
| 0 0010 10rr rrrr | 02rr | AND A, R | A & R → A | Z |
| 0 0010 11rr rrrr | 02rr | AND R, A | A & R → R | Z |
| 0 0011 00rr rrrr | 03rr | XOR A, R | A ⊕ R → A | Z |
| 0 0011 01rr rrrr | 03rr | XOR R, A | A ⊕ R → R | Z |
| 0 0011 10rr rrrr | 03rr | ADD A, R | A + R → A | Z,C,DC |
| 0 0011 11rr rrrr | 03rr | ADD R, A | A + R → R | Z,C,DC |
| 0 0100 00rr rrrr | 04rr | MOV A, R | R → A | Z |
| 0 0100 01rr rrrr | 04rr | MOV R, R | R → R | Z |
| 0 0100 10rr rrrr | 04rr | COMA R | /R → A | Z |
| 0 0100 11rr rrrr | 04rr | COM R | /R → R | Z |
| 0 0101 00rr rrrr | 05rr | INCA R | R+1 → A | Z |
| 0 0101 01rr rrrr | 05rr | INC R | R+1 → R | Z |
| 0 0101 10rr rrrr | 05rr | DJZA R | R-1 → A, skip if zero | None |
| 0 0101 11rr rrrr | 05rr | DJZ R | R-1 → R, skip if zero | None |

| Binary Instruction | | | | | Hex | Mnemonic | Operation | Status Affected |
|--------------------|------|------|------|--|------|----------|--|-----------------|
| 0 | 0110 | 00rr | rrrr | | 06rr | RRCA R | $R(n) \rightarrow A(n-1)$, $R(0) \rightarrow C$, $C \rightarrow A(7)$ | C |
| 0 | 0110 | 01rr | rrrr | | 06rr | RRC R | $R(n) \rightarrow R(n-1)$, $R(0) \rightarrow C$, $C \rightarrow R(7)$ | C |
| 0 | 0110 | 10rr | rrrr | | 06rr | RLCA R | $R(n) \rightarrow A(n+1)$, $R(7) \rightarrow C$, $C \rightarrow A(0)$ | C |
| 0 | 0110 | 11rr | rrrr | | 06rr | RLC R | $R(n) \rightarrow R(n+1)$, $R(7) \rightarrow (C)$, $C \rightarrow (R(0))$ | C |
| 0 | 0111 | 00rr | rrrr | | 07rr | SWAPA R | $R(0-3) \rightarrow (A(4-7))$, $R(4-7) \rightarrow (A(0-3))$ | None |
| 0 | 0111 | 01rr | rrrr | | 07rr | SWAP R | $R(0-3) \rightarrow (R(4-7))$ | None |
| 0 | 0111 | 10rr | rrrr | | 07rr | JZA R | $R+1 \rightarrow A$, skip if zero | None |
| 0 | 0111 | 11rr | rrrr | | 07rr | JZ R | $R+1 \rightarrow R$, skip if zero | None |
| 0 | 100b | bbrr | rrrr | | 0xxx | BC R, b | $0 \rightarrow (R(b))$ | None |
| 0 | 101b | bbrr | rrrr | | 0xxx | BS R, b | $1 \rightarrow (R(b))$ | None |
| 0 | 110b | bbrr | rrrr | | 0xxx | JBC R, b | if $R(b)=0$, skip | None |
| 0 | 111b | bbrr | rrrr | | 0xxx | JBS R, b | if $R(b)=1$, skip | None |
| 1 | 00kk | kkkk | kkkk | | 1kkk | CALL k | $PC+1 \rightarrow [SP]$, $(Page, k) \rightarrow (PC)$ | None |
| 1 | 01kk | kkkk | kkkk | | 1kkk | JMP k | $(Page, k) \rightarrow (PC)$ | None |
| 1 | 1000 | kkkk | kkkk | | 18kk | MOV A, k | $k \rightarrow A$ | None |
| 1 | 1001 | kkkk | kkkk | | 19kk | OR A, k | $A \vee k \rightarrow A$ | Z |
| 1 | 1010 | kkkk | kkkk | | 1Akk | AND A, k | $A \& k \rightarrow A$ | Z |
| 1 | 1011 | kkkk | kkkk | | 1Bkk | XOR A, k | $A \oplus k \rightarrow A$ | Z |
| 1 | 1100 | kkkk | kkkk | | 1Ckk | RETL k | $k \rightarrow A$, [Top of Stack] $\rightarrow PC$ | None |
| 1 | 1101 | kkkk | kkkk | | 1Dkk | SUB A, k | $k-A \rightarrow A$ | Z,C,DC |
| 1 | 1111 | kkkk | kkkk | | 1Fkk | ADD A, k | $k+A \rightarrow A$ | Z,C,DC |
| 1 | 1110 | 1000 | kkkk | | 1E8k | PAGE k | $K \rightarrow R5(6:4)$ | None |
| 1 | 1110 | 1001 | kkkk | | 1E9k | BANK k | $K \rightarrow R4(7:6)$ | None |

Note: ¹ This instruction is applicable to IOC50~IOF0, IOC61~IOCE1.

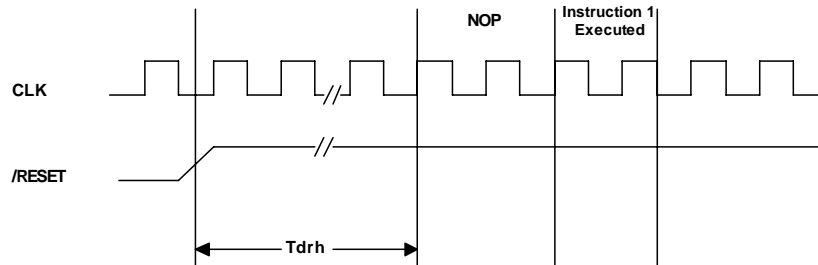
6.13 Timing Diagram

AC Test Input/Output Waveform

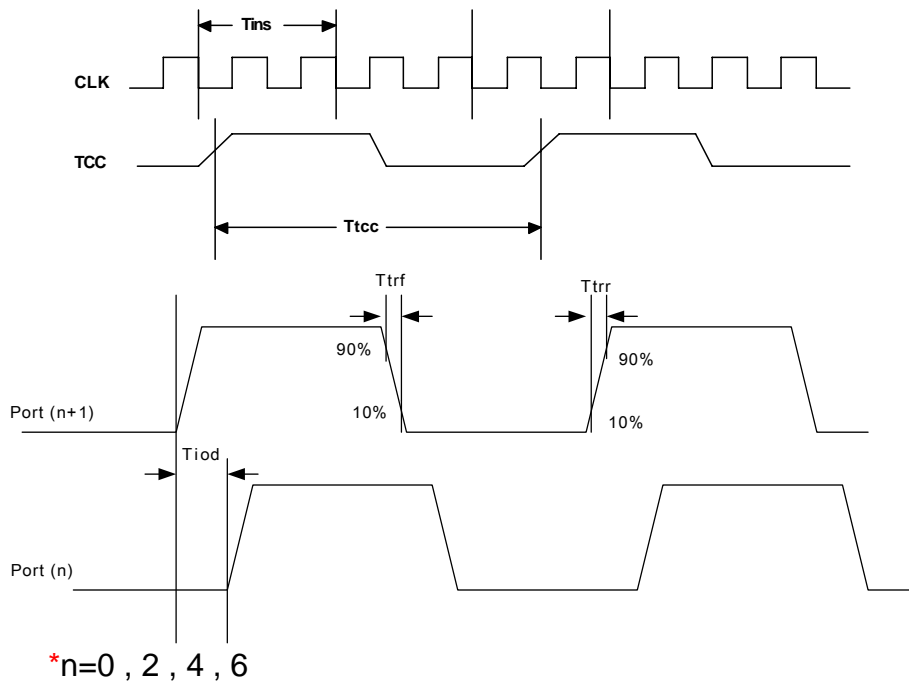


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



7 Absolute Maximum Ratings

| Items | Symbol | Condition | Rating | | Unit |
|-----------------------|------------------|-----------------|---------|---------|------|
| | | | Min. | Max. | |
| Supply voltage | VDD | – | GND-0.3 | +7.0 | V |
| Input voltage | V _I | Port 5 ~ Port 8 | GND-0.3 | VDD+0.3 | V |
| Output voltage | V _O | Port 5 ~ Port 8 | GND-0.3 | VDD+0.3 | V |
| Operation temperature | T _{OPR} | – | 0 | 70 | °C |
| Storage temperature | T _{STG} | – | -65 | 150 | °C |
| Power consumption | P _D | – | – | 500 | mW |
| Operating Frequency | – | – | 32.768K | 10M | Hz |

8 Electrical Characteristic

8.1 DC Electrical Characteristics

Ta= 25°C, VDD= 5.0V, GND= 0V

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|--|---|--------|--------|------|------|
| FXT | Crystal: VDD to 5V | Two cycles with two clocks | 32.768 | 8M | 10M | kHz |
| Fs | Sub-oscillator | Two cycles with two clocks | – | 32.768 | – | kHz |
| ERIC | External R, Internal C for Sub-oscillator | R: 300KΩ, internal capacitance | 270 | 384 | 500 | kHz |
| | External R, Internal C for Sub-oscillator | R: 2.2MΩ, internal capacitance | 22.9 | 32.768 | 42.6 | kHz |
| IIL | Input Leakage Current for Input pins | VIN = VDD, GND | -1 | 0 | 1 | μA |
| VIH1 | Input High Threshold Voltage (Schmitt Trigger) | Ports 5, 6, 7, 8 | 2.4 | – | – | V |
| VIL1 | Input High Threshold Voltage (Schmitt Trigger) | Ports 5, 6, 7, 8 | – | – | 0.8 | V |
| VIHT1 | Input High Threshold Voltage (Schmitt Trigger) | /RESET | 2.4 | – | – | V |
| VILT1 | Input Low Threshold Voltage (Schmitt Trigger) | /RESET | – | – | 0.8 | V |
| VIHT2 | Input High Threshold Voltage (Schmitt Trigger) | TCC, INT0, INT1 | 2.4 | – | – | V |
| VILT2 | Input Low Threshold Voltage (Schmitt Trigger) | TCC, INT0, INT1 | – | – | 0.8 | V |
| IOH1 | Output High Voltage (Ports 5~8) | VOH = 2.4V, IROCS="0" | -9 | – | – | mA |
| IOL1 | Output Low Voltage (Ports 5~8) | VOL = 0.4V, IROCS="0" | – | – | 9 | mA |
| IOH1 | Output high voltage (P5.7/IROUT pin) | VOH = 2.4V, IROCS="1" | -18 | – | – | mA |
| IOL2 | Output Low Voltage (P5.7/IR OUT pin) | VOL = 0.4V, IROCS="1" | – | – | 18 | mA |
| IPH | Pull-high current | Pull-high active, input pin at GND | -55 | -75 | -95 | μA |
| IPL | Pull-low current | Pull-low active, input pin at VDD | 55 | 75 | 95 | μA |
| ISB | Sleep mode current | All input and I/O pins at VDD, Output pin floating, WDT disabled | – | 0.5 | 1.5 | μA |
| ICC1 | Idle mode current | /RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, LCD enabled, no load | – | 14 | 18 | μA |
| ICC2 | Green mode current | /RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled | – | 22 | 30 | μA |
| ICC3 | Normal mode | /RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating | – | 2.2 | 3 | mA |
| ICC4 | Normal mode | /RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating | – | 3.1 | 4 | mA |

Ta= 25 °C, VDD= 3.0V, GND= 0V

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|--------|--|---|--------|--------|------|---------|
| FXT | Crystal: VDD to 5V | Two cycles with two clocks | 32.768 | 8M | 10M | kHz |
| Fs | Sub-oscillator | Two cycles with two clocks | – | 32.768 | – | kHz |
| ERIC | External R, Internal C for Sub-oscillator | R: 300K Ω , internal capacitance | 270 | 384 | 500 | kHz |
| | External R, Internal C for Sub-oscillator | R: 2.2M Ω , internal capacitance | 22.9 | 32.768 | 42.6 | kHz |
| IIL | Input Leakage Current for Input pins | VIN = VDD, GND | -1 | 0 | 1 | μ A |
| VIH1 | Input High Threshold Voltage (Schmitt Trigger) | Ports 5, 6, 7, 8 | 1.8 | – | – | V |
| VIL1 | Input High Threshold Voltage (Schmitt Trigger) | Ports 5, 6, 7, 8 | – | – | 0.6 | V |
| VIHT1 | Input High Threshold Voltage (Schmitt Trigger) | /RESET | 1.8 | – | – | V |
| VILT1 | Input Low Threshold Voltage (Schmitt Trigger) | /RESET | – | – | 0.6 | V |
| VIHT2 | Input High Threshold Voltage (Schmitt Trigger) | TCC, INT0, INT1 | 1.8 | – | – | V |
| VILT2 | Input Low Threshold Voltage (Schmitt Trigger) | TCC, INT0, INT1 | – | – | 0.6 | V |
| IOH1 | Output High Voltage (Ports 5~8) | VOH = 2.4V, IROCS="0" | -1.8 | – | – | mA |
| IOL1 | Output Low Voltage (Ports 5~8) | VOL = 0.4V, IROCS="0" | – | – | 6 | mA |
| IOH1 | Output high voltage (P5.7/IROUT pin) | VOH = 2.4V, IROCS="1" | -3.5 | – | – | mA |
| IOL2 | Output Low Voltage (P5.7/IR OUT pin) | VOL = 0.4V, IROCS="1" | – | – | 12 | mA |
| IPH | Pull-high current | Pull-high active, input pin at GND | -16 | -23 | -30 | μ A |
| IPL | Pull-low current | Pull-low active, input pin at VDD | 16 | 23 | 30 | μ A |
| ISB | Sleep mode current | All input and I/O pins at VDD, Output pin floating, WDT disabled | – | 0.1 | 1 | μ A |
| ICC1 | Idle mode current | /RESET= 'High', CPU OFF, Sub-oscillator clock (32.768kHz) ON, output pin floating, LCD enabled, no load | – | 4 | 8 | μ A |
| ICC2 | Green mode current | /RESET= 'High', CPU ON, Sub-oscillator clock (32.768kHz), Output pin floating, WDT enabled, LCD enabled | – | 10 | 20 | μ A |
| ICC3 | Normal mode | /RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating | – | .73 | 1.2 | mA |

8.2 AC Electrical Characteristics

Ta = -40°C ~ 85 °C, VDD = 5V ± 5%, GND = 0V

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------------------------------|--------------|--------------|------|------|------|
| Dclk | Input CLK duty cycle | – | 45 | 50 | 55 | % |
| Tins | Instruction cycle time (CLKS="0") | Crystal type | 100 | – | DC | ns |
| | | RC type | 500 | – | DC | ns |
| Ttcc | TCC input period | – | (Tins+20)/N* | – | – | ns |
| Tdrh | Device reset hold time | Ta = 25°C | 11.3 | 16.2 | 21.6 | ms |
| Trst | /RESET pulse width | Ta = 25°C | 2000 | – | – | ns |
| Twdt | Watchdog timer period | Ta = 25°C | 11.3 | 16.2 | 21.6 | ms |
| Tset | Input pin setup time | – | – | 0 | – | ns |
| Thold | Input pin hold time | – | – | 20 | – | ns |
| Tdelay | Output pin delay time | Cload = 20pF | – | 50 | – | ns |

* N = selected prescaler ratio

9 Application Circuit

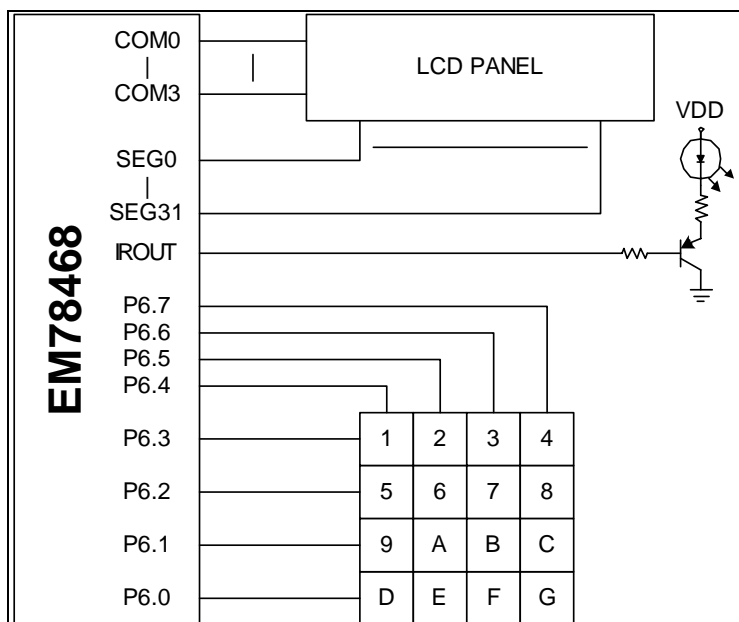


Fig. 9-1 IROUT Control External BJT Circuit to Drive Infrared Emitting Diodes

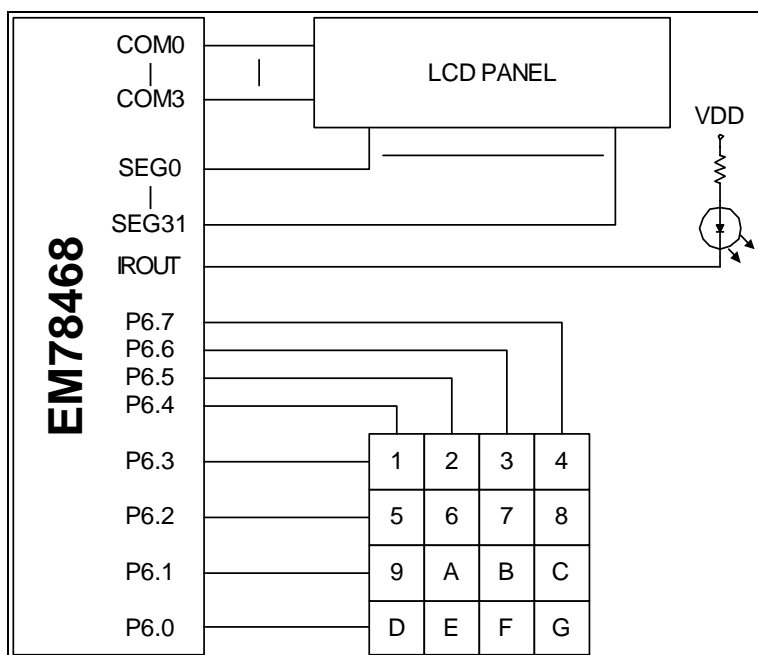


Fig. 9-2 IROUT Direct Drive Infrared Emitting Diodes

APPENDIX

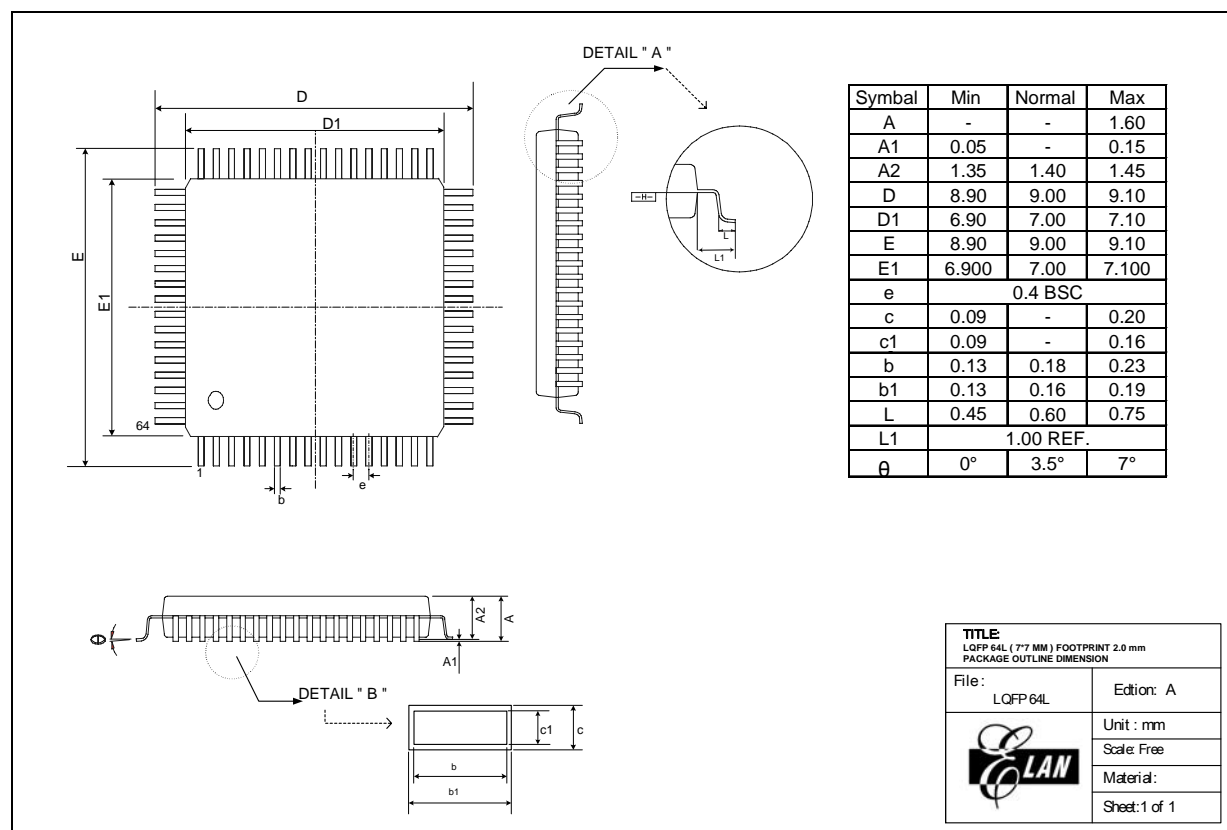
A Packaging

A.1 Package Type

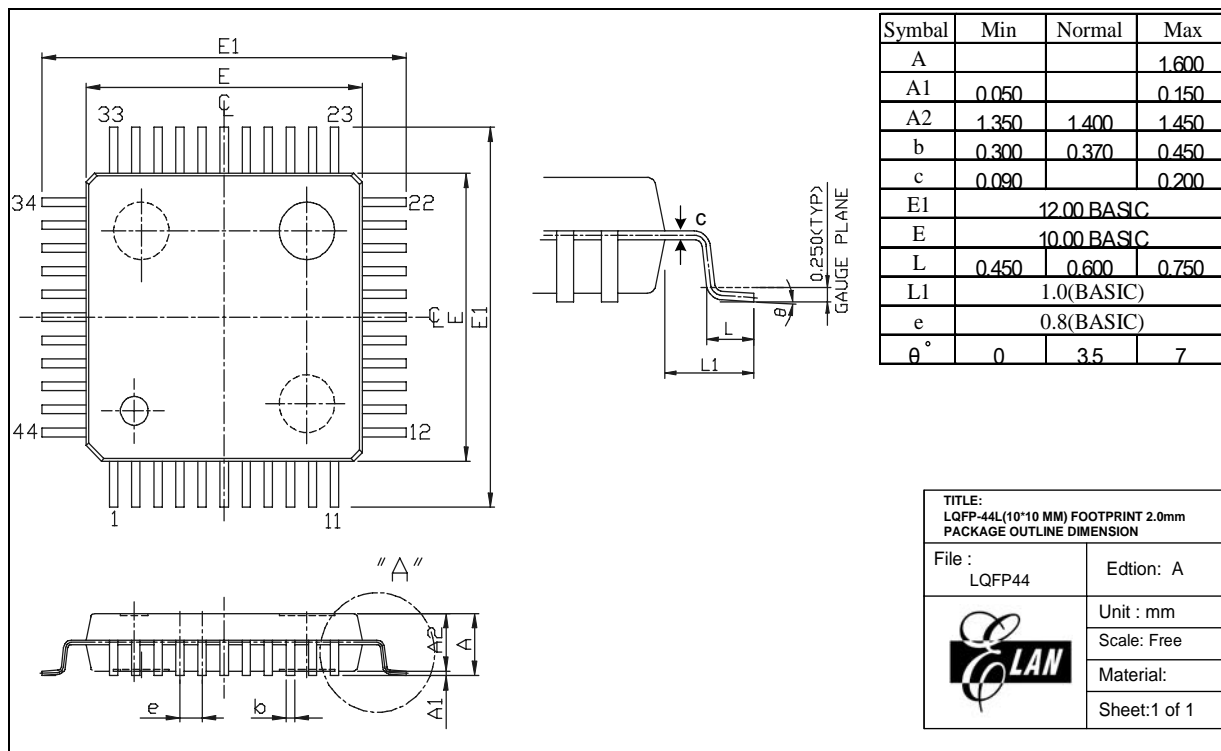
| Name | Package Type | Pin Count | Package Body Size |
|-----------|--------------|-----------|-------------------|
| EM78468H | Dice | 59 | — |
| EM78468AQ | LQFP | 64 | 7 mm × 7 mm |
| EM78468BQ | LQFP | 44 | 10 mm × 10 mm |

A.2 Package Information

LQFP – 64



LQFP – 44

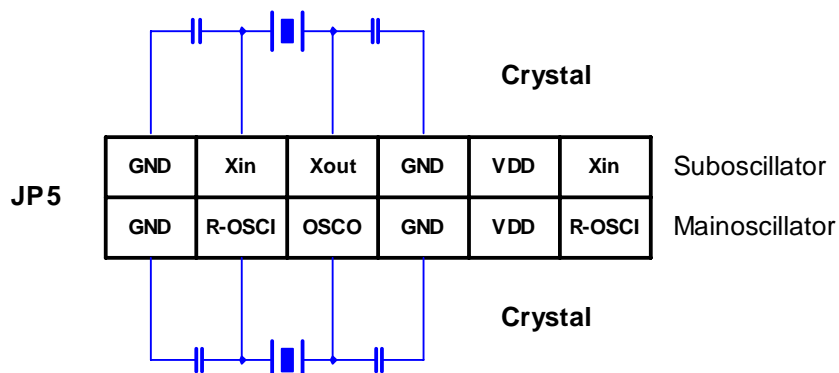


B ICE 468XA

B.1 ICE 468XA Oscillator Circuit (JP 5)

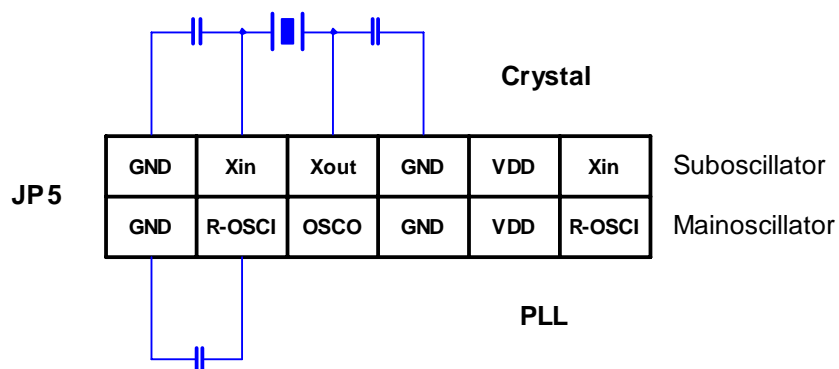
Mode 1:

Main oscillator: Crystal mode, Sub oscillator: Crystal mode



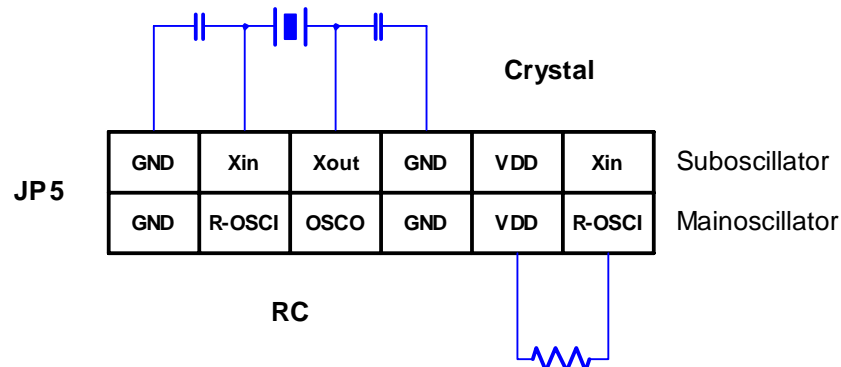
Mode 2:

Main oscillator: PLL mode, Sub oscillator: Crystal mode



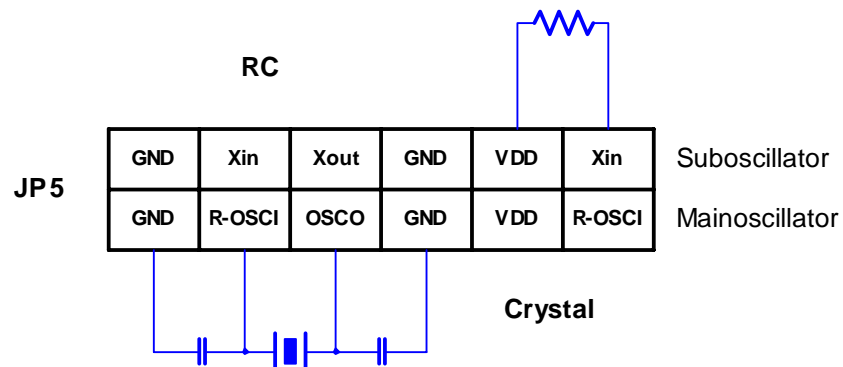
Mode 3:

Main oscillator: RC mode, Sub oscillator: Crystal



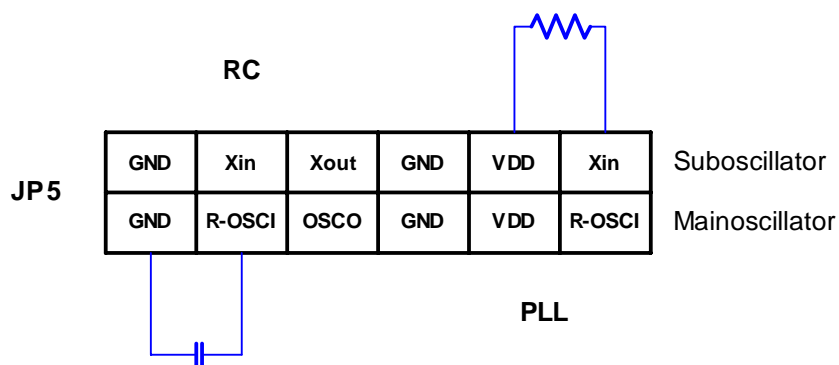
Mode 4:

Main oscillator: Crystal mode, Sub oscillator: RC mode



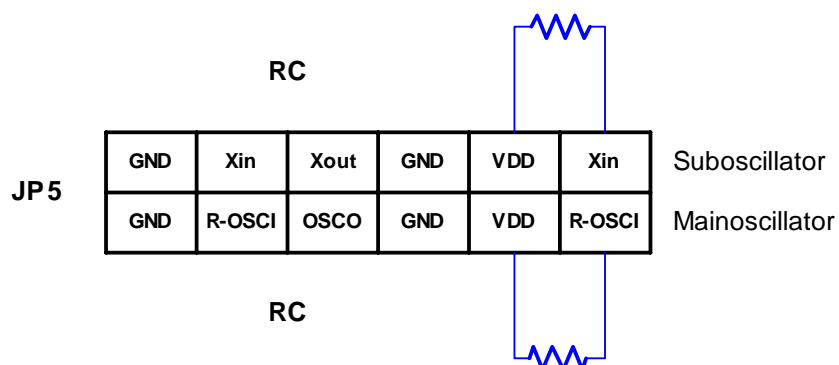
Mode 5:

Main oscillator: PLL mode, Sub oscillator: RC mode



Mode 6:

Main oscillator: RC mode, Sub oscillator: RC mode



B.2 ICE 468XA Output Pin Assignment (JP 3)

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|--|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| JP 3 | VA | | | | | | | | | | | | | | | | VB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | 34 | 36 | 38 | 40 | 42 | 44 | 46 | 48 | 50 | 52 | 54 | 56 | 58 | 60 | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31 | 33 | 35 | 37 | 39 | 41 | 43 | 45 | 47 | 49 | 51 | 53 | 55 | 57 |
| | VLCD3 GND OSCO Xin P5.4/INT0 P5.6/TCC P6.0 P6.2 P6.4 P6.6 SEG31/P8.7 SEG29/P8.5 SEG27/P8.3 SEG25/P8.1 SEG23/P7.7 SEG21/P7.5 SEG19/P7.3 SEG17/P7.1 SEG15 SEG13 SEG11 SEG9 SEG7 SEG5 SEG3 SEG1 COM3 COM1 X | | | | | | | | | | | | | | | | VLCD2 /RESET R-OSCI VDD Xout P5.5/INT1 P5.7/ROUT P6.1 P6.3 P6.5 P6.7 SEG30/P8.6 SEG28/P8.4 SEG26/P8.2 SEG24/P8.0 SEG22/P7.6 SEG20/P7.4 SEG18/P7.2 SEG16/P7.0 SEG14 SEG12 SEG10 SEG8 SEG6 SEG4 SEG2 SEG0 COM2 COM0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

C Quality Assurance and Reliability

| Test Category | Test Conditions | Remarks |
|--|--|---|
| Solderability | Solder temperature= $245\pm 5^{\circ}\text{C}$, for 5 seconds up to the stopper using a rosin-type flux | — |
| Pre-condition | Step 1: TCT, 65°C (15mins)~ 150°C (15mins), 10 cycles | For SMD IC (such as SOP, QFP, SOJ, etc) |
| | Step 2: Bake at 125°C , TD (endurance)=24 hrs | |
| | Step 3: Soak at $30^{\circ}\text{C}/60\%$, TD (endurance)=192 hrs | |
| | Step 4: IR flow 3 cycles (Pkg thickness $\geq 2.5\text{mm}$ or Pkg volume $\geq 350\text{mm}^3$ ---- $225\pm 5^{\circ}\text{C}$) (Pkg thickness $\leq 2.5\text{mm}$ or Pkg volume $\leq 350\text{mm}^3$ ---- $240\pm 5^{\circ}\text{C}$) | |
| Temperature cycle test | -65°C (15mins)~ 150°C (15mins), 200 cycles | — |
| Pressure cooker test | $T_A = 121^{\circ}\text{C}$, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs | — |
| High temperature / High humidity test | $T_A = 85^{\circ}\text{C}$, RH=85%, TD (endurance) = 168, 500 hrs | — |
| High-temperature storage life | $T_A = 150^{\circ}\text{C}$, TD (endurance) = 500, 1000 hrs | — |
| High-temperature operating life | $T_A = 125^{\circ}\text{C}$, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs | — |
| Latch-up | $T_A = 25^{\circ}\text{C}$, VCC = Max. operating voltage, 150mA/20V | — |
| ESD (HBM) | $T_A = 25^{\circ}\text{C}$, $\geq \pm 3\text{KV}$ | IP_ND, OP_ND, IO_ND IP_NS, OP_NS, IO_NS IP_PD, OP_PD, IO_PD |
| ESD (MM) | $T_A = 25^{\circ}\text{C}$, $\geq \pm 300\text{V}$ | IP_PS, OP_PS, IO_PS VDD-VSS(+), VDD_VSS (-) Mode |

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.