



17-V, 1.5-A SYNCHRONOUS STEP-DOWN CONVERTER

FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **High-Efficiency Synchronous Step-Down Converter With up to 95% Efficiency**
- **3.1-V to 17-V Operating Input Voltage Range**
- **Adjustable Output Voltage Range From 1.2 V to 16 V**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Fixed Output Voltage Options Available in 3.3 V and 5 V**
- **Synchronizable to External Clock Signal up to 1.4 MHz**
- **Up to 1.5-A Output Current**
- **High Efficiency Over a Wide Load-Current Range Due to PFM/PWM Operation Mode**
- **100% Maximum Duty Cycle for Lowest Dropout**
- **20- μ A Quiescent Current (Typical)**
- **Overtemperature and Overcurrent Protected**
- **Available in 16-Pin QFN Package**

APPLICATIONS

- **Point-of-Load Regulation From 12-V Bus**
- **Organizers, PDAs, and Handheld PCs**
- **Handheld Scanners**

DESCRIPTION/ORDERING INFORMATION

The TPS62110-EP device is a low-noise synchronous step-down dc-dc converter that is ideally suited for systems powered from a 2-cell Li-ion battery or from a 12-V or 15-V rail.

The TPS62110-EP is a synchronous PWM converter with integrated – and P-channel power MOSFET switches. Synchronous rectification is used to increase efficiency and to reduce external component count. To achieve highest efficiency over a wide load-current range, the converter enters a power-saving, pulse frequency modulation (PFM) mode at light load currents. Operating frequency is typically 1 MHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 0.8 MHz to 1.4 MHz. For low noise operation, the converter can be operated in PWM-only mode. In the shutdown mode, the current consumption is reduced to less than 2 μ A. The TPS62110-EP is available in the 16-pin (RSA) QFN package, and operates over a free-air temperature range of –55°C to 125°C.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges; HBM according to EIA/JESD22-A114-B, MM according to EIA/JESD22-A115-A, and CDM according to EIA/JESD22C101C; however, it is advised that precautions be taken to avoid application of any voltage higher



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than maximum-rated voltages to these high-impedance circuits. During storage or handling the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

ORDERING INFORMATION

T _A	ORDERABLE PART NUMBER 16-Pin (RSA) QFN	OUTPUT VOLTAGE	LBI/LBO FUNCTIONALITY	MARKING
–55°C to 125°C	TPS62110MRSAREP	Adjustable 1.2 V to 16 V	Standard	TPS62110-EP

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	UNIT	
V _{CC} Supply voltage at VIN, VINA	–0.3 V to 20 V	
V _I	Voltage at SW	–0.3 V to V _I
	Voltage at EN, SYNC, LBO, PG	–0.3 V to 20 V
	Voltage at LBI, FB	–0.3 V to 7 V
I _O Output current at SW	2400 mA	
T _J Maximum junction temperature ⁽²⁾	150°C	
T _{stg} Storage temperature	–65°C to 150°C	
	Lead temperature 1,6 mm (1/16-in) from case for 10 s	300°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Long-term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information about enhanced plastic packaging.

DISSIPATION RATINGS⁽¹⁾

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
RSA	2.5 W	25 mW/°C	1.375 W	1 W

- (1) Based on a thermal resistance of 40 K/W soldered onto a high K board

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
V _{CC} Supply voltage at VIN, VINA	3.1	17	V
Maximum voltage at power-good, LBO, EN, SYNC		17	V
T _J Operating junction temperature	–55	125	°C

ELECTRICAL CHARACTERISTICS
 $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $I_O = 600\text{ mA}$, $EN = V_I$, $T_A = T_J = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range ⁽¹⁾		3.1		17	V
$I_{(Q)}$	Operating quiescent current	$I_O = 0\text{ mA}$, SYNC = GND, $V_I = 7.2\text{ V}$, $T_A = 25^\circ\text{C}$ ⁽²⁾		20		μA
		$I_O = 0\text{ mA}$, SYNC = GND, $V_I = 17\text{ V}$ ⁽²⁾		23	26	
$I_{(SD)}$	Shutdown current	EN = GND		1.5	5	μA
		EN = GND, $T_A = 25^\circ\text{C}$, $V_I = 7.2\text{ V}$		1.5	3	
ENABLE						
V_{IH}	EN high-level input voltage		1.3			V
V_{IL}	EN low-level input voltage				0.3	V
	EN trip-point hysteresis			170		mV
I_{IKG}	EN input leakage current	EN = GND or V_I , $V_I = 17\text{ V}$		0.01	0.2	μA
$I_{(EN)}$	EN input current	$0.6\text{ V} \leq V_{(EN)} \leq 4\text{ V}$		10		μA
$V_{(UVLO)}$	Undervoltage lockout threshold	Input voltage falling	2.8	3	3.1	V
	Undervoltage lockout hysteresis			250		mV
POWER SWITCH						
$r_{DS(ON)}$	P-channel MOSFET on resistance	$V_I \geq 5.4\text{ V}$, $I_O = 350\text{ mA}$		165	250	$\text{m}\Omega$
		$V_I = 3.5\text{ V}$, $I_O = 200\text{ mA}$		340		
		$V_I = 3\text{ V}$, $I_O = 100\text{ mA}$		490		
	P-channel MOSFET leakage current	$V_{DS} = 17\text{ V}$		0.1	1	μA
	P-channel MOSFET current limit	$V_I = 7.2\text{ V}$, $V_O = 3.3\text{ V}$		2400		mA
$r_{DS(ON)}$	N-channel MOSFET on resistance	$V_I \geq 5.4\text{ V}$, $I_O = 350\text{ mA}$		145	200	$\text{m}\Omega$
		$V_I = 3.5\text{ V}$, $I_O = 200\text{ mA}$		170		
		$V_I = 3\text{ V}$, $I_O = 100\text{ mA}$		200		
	N-channel MOSFET leakage current	$V_{DS} = 17\text{ V}$		0.1	3	μA
POWER GOOD OUTPUT, LBI, LBO						
$V_{(PG)}$	PG trip voltage			$V_O - 1.6\%$		V
	PG delay time	V_O ramping positive		50		μs
		V_O ramping negative		200		
V_{OL}	PG, LBO output low voltage	$V_{FB} = 1.1 \times V_O$ nominal, $I_{OL} = 1\text{ mA}$			0.3	V
I_{OL}	PG, LBO sink current			1		mA
	PG, LBO output leakage current	$V_{FB} = V_O$ nominal		0.01	0.25	μA
	Minimum supply voltage for valid PG, LBI, LBO signal			3		V
V_{LBI}	LBI trip voltage	Input voltage falling		1.256		V
I_{LBI}	LBI input leakage current			10	100	nA
	LBI trip-point accuracy			1.5%		
$V_{LBI,HYS}$	LBI hysteresis			25		mV
OSCILLATOR						
f_S	Oscillator frequency		900	1000	1100	kHz
$f_{(SYNC)}$	Synchronization range	CMOS-logic clock signal on SYNC pin	800		1400	kHz
V_{IH}	SYNC high-level input voltage		1.5			V
V_{IL}	SYNC low-level input voltage				0.3	V

(1) Not Production Tested.

(2) Device is not switching.

ELECTRICAL CHARACTERISTICS (continued)
 $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$, $I_O = 600\text{ mA}$, $EN = V_I$, $T_A = T_J = -55^\circ\text{C}$ to 125°C (unless otherwise noted)

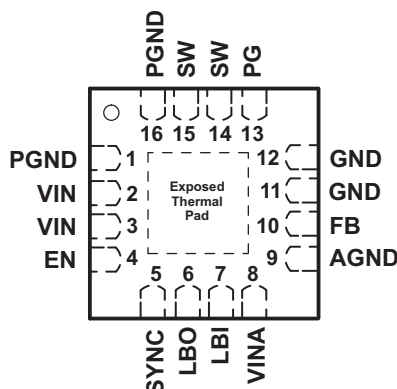
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IKG}	SYNC input leakage current	SYNC = GND or VIN		0.01	0.2	μA
	SYNC trip-point hysteresis			170		mV
	SYNC input current	$0.6\text{ V} \leq V_{I(\text{SYNC})} \leq 4\text{ V}$		10		μA
	Duty cycle of external clock signal		30%		90%	
OUTPUT						
V_O	Adjustable output voltage range ⁽³⁾		1.153		16	V
V_{FB}	FB voltage			1.153		V
	FB leakage current			10	100	nA
	FB voltage tolerance ⁽³⁾	$V_I = 3.1\text{ V}$ to 17 V , $0\text{ mA} < I_O < 1500\text{ mA}$ ⁽⁴⁾	-6%		6%	
I_O	Maximum output current	$V_I \geq 3\text{ V}$ (once undervoltage lockout voltage exceeded)		100		mA
		$V_I \geq 3.5\text{ V}$		500		
		$V_I \geq 4.3\text{ V}$		1200		
		$V_I \geq 6\text{ V}$		1500		
	Current into internal voltage divider for fixed-voltage versions			5		μA
η	Efficiency	$V_I = 7.2\text{ V}$, $V_O = 3.3\text{ V}$, $I_O = 600\text{ mA}$		92%		
		$V_I = 12\text{ V}$, $V_O = 5\text{ V}$, $I_O = 600\text{ mA}$				
	Duty-cycle range for main switches	At 1 MHz	10%		100%	
	Minimum t_{on} time for main switch			100		ns
	Shutdown temperature			145		$^\circ\text{C}$
	Start-up time	$I_O = 800\text{ mA}$, $V_I = 12\text{ V}$, $V_O = 3.3\text{ V}$		1		ms

(3) Not Production Tested.

(4) The maximum output current depends on the input voltage.

DEVICE INFORMATION

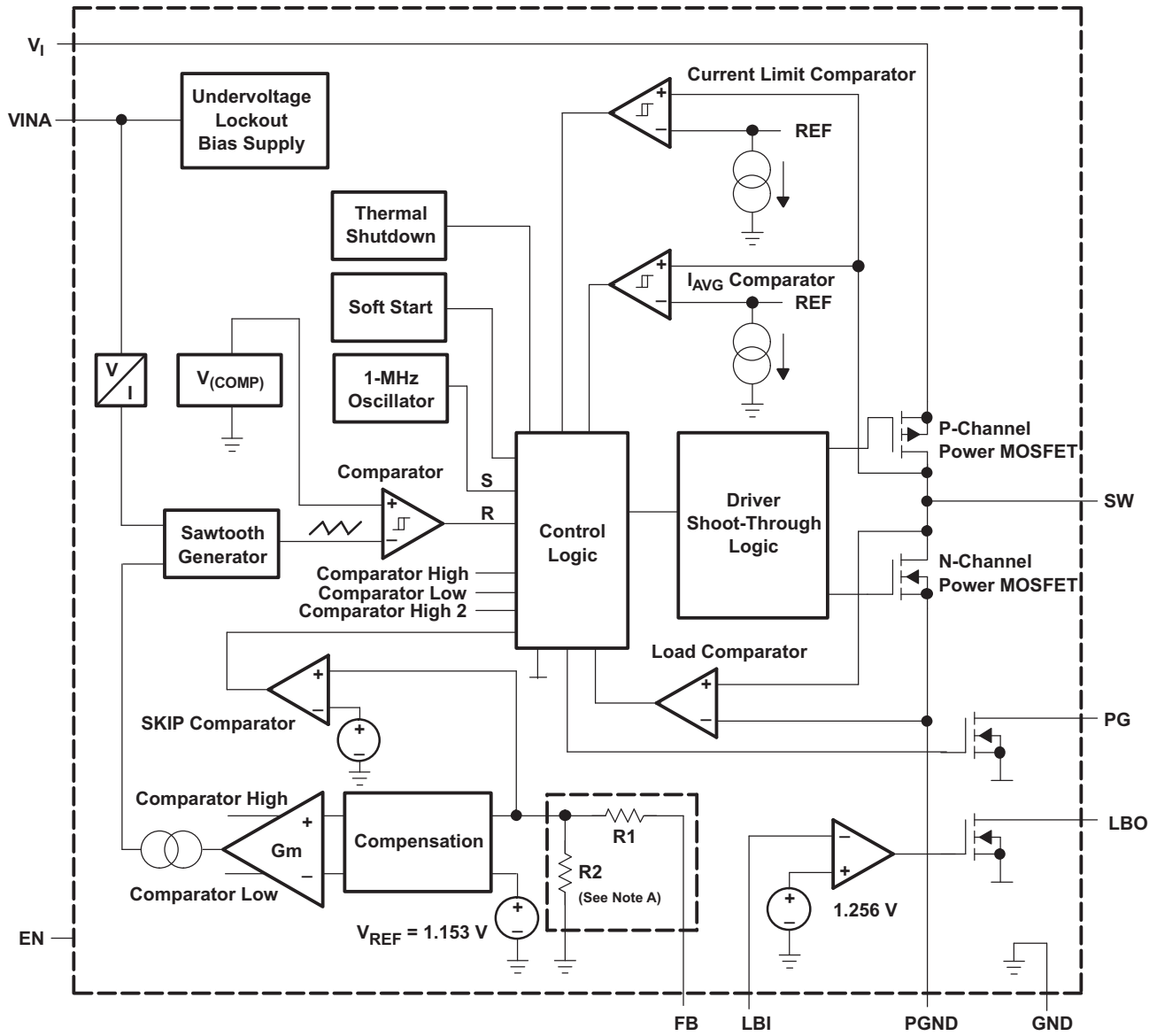
PIN ASSIGNMENT TOP VIEW



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	9	I	Analog ground. Connect to GND and PGND.
EN	4	I	Enable. A logic high enables the converter; logic low forces the device into shutdown mode reducing the supply current to less than 2 μ A.
FB	10	I	Feedback for the fixed output voltage option. For the adjustable version, an external resistive divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
GND	11, 12	I	Ground
LBI	7	I	Low-battery input
LBO	6	O	Low-battery output (open drain). This pin is pulled low if LBI is below its threshold.
PG	13	O	Power-good comparator. This is an open-drain output. A pullup resistor should be connected between PG and VOUT. The output goes active high when the output voltage is greater than 98.4% of the nominal value.
PGND	1, 16	I	Power ground. Connect all power grounds to this pin.
PowerPAD™			Connect to AGND
SW	14, 15	O	Switch. Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.
SYNC	5	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level: SYNC = HIGH: Low-noise mode enabled, fixed-frequency PWM operation is forced. SYNC = LOW (GND): Power-save mode enabled, PFM/PWM mode enabled
VIN	2, 3	I	Supply-voltage input (power stage)
VINA	8	I	Supply-voltage input (support circuits)

FUNCTIONAL BLOCK DIAGRAM



A. For the adjustable version (TPS62110-EP), the internal feedback divider is disabled and the FB pin is directly connected to the internal GM amplifier.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
Efficiency	vs	Output current (1.8 V)	1, 2
Efficiency	vs	Output current (1.5 V)	3, 4
Switching frequency	vs	Input voltage	5
Quiescent current	vs	Input voltage	6

Graphs with $V_O = 1.8\text{ V}$ were taken using the circuit according to [Figure 10](#).

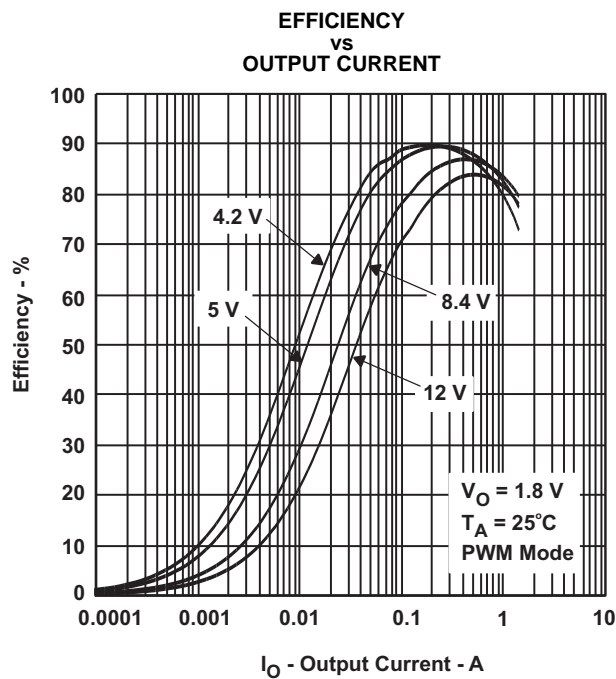


Figure 1.

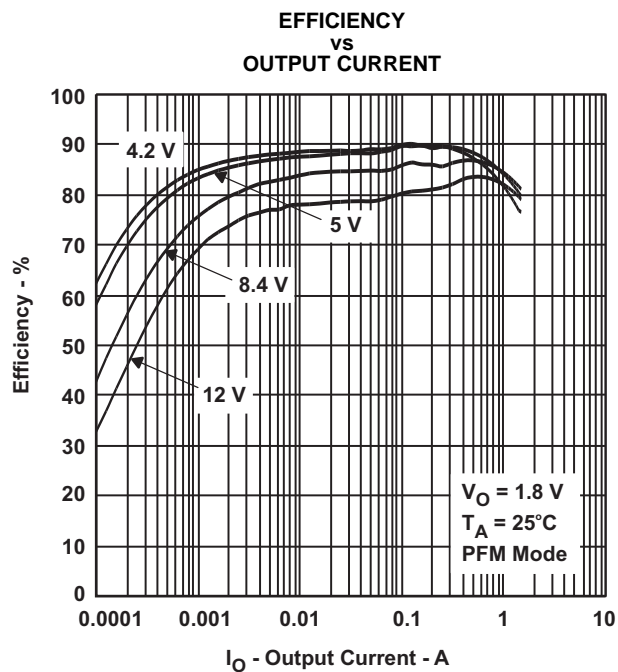


Figure 2.

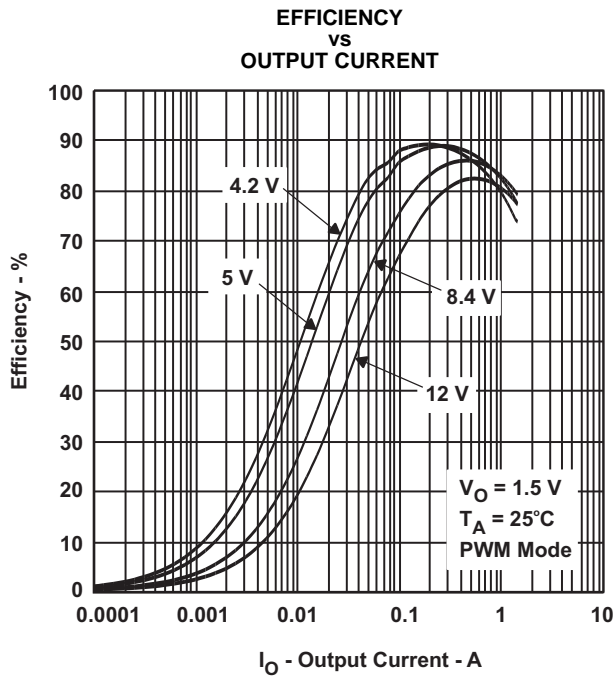


Figure 3.

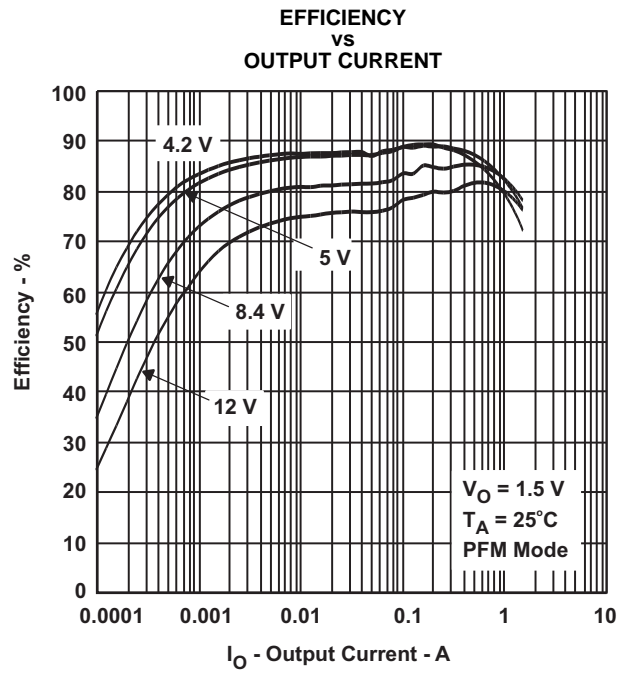


Figure 4.

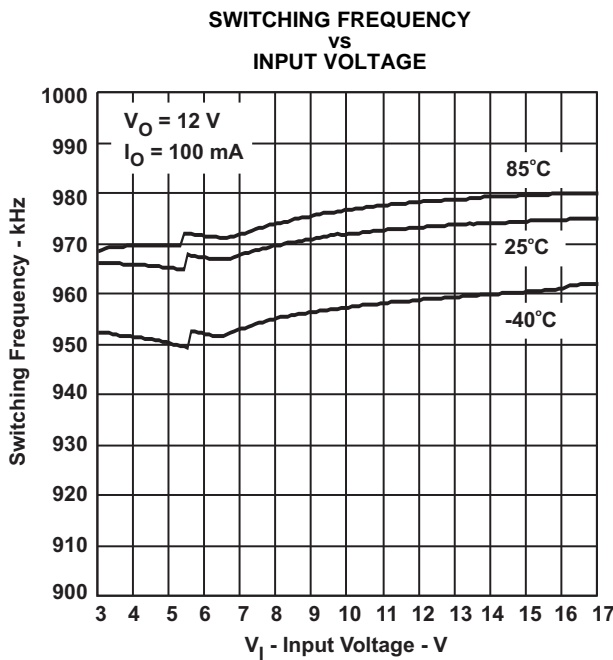


Figure 5.

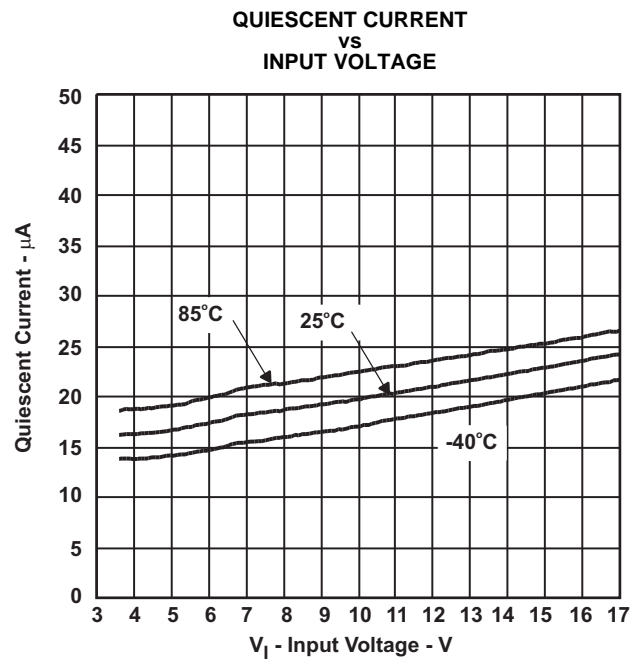


Figure 6.

The graphs were generated using the EVM with the setup according to [Figure 7](#), unless otherwise noted. The output voltage divider was adjusted according to [Table 4](#).

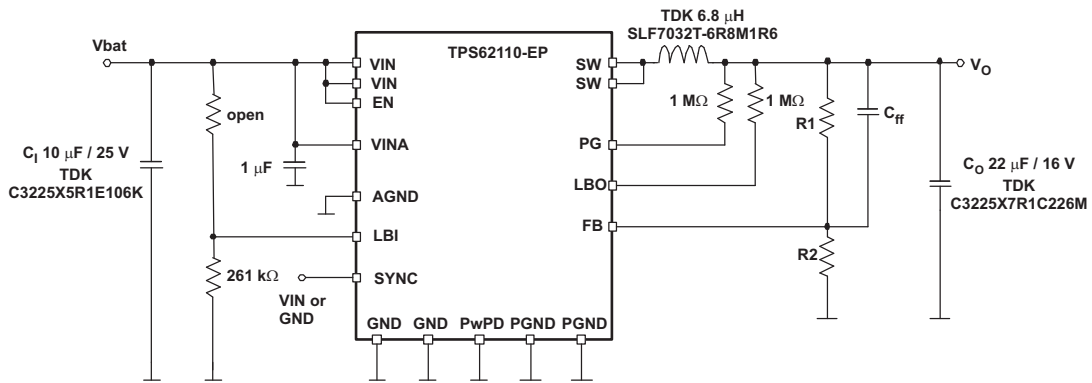


Figure 7. Test Setup

DETAILED DESCRIPTION

OPERATION

The TPS62110-EP is a synchronous step-down converter that operates with a 1-MHz fixed-frequency pulse width modulation (PWM) at moderate-to-heavy load currents and enters the power-save mode at light load current.

During PWM operation, the converter uses a unique fast-response voltage-mode control scheme with input voltage feedforward. Good line and load regulation is achieved with the use of small input and output ceramic capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns the switch off. The switch is turned off by the current limit comparator if the current limit of the P-channel switch is exceeded. After the dead time prevents current shoot through, the N-channel MOSFET rectifier is turned on, and the inductor current ramps down. The next cycle is initiated by the clock signal turning off the N-channel rectifier, and turning on the P-channel switch.

The error amplifier as well as the input voltage determines the rise time of the sawtooth generator. Therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter giving a very good line and load transient regulation.

CONSTANT FREQUENCY MODE OPERATION (SYNC = HIGH)

In constant frequency mode, the output voltage is regulated by varying the duty cycle of the PWM signal in the range of 100% to 10%. Connecting the SYNC pin to a voltage greater than 1.5 V forces the converter to operate permanently in the PWM mode even at light or no-load currents. The advantage is that the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. The N-MOSFET of the devices stay on even when the current into the output drops to zero. This prevents the device from going into discontinuous mode, and the device transfers unused energy back to the input. Therefore, there is no ringing at the output, which usually occurs in discontinuous mode. The duty cycle range in constant frequency mode is 100% to 10%.

It is possible to switch from forced PWM mode to the power-save mode during operation by pulling the SYNC pin LOW. The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS62110-EP to the specific system requirements.

POWER-SAVE MODE OPERATION (SYNC = LOW)

As the load current decreases, the converter enters the power-save mode operation. During power-save mode, the converter operates with reduced switching frequency in pulse frequency modulation (PFM), and with a minimum quiescent current to maintain high efficiency. When the average output current goes below the skip threshold, the converter enters the power-save mode. The average current depends on the input voltage. It is about 200 mA at low input voltages and up to 400 mA with maximum input voltage. The average output current must be below the threshold for at least 32 clock cycles to enter the power-save mode. During the power-save mode, the output voltage is monitored with a comparator and the output voltage is regulated in to a typical value between the nominal output voltage and 0.8% above the nominal output voltage. When the output voltage falls below the nominal output voltage, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The N-channel rectifier is turned on, and the inductor current ramps down. As the inductor current approaches zero, the N-channel rectifier is turned off and the switch is turned on starting the next pulse. When the output voltage can not be reached with a single pulse, the device continues to switch with its normal operating frequency until the comparator detects the output voltage to be 0.8% above the nominal output voltage. This control method reduces the quiescent current to 20 μ A (typical), and reduces the switching frequency to a minimum that achieves the highest converter efficiency.

DETAILED DESCRIPTION (continued)

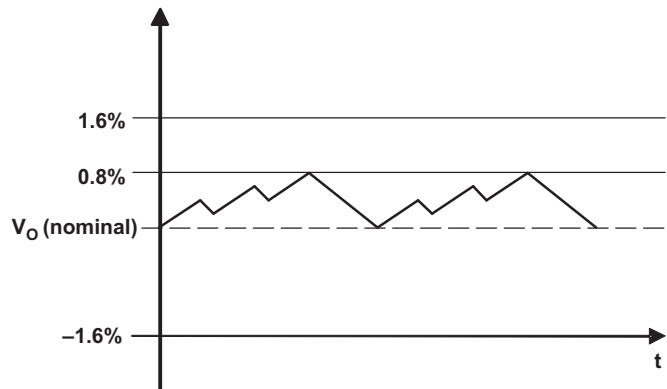


Figure 8. Power-Save Mode Output Voltage Thresholds

The typical PFM (skip) current threshold for the TPS62110-EP is given by:

$$I_{SKIP} \approx \frac{V_I}{25\Omega} \quad (1)$$

Equation 1 is valid for input voltages up to 7 V. For higher voltages, the skip current threshold is not increased further. The converter enters the fixed-frequency PWM mode as soon as the output voltage falls below $V_O - 1.6\%$ (nominal).

SOFT START

The TPS62110-EP has an internal soft-start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage when a battery or a high-impedance power source is connected to the input of the TPS62110-EP.

The soft start is implemented as a digital circuit increasing the switch current in steps of 300 mA, 600 mA, and 1200 mA. The typical switch current limit is 2.4 A. Therefore, the start-up time depends on the output capacitor and load current. Typical start-up time, with a 22- μ F output capacitor and 800-mA load current, is 1 ms.

100% DUTY CYCLE LOW-DROPOUT OPERATION

The TPS62110-EP offers the lowest possible input-to-output voltage difference, while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time, taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, and is calculated as:

$$V_I \min = V_O \max + I_O \max \cdot (r_{DS(on)} \max + R_{(L)}) \quad (2)$$

Where:

$I_O \max$ = Maximum output current plus inductor ripple current

$r_{DS(on)} \max$ = Maximum P-channel switch $r_{DS(on)}$

$R_{(L)}$ = DC resistance of the inductor

$V_O \max$ = Nominal output voltage plus maximum output voltage tolerance

DETAILED DESCRIPTION (continued)

ENABLE

Logic low on the enable (EN) input forces the TPS62110-EP into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 2 μA in the shutdown mode. When the device is in thermal shutdown, the bandgap is forced to be switched on, even if the device is set into shutdown by pulling EN to GND.

If an output voltage is present when the device is disabled, which could be due to an external voltage source or a super capacitor, the reverse leakage current is specified under *Electrical Characteristics*. Pulling EN high starts up the TPS62110-EP with the soft start. If EN is connected to any voltage other than V_1 or GND, an increased leakage current of typically 10 μA , and up to 20 μA , can occur.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low-input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The minimum input voltage to start up the TPS62110-EP is 3.4 V (worst case). The device shuts down at 2.8 V minimum.

SYNCHRONIZATION

If no clock signal is applied, the converter operates with a typical switching frequency of 1 MHz. It is possible to synchronize the converter to an external clock within a frequency range from 0.8 MHz to 1.4 MHz. The device automatically detects the rising edge of the first clock and synchronizes immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation. The switch over is initiated if no rising edge on the synchronization (SYNC) input is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 6.25 μs if the internal clock has its minimum frequency of 800 kHz.

If the device is synchronized to an external clock, the power-save mode is disabled, and the devices stay in forced PWM mode.

Connecting SYNC to the GND pin enables the power-save mode. The converter operates in the PWM mode at moderate-to-heavy loads, and in the PFM mode during light loads, which maintains high efficiency over a wide load-current range.

POWER GOOD COMPARATOR

The power good (PG) comparator has an open-drain output capable of sinking 1 mA (typical). The PG output is only active when the device is enabled (EN=high). When the device is disabled (EN=low), PG is pulled to GND.

PG is only valid after a 250- μs delay when the device is enabled, and the supply voltage is greater than the undervoltage lockout $V_{(UVLO)}$. PG is low during the first 250 μs after shutdown and in shutdown.

PG becomes active high when the output voltage exceeds 98.4% (typical) of its nominal value. Leave PG unconnected when not used.

LOW-BATTERY DETECTOR

The low-battery output (LBO) is an open-drain type that goes low when the voltage at the low-battery input (LBI) falls below the trip point of $1.256\text{ V} \pm 1.5\%$. The voltage at which the low-battery warning is issued can be adjusted with a resistive divider as shown in [Figure 9](#). The sum of resistors ($R_1 + R_2$), as well as the sum of ($R_5 + R_6$), is recommended to be in the 100-k Ω to 1-M Ω range for high efficiency at low output current. An external pullup resistor can be connected to OUT or any other voltage rail in the voltage range of 0 V to 16 V. During start-up, the LBO output signal is invalid for the first 500 μs . LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground. The low-battery detector is disabled when the device is disabled.

The logic level of LBO is not defined for the first 500 μs after EN is pulled high.

When the LBI is used to supervise the battery voltage and shut down the TPS62110-EP at low-input voltages, the battery voltage rises when the current drops to zero. The implemented hysteresis on the LBI pin may not be sufficient for all types of batteries. [Figure 9](#) shows how an additional external hysteresis can be implemented.

DETAILED DESCRIPTION (continued)

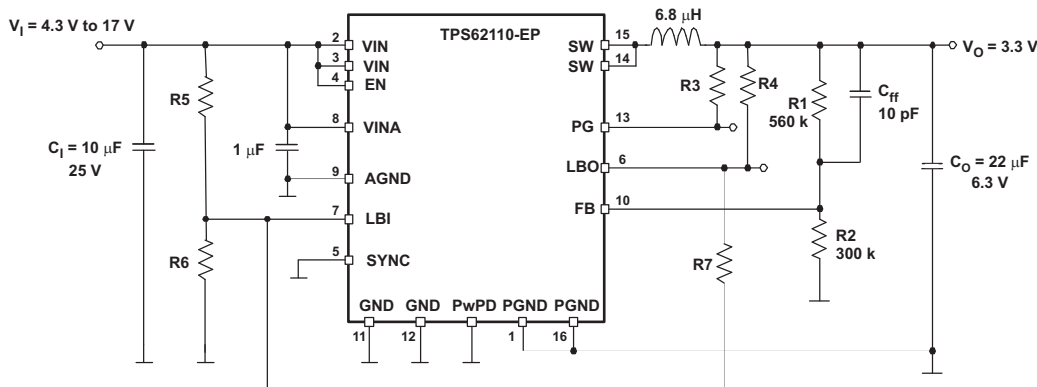


Figure 9. LBI With Increased Hysteresis

NO-LOAD OPERATION

When the converter operates in the forced PWM mode and there is no load connected to the output, the converter regulates the output voltage by allowing the inductor current to reverse for a short time.

THEORY OR OPERATION/DESIGN PROCEDURE

Table 1. List of Inductors

MANUFACTURER ⁽¹⁾	TYPE	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
Coilcraft	MSS6132-682	6.8 µH	65 mR (max)	1.5 A
Epcos	B82462G4682M	6.8 µH	50 mR (max)	1.5 A
Sumida	CDRH5D28-6R2	6.2 µH	33 mR (typ)	1.8 A
TDK	SLF6028T-6R8M1R5	6.8 µH	35 mR (typ)	1.5 A
	SLF7032T-6R8M1R6	6.8 µH	41 mR (typ)	1.6 A
Würth	7447789006	6.8 µH	44 mR (typ)	2.75 A
	7447779006	6.8 µH	33 mR (typ)	3.3 A
	744053006	6.2 µH	45 mR (typ)	1.8 A

(1) The manufacturer's part numbers are used for test purposes only.

Inductor Selection

The control loop of the TPS62110-EP requires a certain value for the output inductor and the output capacitor for stable operation. As long as the nominal value of $L \times C \geq 6.2 \mu\text{H} \times 22 \mu\text{F}$, the control loop has enough phase margin and the device is stable. Reducing the inductor value, without increasing the output capacitor (or vice versa), may cause stability problems. There are applications where it may be useful to increase the value of the output capacitor, e.g., for a low transient output voltage change. From a stability point of view, the inductor value could be decreased to keep the $L \times C$ product constant. However, there are drawbacks if the inductor value is decreased. A low inductor value causes a high inductor ripple current and, therefore, reduces the maximum dc output current. [Table 2](#) gives the advantages and disadvantages when designing the inductor and output capacitor.

Table 2. Advantages and Disadvantages When Designing the Inductor and Output Capacitor

	INFLUENCE ON STABILITY	ADVANTAGE	DISADVANTAGE
Increase Cout (>22 µF)	Uncritical	Less output voltage ripple	None
		Less output voltage overshoot/undershoot during load transient	
Decrease Cout (<22 µF)	Critical Increase inductor value >6.8 µH also	None	Higher output voltage ripple High output voltage overshoot/undershoot during load transient Less gain and phase margin
Increase L (>6.8 µH)	Uncritical	Less inductor current ripple Higher dc output current possible if operated close to the current limit	More energy stored in the inductor → higher voltage overshoot during load transient Smaller current rise → higher voltage undershoot during load transient → do not decrease the value of Cout due to these effects
Decrease L (<6.8 µH)	Critical Increase output capacitor value > 22 µF also	Small voltage overshoot/undershoot during load transient	High inductor current ripple especially at high input voltage and low output voltage

As shown in [Table 2](#), the inductor value can be increased to higher values. For good performance, the peak-to-peak inductor current ripple should be less than 30% of the maximum dc output current. At input voltages above 12 V, it makes sense to increase the inductor value in order to keep the inductor current ripple low. In such applications, the inductor value can be increased to 10 µH or 22 µH. Values above 22 µH should be avoided in order to keep the voltage overshoot during load transient in an acceptable range.

After choosing the inductor value, two additional inductor parameters should be considered:

- Current rating of the inductor
- DC resistance

The dc resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency. In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current which is calculated as:

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_{L \max} = I_{O \max} + \frac{\Delta I_L}{2} \qquad (3)$$

Where:

f = Switching frequency (1000 kHz typical)

L = Inductor value

ΔI_L = Peak-to-peak inductor ripple current

$I_{L \max}$ = Maximum inductor current

The highest inductor current occurs at maximum V_I . A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS62110-EP, which is 2.4 A (typically). See [Table 1](#) for recommended inductors.

OUTPUT CAPACITOR SELECTION

A 22- μ F (typical) output capacitor is needed with a 6.8- μ H inductor. For an output voltage greater than 5 V, a 33- μ F (minimum) output capacitor is required for stability. For best performance, a low ESR ceramic output capacitor is needed.

Just for completeness, the RMS ripple current is calculated as:

$$I_{RMS}(C_O) = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR, plus the voltage ripple caused by charge and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + R_{ESR} \right) \quad (5)$$

Where the highest output voltage ripple occurs at the highest input voltage, V_I .

INPUT CAPACITOR SELECTION

The nature of the buck converter is a pulsating input current; therefore, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor should have a minimum value of 10 μ F and can be increased without any limit for better input voltage filtering. The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_O \max \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I} \right)} \quad (6)$$

The worst-case RMS ripple current occurs at $D = 0.5$ and is calculated as: $I_{RMS} = I_O/2$. Ceramic capacitors show a good performance because of their low ESR value, and they are less sensitive against voltage transients compared to tantalum capacitors. Place the input capacitor as close as possible to the input pin of the IC for best performance

FEEDFORWARD CAPACITOR SELECTION

The feedforward capacitor (C_{ff}) is needed to compensate for parasitic capacitance from the feedback pin to GND. Typically, a value of 4.7 pF to 22 pF is needed for an output voltage divider, with a equivalent resistance (R_1 in parallel with R_2) in the 150-k Ω range. The value can be chosen based on best transient performance and lowest output voltage ripple in PFM mode.

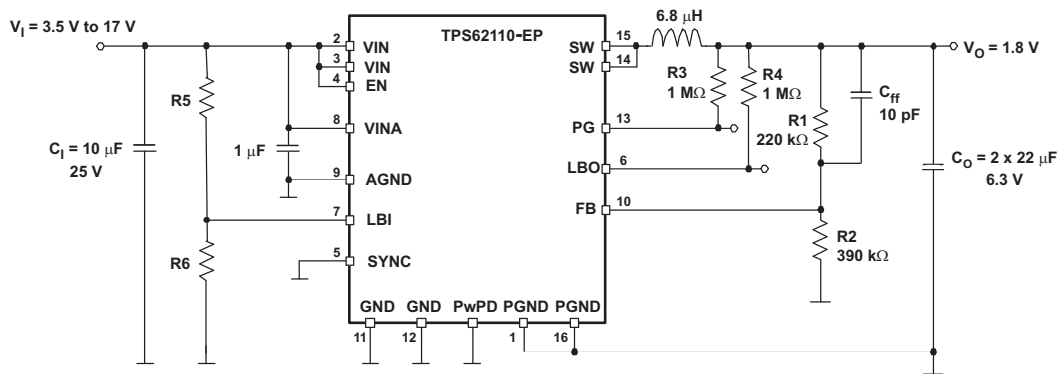
RECOMMENDED CAPACITORS

It is recommended that only X5R or X7R ceramic capacitors be used as input/output capacitors. Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output and input capacitor of a dc/dc converter. The effect may lead to a significant capacitance drop, particularly for high input/output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point. The capacitors listed in [Table 3](#) have been tested with the TPS62110-EP with good performance.

Table 3. List of Capacitors

MANUFACTURER	PART NUMBER	SIZE	VOLTAGE	CAPACITANCE	TYPE
Taiyo Yuden	TMK316BJ106KL	1206	25 V	10 μ F	Ceramic
	EMK325BJ226KM	1210	16 V	22 μ F	
TDK	C3225X5R1E106M	1210	25 V	10 μ F	Ceramic
	C3225X7R1C226M		16 V	22 μ F	
	C3216X5R1E106MT	1206	25 V	10 μ F	

APPLICATION INFORMATION



- A. For an output voltage lower than 2.5 V, an output capacitor of 33 µF or greater is recommended to improve load transient.

Figure 10. Standard Connection

$$V_O = V_{FB} \times \frac{R1 + R2}{R2}$$

$$R1 = R2 \times \left(\frac{V_O}{V_{FB}} \right) - R2$$

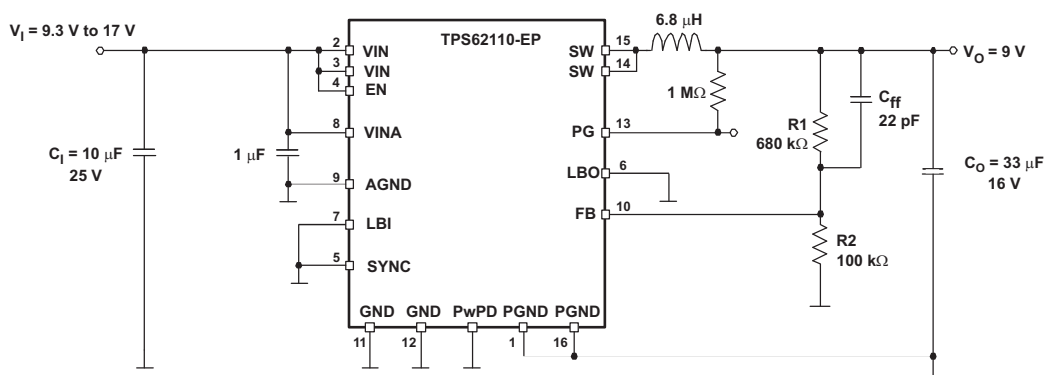
(7)

Where:

$$V_{FB} = 1.153 \text{ V}$$

Table 4. Recommended Resistors

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	TYPICAL C _{ff}
9 V	680 kΩ	100 kΩ	8.993 V	22 pF
5 V	510 kΩ	150 kΩ	5.073 V	10 pF
3.3 V	560 kΩ	300 kΩ	3.305 V	10 pF
2.5 V	390 kΩ	330 kΩ	2.515 V	10 pF
1.8 V	220 kΩ	390 kΩ	1.803 V	10 pF
1.5 V	100 kΩ	330 kΩ	1.502 V	10 pF



- A. For an output voltage greater than 5 V, an output capacitor of 33 µF minimum is required for stability.

Figure 11. Application With 9-V Output

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS62110MRSAREP	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

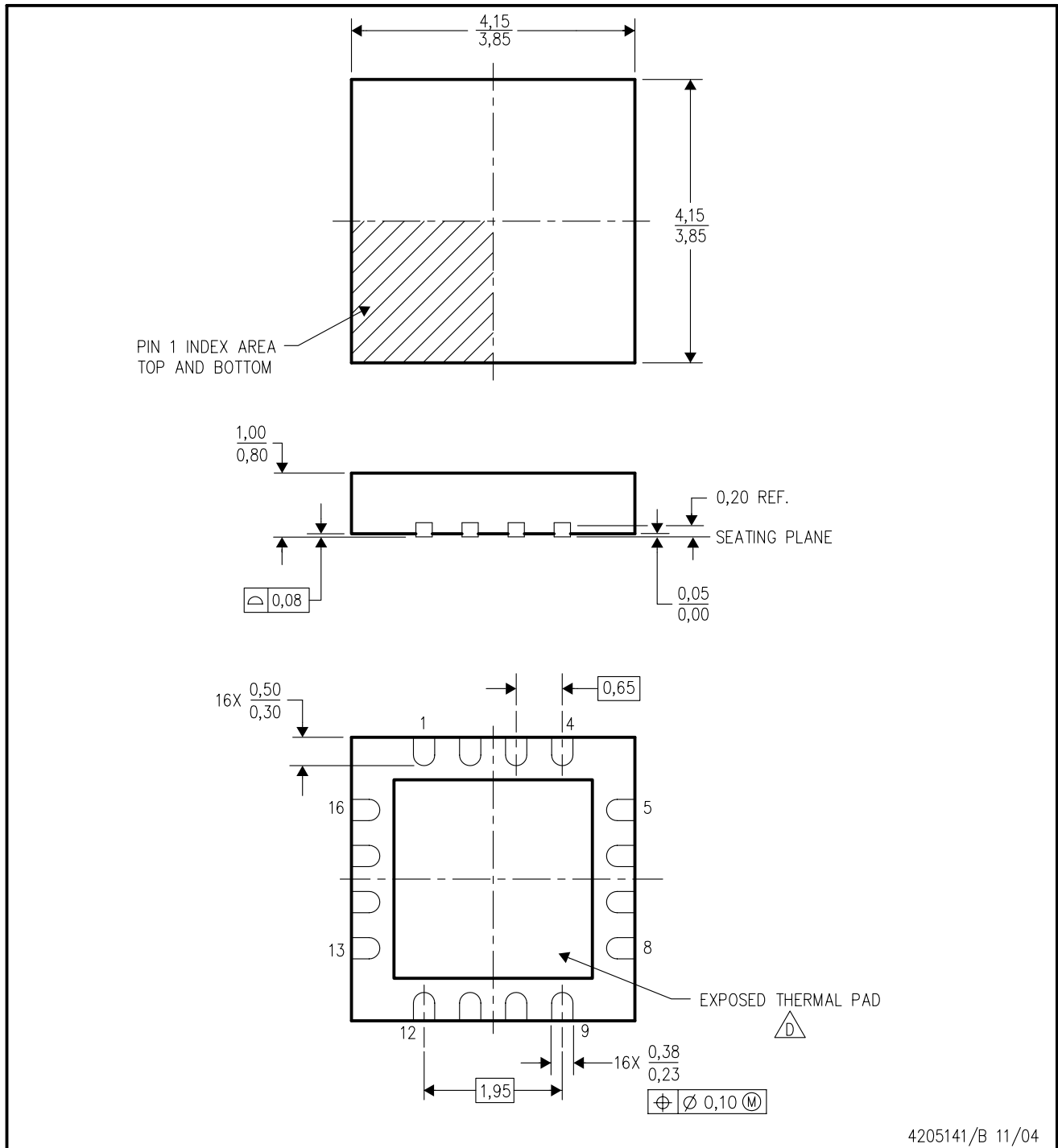
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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RSA (S-PQFP-N16)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - △ The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

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