FUJITSU
MICROELECTRONICS, INC. MBM2764

MBM2764-20
MBM2764-25
MBM2764-30
MBM2764-30-X

NMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

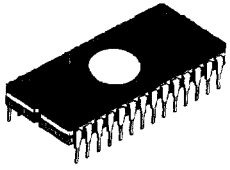
2764LCC

DESCRIPTION

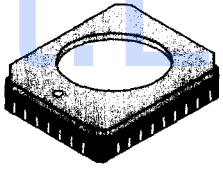
The Fujitsu MBM2764 is a high-speed 65,536-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package with a transparent lid is used to package the MBM2764. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2764 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERDIP PACKAGE
DIP-28C-C01



LCC Package
LCC-32C-A01

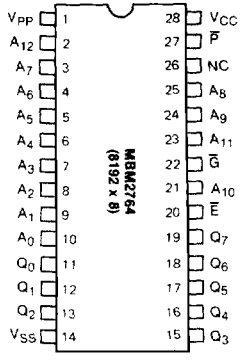
FEATURES

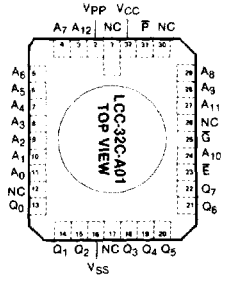
- **Organized as 8192 words by 8-bits, fully decoded**
- **Fast Access Time:**

MBM2764-20	**200 ns**
MBM2764-25	**250 ns**
MBM2764-30	**300 ns**
MBM2764-30-X	**300 ns**

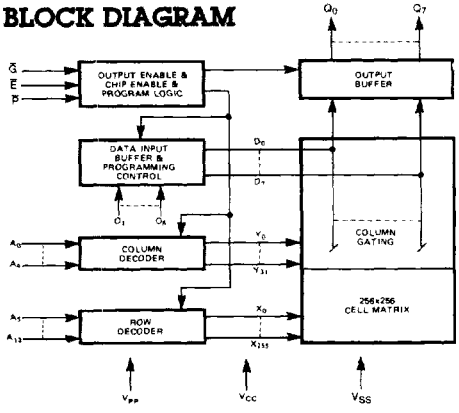
- **Simple programming requirements**
- **Single location programming**
- **Programs with Quick Pro™ (see page 4-7)**
- **Low power requirement: 550mW active 193mW standby**
- **Extended temperature range: MBM2764-30-X: −40°C to +85°C**
- **No clocks required, Fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable $\overline{G}$ pin for simplified memory expansion**
- **Single +5V Operation**
- **Standard 28-pin DIP package**
- **Pin compatible with Intel 2764**

PIN ASSIGNMENT





MBM2764 BLOCK DIAGRAM



2764LCC

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Temperature Under Bias	MBM2764-20/-25/30	T_A	−25 to +85	°C
	MBM2764-30-X		−50 to +95	
Storage Temperature		T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}		V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

FUNCTIONS AND PIN CONNECTIONS V_{CC} (28) = +5, V_{SS} (14) = GND

Mode \ Function (DIP Pin No.)	Address Input (2 ~ 10,21,23 ~ 25)	Data Q (11 ~ 13,15 ~ 19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	Don't Care	I_{CC2}	V_{CC}
				Don't Care	V_{IL}		
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{CC}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	I_{CC2}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{PP}

Note: 1. $\overline{P}$ works as if G (output enable) during reading operation.

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Ouput Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature	
						MBM2764-20/-25/-30	MBM2764-30-X
Supply Voltage	V_{CC}	4.50	5.0	5.50	V	0°C to +70°C	−40°C to +85°C
Supply Voltage	V_{PP}	V_{CC} −0.6	—	V_{CC} + 0.6	V		
Supply Voltage	V_{SS}	—	GND	—	V		
Input High Voltage	V_{IH}	2.0	—	V_{CC} +1	V		
Input Low Voltage	V_{IL}	−0.1	—	0.8	V		

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Symbol	Min	Max	Unit
Input Load Current	$V_{IN} = 5.5V$	I_{LI}	—	10	μA
Output Leakage Current	$V_{OUT} = 5.5V$	I_{LO}	—	10	μA
V_{PP} Supply Current	$V_{PP} = V_{CC} \pm 0.6V$	I_{PP}	—	15	mA
V_{CC} Standby Current	$\overline{E} = V_{IH}$	I_{CC1}	—	35	mA
V_{CC} Supply Current (Active)	$\overline{E} = V_{IL}$	I_{CC2}	—	100	mA
Input Low Voltage	—	V_{IL}	−0.1	+0.8	V
Input High Voltage	—	V_{IH}	2.0	$V_{CC}+1$	V
Output Low Voltage	$I_{OL} = 2.1mA$	V_{OL}	—	0.45	V
Output High Voltage	$I_{OH} = -400\mu A$	V_{OH}	2.4	—	V

AC CHARACTERISTICS

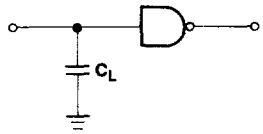
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM2764-20		MBM2764-25		MBM2764-30 MBM2764-30-X		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	TAVQV	—	200	—	250	—	300	ns	$\overline{E} = \overline{G} = V_{IL}$
$\overline{E}$ to Output Delay	TELQV	—	200	—	250	—	300	ns	$\overline{E} = V_{IL}$
$\overline{G}$ to Output Delay	TGLQV	10	70	10	100	10	120	ns	$\overline{E} = V_{IL}$
Output Enable High to Output Float	TGHQZ, TEHQZ	0	60	0	60	0	105	ns	$\overline{E} = V_{IL}$
Address to Output Hold	TAXQX	0	—	0	—	0	—	ns	$\overline{E} = \overline{G} = V_{IL}$

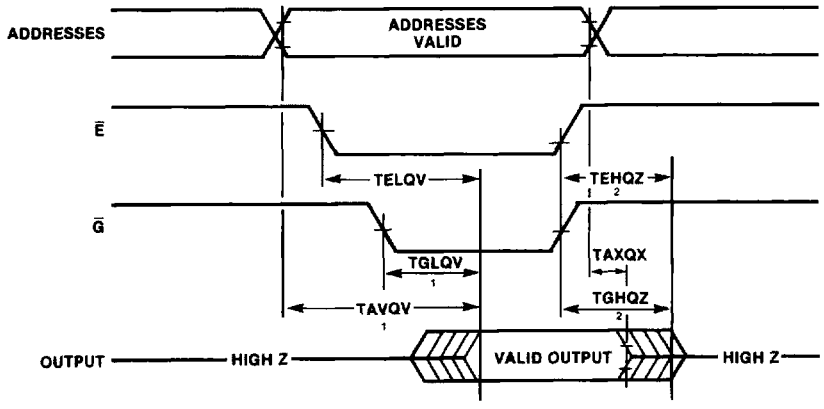
AC TEST CONDITIONS

Input Pulse levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤20nsec
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
1 TTL gate and C_L = 100 pF

Output Load:



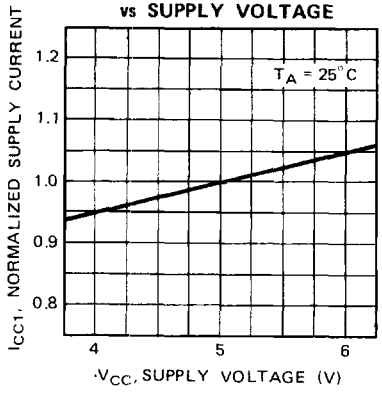
OPERATION TIMING DIAGRAM



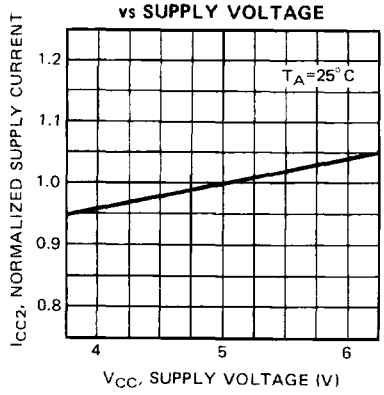
Notes: (1) $\overline{G}$ may be delay up to TAVQV—TGLQV after the falling edge of $\overline{E}$ without impact on TAVQV.
(2) TGHQZ or TEHQZ are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

TYPICAL CHARACTERISTICS CURVES

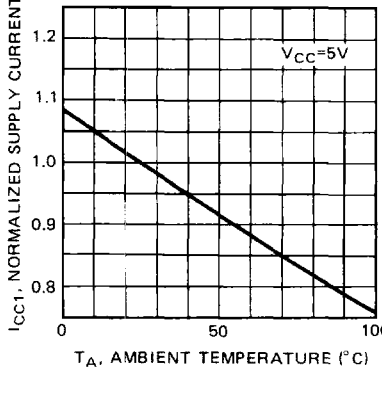
SUPPLY CURRENT (STANDBY) vs SUPPLY VOLTAGE



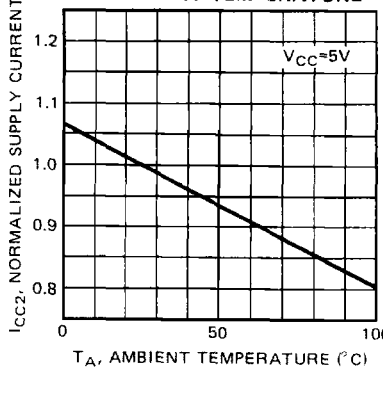
SUPPLY CURRENT (ACTIVE) vs SUPPLY VOLTAGE



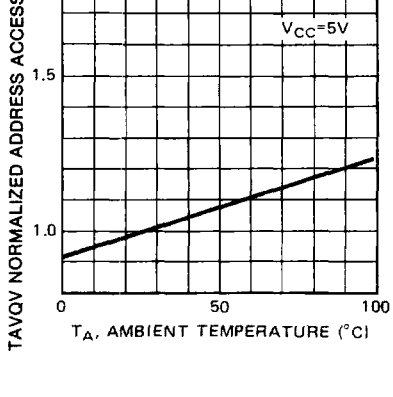
SUPPLY CURRENT (STANDBY) vs AMBIENT TEMPERATURE



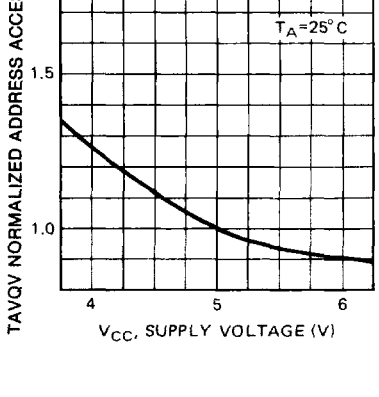
SUPPLY CURRENT (ACTIVE) vs AMBIENT TEMPERATURE



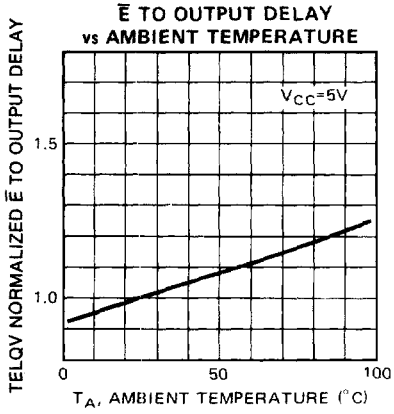
ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

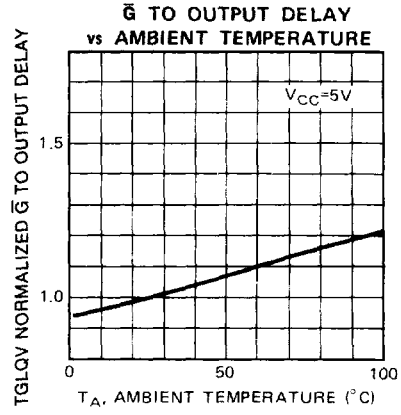


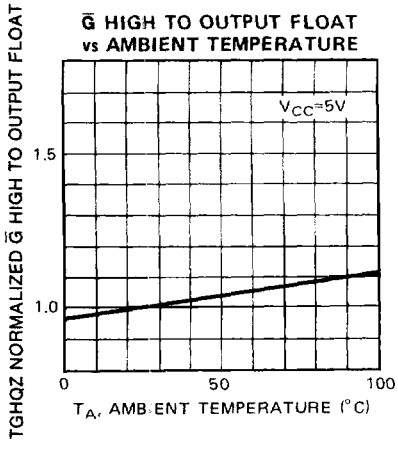
ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

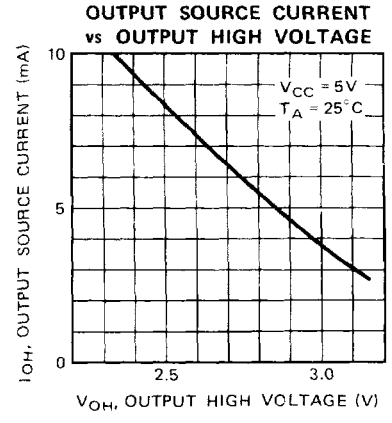


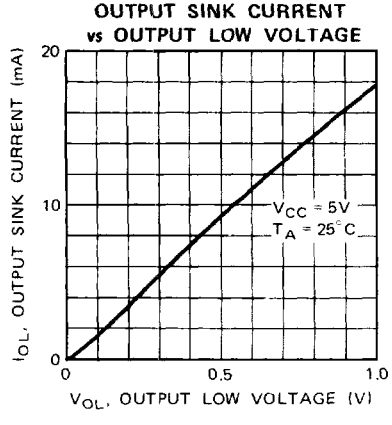
TYPICAL CHARACTERISTICS CURVES (Continued)

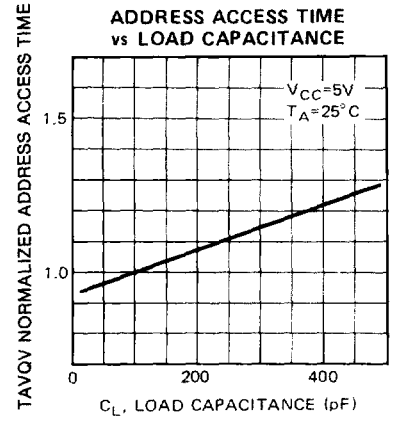












PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM2764 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Fig. 1 — MEMORY CELL

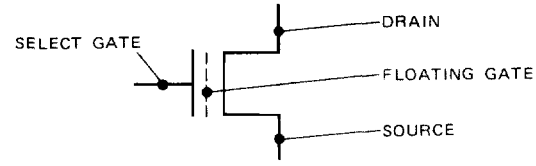
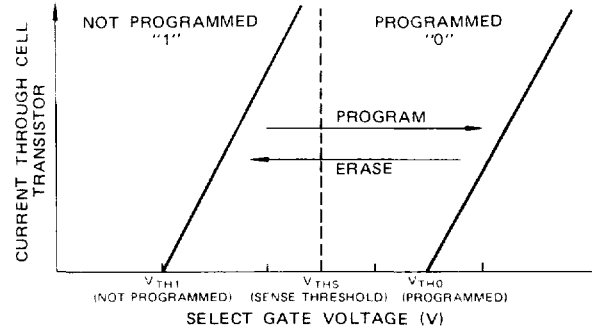


Fig. 2 — MEMORY CELL THRESHOLD SHIFT



CONVENTIONAL PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2764 has all 65,536-bits in the "1" or high state. "0's" are loaded into the MBM2764 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1 μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec. TTL low level pulse is applied to the $\overline{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

QUICK PRO™

In addition to the standard 50 millisecond pulse width programming procedure, the MBM2764 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input. Conversely, a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2764 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM2764. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2 for 15 to 20 minutes.

The MBM2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2764 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM2764 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING / ERASING INFORMATION (Continued)

DC CHARACTERISTICS

(T_A = 25 ± 5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 0.45V–5.25V
Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = −400μA
V_{CC} Supply Current	I_{CC}	—	100	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} +1	V	—
V_{PP} Supply Current	I_{PP}	—	30	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

AC CHARACTERISTICS

(T_A = 25 ± 5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
$\overline{E}$ Setup Time	TELPL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Chip Enable to Output Float Delay	TGHQZ	—	—	130	ns
V_{PP} Setup Time	TVPPHL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	45	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.45	1.00	1.05	ms
$\overline{G}$ Setup Time [1]	TDZGL	2	—	—	μs
Data Valid from $\overline{G}$	TGLQV	—	—	150	ns

Notes:
[1] TPHDZ + TDZQL ≥ 50μs.

PROGRAMMING WAVEFORM