

Standard Power MOSFETs

File Number 1562

IRFF110, IRFF111, IRFF112, IRFF113

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 60V-100V  
 $r_{DS(on)} = 0.6 \Omega$  and  $0.8 \Omega$

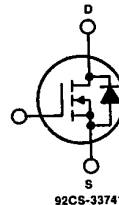
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRFF110, IRFF111, IRFF112 and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

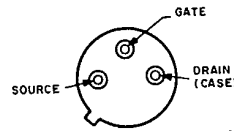
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Datasheet.Live

Absolute Maximum Ratings

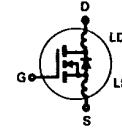
Parameter	IRFF110	IRFF111	IRFF112	IRFF113	Units
$V_{DS}$ Drain - Source Voltage ①	100	60	100	60	V
$V_{DGR}$ Drain - Gate Voltage ( $R_{GS} = 20 K\Omega$ ) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ C$ Continuous Drain Current	3.5	3.5	3.0	3.0	A
$I_{DM}$ Pulsed Drain Current ②	14	14	12	12	A
$V_{GS}$ Gate - Source Voltage	$\pm 20$				V
$P_D @ T_C = 25^\circ C$ Max. Power Dissipation	15		(See Fig. 14)		W
Linear Derating Factor	0.12				(See Fig. 14) W/ $^\circ C$
$I_{LM}$ Inductive Current, Clamped	14	(See Fig. 15 and 16) 14	12	12	A
$T_J$ Operating Junction and Storage Temperature Range	-55 to 150				$^\circ C$
$T_{stg}$ Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ C$

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Electrical Characteristics @ T<sub>C</sub> = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub> Drain-Source Breakdown Voltage	IRFF110 IRFF112	100	—	—	V	V <sub>GS</sub> = 0V
	IRFF111 IRFF113	60	—	—	V	I <sub>D</sub> = 250μA
V <sub>GS(th)</sub> Gate Threshold Voltage	ALL	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>GSS</sub> Gate-Source Leakage Forward	ALL	—	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub> Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub> Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V <sub>DS</sub> = Max. Rating, V <sub>GS</sub> = 0V
I <sub>D(on)</sub> On-State Drain Current ②	IRFF110 IRFF111	3.5	—	—	A	V <sub>DS</sub> = I <sub>D(on)</sub> × R <sub>DS(on)</sub> max., V <sub>GS</sub> = 10V
	IRFF112 IRFF113	3.0	—	—	A	
R <sub>DS(on)</sub> Static Drain-Source On-State Resistance ②	IRFF110 IRFF111	—	0.5	0.6	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.5A
	IRFF112 IRFF113	—	0.6	0.8	Ω	
g <sub>fs</sub> Forward Transconductance ②	ALL	1.0	1.5	—	S (Ω)	V <sub>DS</sub> = I <sub>D(on)</sub> × R <sub>DS(on)</sub> max., I <sub>D</sub> = 1.5A
C <sub>iss</sub> Input Capacitance	ALL	—	135	200	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0 MHz See Fig. 10
C <sub>oss</sub> Output Capacitance	ALL	—	80	100	pF	
C <sub>rss</sub> Reverse Transfer Capacitance	ALL	—	20	25	pF	
t <sub>d(on)</sub> Turn-On Delay Time	ALL	—	10	20	ns	V <sub>DD</sub> = 0.5 BV <sub>DSS</sub> , I <sub>D</sub> = 1.5A, Z <sub>0</sub> = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t <sub>r</sub> Rise Time	ALL	—	15	25	ns	
t <sub>d(off)</sub> Turn-Off Delay Time	ALL	—	15	25	ns	
t <sub>f</sub> Fall Time	ALL	—	10	20	ns	
Q <sub>g</sub> Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 8.0A, V <sub>DS</sub> = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q <sub>gs</sub> Gate-Source Charge	ALL	—	2.0	—	nC	
Q <sub>gd</sub> Gate-Drain ("Miller") Charge	ALL	—	3.0	—	nC	
L <sub>D</sub> Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L <sub>S</sub> Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R <sub>thJC</sub> Junction-to-Case	ALL	—	—	8.33	°C/W	
R <sub>thJA</sub> Junction-to-Ambient	ALL	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I <sub>S</sub> Continuous Source Current (Body Diode)	IRFF110 IRFF111	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRFF112 IRFF113	—	—	3.0	A	
I <sub>SM</sub> Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	—	—	14	A	
	IRFF112 IRFF113	—	—	12	A	
V <sub>SD</sub> Diode Forward Voltage ②	IRFF110 IRFF111	—	—	2.5	V	T <sub>C</sub> = 25°C, I <sub>S</sub> = 3.5A, V <sub>GS</sub> = 0V
	IRFF112 IRFF113	—	—	2.0	V	T <sub>C</sub> = 25°C, I <sub>S</sub> = 3.0A, V <sub>GS</sub> = 0V
t <sub>rr</sub> Reverse Recovery Time	ALL	—	200	—	ns	T <sub>J</sub> = 150°C, I <sub>F</sub> = 3.5A, dI <sub>F</sub> /dt = 100A/μs
Q <sub>RR</sub> Reverse Recovered Charge	ALL	—	1.0	—	μC	T <sub>J</sub> = 150°C, I <sub>F</sub> = 3.5A, dI <sub>F</sub> /dt = 100A/μs
t <sub>on</sub> Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

① T<sub>J</sub> = 25°C to 150°C.

② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

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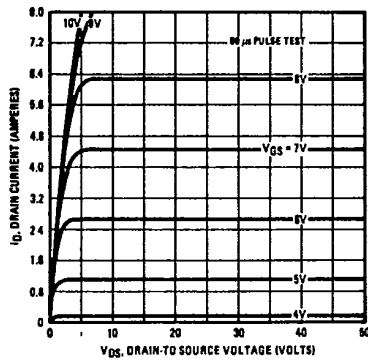


Fig. 1 - Typical Output Characteristics

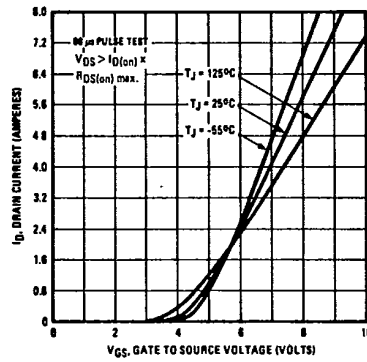


Fig. 2 - Typical Transfer Characteristics

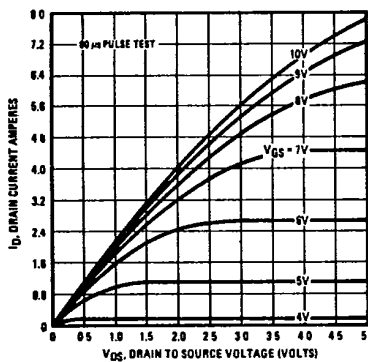


Fig. 3 - Typical Saturation Characteristics

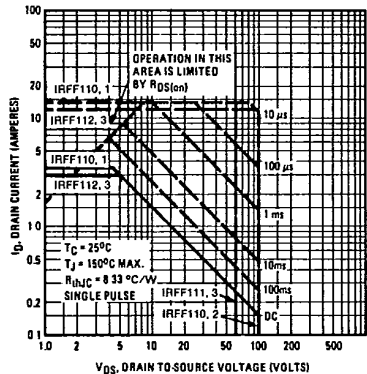


Fig. 4 - Maximum Safe Operating Area

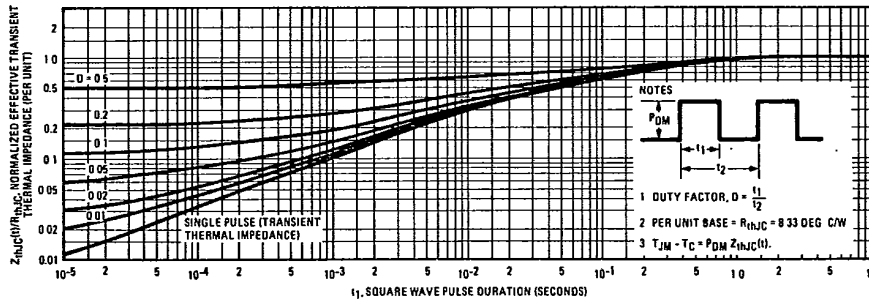


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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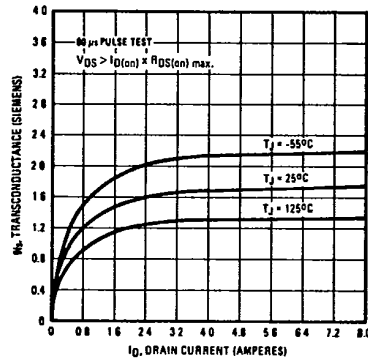


Fig. 6 - Typical Transconductance Vs. Drain Current

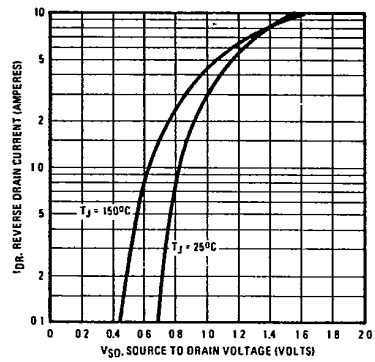


Fig. 7 - Typical Source-Drain Diode Forward Voltage

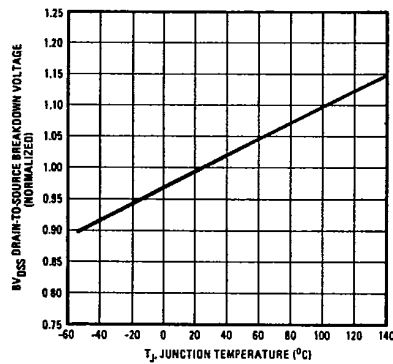


Fig. 8 - Breakdown Voltage Vs. Temperature

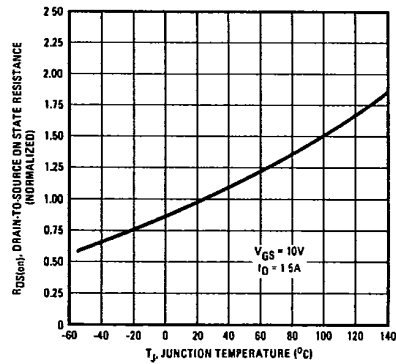


Fig. 9 - Normalized On-Resistance Vs. Temperature

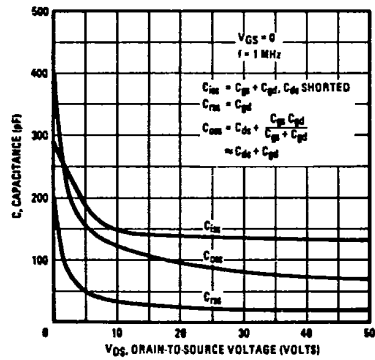


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

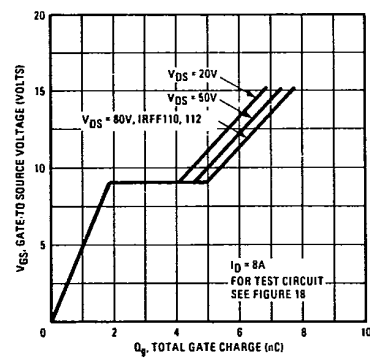


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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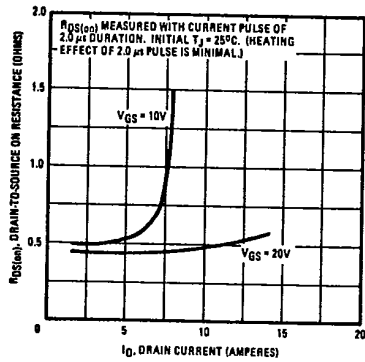


Fig. 12 - Typical On-Resistance Vs. Drain Current

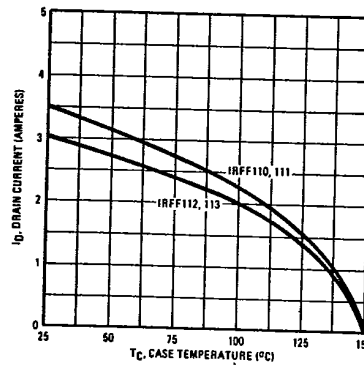


Fig. 13 - Maximum Drain Current Vs. Case Temperature

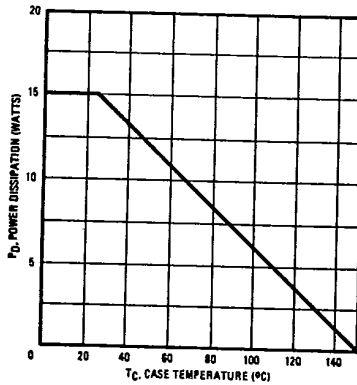


Fig. 14 - Power Vs. Temperature Derating Curve

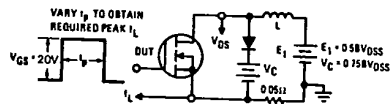


Fig. 15 - Clamped Inductive Test Circuit

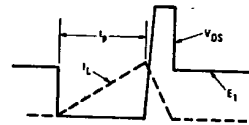


Fig. 16 - Clamped Inductive Waveforms

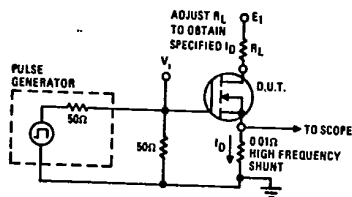


Fig. 17 - Switching Time Test Circuit

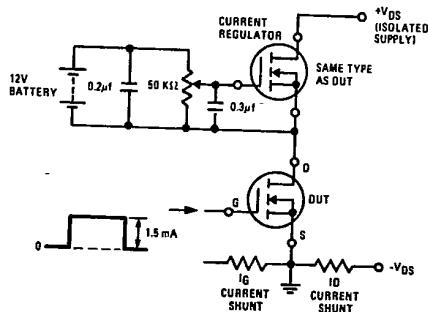


Fig. 18 - Gate Charge Test Circuit