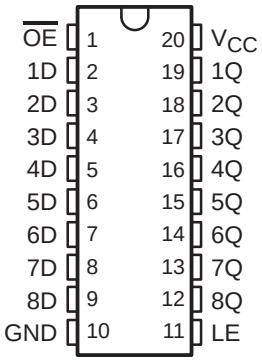
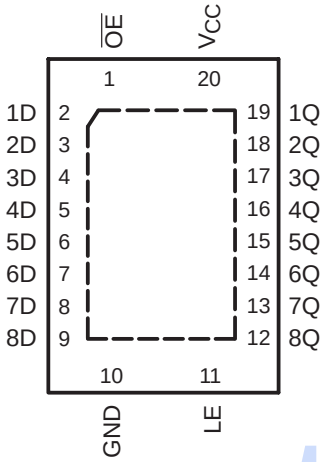
- Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C
- High-Drive Outputs (−32-mA I_{OH}, 64-mA I_{OL})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

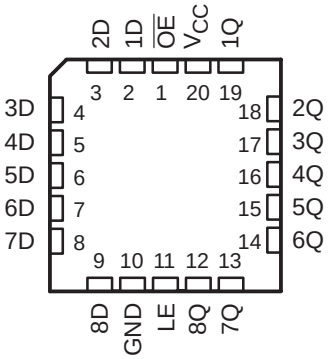
SN54ABT573 . . . J OR W PACKAGE
SN74ABT573A . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74ABT573A . . . RGY PACKAGE
(TOP VIEW)



SN54ABT573 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube	SN74ABT573AN	SN74ABT573AN
	QFN − RGY	Tape and reel	SN74ABT573ARGYR	AB573A
	SOIC − DW	Tube	SN74ABT573ADW	ABT573A
		Tape and reel	SN74ABT573ADWR	
	SOP − NS	Tape and reel	SN74ABT573ANSR	ABT573A
	SSOP − DB	Tape and reel	SN74ABT573ADBR	AB573A
	TSSOP − PW	Tube	SN74ABT573APW	AB573A
		Tape and reel	SN74ABT573APWR	
	VFBGA − GQN	Tape and reel	SN74ABT573AGQNR	AB573A
	VFBGA − ZQN (Pb-free)		SN74ABT573AZQNR	
−55°C to 125°C	CDIP − J	Tube	SNJ54ABT573J	SNJ54ABT573J
	CFP − W	Tube	SNJ54ABT573W	SNJ54ABT573W
	LCCC − FK	Tube	SNJ54ABT573FK	SNJ54ABT573FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

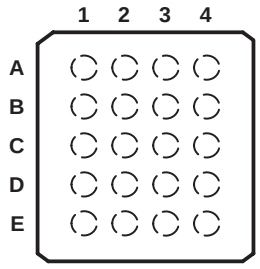
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

SN74ABT573A . . . GQN OR ZQN PACKAGE
(TOP VIEW)



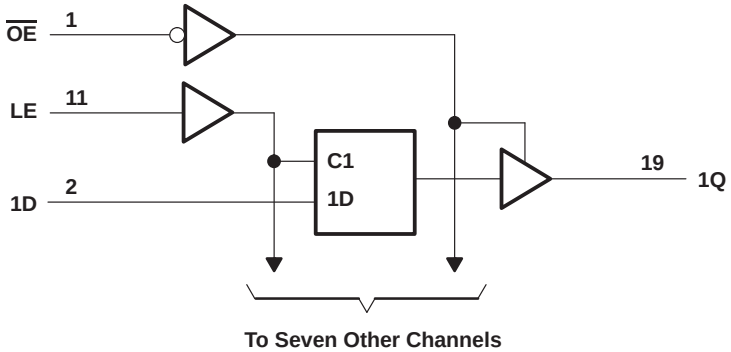
terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	LE	8Q

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . −0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT573 . . . . . 96 mA
SN74ABT573A . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
(see Note 2): DW package . . . . . 58°C/W
(see Note 2): GQN/ZQN package . . . . . 78°C/W
(see Note 2): N package . . . . . 69°C/W
(see Note 2): NS package . . . . . 60°C/W
(see Note 2): PW package . . . . . 83°C/W
(see Note 3): RGY package . . . . . 37°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			SN54ABT573		SN74ABT573A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		5	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT573		SN74ABT573A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2		−1.2		−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = −3 mA		3			3		3		
	V_{CC} = 4.5 V	I_{OH} = −24 mA		2			2				
		I_{OH} = −32 mA		2*					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55*				0.55	
V_{hys}					100						mV
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1		±1		±1	µA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				10‡		10‡		10‡	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−10‡		−10‡		−10‡	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V	Outputs high			50		50		50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND		Outputs high		1	250		250		250	µA
			Outputs low		24	30		30		30	mA
			Outputs disabled		0.5	250		250		250	µA
ΔI_{CC}¶	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND					1.5		1.5		1.5	mA
C_i	V_I = 2.5 V or 0.5 V				3.5						pF
C_o	V_O = 2.5 V or 0.5 V				6.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at V_{CC} = 5 V.
‡ This data sheet limit may vary among suppliers.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT573			UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN MAX	
			MIN	MAX		
t_w	Pulse duration, LE high		3.3		3.3	ns
t_{su}	Setup time, data before LE↓	High	1.9		2.5	ns
		Low	1.5		2.5	
t_h	Hold time, data after LE↓		1		2.5	ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT573A				UNIT
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	
			MIN	MAX			
t_w	Pulse duration, LE high		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	High	1.9		1.9		ns
		Low	1.5		1.5		
t_h	Hold time, data after LE↓		1.8†		1.8†		ns

† This data-sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

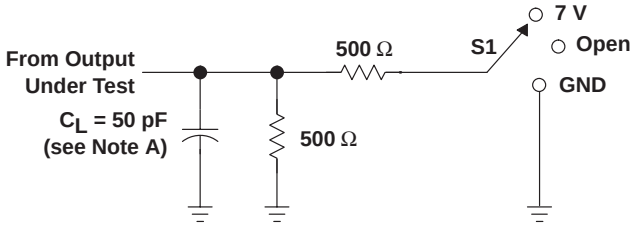
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT573					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.9	3.2	5.4	1.4	6.4	ns
t_{PHL}			2.2	4.2	5.7	1.6	6.7	
t_{PLH}	LE	Q	2.2	4	6.1	2	7.1	ns
t_{PHL}			3.2	5.2	6.7	2.8	7.5	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	0.8	6.2	ns
t_{PZL}			2.7	4.7	6.2	2	7.2	
t_{PHZ}	$\overline{OE}$	Q	2.5	4.9	6.4	2.2	7.7	ns
t_{PLZ}			2	4.2	6	1.4	7	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT573A					UNIT
			V_{CC} = 5 V, T_A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	D	Q	1.9	3.2	5.4	1.9	5.9	ns
t_{PHL}			2.2	4.2	5.7	2.2	6.2	
t_{PLH}	LE	Q	2.2	4	6.1	2.2	6.6	ns
t_{PHL}			3.2	5.2	6.7	3.2	7.2	
t_{PZH}	$\overline{OE}$	Q	1.2	3.2	4.7	1.2	5.2	ns
t_{PZL}			2.5†	4.7	6.2	2.5†	6.7	
t_{PHZ}	$\overline{OE}$	Q	2.5	4.9	6.4	2.5	7.1†	ns
t_{PLZ}			2	4.2	6	2	6.5	

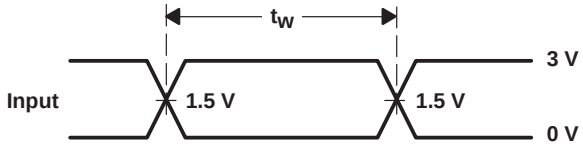
† This data-sheet limit may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

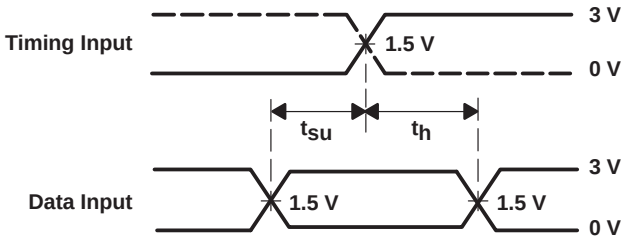


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

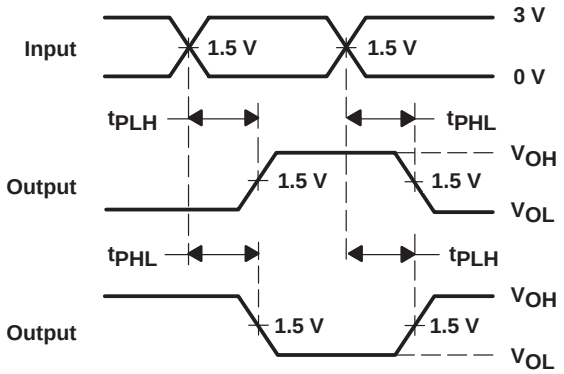
LOAD CIRCUIT



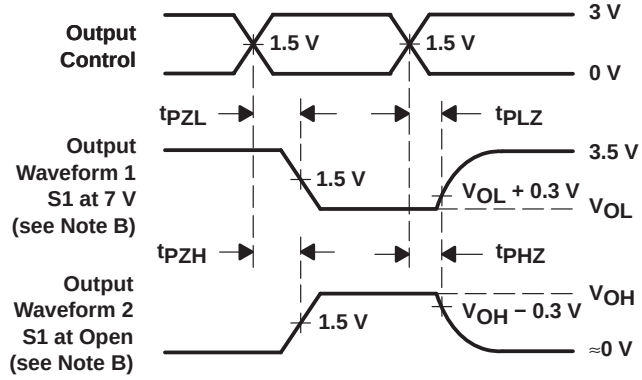
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9321901Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9321901QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9321901QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC
SN74ABT573ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74ABT573ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573AGQNR	ACTIVE	VFBGA	GQN	20	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74ABT573AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ABT573ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ABT573ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74ABT573APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT573ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74ABT573ARGYRG4	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74ABT573AZQNR	ACTIVE	VFBGA	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
SNJ54ABT573FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ABT573J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ABT573W	ACTIVE	CFP	W	20	1	TBD	Call TI	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

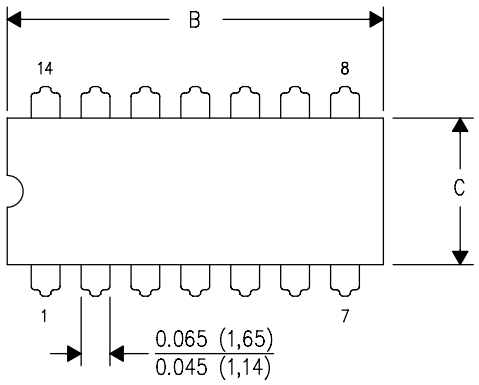
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

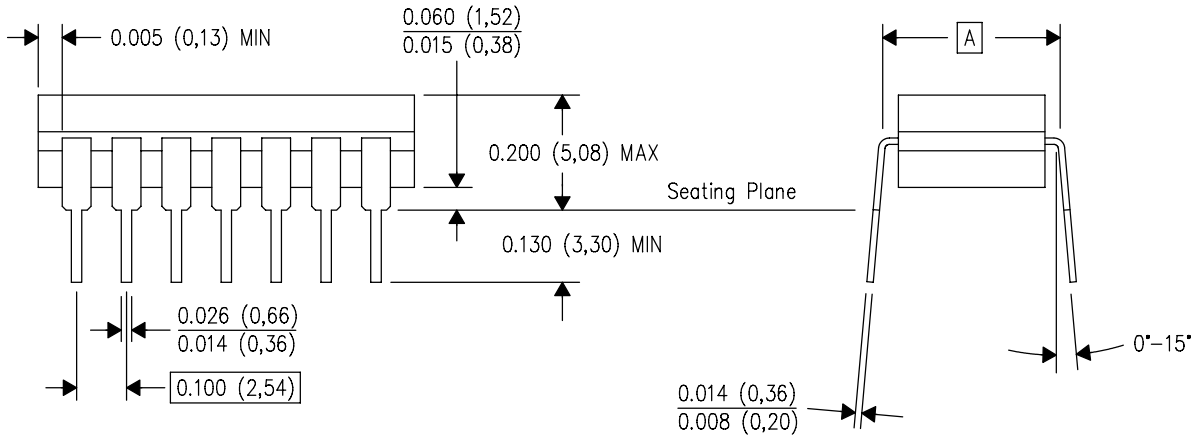
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



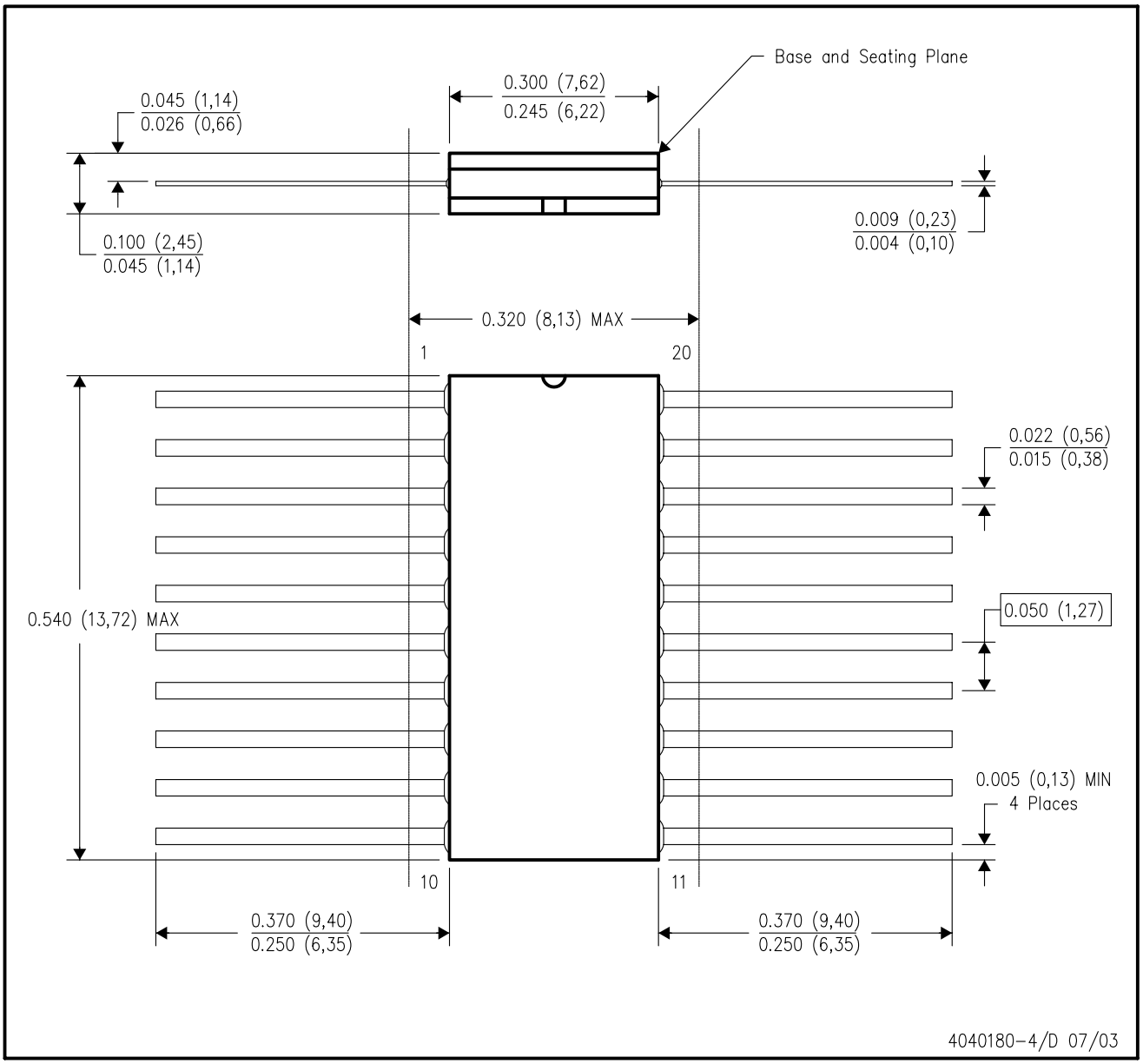
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

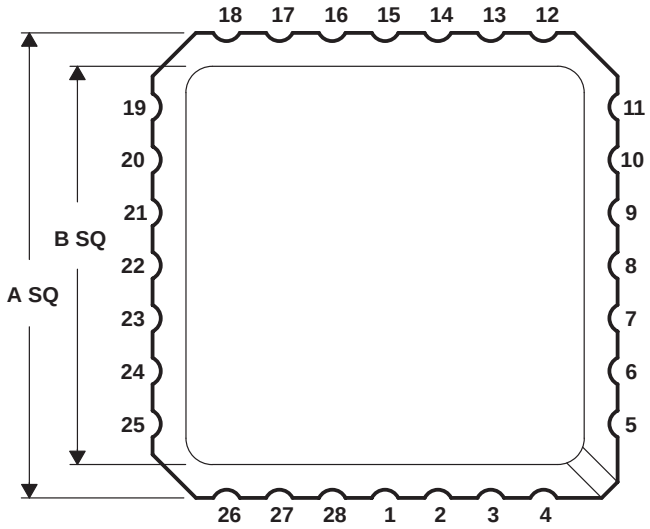
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



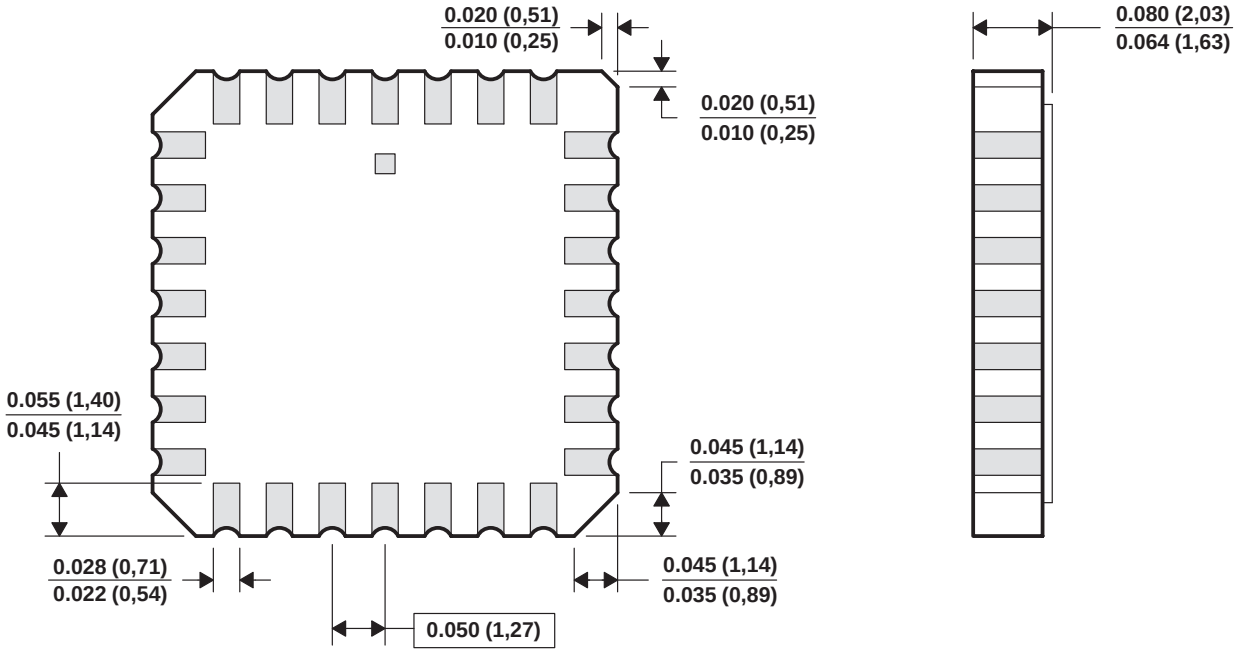
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



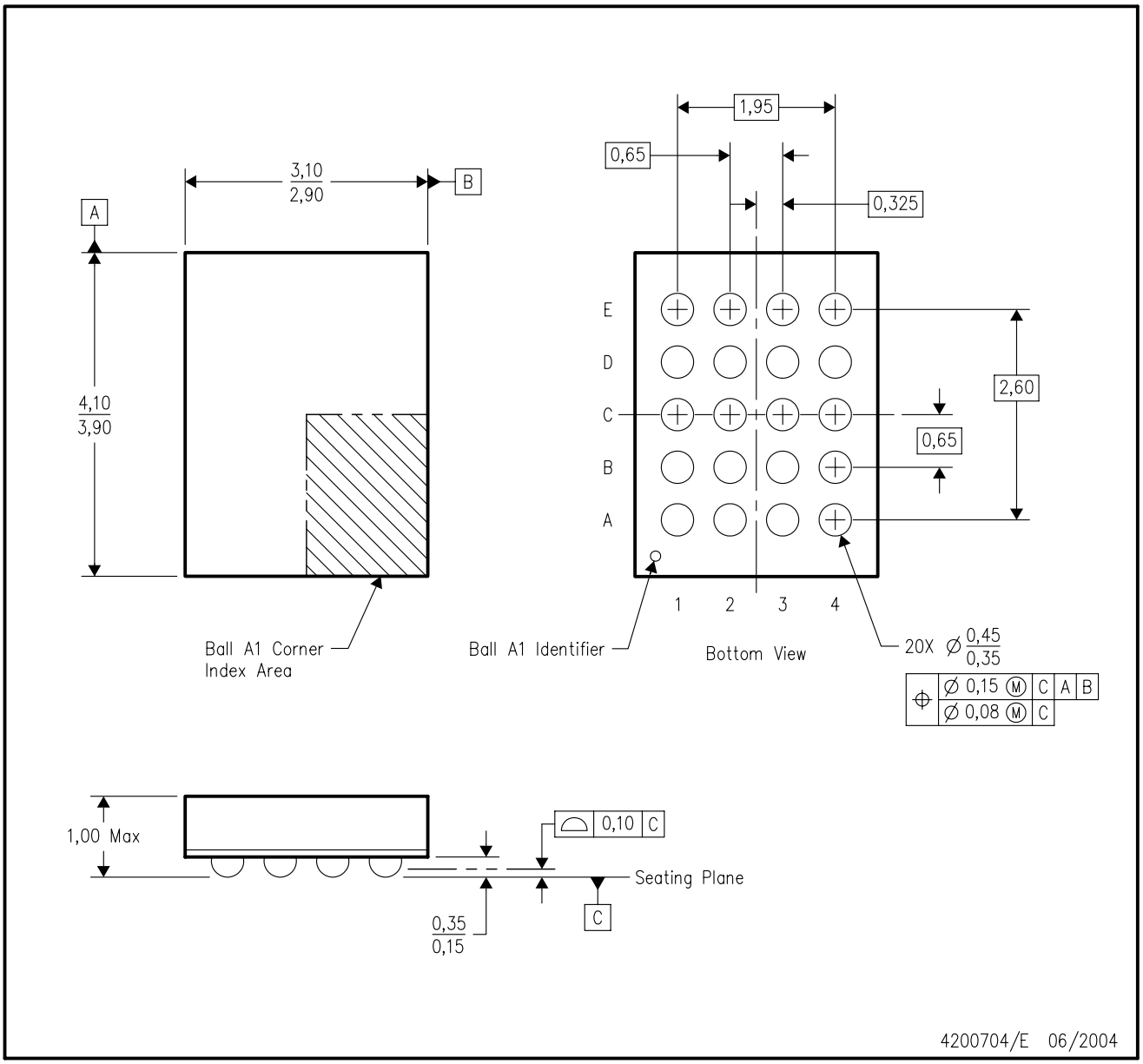
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

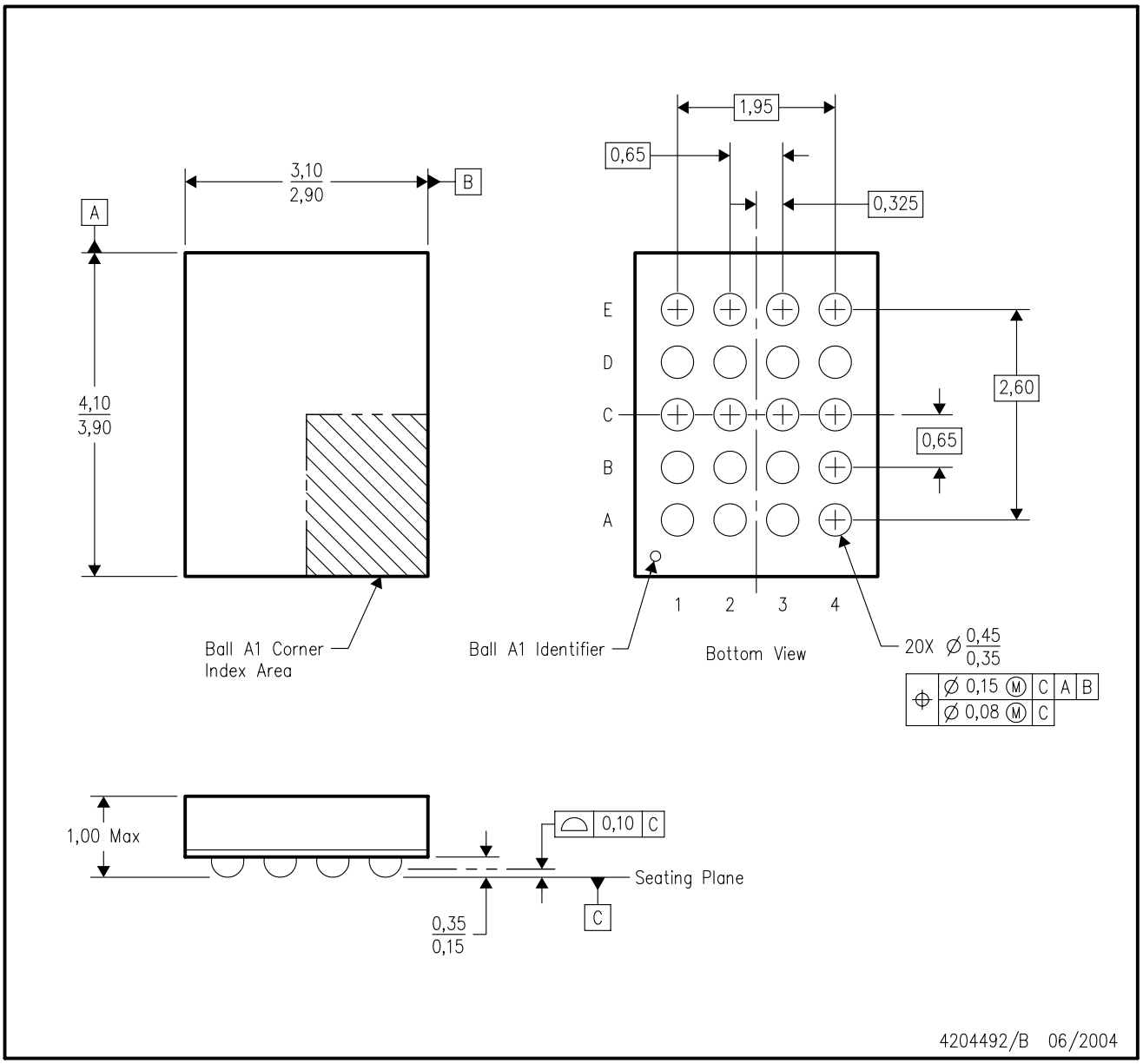
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

GQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is tin–lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead–free.

ZQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY

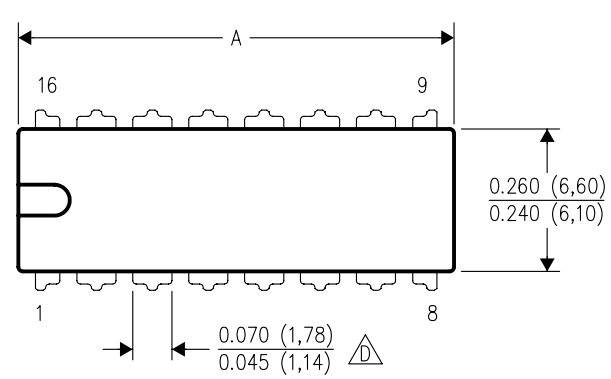


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

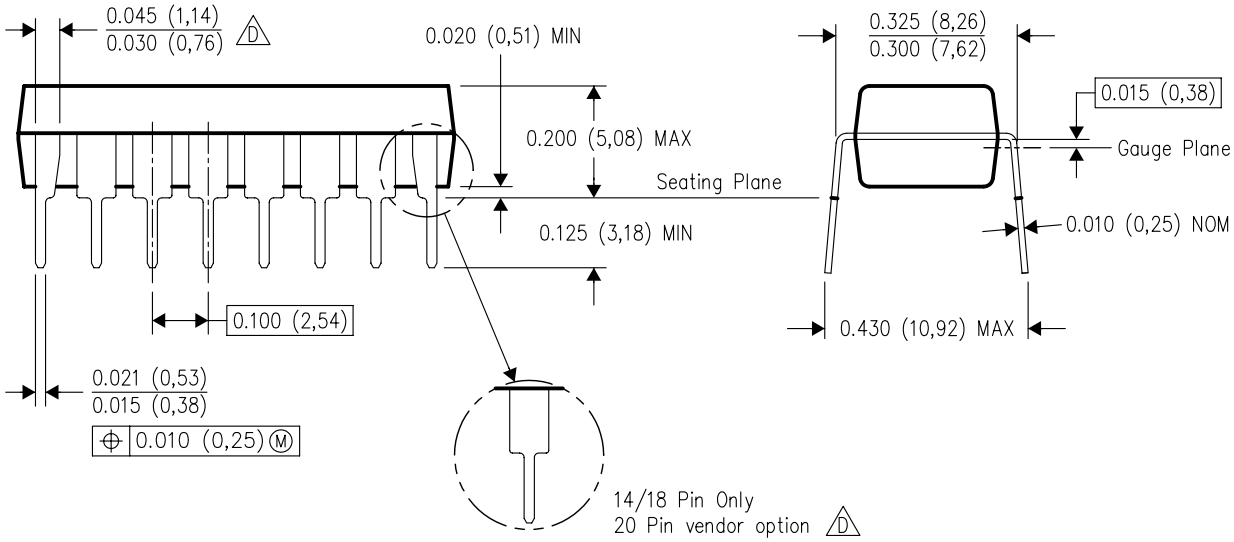
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



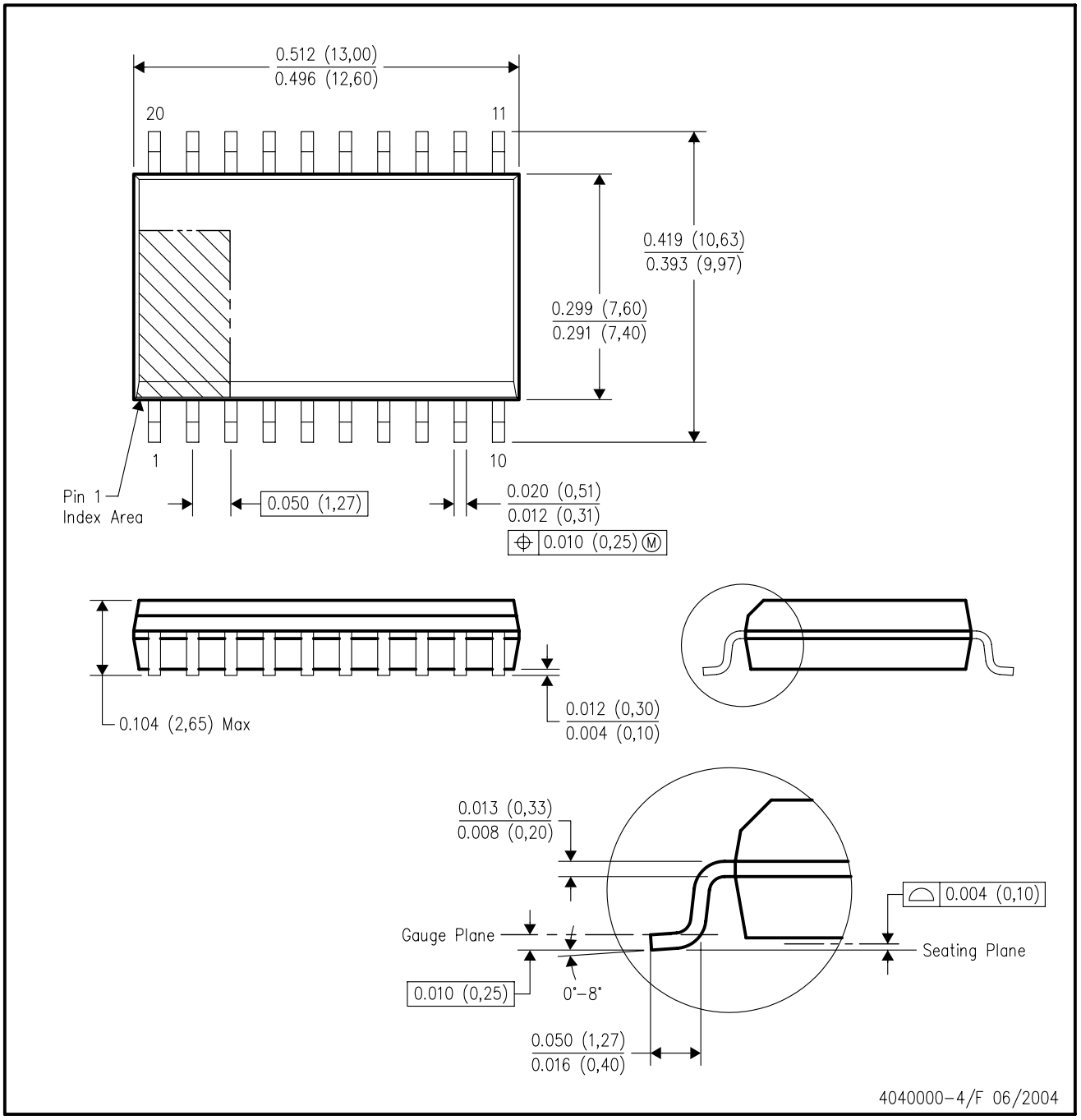
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

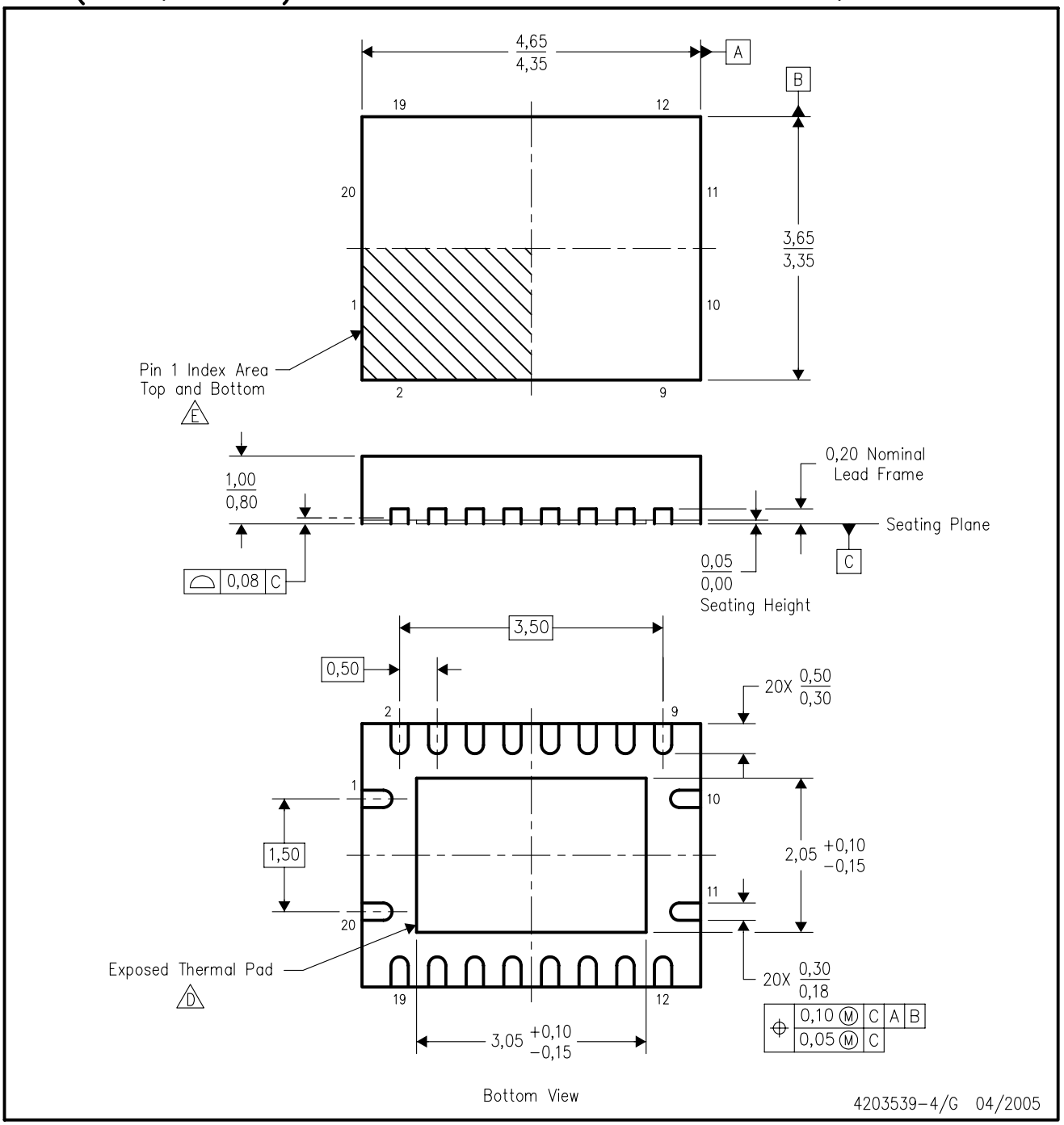
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK

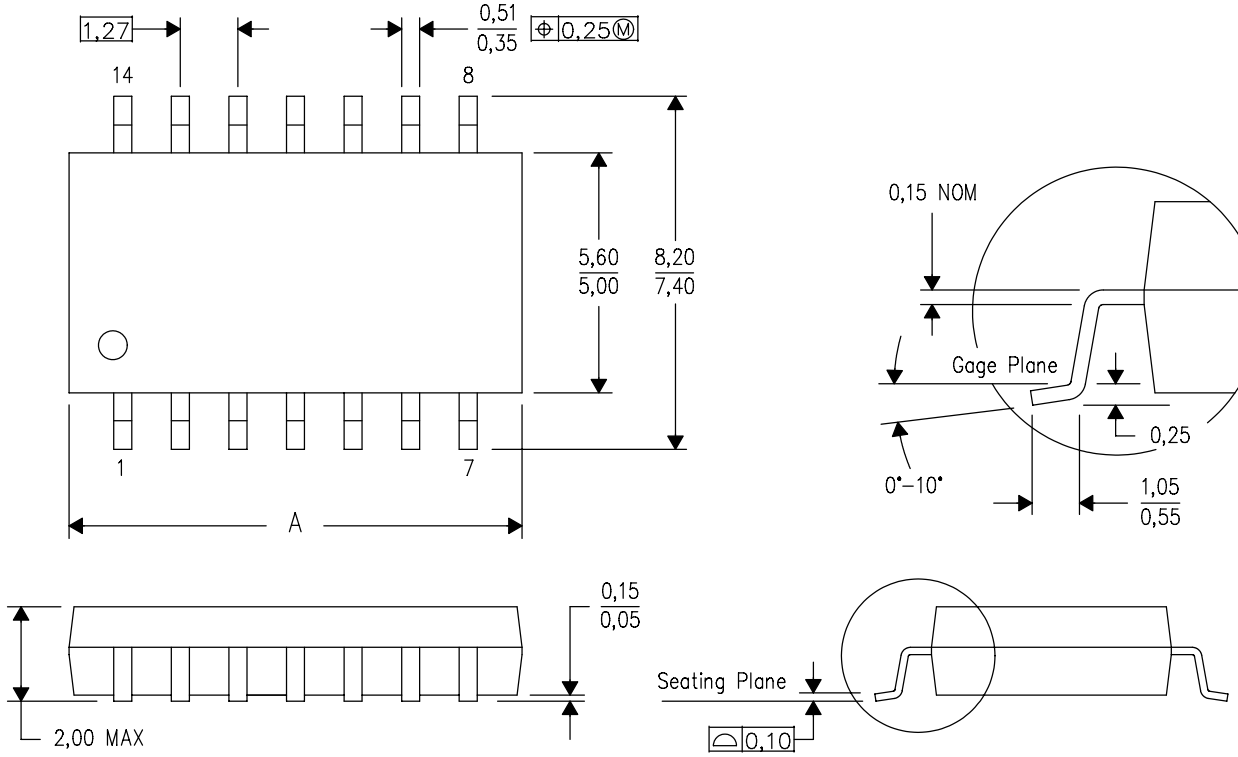


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

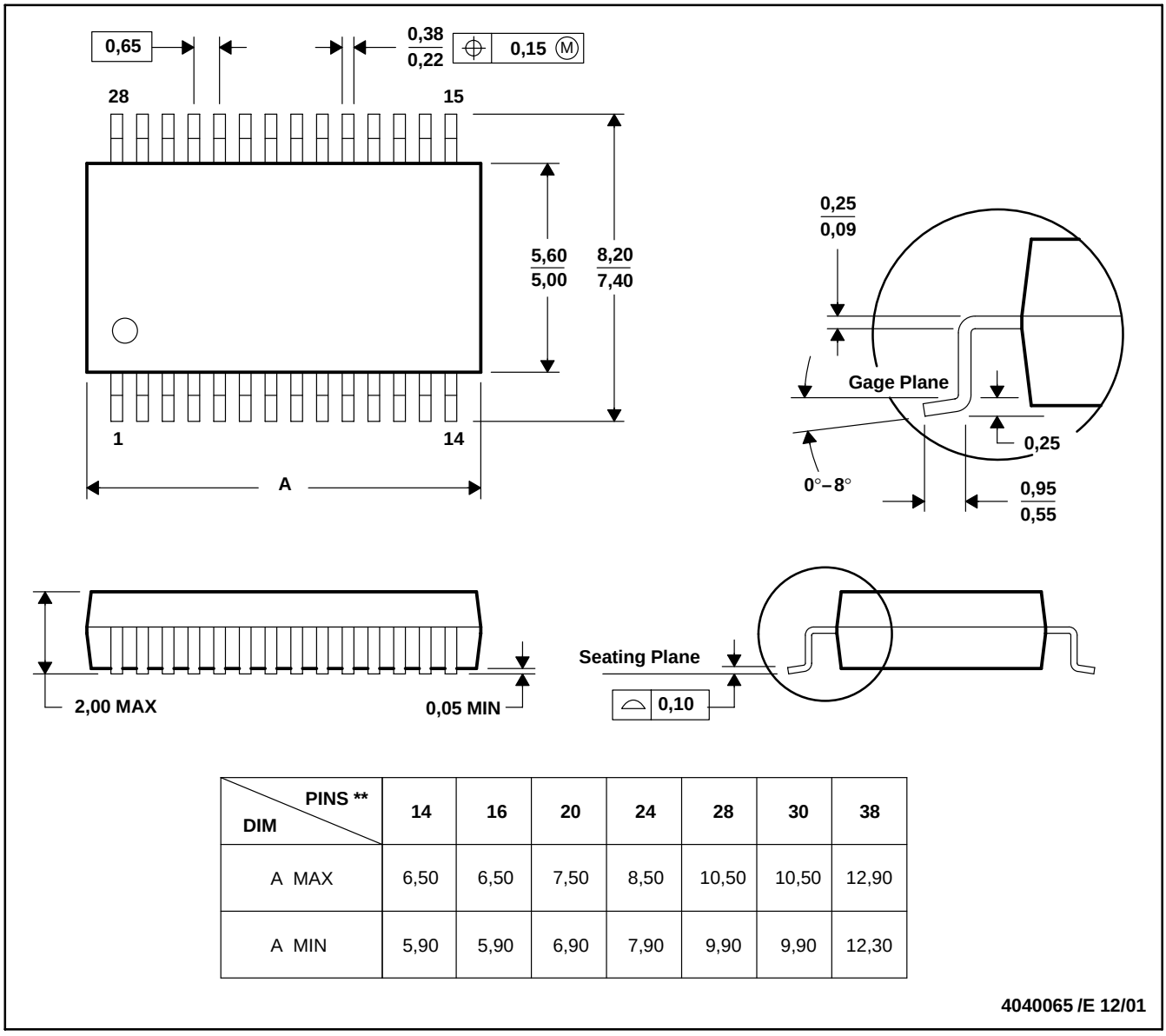
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



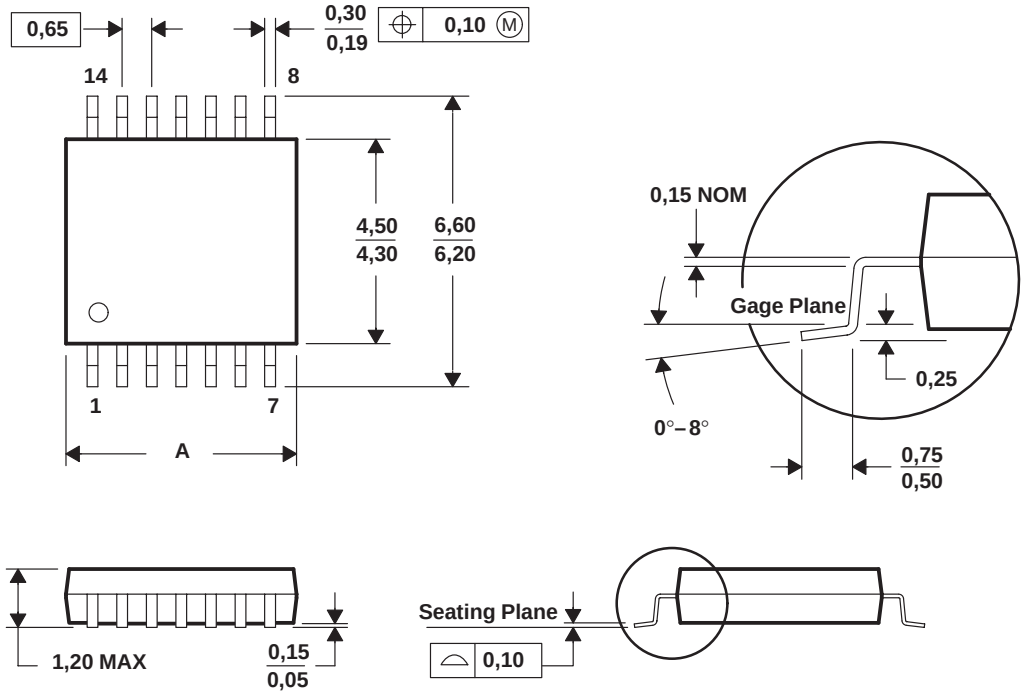
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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View RoHS Compliant Devices

SN74ABT573A, Status: ACTIVE

Octal Transparent D-Type Latches With 3-State Outputs

Features	Samples	Technical Documents
Quality & Pb-Free Data	Pricing/Packaging	Applications Notes
Related Products	Inventory	Simulation Models
Tools & Software	Symbols/Footprints	Reference Designs

Refine Your Selection
- Logic: D-Type Latches

Support
- KnowledgeBase
- Contact Technical Supp
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomencla

Datasheet

Download Datasheet **SN54ABT573, SN74ABT573A (Rev. F)** (sn74abt573a.pdf, 762 KB)
09 Sep 2003 Download

	SN74ABT573A
Voltage Nodes(V)	5
Vcc range(V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
Logic	True
No. of Outputs	8
Output Drive(mA)	-32/64
Static Current	15.12
th(ns)	1
tsu(ns)	1.9
tpd max(ns)	6.2
	Samples
	Inventory

Product Information

Features

Save this to your personal library

Typical V_{OLP} (Output Ground Bounce)
<1 V at V_{CC} = 5 V, T_A = 25°C
High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})
I_{off} Supports Partial-Power-Down Mode Operation
Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
ESD Protection Exceeds JESD 22
2000-V Human-Body Model (A114-A)
200-V Machine Model (A115-A)

Description

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the SN54ABT573 and SN74ABT573A are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE)\ input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE\ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price ($US) | QTY	Industry Standard (TI Pkg) | Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74ABT573ADBLE	OBSOLETE	-40 to 85		SSOP (DB) | 20	View			Not Available
SN74ABT573ADBR	ACTIVE	-40 to 85	0.44 | 1KU	SSOP (DB) | 20	View	2000		Purchase Samples
SN74ABT573ADBRE4	ACTIVE	-40 to 85	0.44 | 1KU	SSOP (DB) | 20	View	2000		Purchase Samples
SN74ABT573ADW	ACTIVE	-40 to 85	0.44 | 1KU	SOIC (DW) | 20	View	25		Purchase Samples
SN74ABT573ADWE4	ACTIVE	-40 to 85	0.44 | 1KU	SOIC (DW) | 20	View	25		Purchase Samples
SN74ABT573ADWR	ACTIVE	-40 to 85	0.44 | 1KU	SOIC (DW) | 20	View	2000		Purchase Samples
SN74ABT573ADWRE4	ACTIVE	-40 to 85	0.44 | 1KU	SOIC (DW) | 20	View	2000		Purchase Samples
SN74ABT573AGQNR	ACTIVE	-40 to 85	0.77 | 1KU	VFBGA (GQN) | 20		1000		Purchase Samples
SN74ABT573AN	ACTIVE	-40 to 85	0.44 | 1KU	PDIP (N) | 20	View	20		Purchase Samples
SN74ABT573ANE4	ACTIVE	-40 to 85	0.44 | 1KU	PDIP (N) | 20	View	20		Request Free Samples
SN74ABT573ANSR	ACTIVE	-40 to 85	0.44 | 1KU	SO (NS) | 20	View	2000		Purchase Samples
SN74ABT573ANSRE4	ACTIVE	-40 to 85	0.44 | 1KU	SO (NS) | 20	View	2000		Purchase Samples
SN74ABT573APW	ACTIVE	-40 to 85	0.44 | 1KU	TSSOP (PW) | 20	View	70		Purchase Samples
SN74ABT573APWE4	ACTIVE	-40 to 85	0.44 | 1KU	TSSOP (PW) | 20	View	70		Purchase Samples
SN74ABT573APWLE	OBSOLETE	-40 to 85		TSSOP (PW) | 20	View			Not Available
SN74ABT573APWR	ACTIVE	-40 to 85	0.44 | 1KU	TSSOP (PW) | 20	View	2000		Purchase Samples
SN74ABT573APWRE4	ACTIVE	-40 to 85	0.44 | 1KU	TSSOP (PW) | 20	View	2000		Purchase Samples
SN74ABT573ARGYR	ACTIVE	-40 to 85	0.51 | 1KU	QFN (RGY) | 20		1000		Request Free Samples
SN74ABT573ARGYRG4	ACTIVE	-40 to 85	0.48 | 1KU	QFN (RGY) | 20		1000		Request Free Samples
SN74ABT573AZQNR	ACTIVE	-40 to 85	0.51 | 1KU	VFBGA (ZQN) | 20		1000		Purchase Samples

Inventory

	TI Inventory Status			Reported Distributor Inventory			
SN74ABT573ADBR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2000 | 12 Dec	10 Weeks	Americas	Avnet	>1k	
		859 | 29 Dec			DigiKey	498	
		>10k | 16 Feb					
SN74ABT573ADBRE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY | Date	Lead Time	Region	Company	In Stock	Purchase

View all Distributors

Choose a Region

	0*	2000 | 12 Dec	10 Weeks	None Reported View Distributors			
		859 | 29 Dec					
		>10k | 16 Feb					
SN74ABT573ADW	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	851 | 30 Jan	9 Weeks	Americas	Arrow	>1k	
					Avnet	662	
					DigiKey	>1k	
				Asia	P&S	375	
				Europe	Arrow Southern Europe	>1k	
					EBV Elektronik	>1k	
SN74ABT573ADWE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	851 | 30 Jan	9 Weeks	None Reported View Distributors			
SN74ABT573ADWR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	862 | 30 Jan	12 Weeks	Americas	DigiKey	>1k	
SN74ABT573ADWRE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	862 | 30 Jan	12 Weeks	None Reported View Distributors			
SN74ABT573AGQNR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	820 | 27 Dec	10 Weeks	Americas	DigiKey	970	
		>10k | 7 Feb					
SN74ABT573AN	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	1491*	>10k | 6 Feb	10 Weeks	Americas	Avnet	>1k	
					DigiKey	65	
				Europe	Arrow Southern Europe	403	
SN74ABT573ANE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	1491*	>10k | 6 Feb	10 Weeks	None Reported View Distributors			
SN74ABT573ANSR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**

	0*	858 | 30 Dec	10 Weeks	None Reported View Distributors			
		>10k | 3 Feb					
SN74ABT573ANSRE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	858 | 30 Dec	10 Weeks	None Reported View Distributors			
		>10k | 3 Feb					
SN74ABT573APW	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 31 Mar	16 Weeks	None Reported View Distributors			
SN74ABT573APWE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 31 Mar	16 Weeks	None Reported View Distributors			
SN74ABT573APWR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 3 Apr	16 Weeks	Americas	DigiKey	>1k	
SN74ABT573APWRE4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	>10k | 3 Apr	16 Weeks	None Reported View Distributors			
SN74ABT573ARGYR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	807 | 9 Jan	11 Weeks	Americas	DigiKey	855	
		>10k | 13 Feb					
SN74ABT573ARGYRG4	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	807 | 9 Jan	11 Weeks	None Reported View Distributors			
		>10k | 13 Feb					
SN74ABT573AZQNR	As of 9:22 AM GMT, 29 Nov 2005			As of 9:22 AM GMT, 29 Nov 2005			
	In Stock	**In Progress QTY | Date**	**Lead Time**	**Region**	**Company**	**In Stock**	**Purchase**
	0*	834 | 28 Dec	10 Weeks	None Reported View Distributors			
		>10k | 8 Feb					

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your TI Authorized Distributor, including those listed above, for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred TI Authorized Distributor for additional information.

Quality & Lead (Pb)-Free Data

	Product Content				MTBF/FIT Rate
Device	**Eco Plan***	**Lead/Ball Finish**	**MSL Rating/Peak Reflow**	**Details**	**Details**
SN74ABT573ADBR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ADBRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ADW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ADWE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ADWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ADWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573AGQNR	TBD	SNPB	Level-1-240C-UNLIM	View	View
SN74ABT573AN	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74ABT573ANE4	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74ABT573ANSR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ANSRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573APW	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573APWE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573APWR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573APWRE4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74ABT573ARGYR	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View
SN74ABT573ARGYRG4	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View
SN74ABT573AZQNR	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

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