

N-CHANNEL VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-39 envelope and designed for application as low-power, high-frequency inverters and line drivers.

Features:

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low R_{DSon}

QUICK REFERENCE DATA

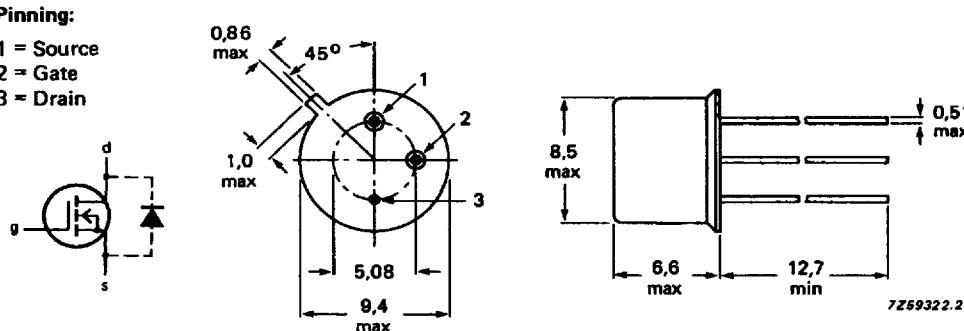
		2N6659	2N6660	2N6661
Drain-source voltage	V_{DS}	max. 35	60	90 V
Gate-source voltage (open drain)	V_{GSO}	max. 30	30	30 V
Drain current (DC)	I_D	max. 1.4	1.1	0.9 A
Total power dissipation up to $T_c = 25^\circ\text{C}$	P_{tot}	max. 6.25	6.25	6.25 W
Drain-source ON-resistance $I_D = 1.0 \text{ A}; V_{GS} = 10 \text{ V}$	R_{DSon}	typ. 0.9 max. 1.8	1.4 3.0	1.9 Ω 4.0 Ω
Transfer admittance at $f = 1 \text{ kHz}$ $I_D = 0.5 \text{ A}; V_{DS} = 25 \text{ V}$	$ Y_{fs} $	max. 170	170	170 mS

MECHANICAL DATA

Fig. 1 TO-39.

Pinning:

- 1 = Source
- 2 = Gate
- 3 = Drain



Dimensions in mm

Maximum lead diameter is guaranteed only for 12.7 mm

Accessories: 56245 (distance disc).

2N6659
2N6660
2N6661

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

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Drain-source voltage	V_{DS}	max.	35	60	90 V
Gate-source voltage (open drain)	V_{GSO}	max.	30	30	30 V
Drain current (DC)	I_D	max.	1.4	1.1	0.9 A
Drain current (peak) (note 1)	I_{DM}	max.		3.0	A
Total power dissipation up to $T_c = 25^\circ\text{C}$	P_{tot}	max.		6.25	W
Storage temperature range	T_{stg}			-65 to + 150	$^\circ\text{C}$
Junction temperature	T_j	max.		150	$^\circ\text{C}$

THERMAL RESISTANCE

From junction to case	R_{thj-c}	=	20	K/W
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CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

		2N6659	2N6660	2N6661	
Drain-source breakdown voltage $I_D = 10 \mu\text{A}; V_{GS} = 0$	$V_{(BR)DSS}$	min.	35	60	90 V
Drain-source leakage current at $V_{DS} = V_{DS\text{max}}; V_{GS} = 0$	I_{DSS}	max.	10	10	10 μA
Gate-source leakage current at $V_{GS} = 15 \text{ V}; V_{DS} = 0$	I_{GSS}	max.	100	100	100 nA
Gate threshold voltage $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$	$V_{GS(\text{th})}$	min. max.	0.8 2.0	0.8 2.0	0.8 V 2.0 V
ON-state drain current $V_{DS} = 25 \text{ V}; V_{GS} = 10 \text{ V}$	$I_{D(\text{on})}$	min. typ.	1.0 2.0	1.0 2.0	1.0 A 2.0 A
Drain-source ON-resistance $I_D = 0.3 \text{ A}; V_{GS} = 5 \text{ V}$	R_{DSon}	typ. max.	1.5 5.0	1.8 5.0	2.4 Ω 5.3 Ω
$I_D = 1.0 \text{ A}; V_{GS} = 10 \text{ V}$	R_{DSon}	typ. max.	0.9 1.8	1.4 3.0	1.9 Ω 4.0 Ω
Transfer admittance at $f = 1 \text{ kHz}$ $I_D = 0.5 \text{ A}; V_{DS} = 25 \text{ V}$	$ Y_{fs} $	min.	170	170	170 mS
Input capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 25 \text{ V}; V_{GS} = 0$	C_{iss}	max.	50	50	50 pF
Output capacitance at $f = 1 \text{ MHz}$ $V_{DS} = 25 \text{ V}; V_{GS} = 0$	C_{oss}	max.	50	40	40 pF

Note

1. Pulse conditions: $t_p \leq 300 \mu\text{s}; \delta = 0.01$.

Feedback capacitance at $f = 1$ MHz $V_{DS} = 25$ V; $V_{GS} = 0$

Switching times

 $I_D = 1.0$ A; $V_D = 25$ V; V_{GS} = 0 to 10 V

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C_{rss}	max.	15	15
			15 pF
t_{on}	typ.	5	5
	max.	10	10 ns
t_{off}	typ.	5	5 ns
	max.	10	10 ns

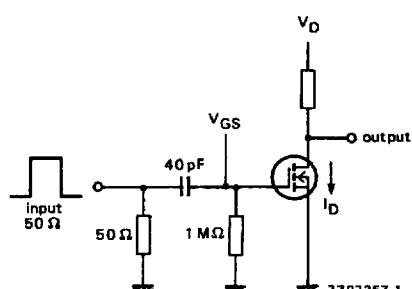


Fig. 2 Switching times test circuit.

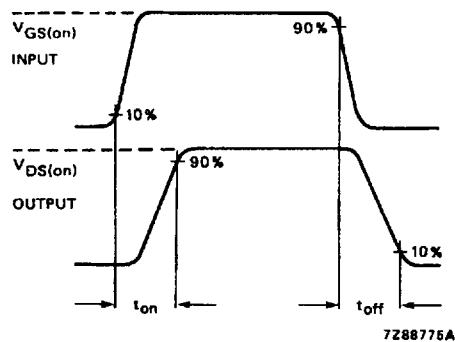


Fig. 3 Input and output waveforms.