

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.0A and 3.5A, 60V-100V

$r_{DS(on)}$ = 0.6 Ω and 0.8 Ω

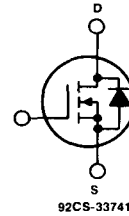
Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRFF110, IRFF111, IRFF112 and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

N-CHANNEL ENHANCEMENT MODE

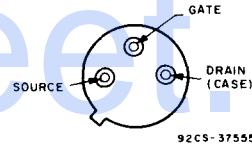


92CS-33741

3

TERMINAL DIAGRAM

TERMINAL DESIGNATION



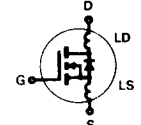
JEDEC TO-205AF

Absolute Maximum Ratings

Parameter	IRFF110	IRFF111	IRFF112	IRFF113	Units
V_{DS} Drain - Source Voltage ①	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20\text{ k}\Omega$) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM} Pulsed Drain Current ③	14	14	12	12	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	15 (See Fig. 14)				W
Linear Derating Factor	0.12 (See Fig. 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100\mu\text{H}$				A
T_J Operating Junction and	-55 to 150				$^\circ\text{C}$
T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

IRFF110, IRFF111, IRFF112, IRFF113


Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS} Drain-Source Breakdown Voltage	IRFF110 IRFF112	100	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\mu\text{A}$	
	IRFF111 IRFF113	60	—	—	V		
	ALL	2.0	—	4.0	V		
V _{GS(th)} Gate Threshold Voltage	ALL	—	—	100	nA	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	-100	nA	$V_{GS} = 20\text{V}$	
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	250	μA	$V_{GS} = -20\text{V}$	
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	1000	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$	
	ALL	—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$	
I _{D(on)} On-State Drain Current ②	IRFF110 IRFF111	3.5	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max.; $V_{GS} = 10\text{V}$	
	IRFF112 IRFF113	3.0	—	—	A		
	ALL	—	0.5	0.6	Ω		
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRFF110 IRFF111	—	0.5	0.6	Ω	$V_{GS} = 10\text{V}$, $I_D = 1.5\text{A}$	
IRFF112 IRFF113	—	0.6	0.8	Ω			
ALL	—	1.0	1.5	—	S (Ω)		
g _{fs} Forward Transconductance ②	ALL	—	135	—	pF	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max.; $I_D = 1.5\text{A}$	
C _{iss} Input Capacitance	ALL	—	80	—	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$	
C _{oss} Output Capacitance	ALL	—	20	—	pF	See Fig. 10	
C _{rss} Reverse Transfer Capacitance	ALL	—	10	20	ns	$V_{DD} = 0.5\text{BV}_{DSS}$, $I_D = 1.5\text{A}$, $Z_\theta = 50\Omega$	
t _{d(on)} Turn-On Delay Time	ALL	—	15	25	ns		
t _r Rise Time	ALL	—	15	25	ns	See Fig. 17	
t _{d(off)} Turn-Off Delay Time	ALL	—	10	20	ns	(MOSFET switching times are essentially independent of operating temperature.)	
t _f Fall Time	ALL	—	10	20	ns		
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	5.0	7.5	nC	$V_{GS} = 10\text{V}$, $I_D = 8.0\text{A}$, $V_{DS} = 0.8$ Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	
Q _{gs} Gate-Source Charge	ALL	—	2.0	3.0	nC		
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	3.0	4.5	nC		
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.	<p>Modified MOSFET symbol showing the internal device inductances.</p> 
L _S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.	

Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	8.33	$^\circ\text{C}/\text{W}$	
R _{thJA} Junction-to-Ambient	ALL	—	—	175	$^\circ\text{C}/\text{W}$	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRFF110 IRFF111	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRFF112 IRFF113	—	—	3.0	A	
	ALL	—	—	14	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	—	—	14	A	
	IRFF112 IRFF113	—	—	12	A	
V _{SD} Diode Forward Voltage ②	IRFF110 IRFF111	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 3.5\text{A}$, $V_{GS} = 0\text{V}$
	IRFF112 IRFF113	—	—	2.0	V	$T_C = 25^\circ\text{C}$, $I_S = 3.0\text{A}$, $V_{GS} = 0\text{V}$
t _{rr} Reverse Recovery Time	ALL	—	200	—	ns	$T_J = 150^\circ\text{C}$, $I_F = 3.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q _{RR} Reverse Recovered Charge	ALL	—	1.0	—	μC	$T_J = 150^\circ\text{C}$, $I_F = 3.5\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① $T_J = 25^\circ\text{C}$ to 150°C .

② Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited

by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

IRFF110, IRFF111, IRFF112, IRFF113

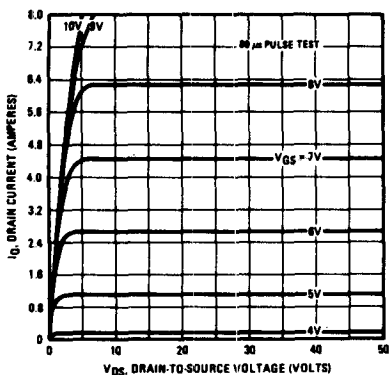


Fig. 1 - Typical Output Characteristics

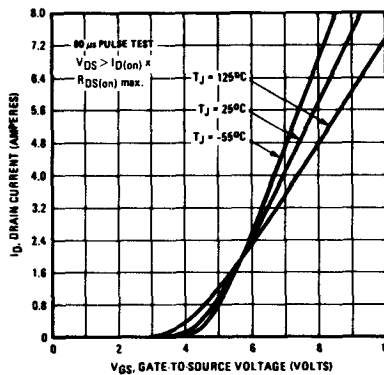


Fig. 2 - Typical Transfer Characteristics

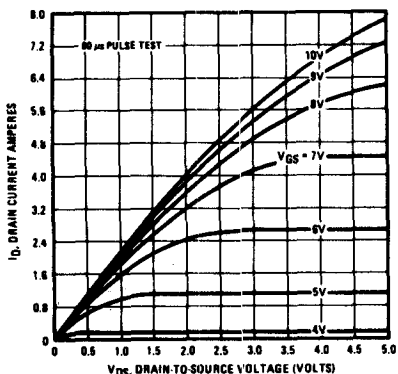


Fig. 3 - Typical Saturation Characteristics

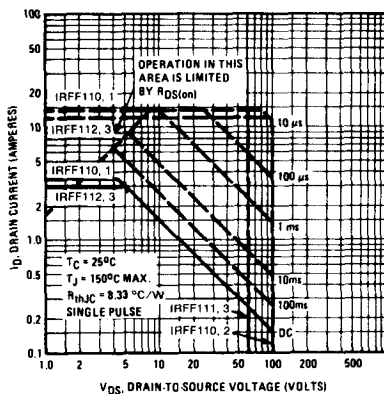


Fig. 4 - Maximum Safe Operating Area

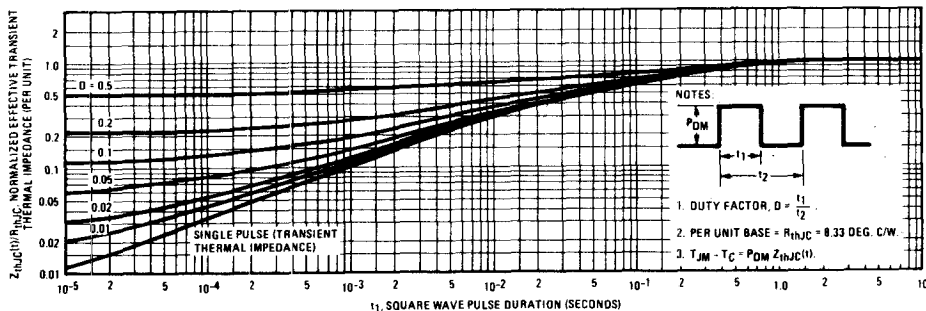


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFF110, IRFF111, IRFF112, IRFF113

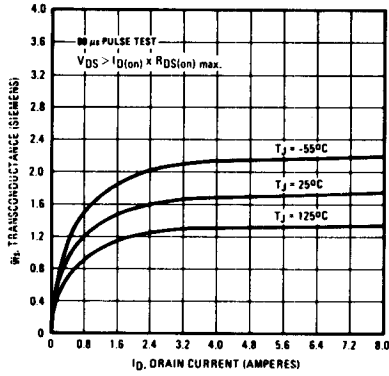


Fig. 6 – Typical Transconductance Vs. Drain Current

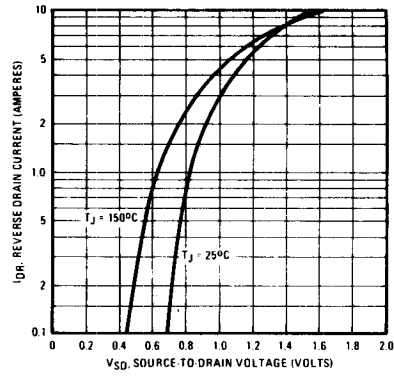


Fig. 7 – Typical Source-Drain Diode Forward Voltage

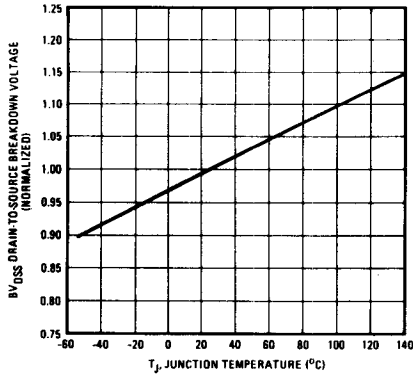


Fig. 8 – Breakdown Voltage Vs. Temperature

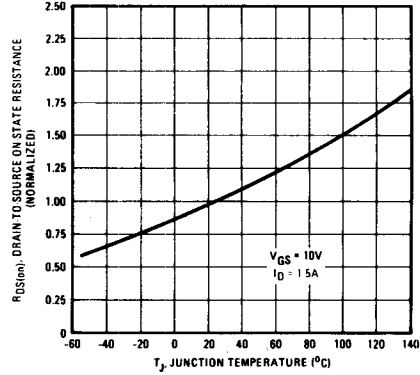


Fig. 9 – Normalized On-Resistance Vs. Temperature

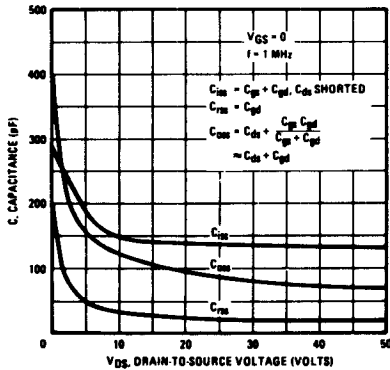


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

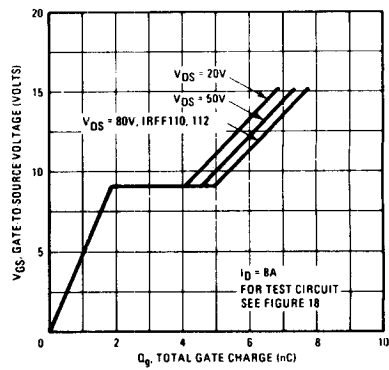


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRFF110, IRFF111, IRFF112, IRFF113

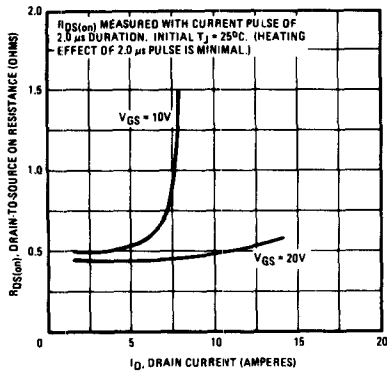


Fig. 12 - Typical On-Resistance Vs. Drain Current

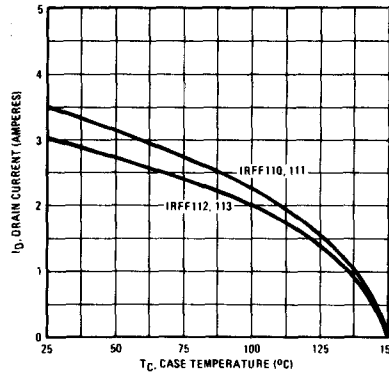


Fig. 13 - Maximum Drain Current Vs. Case Temperature

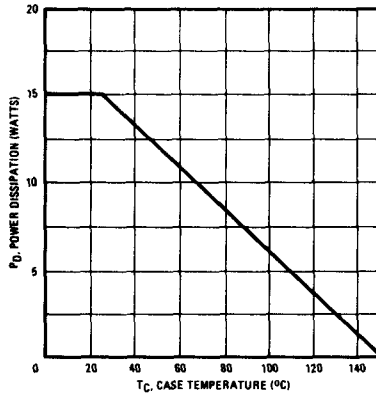


Fig. 14 - Power Vs. Temperature Derating Curve

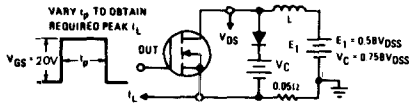


Fig. 15 - Clamped Inductive Test Circuit

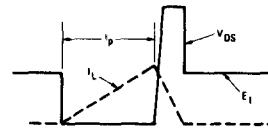


Fig. 16 - Clamped Inductive Waveforms

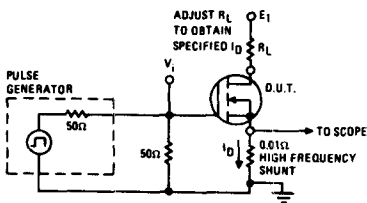


Fig. 17 - Switching Time Test Circuit

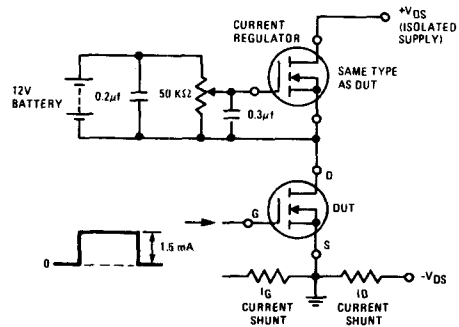


Fig. 18 - Gate Charge Test Circuit