

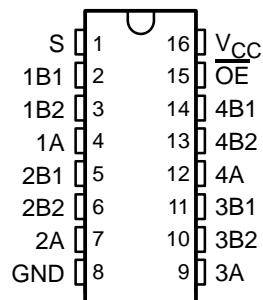
SN74CBTLV3257

LOW-VOLTAGE 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULITPLEXER

SCDS040G – DECEMBER 1997 – REVISED JANUARY 2003

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

**D, DBQ, DGV, OR PW PACKAGE
(TOP VIEW)**



description

The SN74CBTLV3257 is a 4-bit 1-of-2 high-speed FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S) input controls the data flow. The FET multiplexers/demultiplexers are disabled when the output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – DBQ	Tape and reel	SN74CBTLV3257DBQR	CL257
	SOIC – D	Tube	SN74CBTLV3257D	CBTLV3257
	TSSOP – PW	Tape and reel	SN74CBTLV3257PWR	CL257
	TVSOP – DGV	Tape and reel	SN74CBTLV3257DGVR	CL257

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		FUNCTION
\overline{OE}	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect



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 **TEXAS
INSTRUMENTS**

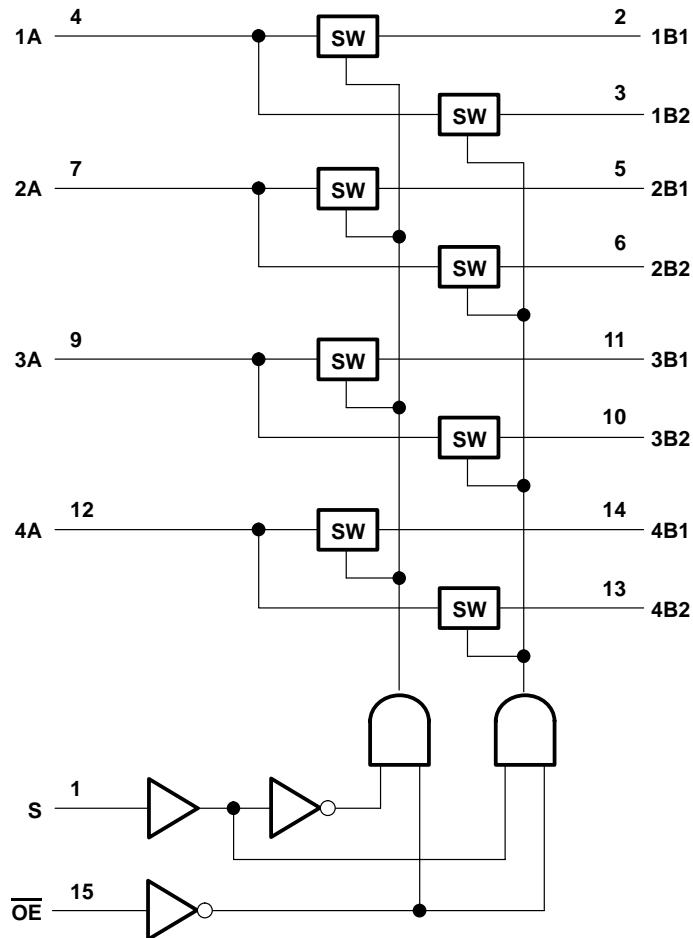
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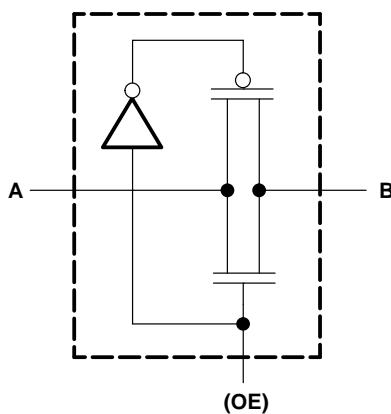
LOW-VOLTAGE 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULITPLEXER

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logic diagram (positive logic)



simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7		V
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
T _A	Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$				-1.2	V	
I_I		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND				± 1	μA	
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 3.6 V				15	μA	
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$,		$V_I = V_{CC}$ or GND		10	μA	
$\Delta I_{CC}^{\$}$	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V ,		Other inputs at V_{CC} or GND		300	μA	
C_i	Control inputs	$V_I = 3\text{ V}$ or 0				3	pF	
$C_{io(OFF)}$	A port	$V_O = 3\text{ V}$ or 0, $\overline{OE} = V_{CC}$				10.5	pF	
	B port					5.5		
r_{on}^{\parallel}	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5		8	Ω	
			$I_I = 24\text{ mA}$	5		8		
		$V_I = 1.7\text{ V}$,	$I_I = 15\text{ mA}$	27		40		
		$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$	5			
			$I_I = 24\text{ mA}$	5		7		
			$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$	10		15	

[‡]All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

[§]This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

SN74CBTLV3257

LOW-VOLTAGE 4-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B [†]	B or A		0.15		0.25	ns
	S	A or B	1.8	6.1	1.8	5.3	
t_{en}	S	A or B	1.7	6.1	1.7	5.3	ns
t_{dis}	S	A or B	1	4.8	1	4.5	ns
t_{en}	\overline{OE}	A or B	1.9	5.6	2	5	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1.6	5.5	ns

[†]The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

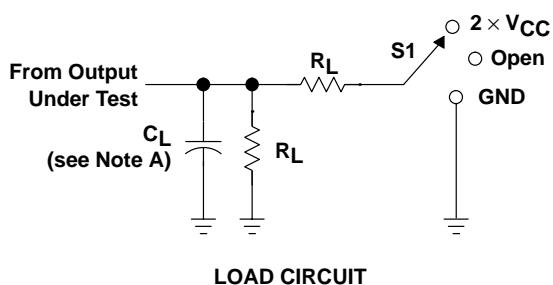


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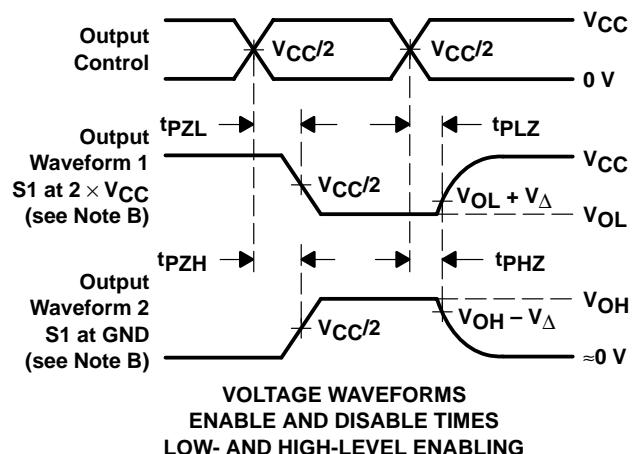
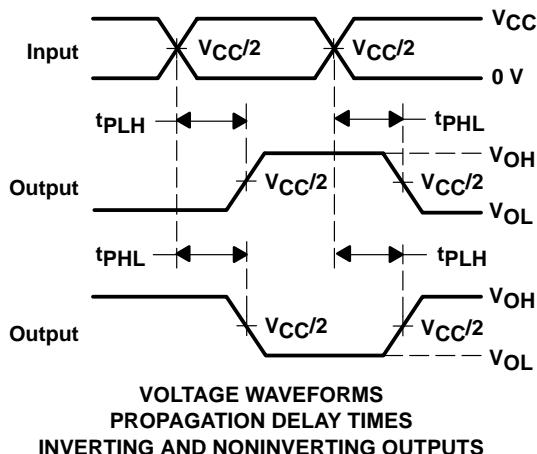
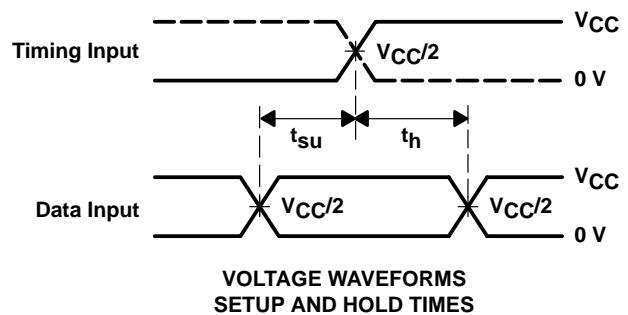
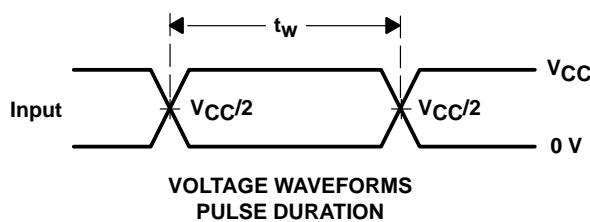
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
$2.5 V \pm 0.2 V$	30 pF	500 Ω	0.15 V
$3.3 V \pm 0.3 V$	50 pF	500 Ω	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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[APPLICATION NOTES](#) | [USER GUIDES](#) | [MORE LITERATURE](#) | [MODELS](#)

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SN74CBTLV3257, Low-Voltage 4-Bit 1-Of-2 FET Multiplexer/Demultiplexer

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN74CBTLV3257
Voltage Nodes (V)	3.3, 2.5
Vcc range (V)	2.3 to 3.6
No. of Bits	4
ron(max) (ohms)	7
tpd max (ns)	0.25

FEATURES

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- 5-Ω Switch Connection Between Two Ports
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 - 2000-V Human-Body Model (A114-A)
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DESCRIPTION

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [sn74cbtlv3257.pdf](#) (86 KB, Rev.G) (Updated: 01/03/2003)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Bus FET Switch Solutions for Live Insertion Applications](#) (SCDA009 - Updated: 02/07/2003)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Low Voltage Logic Families \(Rev. A\)](#) (SCVAE01A - Updated: 06/01/1998)
- [Selecting the Right Texas Instruments Signal Switch](#) (SZZA030 - Updated: 09/07/2001)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Texas Instruments Crossbar Switches \(Rev. A\)](#) (SCDA001A - Updated: 06/01/1995)
- [Texas Instruments Little Logic Application Report](#) (SCEA029 - Updated: 11/01/2002)

- [Texas Instruments Solution for Undershoot Protection for Bus Switches \(SCDA007 - Updated: 04/13/2000\)](#)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\) \(SZZA036A - Updated: 02/27/2003\)](#)

MORE LITERATURE[▲Back to Top](#)

- [Enhanced Plastic Portfolio Brochure \(SGZB004, 387 KB - Updated: 08/19/2002\)](#)
- [Logic Reference Guide \(SCYB004, 1032 KB - Updated: 10/23/2001\)](#)
- [MicroStar Junior BGA Design Summary \(SCET004, 167 KB - Updated: 07/28/2000\)](#)
- [Military Brief \(SGYN138, 803 KB - Updated: 10/10/2000\)](#)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\) \(SDYZ001A, 138 KB - Updated: 07/01/1996\)](#)
- [Palladium Lead Finish User's Manual \(SDYV001, 2041 KB - Updated: 11/01/1996\)](#)
- [QML Class V Space Products Military Brief \(Rev. A\) \(SGZN001A, 257 KB - Updated: 10/07/2002\)](#)
- [Standard Linear & Logic for PCs, Servers & Motherboards \(SCYB005, 3997 KB - Updated: 06/13/2002\)](#)

USER GUIDES[▲Back to Top](#)

- [CBT \(5-V\) And CBTLV \(3.3-V\) Bus Switches Data Book \(Rev. B\) \(SCDD001B, 5433 KB - Updated: 12/01/1998\)](#)
- [LOGIC Pocket Data Book \(SCYD013, 4837 KB - Updated: 12/05/2002\)](#)
- [Signal Switch Data Book \(SCDD003, 10259 KB - Updated: 03/19/2001\)](#)

SAMPLES[▲Back to Top](#)

<u>ORDERABLE DEVICE</u>	<u>PACKAGE INDUSTRY (TI)</u>	<u>PINS</u>	<u>TEMP (°C)</u>	<u>STATUS</u>	<u>PRODUCT CONTENT</u>	<u>SAMPLES</u>
SN74CBTLV3257D	SOIC (D)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74CBTLV3257DBQR	SSOP (DBQ)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74CBTLV3257DGVR	TVSOP (DGV)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74CBTLV3257DR	SOIC (D)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74CBTLV3257PWR	TSSOP (PW)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG[▲Back to Top](#)**DEVICE INFORMATION**

Updated Daily

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SN74CBTLV3257D	ACTIVE	SOIC (D) 16	-40 TO 85	View Contents	1KU 0.48	40
SN74CBTLV3257DBQR	ACTIVE	SSOP (DBQ) 16	-40 TO 85	View Contents	1KU 0.48	2500
SN74CBTLV3257DGVR	ACTIVE	TVSOP (DGV) 16	-40 TO 85	View Contents	1KU 0.48	2000

TI INVENTORY STATUS

As Of 09:00 AM GMT, 17 Apr 2003

<u>IN STOCK</u>	<u>IN PROGRESS QTY DATE</u>	<u>LEAD TIME</u>
4960*	>10k 13 May	4 WKS
>10k*	>10k 09 May	2 WKS

REPORTED DISTRIBUTOR INVENTORY

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SN74CBTLV3257PW	ACTIVE	<u>TSSOP (PW)</u>	16	-40 TO 85	View Contents	1KU 0.91	90
SN74CBTLV3257PWR	ACTIVE	<u>TSSOP (PW)</u>	16	-40 TO 85	View Contents	1KU 0.48	2000
SN74CBTLV3257RGYR	ACTIVE	<u>QFN (RGY)</u>	16	-40 TO 85	View Contents	1KU 1.58	1000

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	19 12 May				
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- [IBIS Model of SN74CBTLV3257](#) (SCDM013, 146 KB - Updated: 11/08/2002)
- [IBIS Model of SN74CBTLV3257](#) (SCDM013, 25 KB, ZIP - Updated: 11/08/2002)

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