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Linear & Switching Voltage Regulator Handbook

ON Semiconductor™

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Linear & Switching Voltage Regulator Applications Information

In Brief . . .

In most electronic systems, voltage regulation is required for various functions. Today's complex electronic systems are requiring greater regulating performance, higher efficiency and lower parts count. Present integrated circuit and power package technology has produced IC voltage regulators which can ease the task of regulated power supply design, provide the performance required and remain cost effective. Available in a growing variety, ON Semiconductor offers a wide range of regulator products from fixed and adjustable voltage types to special–function and switching regulator control ICs.

This handbook describes ON Semiconductor's voltage regulator products and provides information on applying these products. Basic Linear regulator theory and switching regulator topologies have been included along with practical design examples. Other relevant topics include trade–offs of Linear versus switching regulators, series pass elements for Linear regulators, switching regulator component design considerations, heatsinking, construction and layout, power supply supervision and protection, and reliability.

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SECTION 1
BASIC LINEAR REGULATOR THEORY

A. IC Voltage Regulator

The basic functional block diagram of an integrated circuit voltage regulator is shown in Figure 1–1. It consists of a stable reference, whose output voltage is V_{ref}, and a high gain error amplifier. The output voltage (V_O), is equal to or a multiple of V_{ref}. The regulator will tend to keep V_O constant by sensing any changes in V_O and trying to return it to its original value. Therefore, the ideal voltage regulator could be considered a voltage source with a constant output voltage. However, in practice the IC regulator is better represented by the model shown in Figure 1–2.

In this figure, the regulator is modeled as a voltage source with a positive output impedance (Z_O). The value of the voltage source (V) is not constant; instead it varies with changes in supply voltage (V_{CC}) and with changes in IC junction temperature (T_J) induced by changes in ambient temperature and power dissipation. Also, the regulator output voltage (V_O) is affected by the voltage drop across Z_O, caused by the output current (I_O). In the following text, the reference and amplifier sections will be described, and their contributions to the changes in the output voltage analyzed.

B. Voltage Reference

Naturally, the major requirement for the reference is that it be stable; variations in supply voltage or junction temperature should have little or no effect on the value of the reference voltage (V_{ref}).

1. Zener Diode Reference

The simplest form of a voltage reference is shown in Figure 1–3a. It consists of a resistor and a zener diode. The zener voltage (V_Z) is used as the reference voltage. In order to determine V_Z, consider Figure 1–3b. The zener diode (VR1) of Figure 1–3a has been replaced with its equivalent circuit model and the value of V_Z is therefore given by (at a constant junction temperature):

$$V_Z = V_{BZ} + I_Z Z_Z = V_{BZ} + \left(\frac{V_{CC} - V_{BZ}}{R + Z_z}\right) Z_Z \qquad (1)$$

where: V_{BZ} = zener breakdown voltage
I_Z = zener current
Z_Z = zener impedance at I_Z.

Note that changes in the supply voltage give rise to changes in the zener current, thereby changing the value of the reference voltage (V_Z).

Figure 1–1. Voltage Regulator Functional Block Diagram

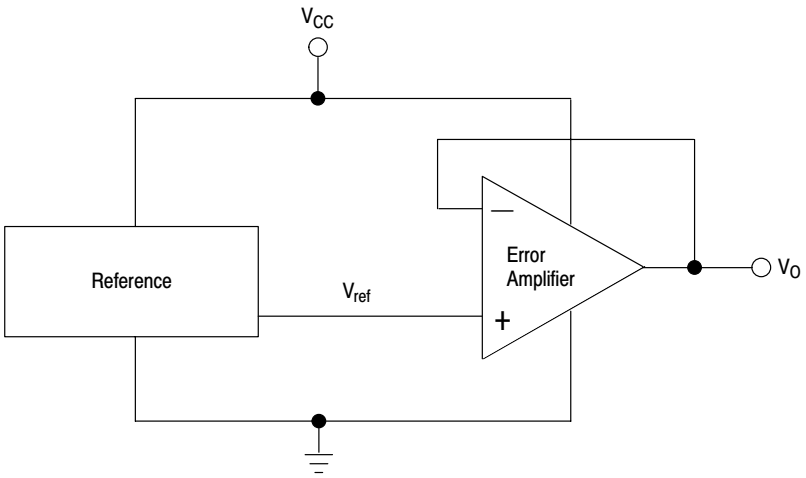


Figure 1–2. Voltage Regulator Equivalent Circuit Model

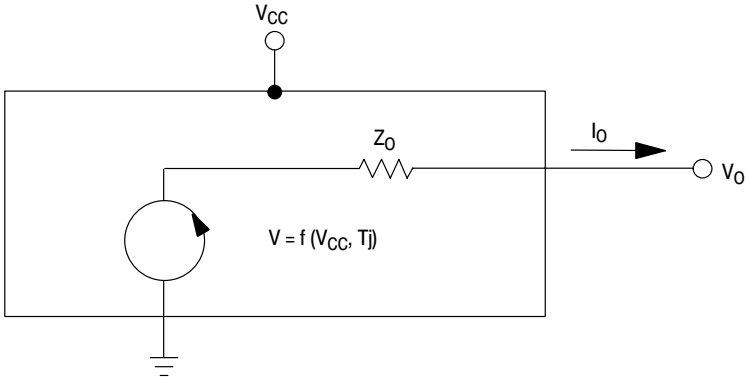
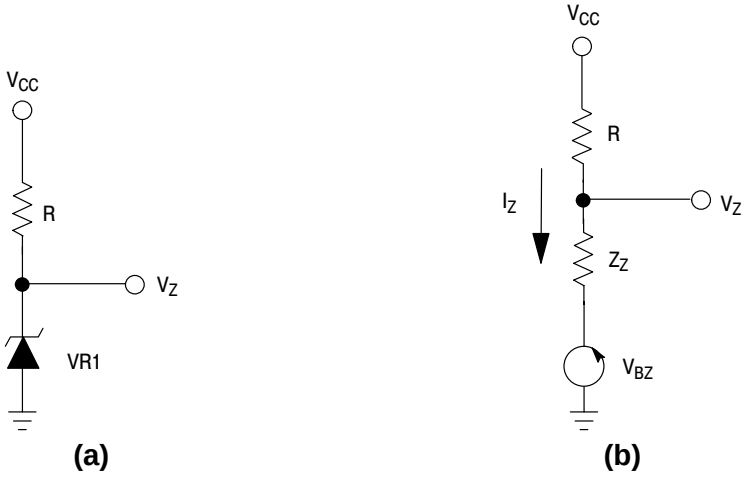


Figure 1–3. Zener Diode Reference



2. Constant Current — Zener Reference

The effect of zener impedance can be minimized by driving the zener diode with a constant current as shown in Figure 1–4. The value of the zener current is largely independent of V_{CC} and is given by:

$$I_Z = \frac{V_{BEQ1}}{R_{SC}} \quad (2)$$

where: V_{BEQ1} = base–emitter voltage of Q1.

This gives a reference voltage of:

$$V_{ref} = V_Z + V_{BEQ1} = V_{BZ} + I_Z Z_Z + V_{BEQ1} \quad (3)$$

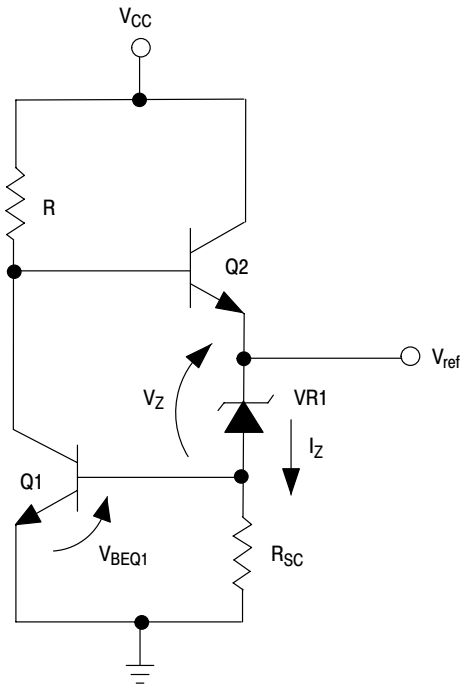
where I_Z is constant and given by Equation 2.

The reference voltage (about 7.0 V) of this configuration is therefore largely independent of supply voltage variations. This configuration has the additional benefit of better temperature stability than that of a simple resistor–zener reference.

Referring back to Figure 1–3a, it can be seen that the reference voltage temperature stability is equal to that of the zener diode, VR1. The stability of zener diodes used in most integrated circuitry is about + 2.2 mV/°C or ≃ 0.04%/°C (for a 6.2 V zener). If the junction temperature varies 100°C, the zener or reference voltage would vary 4%. A variation this large is usually unacceptable.

However, the circuit of Figure 1–4 does not have this drawback. Here the positive 2.2 mV/°C temperature coefficient (TC) of the zener diode is offset by the negative 2.2 mV/°C TC of the V_{BE} of Q1. This results in a reference voltage with very stable temperature characteristics.

Figure 1–4. Constant Current (Zener Reference)



3. Bandgap Reference

Although very stable, the circuit of Figure 1–4 does have a disadvantage in that it requires a supply voltage of 9.0 V or more. Another type of stable reference which requires only a few volts to operate was described by Widlar[1] and is shown in Figure 1–5. In this circuit V_{ref} is given by:

$$V_{ref} = V_{BEQ3} + I_2R_2 \quad (4)$$

where: $$I_2 = \frac{V_{BEQ1} - V_{BEQ2}}{R_1}$$ (neglecting base currents)

The change in V_{ref} with junction temperature is given by:

$$\Delta V_{ref} = \Delta V_{BE3} + \left\{ \frac{\Delta V_{BEQ1} - \Delta V_{BEQ2}}{R_1} \right\} R_2 \quad (5)$$

It can be shown that,

$$\Delta V_{BEQ1} = \Delta T_J K \ln I_1 \quad (6)$$

and, $$\Delta V_{BEQ2} = \Delta T_J K \ln I_2 \quad (7)$$

where: K = a constant

ΔT_J = change in junction temperature

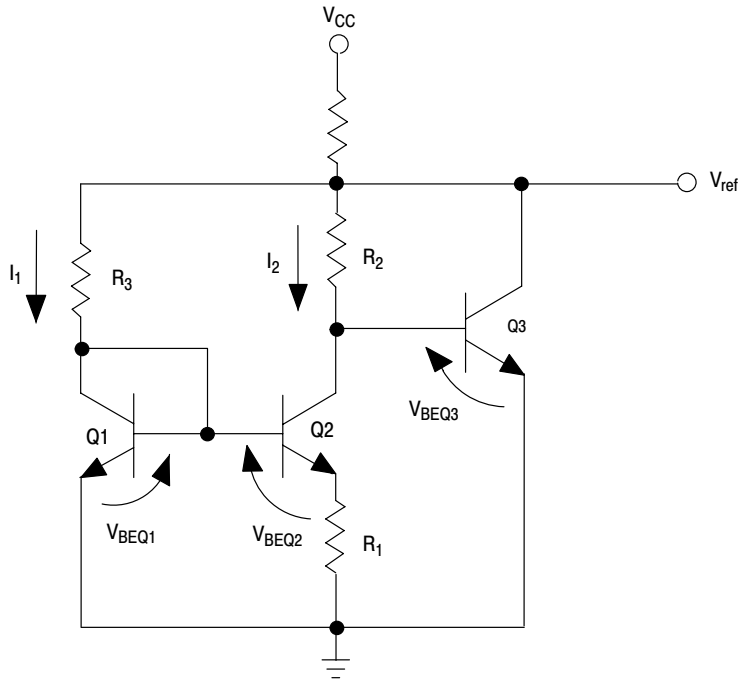
and, $I_1 > I_2$

Combining (5), (6), and (7)

$$\Delta V_{ref} = \Delta V_{BEQ3} + \Delta T_J K \left(\frac{R_2}{R_1} \right) \ln \frac{I_1}{I_2} \quad (8)$$

Since ΔV_{BEQ3} is negative, and with $I_1 > I_2$, $\ln I_1/I_2$ is positive, the net change in V_{ref} with temperature variations can be made to equal zero by appropriately selecting the values of I_1, R_1, and R_2.

Figure 1–5. Bandgap Reference



C. The Error Amplifier

Given a stable reference, the error amplifier becomes the determining factor in integrated circuit voltage regulator performance. Figure 1–6 shows a typical differential error amplifier in a voltage regulator configuration. With a constant supply voltage (V_{CC}) and junction temperature, the output voltage is given by:

$$V_O = A_{VOL}\,\upsilon_i - Z_{OL}\,I_O = A_{VOL}\,\{(V_{ref} \pm V_{IO}) - V_O\,\beta\} - Z_{OL}\,I_O \quad (9)$$

where: A_{VOL} = amplifier open loop gain

V_{IO} = input offset voltage

Z_{OL} = open loop output impedance

$\beta = \dfrac{R_1}{R_1 + R_2}$ = feedback ratio (β is always ≤ 1)

I_O = output current

υ_i = true differential input voltage

Manipulating Equation 9:

$$V_O = \frac{(V_{ref} \pm V_{IO}) - \dfrac{Z_{OL}}{A_{VOL}}\,I_O}{\beta + \dfrac{1}{A_{VOL}}} \quad (10)$$

Note that if the amplifier open loop gain is infinite, this expression reduces to:

$$V_O = \frac{1}{\beta}\,(V_{ref} \pm V_{IO}) = (V_{ref} \pm V_{IO})\quad \left(1 + \frac{R_2}{R_1}\right) \quad (11)$$

The output voltage can thus be set any value equal to or greater than ($V_{ref} \pm V_{IO}$). Note also that if A_{VOL} is not infinite, with constant output current (a non–varying output load), the output voltage can still be "tweaked–in" by varying R_1 and R_2, even though V_O will not exactly equal that given by Equation 11.

Assuming a stable reference and a finite value of A_{VOL}, inaccuracy of the output voltage can be traced to the following amplifier characteristics:

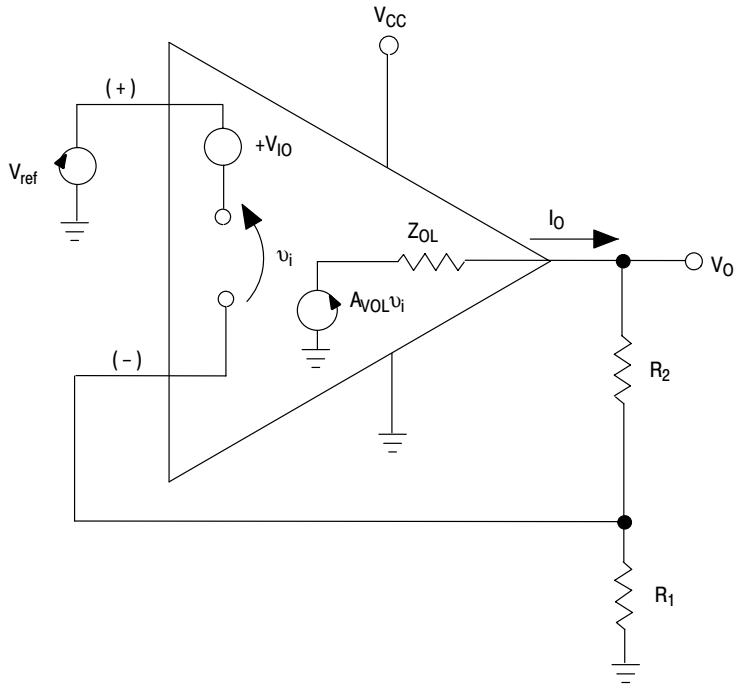
1. Amplifier Input Offset Voltage Drift

The input transistors of integrated circuit amplifiers are usually not perfectly matched. As in operational amplifiers, this is expressed in terms of an input offset voltage (V_{IO}). At a given temperature, this effect can be nulled out of the desired output voltage by adjusting V_{ref} or $1/\beta$. However, V_{IO} drifts with temperature, typically $\pm$ 5.0 μV/°C to +15 μV/°C, causing a proportional change in the output voltage. Closer matching of the internal amplifier input transistors minimizes this effect, as does selecting a feedback ratio (β) to be close to unity.

2. Amplifier Power Supply Sensitivity

Changes in regulator output voltage due to power supply voltage variations can be attributed to two amplifier performance parameters: power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). In modern integrated circuit regulator amplifiers, the utilization of constant current sources gives such large values of PSRR that this effect on V_O can usually be neglected. However, supply voltage changes can affect the output voltage since these changes appear as common mode voltage changes, and they are best measured by the CMRR.

Figure 1–6. Typical Voltage Regulator Configuration



The definition of common mode voltage (V_{CM}), illustrated by Figure 1–7a, is:

$$V_{CM} = \left[\frac{V_1 + V_2}{2}\right] - \left[\frac{(V+) + (V-)}{2}\right] \quad (12)$$

where: V_1 = voltage on amplifier noninverting input
V_2 = voltage on amplifier inverting input
V+ = positive supply voltage
V– = negative supply voltage

Figure 1–7. Definition of Common Mode Voltage Error

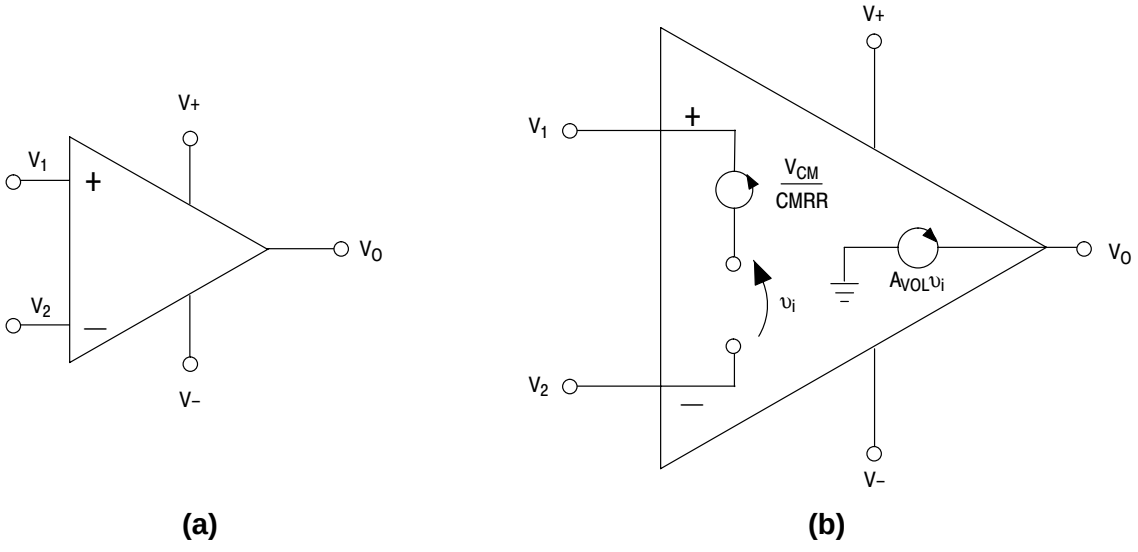
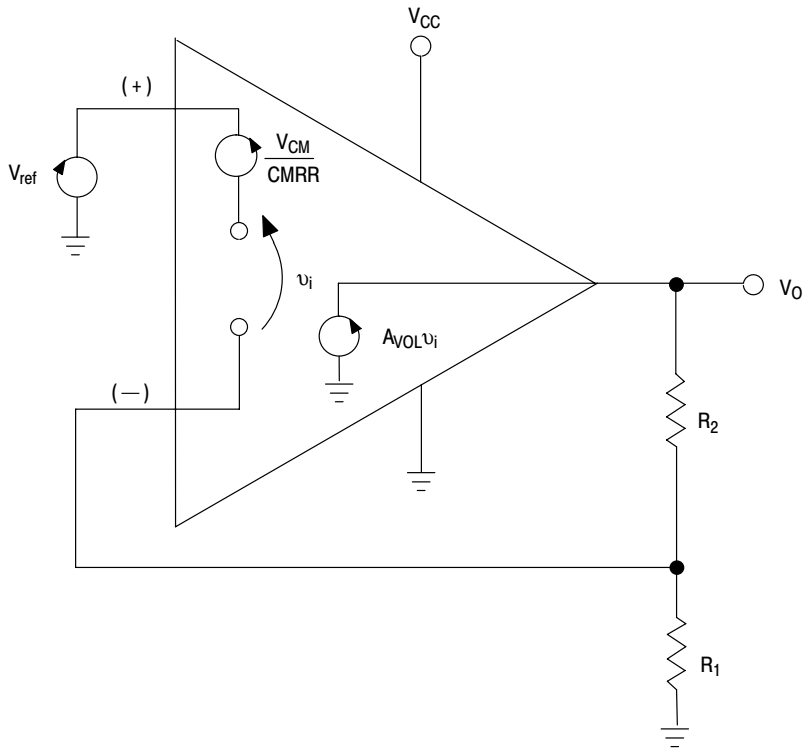


Figure 1–8. Common Mode Regulator Effects



In an ideal amplifier, only the differential input voltage ($V_1 – V_2$) has any effect on the output voltage; the value of V_{CM} would not effect the output. In fact, V_{CM} does influence the amplifier output voltage. This effect can be modeled as an additional voltage offset at the amplifier input equal to V_{CM}/CMRR as shown in Figures 1–7b and 1–8. The latter figure is the same configuration as Figure 1–6, with amplifier input offset voltage and output impedance deleted for clarity and common mode voltage effects added. The output voltage of this configuration is given by:

$$V_O = A_{VOL}\,\upsilon_i = A_{VOL}\left(V_{ref} - \frac{V_{CM}}{CMRR} - \beta V_O\right) \tag{13}$$

Manipulating,

$$V_O = \frac{\left(V_{ref} - \frac{V_{CM}}{CMRR}\right)}{\beta + \frac{1}{A_{VOL}}} \tag{14}$$

where: $V_{CM} = V_{ref} - \frac{V_{CC}}{2}$ (15)

and, CMRR = common mode rejection ratio

It can be seen from Equations (14) and (15) that the output can vary when V_{CC} varies. This can be reduced by designing the amplifier to have a high A_{VOL}, a high CMRR, and by choosing the feedback ratio (β) to be unity.

3. Amplifier Output Impedance

Referring back to Equation (9), it can be seen that the equivalent regulator output impedance (Z_O) is given by:

$$Z_O = \frac{\Delta V_O}{\Delta I_O} \simeq \frac{Z_{OL}}{\beta A_{VOL}} \quad (16)$$

This impedance must be as low as possible, in order to minimize load current effects on the output voltage. This can be accomplished by lowering Z_{OL}, choosing an amplifier with high A_{VOL}, and by selecting the feedback ratio (β) to be unity.

A simple way of lowering the effective value of Z_{OL} is to make an impedance transformation with an emitter follower, as shown in Figure 1–9. Given a change in output current (ΔI_O) the amplifier will see a change of only $\Delta I_O/h_{FEQ1}$ in its output current (I_O'). Therefore, (Z_{OL}) in Equation (16) has been effectively reduced to Z_{OL}/h_{FEQ1}, reducing the overall regulator output impedance (Z_O).

D. The Regulator within a Regulator Approach

In the preceding text, we have analyzed the sections of an integrated circuit voltage regulator and determined how they contribute to its non–ideal performance characteristics. These are shown in Table 1–1 along with procedures which minimize their effects.

It can be seen that in all cases regulator performance can be improved by selecting A_{VOL} as high as possible and $\beta = 1$. Since a limit is soon approached in how much A_{VOL} can be practically obtained in an integrated circuit amplifier, selecting a feedback ratio (β) equal to unity is the only viable way of improving total regulator performance, especially in reducing regulator output impedance. However, this method presents a basic problem to the regulator designer. If the configuration of Figure 1–6 is used, the output voltage cannot be adjusted to a value other than V_{ref}. The solution is to utilize a different regulator configuration known as the *regulator within a regulator* approach.[2] Its greatest benefit is in reducing total regulator output impedance.

Figure 1–9. Emitter Follower Output

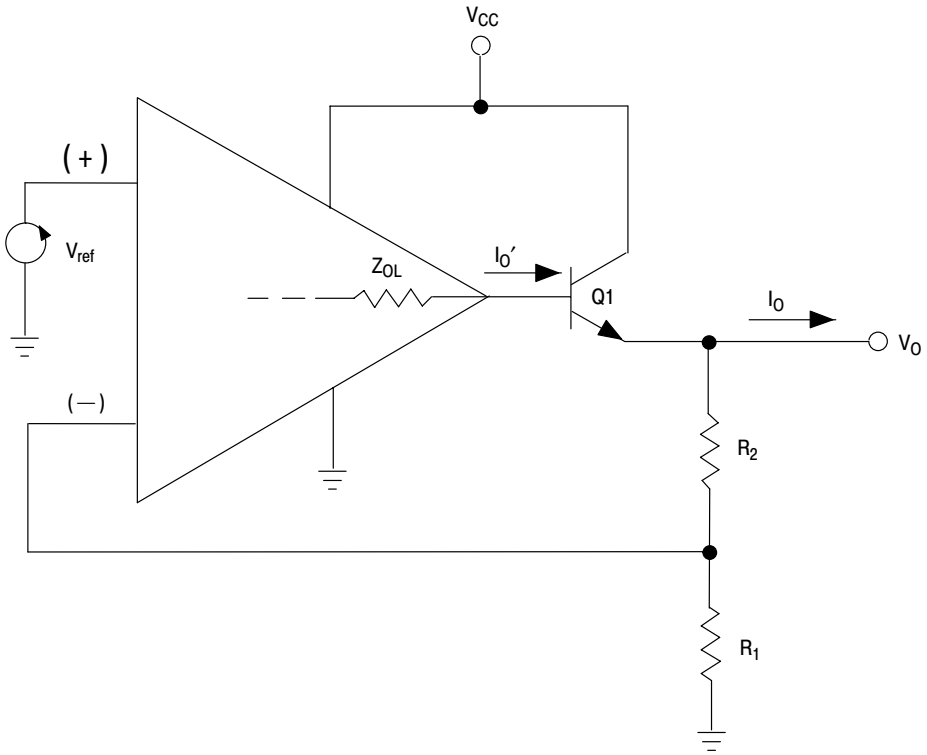


Table 1–1

V_O Changes Section	Effect Can Be Induced By:	Minimized By Selecting:
Reference	V_{CC}	• Constant current–zener method • Bandgap reference
	T_J	• Bandgap reference • TC compensated zener method
Amplifier	V_{CC}	• High CMRR amplifier • High A_{VOL} amplifier • $\beta = 1$
	T_J	• Low V_{IO} drift amplifier • High A_{VOL} amplifier • $\beta = 1$
	I_O	• Low Z_{OL} amplifier • High A_{VOL} amplifier • Additional emitter follower output • $\beta = 1$

As shown in Figure 1–10, amplifier A1 sets up a voltage (V_1) given by:

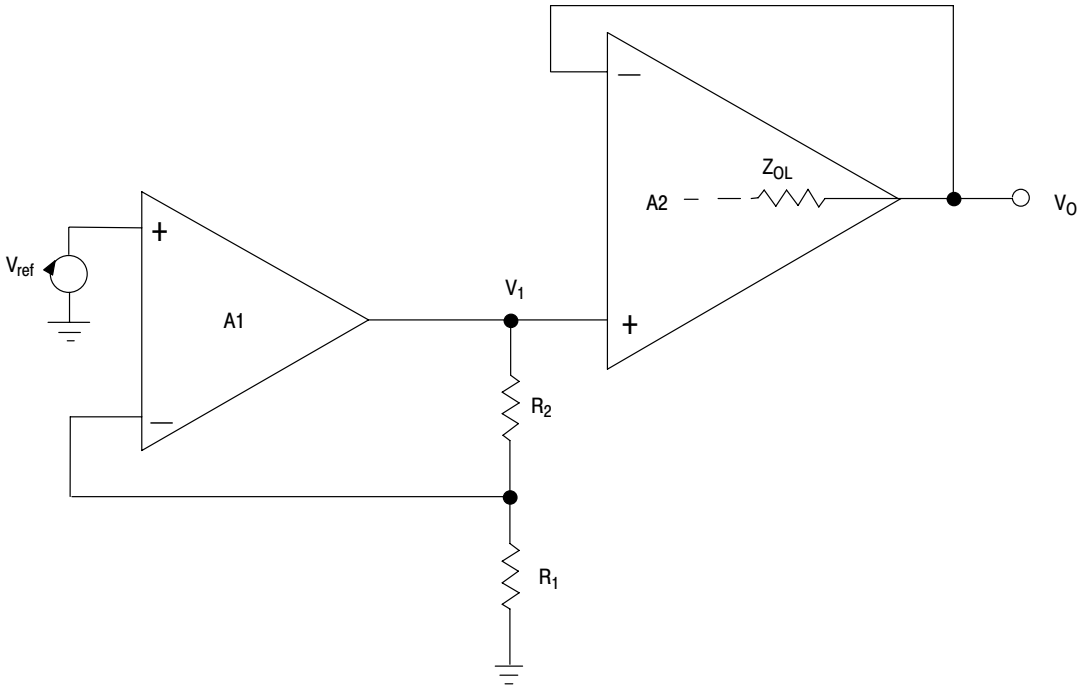
$$V_1 \simeq V_{ref} \left(1 + \frac{R_2}{R_1}\right) \quad (17)$$

V_1 now serves as the reference voltage for amplifier A2, whose output voltage (V_O) is given by:

$$V_O \simeq V_1 \simeq V_{ref} \left(1 + \frac{R_2}{R_1}\right) \quad (18)$$

Note that the output impedance of A2, and therefore the regulator output impedance, has been minimized by selecting A2's feedback factor to be unity; and that output voltage can still be set at voltages greater than V_{ref} by adjusting R_1 and R_2.

Figure 1–10. The "Regulator within a Regulator" Configuration



(1)Widlar, R. J., *New Developments in IC Voltage Regulators*, IEEE Journal of Solid State Circuits, Feb.1971, Vol. SC–6, pgs. 2–7.
(2)Tom Fredericksen, IEEE Journal of Solid State Circuits, Vol. SC–3, Number 4, Dec. 1968, *A Monolithic High Power Series Voltage Regulator.*

SECTION 2
SELECTING A LINEAR IC VOLTAGE REGULATOR

A. Selecting the Type of Regulator

There are five basic linear regulator types; positive, negative, fixed output, tracking and floating regulators. Each has its own particular characteristics and best uses, and selection depends on the designer's needs and trade–offs in performance and cost.

1. Positive Versus Negative Regulators

In most cases, a positive regulator is used to regulate positive voltages and a negative regulator negative voltages. However, depending on the system's grounding requirements, each regulator type may be used to regulate the "opposite" voltage.

Figures 2–1a and 2–1b show the regulators used in the conventional and obvious mode. Note that the ground reference for each (indicated by the heavy line) is continuous. Several positive regulators could be used with the same input supply to deliver several voltages with common grounds; negative regulators may be utilized in a similar manner.

If no other common supplies or system components operate off the input supply to the regulator, the circuits of Figures 2–1c and 2–1d may be used to regulate positive voltages with a negative regulator and vice versa. In these configurations, the input supply is essentially floated, i.e., neither side of the input is tied to the system ground.

There are methods of utilizing positive regulators to obtain negative output voltages without sacrificing ground bus continuity. However, these methods are only possible at the expense of increased circuit complexity and cost. An example of this technique is shown in Section 3.

2. Three–Terminal, Fixed Output Regulators

These regulators offer the designer a simple, inexpensive way to obtain a source of regulated voltage. They are available in a variety of positive or negative output voltages and current ranges.

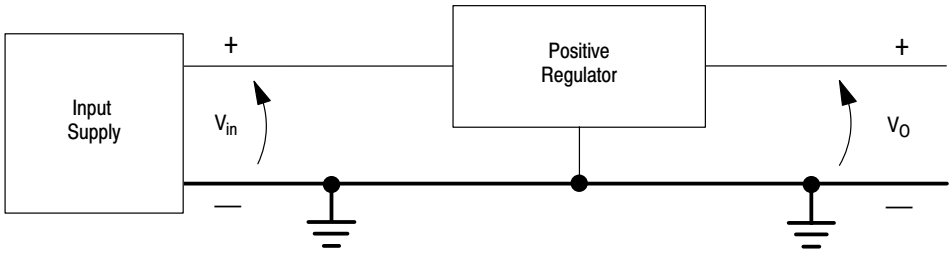
The advantages of these regulators are:

a) Easy to use.
b) Internal overcurrent and thermal protection.
c) No circuit adjustments necessary.
d) Low cost.

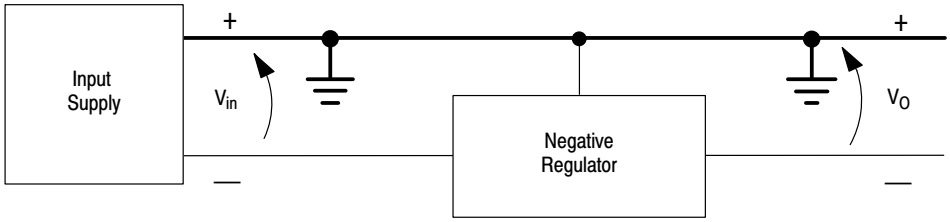
Their disadvantages are:

a) Output voltage cannot be precisely adjusted. (Methods for obtaining adjustable outputs are shown in Section 3).
b) Available only in certain output voltages and currents.
c) Obtaining greater current capability is more difficult than with other regulators. (Methods for obtaining greater output currents are shown in Section 3.)

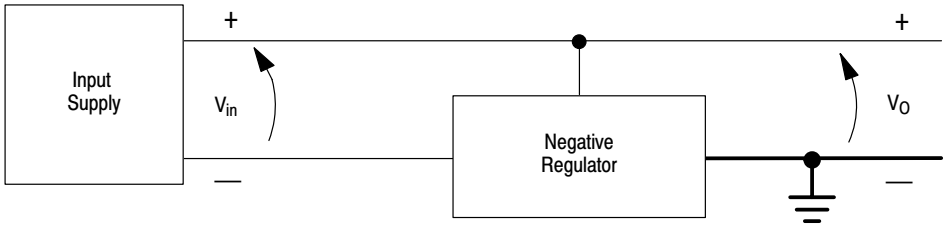
Figure 2–1. Regulator Configurations



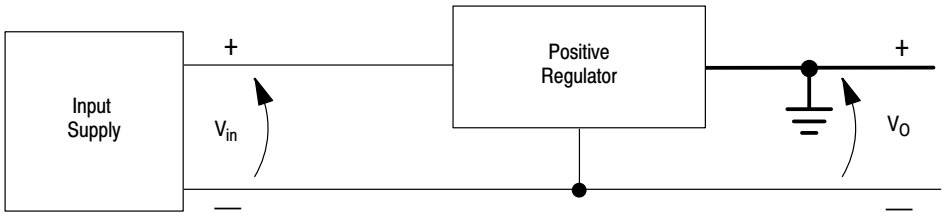
(a) Positive Output Using Positive Regulator



(b) Negative Output Using Negative Regulator



(c) Positive Output Using Negative Regulator



(d) Negative Output Using Positive Regulator

3. Three–Terminal, Adjustable Output Regulators

Like the three–terminal fixed regulators, the three–terminal adjustable regulators are easy and inexpensive to use. These devices provide added flexibility with output voltage adjustable over a wide range, from 1.2 V to nearly 40 V, by means of an external, two–resistor voltage divider. A variety of current ranges from 100 mA to 3.0 A are available.

B. Selecting an IC Regulator

Once the type of regulator is decided upon, the next step is to choose a specific device. To provide higher currents than are available from monolithic technologies, an IC regulator will often be used as a driver to a boost transistor. This complicates the selection and design task, as there are now several overlapping solutions to many of the design problems.

Unfortunately, there is no exact step–by–step procedure that can be followed which will lead to the ideal regulator and circuit configuration for a specific application. The regulating circuit that is finally accepted will be a compromise between such factors as performance, cost, size and complexity. Because of this, the following general design procedure is suggested:

1. Select the regulators which meet or exceed the requirements for line regulation, load regulation, TC of the output voltage and operating ambient temperature range. At this point, do not be overly concerned with the regulator capabilities in terms of output voltage, output current, SOA and special features.

2. Next, select application circuits from Section 3 which meet the requirements for output current, output voltage, special features, etc. Preliminary designs using the chosen regulators and circuit configurations are then possible. From these designs a judgement can be made by the designer as to which regulator circuit configuration combination best meets his or her requirements in terms of cost, size and complexity.

SECTION 3
LINEAR REGULATOR CIRCUIT CONFIGURATION AND DESIGN CONSIDERATIONS

Once the IC regulators, which meet the designer's performance requirements, have been selected, the next step is to determine suitable circuit configurations. Initial designs are devised and compared to determine the IC regulator/circuit configuration that best meets the designer's requirements. In this section, several circuit configurations and design equations are given for the various regulator ICs. Additional circuit configurations can be found on the device data sheets. Organization is first by regulator type and then by variants, such as current boost. Each circuit diagram has component values for a particular voltage and current regulator design.

A. Positive, Adjustable
B. Negative, Adjustable
C. Positive, Fixed
D. Negative, Fixed
E. Tracking
F. Special
    1. Obtaining Extended Output Voltage Range
    2. Electronic Shutdown
G. General Design Considerations

It should be noted that all circuit configurations shown have constant current limiting. If foldback limiting is desired, see Section 4C for techniques and design equations.

A. Positive, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations

Positive Three–Terminal Adjustables

These adjustables, comprised of the LM317L, LM317, and LM350 series devices range in output currents of 100 mA, 500 mA, 1.5 A, and 3.0 A respectively. All of these devices utilize the same basic circuit configuration as shown in Figure 3–1A.

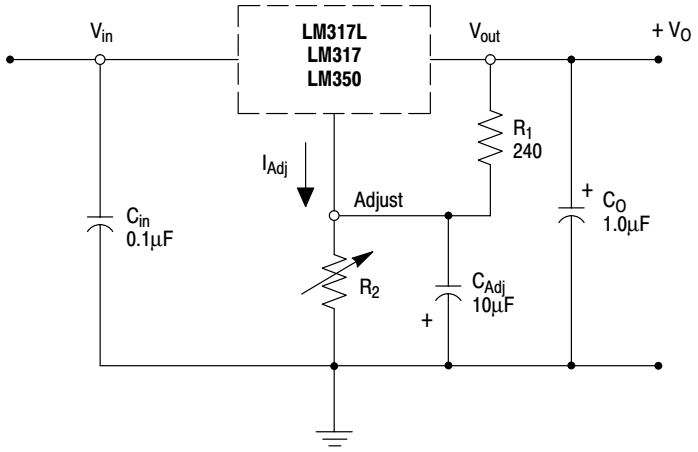
MC1723C

The basic circuit configurations for the MC1723C regulator are shown in Figures 3–2A and 3–3A. For output voltages from $\simeq$ 7.0 V to 37 V the configuration of Figure 3–2A can be used, while Figure 3–3A can be used to obtain output voltages from 2.0 V to $\simeq$ 7.0 V.

2. Output Current Boosting

If output currents greater than those available from the basic circuit configurations are desired, the current boost circuits shown in this section can be used. The output currents which can be obtained with this configurations are limited only by capabilities of the external pass element(s).

Figure 3–1A. Basic Configuration for Positive, Adjustable Output Three–Terminal Regulators



C_{in}: required if regulator is located an appreciable distance from power supply filter.

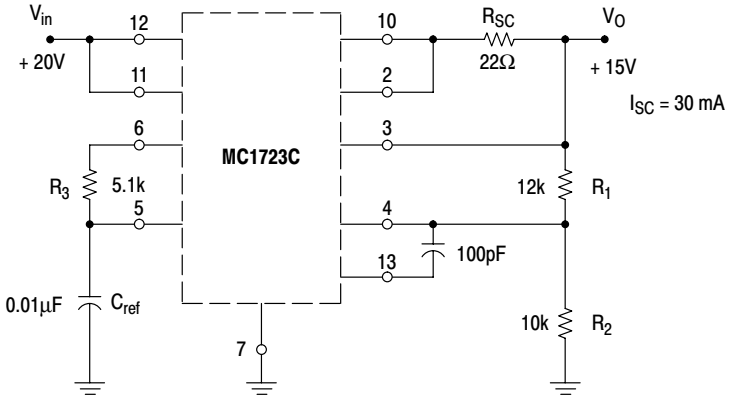
C_O: improves transient response.

C_{Adj}: improves Ripple Rejection.

$$V_{out} = 1.25\ V \left(1 + \left(\frac{R_2}{R_1}\right)\right) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

Figure 3–2A. MC1723C Basic Circuit Configuration for $V_{ref} \le V_O \le 37$ V



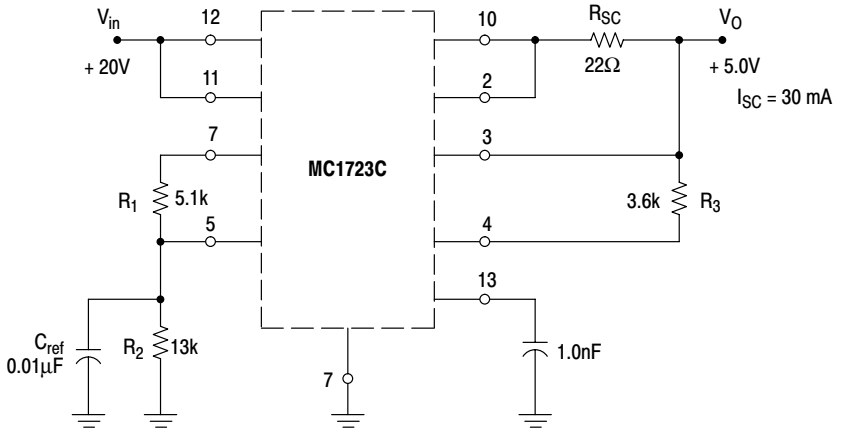
$$R_{SC} \cong \frac{0.66\ V}{I_{SC}} \ ; \ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

$$R_3 \cong R_1 \parallel R_2 \ ; \ 0 \le C_{ref} \le 0.1\ \mu F$$

$$R_2 = \frac{V_{ref}}{V_O}(R_1 + R_2) \approx \frac{7.0\ V}{V_O}(R_1 + R_2)$$

Values shown are for a 15 V, 30 mA regulator using an MC1723CP for a $T_{A(max)}$ = 25°C.

Figure 3–3A. MC1723C Basic Circuit Configuration for 2.0 V ≤ V_O ≤ V_{ref}



$$R_{SC} \simeq \frac{0.66V}{I_{SC}} \; ; \; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

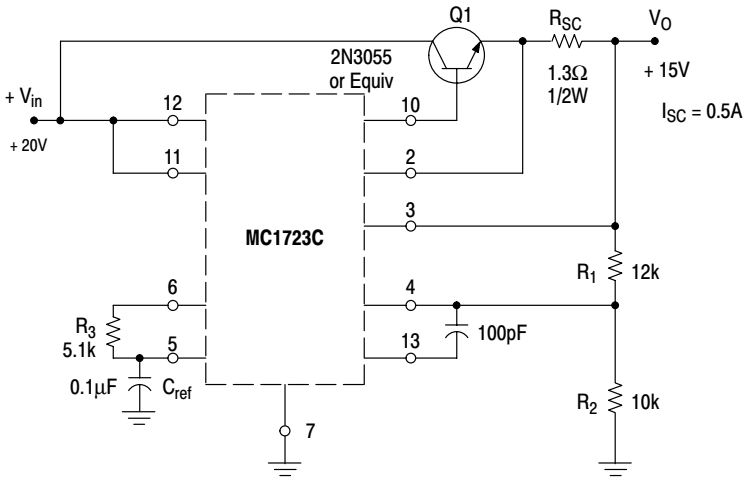
$$R_2 = \frac{V_O}{V_{ref}} (R_1 + R_2) \simeq \frac{V_O}{7.0\ V} (R_1 + R_2)$$

$$R_3 = R_1 \parallel R_2; \; 0 \le C_{ref} \le 0.1\ \mu F$$

Values shown are for a 5.0 V, 30 mA regulator using an MC1723CP for a $T_{A(max)}$ = 70°C.

To obtain greater output currents with the MC1723C the configurations shown in Figures 3–4A and 3–5A can be used. Figure 3–4A uses an NPN external pass element, while a PNP is used in Figure 3–5A.

Figure 3–4A. MC1723C NPN Boost Configuration



$$R_{SC} \cong \frac{0.66\ V}{I_{SC}} \; ; \; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

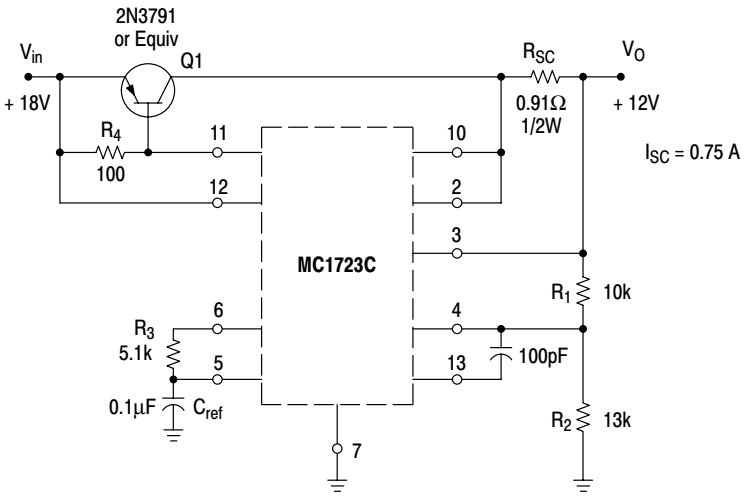
$$R_2 = \frac{V_{ref}}{V_O} (R_1 + R_2) \cong \frac{7.0\ V}{V_O} (R_1 + R_2)$$

$$0 \le C_{ref} \le 0.1\ \mu F \; ; \; R_3 \cong R_1 \parallel R_2$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 15 V, 500 mA regulator using an unheatsinked MC1723CP and a 2N3055 on a 6°C/W heatsink for T_A up to + 70°C.

Figure 3–5A. MC1723C PNP Boost Configuration



$$R_{SC} \cong \frac{0.66\ V}{I_{SC}} ; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega ; 0 \le C_{ref} \le 0.1\ \mu F$$

$$R_2 = \frac{V_{ref}}{V_O} (R_1 + R_2) \cong \frac{7.0\ V}{V_O} (R_1 + R_2)$$

$$R_3 = R_1 \parallel R_2$$

$$0 < R_4 \le V_{BE\ on\ (Q1)} / 5.0\ mA$$

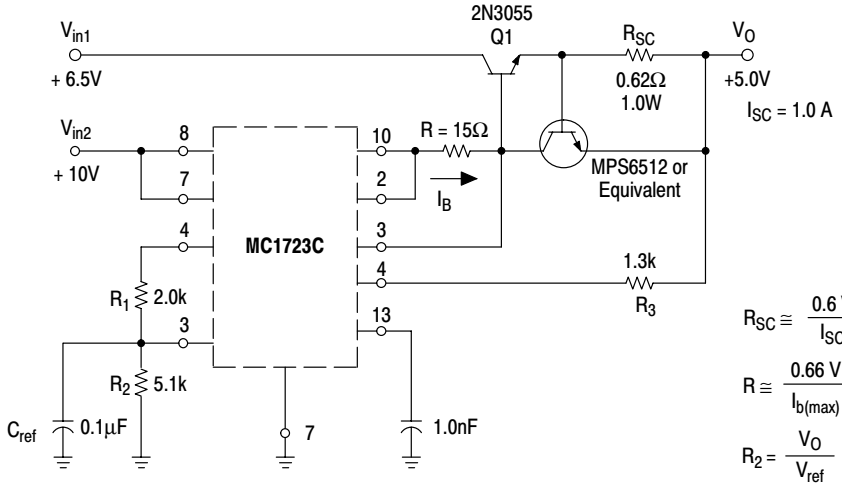
Selection of Q1 based on considerations of Section 4.

Values shown are for a 12 V, 750 mA regulator using an unheatsinked MC1723CP and a 2N3791 on a 4°C/W heatsink for T_A up to + 70°C.

3. High Efficiency Regulator Configurations

When large output currents at voltages under approximately 9.0 V are desired, the configuration of Figure 3–6A can be utilized to obtain increased operating efficiency. This is accomplished by providing a separate low voltage input supply for the pass element. This method, however, usually necessitates that separate short circuit protection be provided for the IC regulator and external pass element. Figure 3–6A shows a high efficiency regulator configuration for the MC1723C.

Figure 3–6A. MC1723C High Efficiency Regulator Configuration



$$R_{SC} \cong \frac{0.6\ V}{I_{SC}}$$

$$R \cong \frac{0.66\ V}{I_{b(max)}} ; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

$$R_2 = \frac{V_O}{V_{ref}} (R_1 + R_2) \cong \frac{V_O}{7.0\ V} (R_1 + R_2)$$

$$0 \le C_{ref} \le 0.1\ \mu F$$

$$R_3 \cong R_1 \parallel R_2$$

See Section 3F for general design considerations.
Selection of Q1 based on considerations of Section 4.

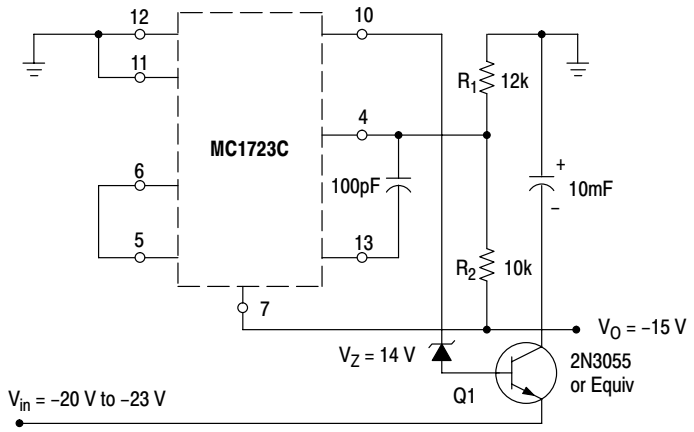
Values shown for a 5.0 V, 1.0 A regulator using an unheatsinked MC1723CP and a 2N3055 on a 10°C/W heatsink for T_A up to + 70°C.

B. Negative, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations (MC1723C)

Although a positive regulator, the MC1723C can be used in a negative regulator circuit configuration. This is done by using an external pass element and a zener level shifter as shown in Figure 3–1B. It should be noted that for proper operation, the input supply must not vary over a wide range, since the correct value for V_Z depends directly on this voltage. In addition, it should be noted that this circuit will not operate with a shorted output.

Figure 3–1B. MC1723C Negative Regulator Configuration



$$|V_O| \geq 10\ V;\ 10\ k\Omega \leq R_1 + R_2 \leq 100\ k\Omega$$

$$R_2 = \frac{V_{ref}}{|V_O|}\ (R_1 + R_2) \cong \frac{7.0\ V}{|V_O|}\ (R_1 + R_2)$$

$$V_Z \leq |V_{in}| - V_{BE(Q1)} - 3.0\ V;\ V_Z \geq |V_{in}| - |V_O| - V_{BE(Q1)} + 6.0\ V$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a −15 V, 750 mA regulator using the MC1723CP with Q1 mounted on a 20°C/W heatsink at T_A up to +70°C. **Do not short circuit output.**

C. Positive, Fixed Output IC Regulator Configurations

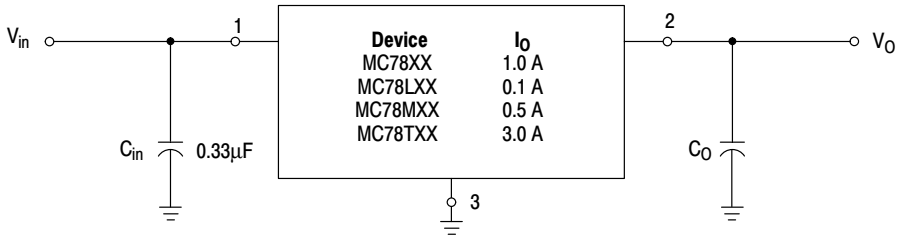
1. Basic Regulator Configuration

The basic current configuration for the positive three–terminal regulators is shown in Figure 3–1C. Depending on which regulator type is used, this configuration can provide output currents in excess of 3.0 A.

2. Output Current Boosting

Figure 3–2C illustrates a method for obtaining greater output currents with the three–terminal positive regulators. Although any of these regulators may be used, usually it is most economical to use the 1.0 A MC7800C in this configuration.

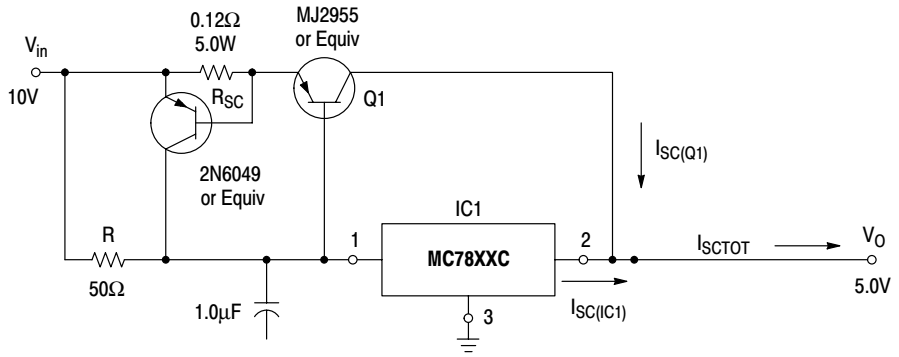
Figure 3–1C. Basic Circuit Configuration for Positive, Fixed Output, Three–Terminal Regulators



C_{in}: required if regulator is located more than a few (≈2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 μF may be needed for C_{in}. (C_{in} should be a high frequency type capacitor.)
C_O: improves transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Figure 3–2C. Current Boost Configuration for Positive Three–Terminal Regulators



XX: two digits of type number indicating nominal output voltage.
R: used to divert IC regulator bias current and determines at what output current level Q1 begins conducting.

$$0 < R \leq \frac{V_{BE\ \ on(Q1)}}{I_{Bias\ (IC1)}} \ ; \ R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}} \ ; \ I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 5.0 V, 5.0 A regulator using an MC7805CT on a 2.5°C/W heatsink and Q1 on a 1°C/W heatsink for T_A up to 70°C.

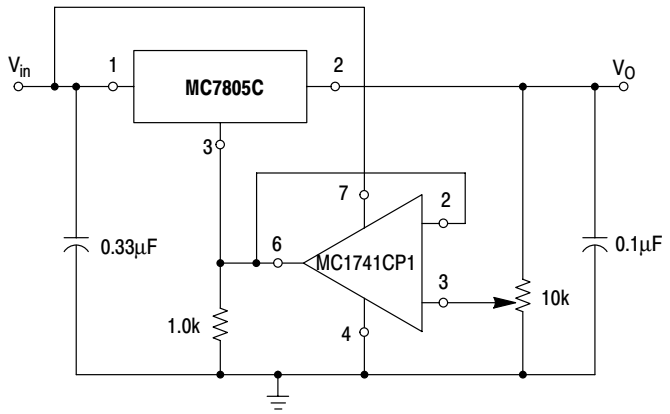
3. Obtaining an Adjustable Output Voltage

With the addition of an op amp, an adjustable output voltage supply can be obtained with the MC7805C. Regulation characteristics of the three–terminal regulators are retained in this configuration, shown in Figure 3–3C. If lower output currents are required, then an MC78M05C (0.5 A) could be used in place of the MC7805C.

4. Current Regulator

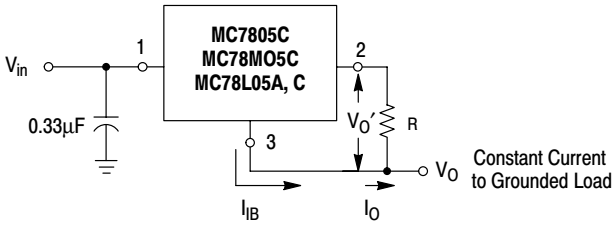
In addition to providing voltage regulation, the three–terminal positive regulators can also be used as current regulators to provide a constant current source. Figure 3–4C shows this configuration. The output current can be adjusted to any value from ≈ 8.0 mA (I_Q, the regulator bias current) up to the available output current of the regulator. Five–volt regulators should be used to obtain the greatest output voltage compliance range for a given input voltage.

Figure 3–3C. Adjustable Output Voltage Configuration Using a Three–Terminal Positive Regulator



V_O = 7.0 V to 33 V
$V_{in} - V_O \geq 2.0$ V
$V_{in} \geq 35$ V

Figure 3–4C. Current Regulator Configuration



$$I_O = \frac{V_O'}{R} + I_{IB}$$

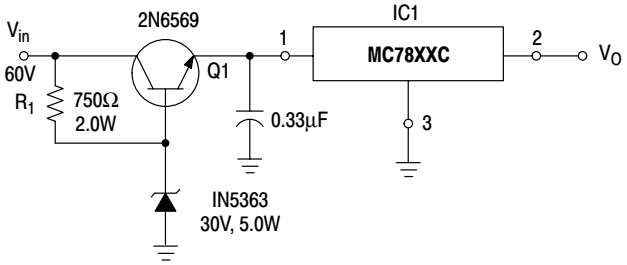
$$\text{Current Reg } \Delta I_O = \frac{\Delta V_O'}{R} + \Delta I_{IB}$$

$V_O + V_O' + 2.0\text{ V} \leq V_{in} \leq 35\text{ V}$

5. High Input Voltage

Occasionally, it may be necessary to power a three–terminal regulator from a supply voltage greater than $V_{in(max)}$, 35 V or 40 V. In these cases a preregulator circuit, as shown in Figure 3–5C, may be used.

Figure 3–5C. Preregulator for Input Voltages Above $V_{in(max)}$



$$R_1 = \left(\frac{V_{in} - 30}{1.5}\right) \bullet h_{fe(Q1)}$$

$V_{CEO(Q1)} \leq V_{in}$

XX: two digits of type number indicating nominal output voltage.

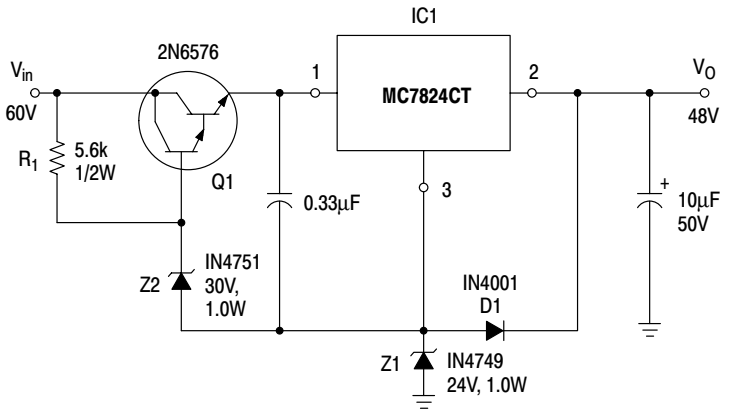
Values shown for V_{in} = 60 V

Q1 should be mounted on a 2°C/W heatsink for operation at T_A up to +70°C. IC1 should be appropriately heatsinked for the package type used.

6. High Output Voltage

If output voltages above 24 V are desired, the circuit configuration of Figure 3–6C may be used. Zener diode (Z1) sets the output voltage, while Q1, Z2, and D1 assure that the MC7824C does not have more than 30 V across it during short circuit conditions.

Figure 3–6C. High Output Voltage Configuration for Three–Terminal Positive Regulators



$$V_O = V_{Z1} + 24; R_1 = \left(\frac{V_{in} - (V_{Z1} + V_{Z2})}{1.5} \right) \bullet h_{fe(Q2)}$$

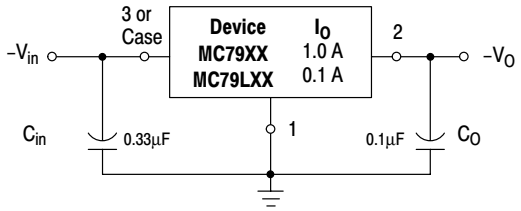
Values shown are for a 48 V, 1.0 A regulator
Q1 mounted on a 10°C/W heatsink
and IC1 mounted on a 2°C/W heatsink for T_A up to +70°C.

D. Negative, Fixed Output IC Regulator Configurations

1. Basic Regulator Configurations

Figure 3–1D gives the basic circuit configuration for the MC79XX and MC79LXX three–terminal negative regulators.

Figure 3–1D. Basic Circuit Configuration for Negative Three–Terminal Regulators



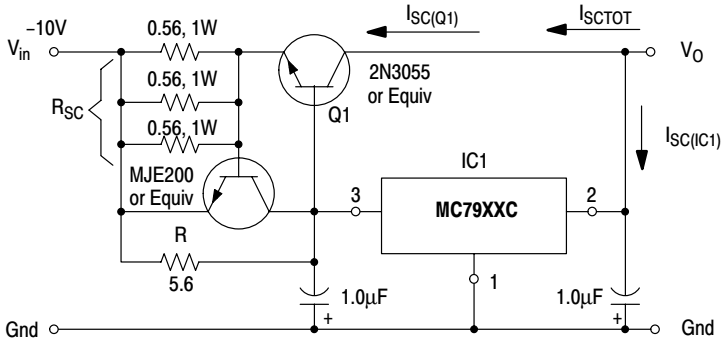
C_{in}: required if regulator is located more than a few (≈ 2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 μF may be required. C_{in} should be a high frequency type capacitor.
C_O: improves stability and transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Output Current Boosting

In order to obtain increased output current capability from the negative three–terminal regulators, the current boost configuration of Figure 3–2D may be used. Currents which can be obtained with this configuration are limited only by the capabilities of the external pass transistor(s).

Figure 3–2D. Output Current Boost Configuration for Three–Terminal Negative Regulators



XX: two digits of type number indicating output voltage. See Section 2 for available voltages.
R: used to divert regulator bias current and determine at what output current level Q1 begins conducting.

$$O < R \leq \frac{V_{BE\ on(Q1)}}{I_{Bias(IC1)}}$$

$$I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

$$R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}}$$

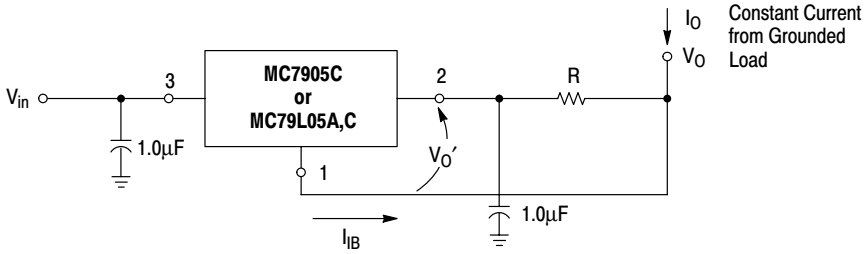
Selection of Q1 based on considerations of Section 4.

Values shown are for a −5.0 V, +4.0 A regulator; using an MC7905CT on a 1.5°C/W heatsink with Q1 mounted on a 1°C/W heatsink for T_A up to +70°C.

2. Current Regulator

The three–terminal negative regulators may also be used to provide a constant current sink, as shown in Figure 3–3D. In order to obtain the greatest output voltage compliance range at a given input voltage, the MC7905C or MC79L05C should be used in this configuration.

Figure 3–3D. Current Regulator Configuration for the Three–Terminal Negative Regulators



$V_{in} \geq -35$ V for MC7905C
$V_{in} \geq -30$ V for MC79L05C
$V_{in} \leq V_O + V_O - 2.0$ V

$$I_O = \frac{V_{O'}}{R} + I_{IB}$$

$$\text{Current regulation: } \Delta I_O = \frac{\Delta V_{O'}}{R} + \Delta I_{IB}$$

F. General Design Considerations

In addition to the design equations given in the regulator circuit configuration panels of Sections 3A–E, there are a few general design considerations which apply to all regulator circuits. These considerations are given below.

1. Regulator Voltages

For any circuit configuration, the worse–case voltages present on each pin of the IC regulator must be within the maximum and/or minimum limits specified on the device data sheets. These limits are instantaneous values, not averages.

They include:
a. $V_{in(min)}$
b. $V_{in(max)}$
c. $(V_{in} - V_{out})$ min
d. $V_{out(min)}$
e. $V_{out(max)}$

For example, the voltage between Pins 12 and 7 (V_{in}) of an MC1723CP must never fall below 9.5 V, even instantaneously, or the regulator will not function properly, (see Figure 3–1B).

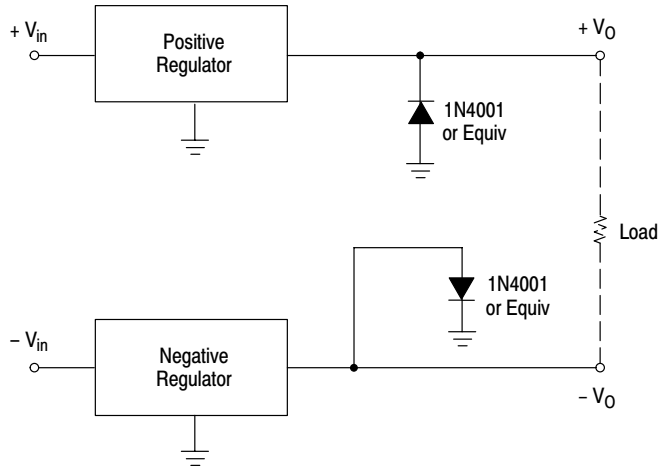
2. Regulator Power Dissipation, Junction Temperature and Safe Operating Area

The junction temperature, power dissipation output current or safe operating area limits of the IC regulator *must never be exceeded*.

3. Operation with a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load which is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g. op amps, level shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3–1F. This protects the regulator, during startup and short circuit operation, from output polarity reversals.

Figure 3–1F. Output Polarity Reversal Protection



4. Reverse Bias Protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is “crowbarred” during an output overvoltage condition. If the output voltage is greater ≈ 7.0 V, the emitter–base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 3–2F.

Figure 3–3F shows a three–terminal positive–adjustable regulator with the recommended protection diodes for output voltages in excess of 25 V, or high output capacitance values (C_O > 25 μF, C_{Adj} >10 μF). Diode D1 prevents C_O from discharging through the regulator during an input short circuit. Diode D2 protects against capacitor C_{Adj} from discharging through the regulator during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the regulator during an input short circuit.

Figure 3–2F. Reverse Bias Protection

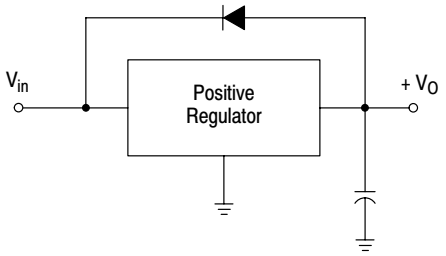
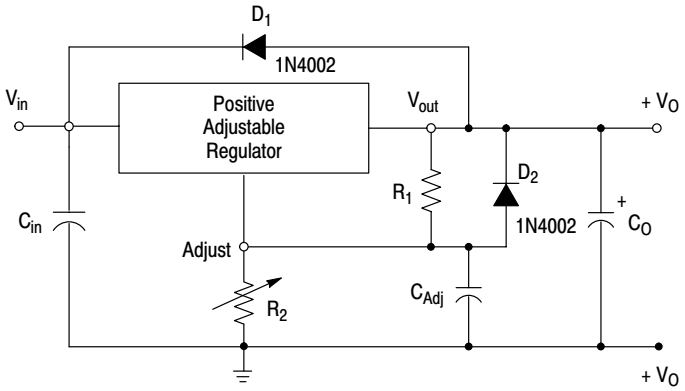


Figure 3–3F. Reverse Bias Protection for Three–Terminal Adjustable Regulators



SECTION 4

SERIES PASS ELEMENT CONSIDERATIONS FOR LINEAR REGULATORS

Presently, most monolithic IC voltage regulators that are available have output current capabilities from 100 mA to 3.0 A. If greater current capability is required, or if the IC regulator does not possess sufficient safe–operating–area (SOA), the addition of an external series pass element is necessary.

In this section, configurations, specifications and current limit techniques for external series pass elements will be considered. For illustrative purposes, pass elements for only positive regulator types will be discussed. However, the same considerations apply for pass elements used with negative regulators.

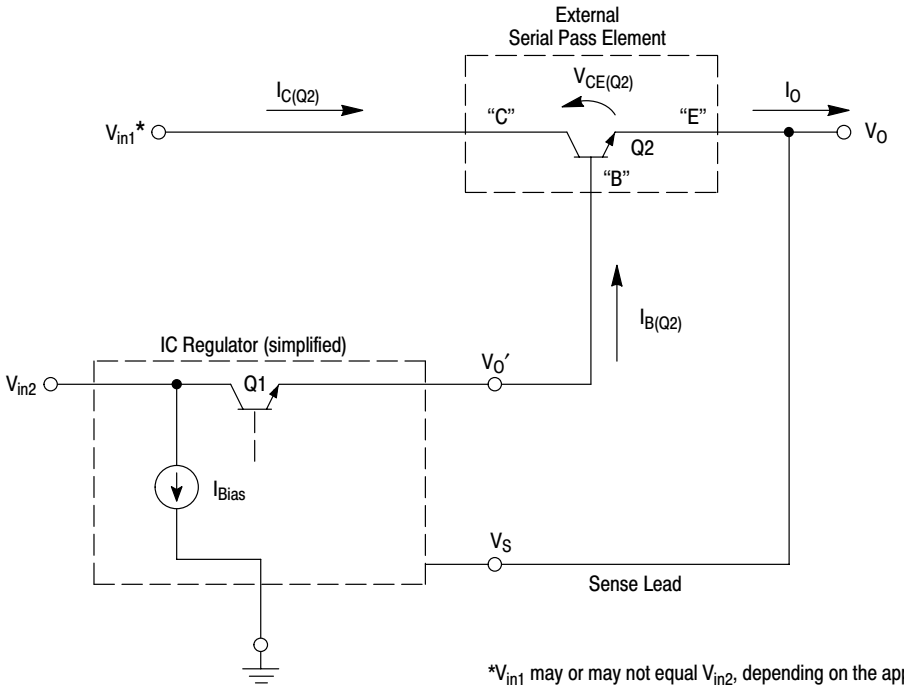
A. Series Pass Element Configurations

Using an NPN Type Transistor

If the IC regulator has an external sense lead, an NPN type series pass element may be used, as shown in Figure 4–1 A. This pass element could be a single transistor or multiple transistors arranged in Darlington and/or paralleled configurations.

In this configuration, the IC regulator supplies the base current (I_B) to the pass element (Q2) which acts as a current amplifier and provides the increased output current (I_O) capability.

Figure 4–1A. NPN Type Series Pass Element Configuration

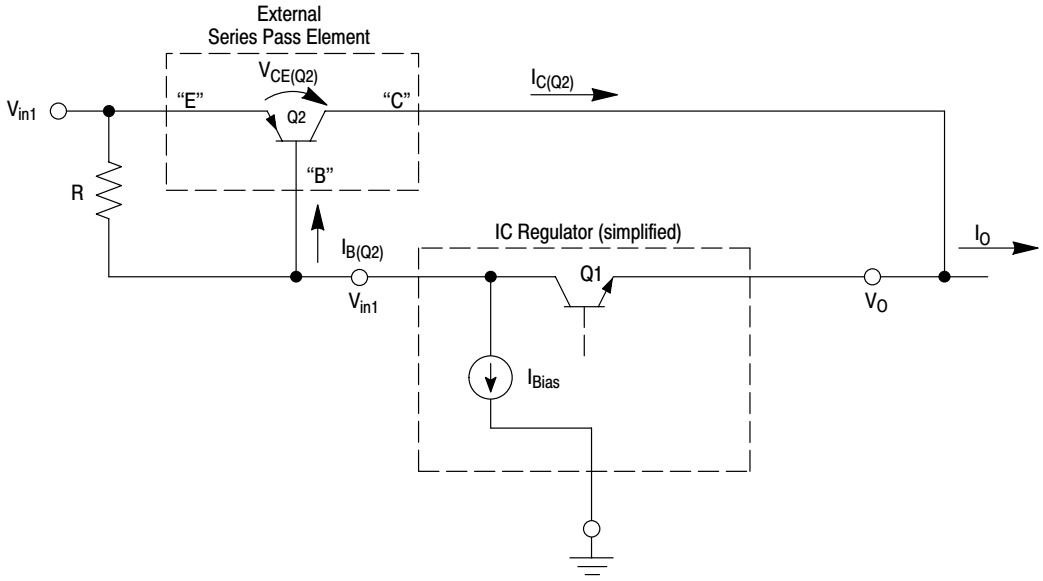


*V_{in1} may or may not equal V_{in2}, depending on the application.

Using a PNP Type Transistor

If the IC regulator does not have an external sense lead, as in the case of the three–terminal fixed output regulators, the configuration of Figure 4–1B can be used. (Regulators which possess an external sense lead may also be used with this configuration.) As before, the PNP type pass element can be a single transistor or multiple transistors.

Figure 4–1B. PNP Type Series Pass Element Configuration



This configuration functions in a similar manner to that of Figure 4–1A, in that the regulator supplies base current to pass element. The resistor (R) serves to route the IC regulator bias current (I_{Bias}) away from the base of Q2. If not included, regulation would be lost at low output currents. The value of R is low enough to prevent Q2 from turning on when I_{Bias} flows through this resistor, and is given by:

$$0 < R \leq \frac{V_{BEon}(Q2)}{I_{Bias}} \tag{4.0}$$

B. Series Pass Element Specifications

Independent of which configuration is utilized, the transistor or transistors that compose the pass element must have adequate ratings for $I_{C(max)}$, V_{CEO}, h_{fe}, power dissipation, and safe operating area.

1. $I_{C(max)}$ — for the pass element of Figure 4–1A, $I_{C(max)}$ is given by:

$$I_{C(max)(Q2)} \geq I_{O(max)} - I_{B(max)(Q2)} = I_{O(max)} - \frac{I_{C(max)(Q2)}}{h_{fe(Q2)}} \tag{4.1}$$

$$\geq I_{O(max)} \tag{4.2}$$

For the configuration of Figure 4–1B:

$$I_{C(max)(Q2)} \geq I_{O(max)} + I_{B(max)(Q2)} \tag{4.3}$$

$$\geq I_{O(max)} \tag{4.4}$$

2. V_{CEO} — since $V_{CE(Q2)}$ is equal to $V_{in1(max)}$ when the output is shorted or during start up:

$$V_{CEO(Q2)} \leq V_{in1(max)} \quad (4.5)$$

3. h_{fe} — the minimum DC current gain for Q2 in Figures 4–1A and 4–1B is given by:

$$h_{fe(min)(Q2)} \geq \frac{I_{C(max)(Q2)}}{I_{B(max)(Q2)}} @ V_{CE} = (V_{in1(min)} - V_O) \quad (4.6)$$

4. Maximum Power Dissipation $P_{D(max)}$, and Safe Operating Area (SOA)

For any transistor there are certain combinations of I_C and V_{CE} at which it may safely be operated. When plotted on a graph, whose axes are V_{CE} and I_C, a safe–operating region is formed.

As an example, the safe–operating–area (SOA) curve for the well known 2N3055 NPN silicon power transistor is shown in Figure 4–2. The boundaries of the SOA curve are formed by $I_{C(max)}$, power dissipation, second breakdown and V_{CEO} ratings of the transistor. Notice that the power dissipation and second breakdown ratings are given for a case temperature of +25°C and must be derated at higher case temperatures. (Derating factors may be found in the transistors' data sheets.) These boundaries must never be exceeded during operation, or destruction of the transistor(s) which constitute the pass element may result. (In addition, the maximum operating junction temperature *must not be exceeded*, see Section 15.)

C. Current Limiting Techniques

In order to select a transistor or transistors with adequate SOA, the locus of pass element I_C and V_{CE} operating points must be known. This locus of points is determined by the input voltage (V_{in1}, output voltage (V_O), output current (I_O) and the type of output current limiting technique employed.

In most cases, V_{in1}, V_O, and the required output current are already known. All that is left to determine is how the chosen current limit scheme affects required pass element SOA.

Note, since the external pass element is merely an extension of the IC regulator, the following discussions apply equally well to IC regulators not using an external pass element.

1. Constant Current Limiting

This method is the simplest to implement and is extensively used, especially at the lower output current levels. The basic circuit configuration is shown in Figure 4–3A, and operates in the following manner.

As the output current increases, the voltage drop across R_{SC} increases, proportionately. When the output current has increased to the point that the voltage drop across R_{SC} is equal to the base–emitter ON voltage of Q3 (V_{BEon}(Q3)), Q3 conducts. This diverts base current (I_{Drive}) away from Q1, the IC regulator's internal series pass element. Base drive ($I_{B(Q2)}$) of Q2 is therefore reduced and its collector–emitter voltage increases, thereby reducing the output voltage below its regulated value, V_{out}. The resulting output voltage–current characteristic is shown in Figure 4–3B.

The value of I_{SC} is given by:

$$I_{SC} = \frac{V_{BEon(Q3)}}{R_{SC}} \quad (4.7)$$

Figure 4–2. 2N3055 Safe Operating Area (SOA)

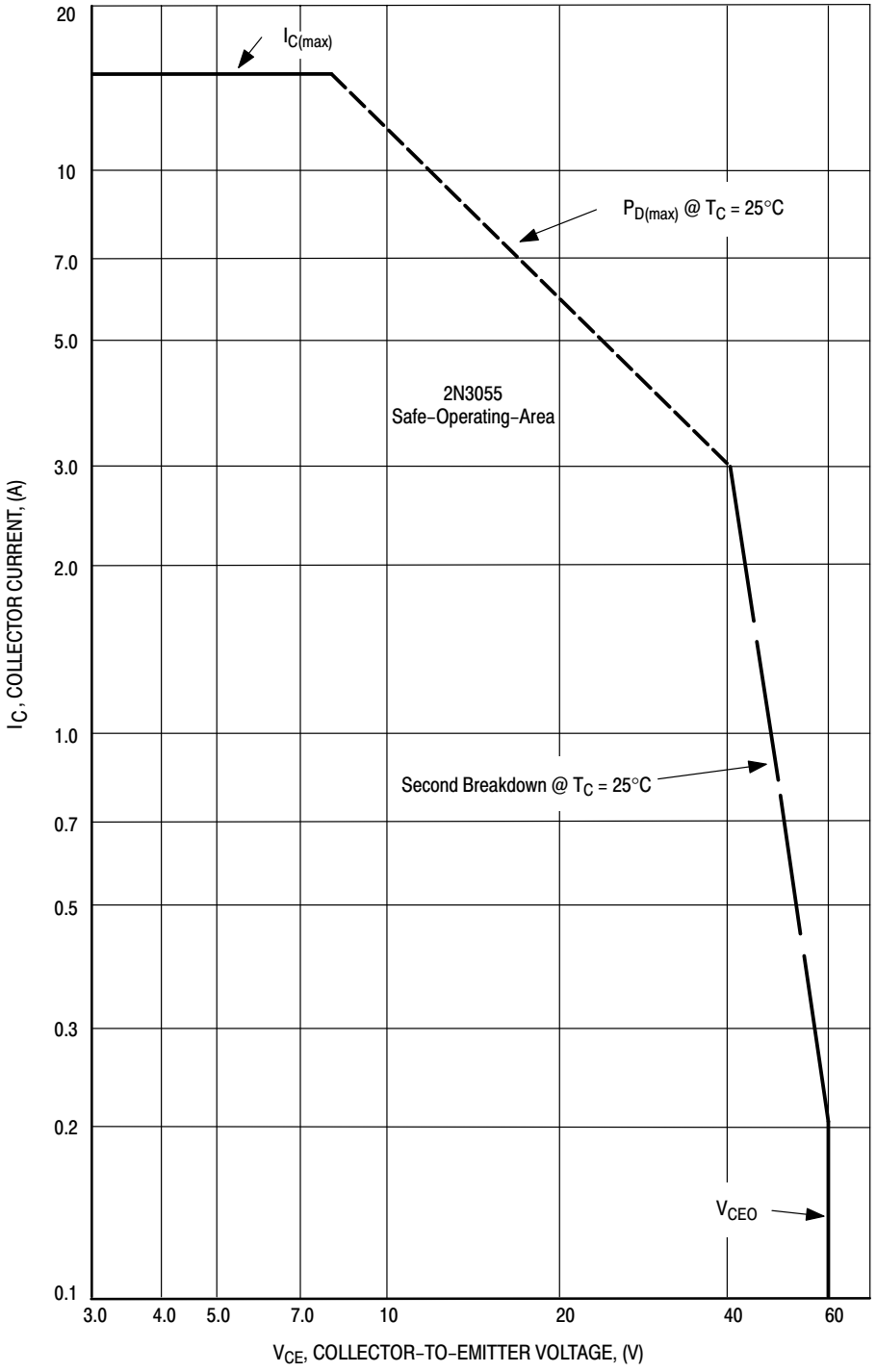
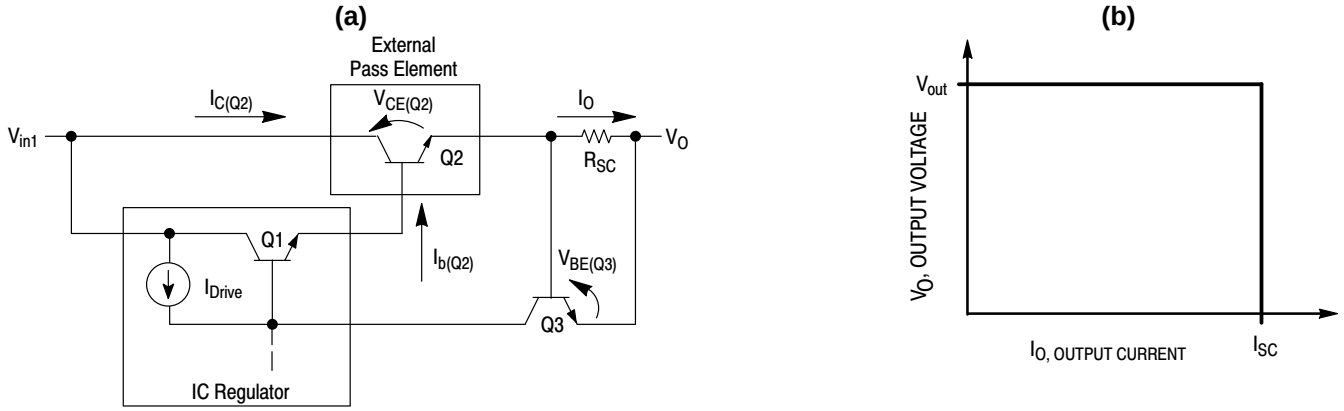


Figure 4–3. Constant Current Limiting



By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to $Isc/h_{fe(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.(1)

The required safe–operating–area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{in1} - V_O - I_O R_{SC} \simeq V_{in1} - V_O \quad (4.8)$$

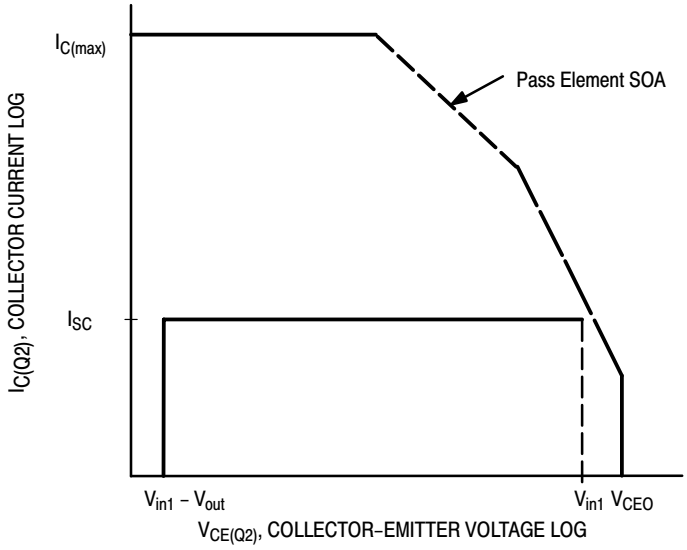
$$I_{C(Q2)} \simeq I_O \quad (4.9)$$

$$\text{where, } V_O = V_{out} \text{ for } 0 \le I_O \le I_{SC} \quad (4.10)$$

$$\text{and, } I_O = I_{SC} \text{ for } 0 \le V_O \le V_{out} \quad (4.11)$$

The resulting plot is shown in Figure 4–4. The transistor chosen for Q2 must have an SOA which encloses this plot, see Figure 4–4. Note that the greatest demand on the transistor's SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

Figure 4–4. Constant Current Limit SOA Requirements
(See Section 3 for Circuit Techniques)



(1) The three–terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive.

2. Foldback Current Limiting

A disadvantage of the constant current limit technique is that in order to obtain sufficient SOA the pass element must have a much greater collector current capability than is actually needed. If the short circuit current could be reduced, while still allowing full output current to be obtained during normal regulator operation, more efficient utilization of the pass elements SOA capability would result. This can be done by using a “foldback” current limiting technique instead of constant current limiting.

The basic circuit configuration for this method is shown in Figure 4–5(A). The circuit operates in a manner similar to that of the constant current limiting circuit, in that output current control is obtained by diverting base drive away from Q1 with Q3.

At low output currents, V_A approximately equals V_O and V_{R2} is less than than V_O. Q3 is therefore non–conducting and the output voltage remains constant. As the output current increases, the voltage drop across R_{SC} increases until V_A and V_{R2} are great enough to bias Q3 on. The output current at which this occurs is I_K, the “knee” current.

Figure 4–5. Foldback Current Limiting

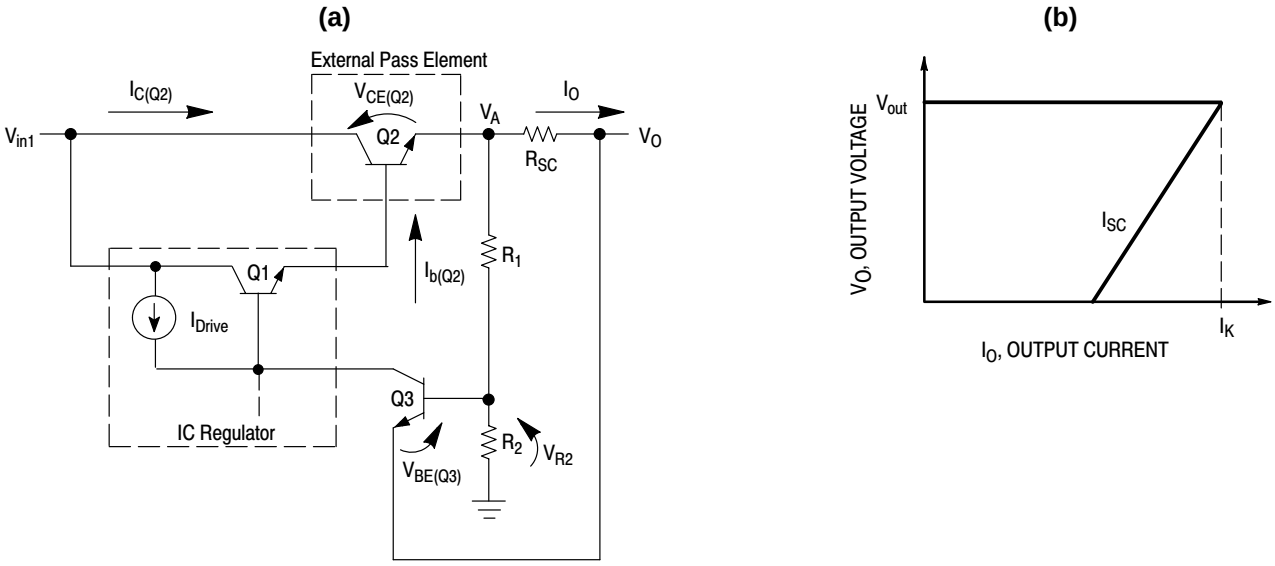
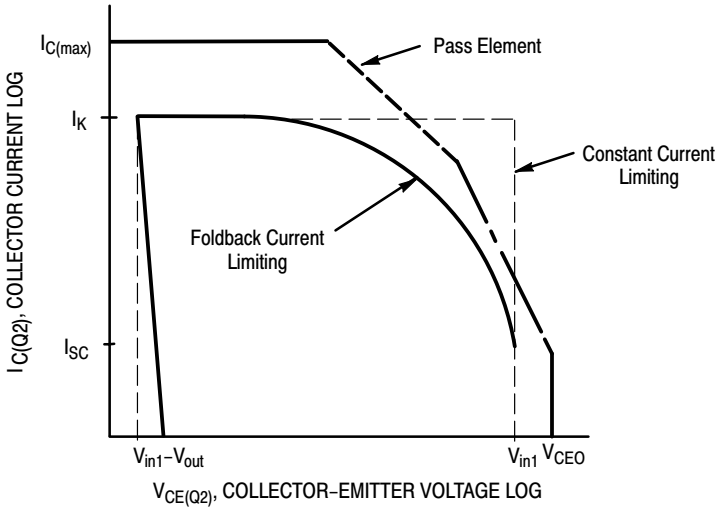


Figure 4–6. Foldback Current Limit SOA Requirements



The output voltage will now decrease. Less output current is now required to keep V_A and V_{R2} at a level sufficient to bias Q3 on since the voltage at its emitter has the tendency to decrease faster than that at its base. The output current will continue to "foldback" as the output voltage decreases, until an output short circuit current level (I_{SC}) is reached when the output voltage is zero. The resulting output current–voltage characteristic is shown in Figure 4–5B. The values for R_1, R_2, and R_{SC} (neglecting base current of Q3) are given by:

$$R_{SC} = \frac{V_{out}/I_{SC}}{\left(1 + \frac{V_{out}}{V_{BEon(Q3)}}\right) - \frac{I_K}{I_{SC}}} \tag{4.12}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_{BEon(Q3)}}{I_{SC}\, R_{SC}} \tag{4.13}$$

$$\text{and, } R_1 + R_2 \leq \frac{V_{out}}{I_{Drive}} \tag{4.14}$$

where: V_{out} = normal regulator output voltage

I_K = knee current

I_{SC} = short circuit current

I_{Drive} = base drive to regulator's internal pass element(s)

A plot of Q2 operating points, which result when using this technique, is shown in Figure 4–6. Note that the pass element is required to operate with a collector current of only I_{SC} during short circuit conditions, not the full output current, I_K. This results in a more efficient utilization of the SOA of Q2 allowing the use of a smaller transistor than if constant current limiting were used. Although foldback current limiting allows use of smaller pass element transistors for a given regulator output current than does constant current limiting, it does have a few disadvantages.

Referring to Equation (4.12), as the foldback ratio (I_K/I_{SC}) is increased, the required value of R_{SC} increases. This results in a greater input voltage at higher foldback ratios. In addition, it can be seen for Equation (4.12) that there exists an absolute limit to the foldback ratio equal to:

$$\left(\frac{I_K}{I_{SC(max)}}\right) = 1 + \frac{V_{out}}{V_{BEon(Q3)}} \text{ for } R_{SC} = \infty \tag{4.15}$$

For these reasons, foldback ratios greater than 2:1 or 3:1 are not usually practical for the lower output voltage regulators.

D. Paralleling Pass Element Transistors

Occasionally, it will not be possible to obtain a transistor with sufficient safe–operating–area. In these cases it is necessary to parallel two or more transistors. Even if a single transistor with sufficient capability is available, it is possible that paralleling two smaller transistors is more economical.

In order to insure that the collector currents of the paralleled transistors are approximately equal, the configuration of Figure 4–7 can be used. Emitter–ballasting resistors are used to force collector–current sharing between Q1 and Q2. The collector–current mismatch can be determined by considering the following, from Figure 4–7,

$$V_{BE1} + V_1 = V_{BE2} + V_2 \tag{4.16}$$

$$\text{and, } \Delta V_{BE} = \Delta V \tag{4.17}$$

where: $V_{BE} = V_{BE1} - V_{BE2}$ and, $\Delta V = V_2 - V_1$

Assuming $I_{E1} \simeq I_{C1}$ and $I_{E2} \simeq O_{C2}$, the collector–current mismatch is given by,

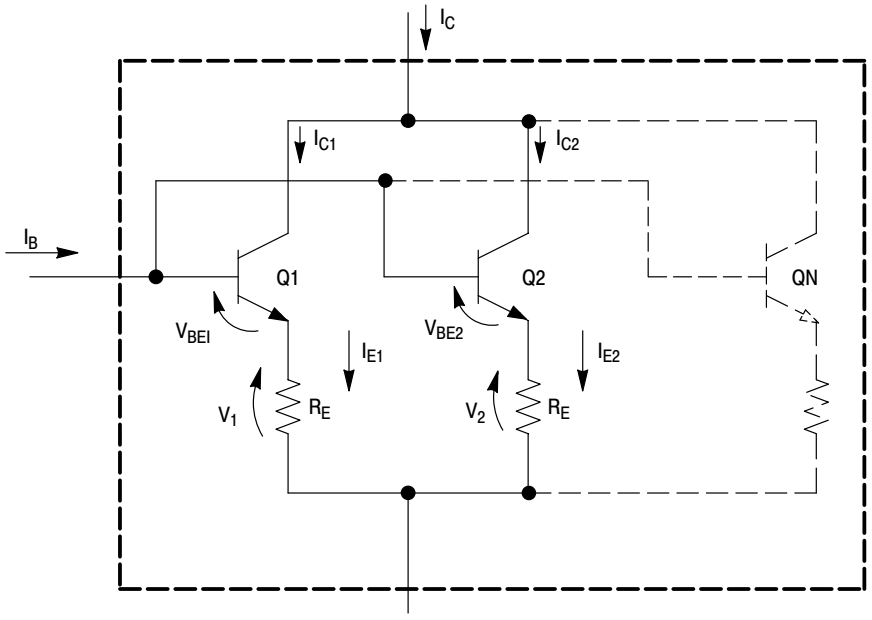
$$\frac{I_{C2} - I_{C1}}{I_{C2}} = \frac{\left(\frac{V_2}{R_E}\right) - \left(\frac{V_1}{R_E}\right)}{\left(\frac{V_2}{R_E}\right)} = \frac{V_2 - V_1}{V_2} = \frac{\Delta V}{V_2} = \frac{\Delta V_{BE}}{V_2} \tag{4.18}$$ (4.19)

$$\text{and, percent collector–current mismatch} = \frac{\Delta V_{BE}}{V_2} \times 100\% \tag{4.20}$$

From Equation (4.20), the collector–current mismatch is dependent on ΔV_{BE} and V_2. Since ΔV_{BE} is usually acceptable, V_2 should be 1.0 V to 0.5 V, respectively. R_E is therefore given by:

$$R_E = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_{C1}} = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_{C2}} = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_C/2} \tag{4.21}$$

Figure 4–7. Paralleling Pass Element Transistors



SECTION 5
LINEAR REGULATOR CONSTRUCTION AND LAYOUT

An important, and often neglected, aspect of the total regulator circuit design is the actual layout and component placement of the circuit. In order to obtain excellent transient response performance, high frequency transistors are used in modern integrated circuit voltage regulators. Proper attention to circuit layout is therefore necessary to prevent regulator instability or oscillations, or degraded performance.

In this section, guidelines will be given on proper regulator layout and placement of circuit components. In addition, topics such as remote voltage sensing, semiconductor mounting techniques, and thermal system evaluations will also be discussed.

1. General Layout and Component Placement Considerations

As mentioned previously, modern integrated circuit regulators are necessarily high bandwidth devices in order to obtain good transient response characteristics. To insure stable closed–loop operation, all these devices are frequency compensated, either internally or externally. This compensation can easily be upset by unwanted stray circuit capacitances and lead inductances, resulting in spurious oscillations. Therefore, it is important that the circuit lead lengths be short and the layout as tight as possible. Particular attention should be paid to locating the compensation and bypass capacitors as close to the IC as possible. Lead lengths associated with the external pass element(s), if used, should also be minimized.

Often overlooked is the stray inductance associated with the input leads to the regulator circuit. If the lead length from the input supply filter capacitor to the regulator input is more than a couple of inches, a 0.01 μF to 1.0 μF high frequency type capacitor (tantalum, ceramic, etc.) should be used to bypass the supply leads close to the regulator input pins.

2. Ground Loops and Remote Voltage Sensing

Ground Loops — Regulator performance can also suffer if ground loops in the circuit wiring are not avoided. The most common ground loop problem occurs when the return lead of the input supply filter capacitor is improperly located, as shown in Figure 5–1. If this return lead is physically connected between the load return and the regulator circuit ground point (“B”), a ripple voltage component (60 Hz or 120 Hz) can be induced on the load voltage (V_L). This is due to the high peaks of the filter capacitor ripple current (I_{ripple}) flowing through the lead resistance between the load and regulator. These peaks can be 5 to 15 times the value of load current. Since the regulator will only keep constant the voltage between its sense lead and ground point, points “A” and “B” in Figure 5–1, this additional ripple voltage (V_{lead}), will appear at the load.

This problem can be avoided by proper placement and connection of the filter capacitor return load as shown in Figure 5–2.

Remote Voltage Sensing — Closely related to the above ground loop problem is resistance in the current carrying leads to the load. This can cause poorer than expected load regulation in cases where the load currents are large or where the load is located some distance from the regulator. This is illustrated in Figure 5–3. As stated previously, the regulator circuit will keep the voltage present between its sense and ground pins constant. From Figure 5–3 we can see that any lead resistance between these points and the load will cause the load voltage (V_L) to vary with varying load current, I_L. This effectively lowers the load regulation of the circuit.

Figure 5–1. Filter Capacitor Ground Loop — WRONG!

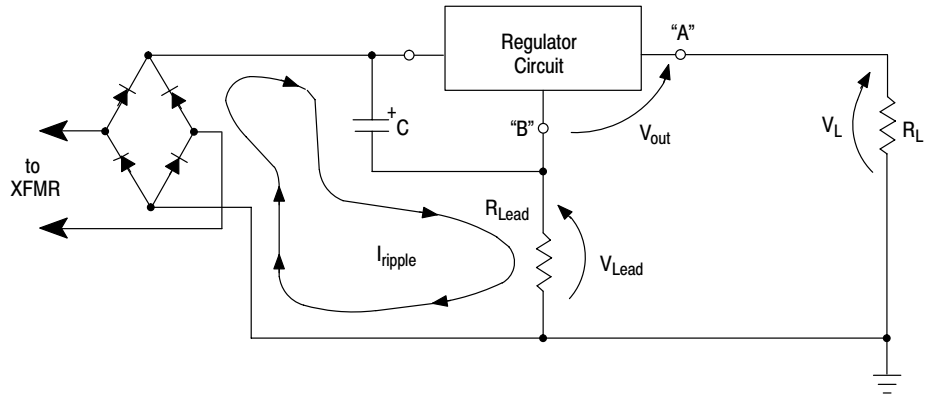
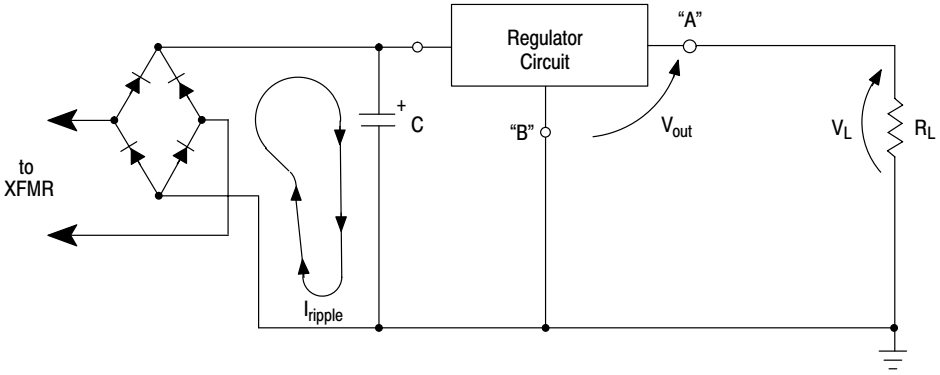


Figure 5–2. Filter Capacitor Ground Loop — RIGHT!



This problem can be avoided by the use of remote Sense leads, as shown in Figure 5–4. The voltage drops in the high current carrying leads now have no effect on the load voltage (V_L). However, since the Sense and Ground leads are usually rather long, care must be exercised that their associated lead inductance is minimized, or loop instability may result. The Ground and Sense leads should be formed into a twisted pair lead to minimize their lead inductance and noise pickup.

Figure 5–3. Effects of Resistance In Output Leads

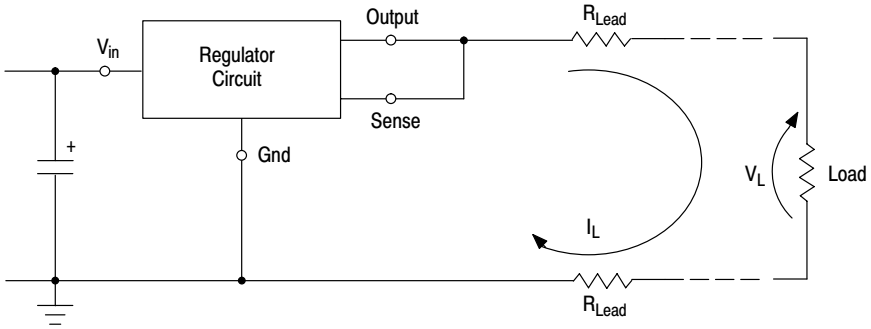
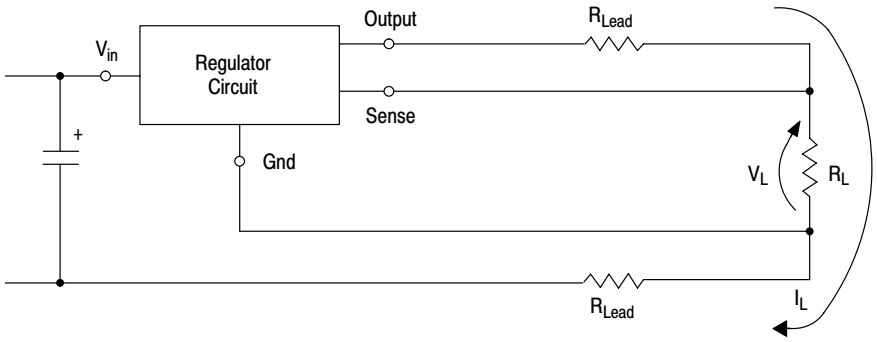


Figure 5–4. Remote Voltage Sensing



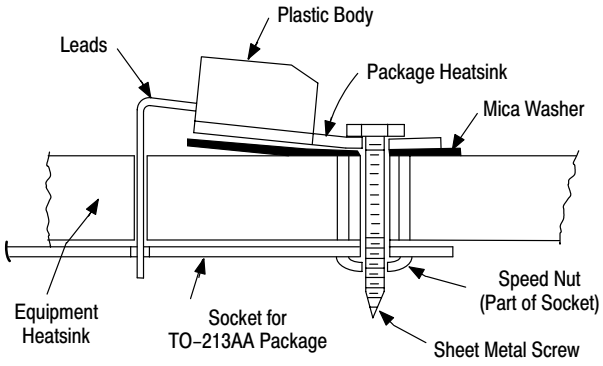
3. Mounting Considerations for Power Semiconductors

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160° to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 5–5 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package, the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

Figure 5–5. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)



(1) MIL–HANDBOOK — 2178, SECTION 2.2.
(2) *Navy Power Supply Reliability — Design and Manufacturing Guidelines* NAVMAT P4855–1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Flange Mount	Tab Mount
Plastic Body Mount	Surface Mount

Appendix A contains a brief review of thermal resistance concepts.

Appendix B discusses measurement difficulties with interface thermal resistance tests.

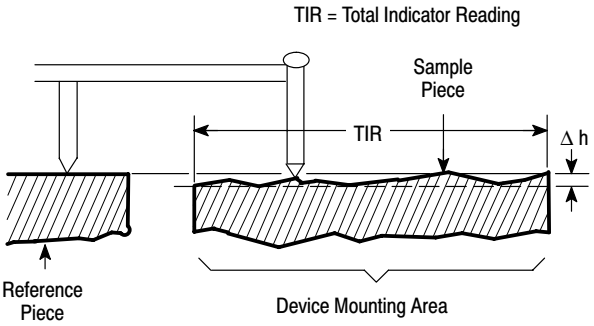
Mounting Surface Preparation

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 5–6. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness (i.e, Δh/TIR) if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Figure 5–6. Surface Flatness Measurement



Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 μin. to 60 μin. is satisfactory. A finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO–204 (TO–3) package with a typical 32 μin. finish, showed that heatsink finishes between 16 μin. and 64 μin. caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–204AA, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate–acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of the paint’s high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 V.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

(3) Catalog #87–HS–9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.

Interface Decisions

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise, the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pockmarked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section. To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct, a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 5–1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Table 5–1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed In ON Semiconductor Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In–Lb	Metal–to–Metal		With Insulator			See Note
			Dry	Lubed	Dry	Lubed	Type	
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 5–7 and 5–8 for additional data on TO–204AA and TO–220 packages.
2. Screw not insulated (see Figure 5–12).

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 5–7. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from AAVID is called KON–DUX. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Insulation Considerations

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non–isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the ON Semiconductor Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the
isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

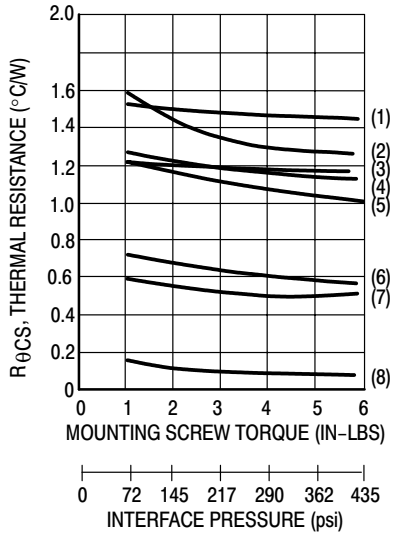
Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, is shown in Figure 5–7, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction–to–case).

Referring to Figure 5–7, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high break down voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

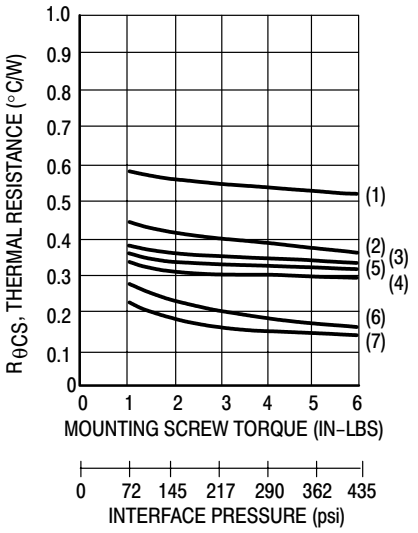
Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figures 5–7(c) and 5–7(d), it can be noted that Thermasil, a filled silicone rubber without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

Figure 5–7. Interface Thermal Resistance Using Different Insulating Materials as a Function of Mounting Screw Torque

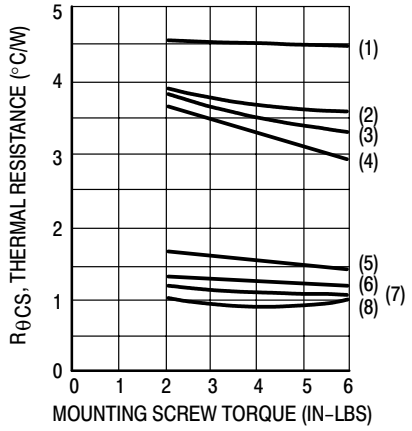


(a) TO–204AA (TO–3)
Without Thermal Grease

(1) **Thermalfilm,** .002 (.05) thick
(2) **Mica,** .003 (.08) thick
(3) **Mica,** .002 (.05) thick
(4) **Hard anodized,** .020 (.51) thick
(5) **Aluminum oxide,** .062 (1.57) thick
(6) **Berylium oxide,** .062 (1.57) thick
(7) **Bare joint —** no finish
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material

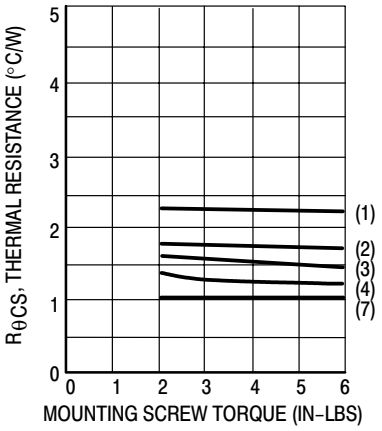


(b) TO–204AA (TO–3)
With Thermal Grease



(c) TO–220
Without Thermal Grease

(1) **Thermalfilm,** .022 (.05) thick
(2) **Mica,** .003 (.08) thick
(3) **Mica,** .002 (.05) thick
(4) **Hard anodized,** .020 (.51) thick
(5) **Thermalsil II,** .009 (.23) thick
(6) **Thermalsil II,** .006 (.15) thick
(7) **Bare joint —** no finish
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material



(d) TO–220
With Thermal Grease

Data Courtesy of Thermalloy

A number of manufacturers offer silicone rubber insulators. Table 5–2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber–Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R\theta_{CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

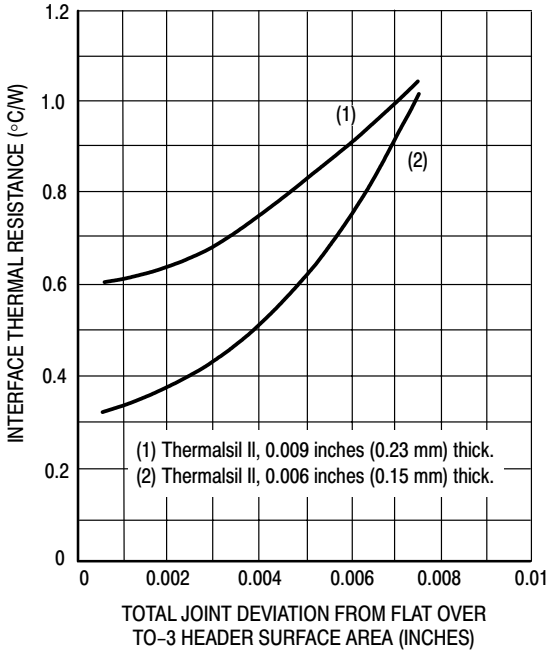
Table 5–2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173–7	0.790	1.175
Bergquist	Sil Pad K–4	0.752	1.470
Stockwell Rubber	1867	0.742	1.015
Bergquist	Sil Pad 400–9	0.735	1.205
Thermalloy	Thermalsil II	0.680	1.045
Shin–Etsu	TC–30AG	0.664	1.260
Bergquist	Sil Pad 400–7	0.633	1.060
Chomerics	1674	0.592	1.190
Wakefield	Delta Pad 174–9	0.574	0.755
Bergquist	Sil Pad 1000	0.529	0.935
Ablestik	Thermal Wafers	0.500	0.990
Thermalloy	Thermalsil III	0.440	1.035
Chomerics	1671	0.367	0.655

*Test Fixture Deviation from flat Thermalloy EIR86–1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown on Figure 5–8. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

Figure 5–8. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators



Data Courtesy of Thermalloy

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho–Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R\theta_{CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With non–conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 5–3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 5–3. Performance of Silicon Rubber Insulators Tested per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Bergquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho–Therm, 1617	0.233	—
Q Pad (non–insulated)	—	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
Cho–therm 1674	0.433	—
Thermasil II	0.500	—
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly, so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak (Case 221C) illustrated in Figure 5–13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

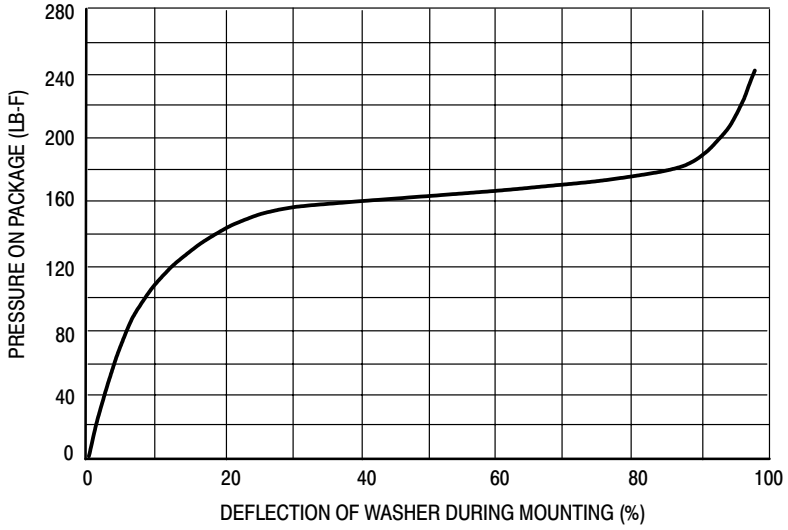
Fastener and Hardware Characteristics

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5–9, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.(4)

Figure 5–9. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors



(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board–mounted or free–standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or Sync Nut) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed nut. If a self–tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not recommended fasteners for any of the plastic packages. When a rugged metal flange–mount package is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field–serviceable systems or low strength types for field–serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

Fastening Techniques

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel or gold–plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

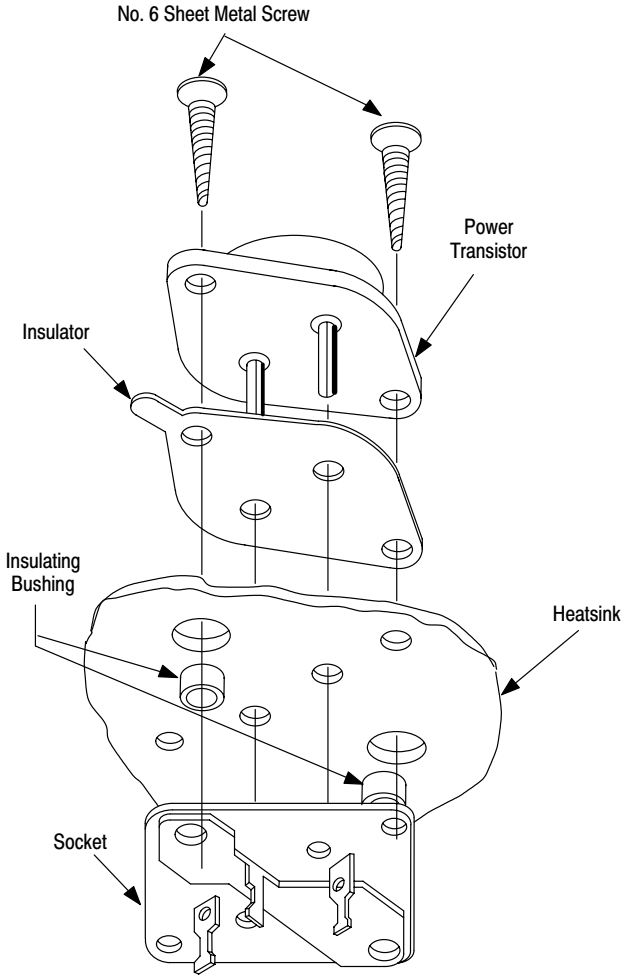
1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Flange Mount

Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting hose combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 5–10. Machine screws (preferred), self–tapping screws, islets or rivets may be used to secure the package using guidelines in the previous section, **Fastener and Hardware Characteristics**.

(5) Robert Batson, Elliot Fraunglass and James P. Moran, *Heat Dissipation Through Thermalloy Conductive Adhesives*, EMTAS ’83 Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

Figure 5–10. Hardware Used for a TO–204AA (TO–3) Flange Mount Part



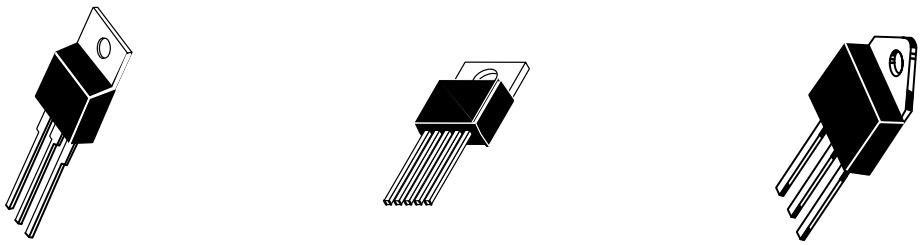
Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 5–11. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 5–12. The rectangular washer shown in Figure 5–12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch–pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, ON Semiconductor TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO–220 package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 5–14(c). To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

Figure 5–11. Several Types of Tab Mounted Parts

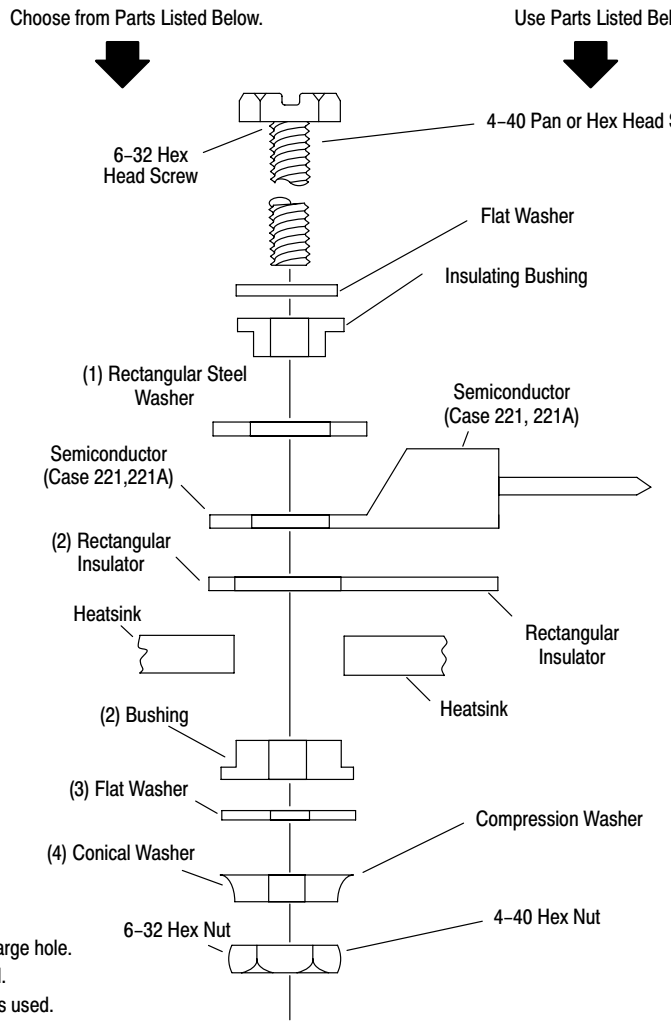


CASE 221A (TO–220AB) | **CASE 314D** | **CASE 340 (TO–218)**

Figure 5–12. Mounting Arrangements for Tab Mount TO–220

a) Preferred Arrangement for Isolated or Non–isolated Mounting. Screw is at Semiconductor Case Potential. 6–32 Hardware is Used.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4–40 Hardware is Used.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

Plastic Body Mount

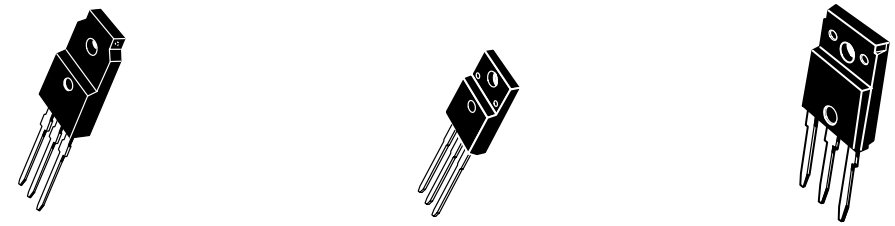
The Full Pak plastic power packages shown in Figure 5–13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance.

The Full Pak (Case 221C) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5–9.

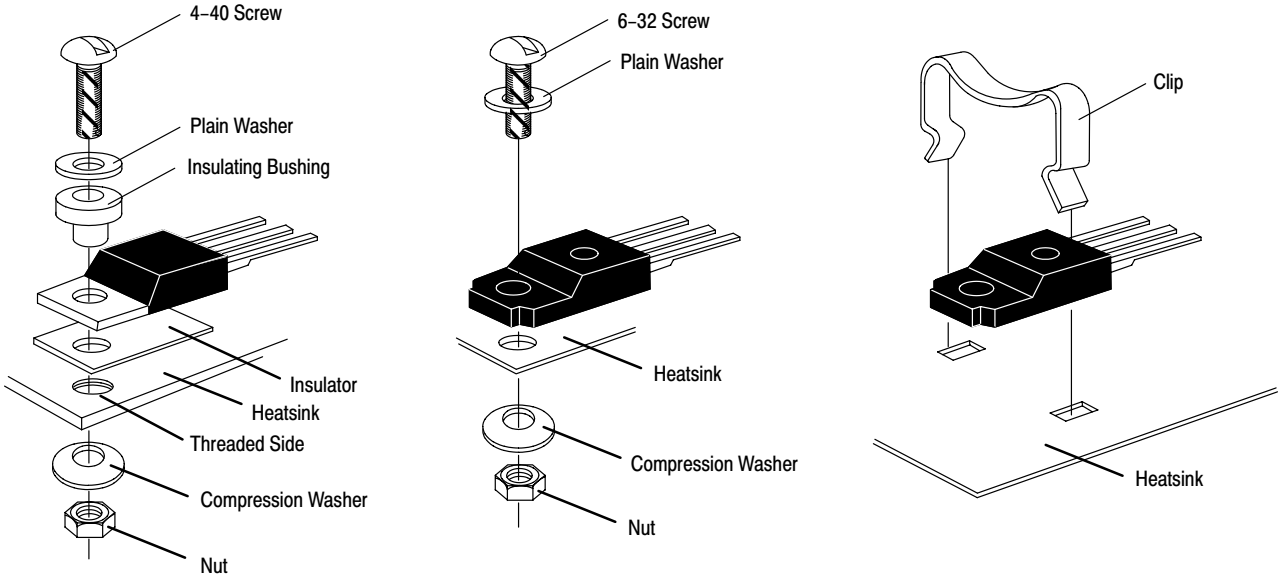
The Full Pak (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 5–14(c), one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 5–14(b) may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 5–14(a).

Figure 5–13. Plastic Body Mounted Packages



CASE 221C (Full Pak) | **CASE 221D (Full Pak)** | **CASE 340B (Full Pak)**

Figure 5–14. Mounting Arrangements for the Full Pak as Compared to a Conventional TO–220



(a) Screw Mounted TO–220 | **(b) Screw Mounted Full Pak** | **(c) Clip Mounted Full Pak**

Surface Mount

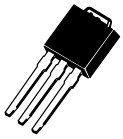
Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 5–15, for example, will accommodate a die up to 112 mils × 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard glass–epoxy 2 oz. boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 5–16 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

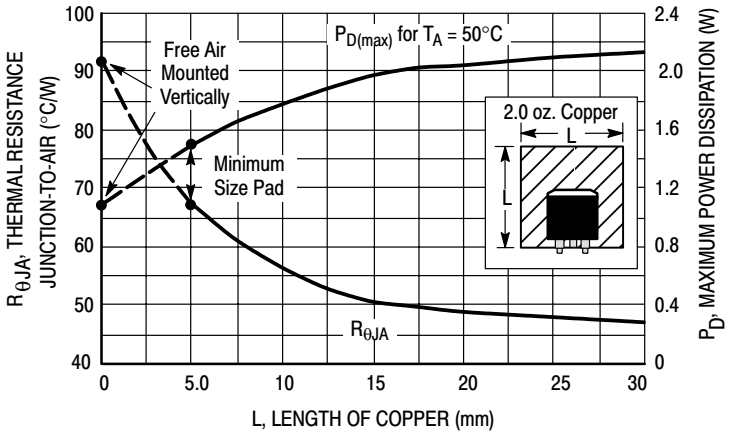
Figure 5–15. Surface Mounted DPAK Packages



CASE 369

CASE 369A

Figure 5–16. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board



(7) Herb Fick, *Thermal Management of Surface Mount Power Devices*, Powerconversion and Intelligent Motion, August 1987.

Free Air and Socket Mounting

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from ON Semiconductor. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

Connecting and Handling Terminals

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from ON Semiconductor on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Cleaning Circuit Boards

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

Thermal System Evaluation

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see ON Semiconductor Application Note, AN569.

Other applications, notably switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where, T_J = junction temperature (°C),
T_C = case temperature (°C),
$R_{\theta JC}$ = thermal resistance junction–to–case as specified on the data sheet (°C/W),
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

Appendix A
Thermal Resistance Concepts

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where, q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

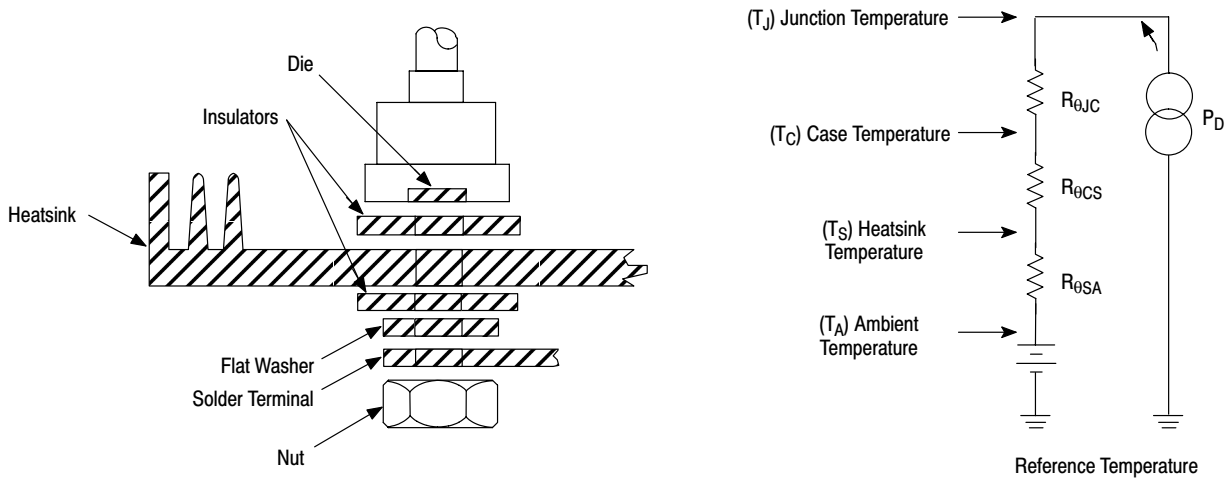
However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance (R_θ) is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation 2 and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A–1.

Figure A–1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor



The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where, T_J = junction temperature,
P_D = power dissipation,
$R_{\theta JC}$ = semiconductor thermal resistance (junction–to–case),
$R_{\theta CS}$ = interface thermal resistance (case–to–heatsink),
$R_{\theta SA}$ = heatsink thermal resistance (heatsink–to–ambient),
T_A = ambient temperature.

The thermal resistance junction–to–ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance ($R_{\theta CS}$) may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

Appendix B
Measurement of Interface Thermal Resistance

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring dc power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

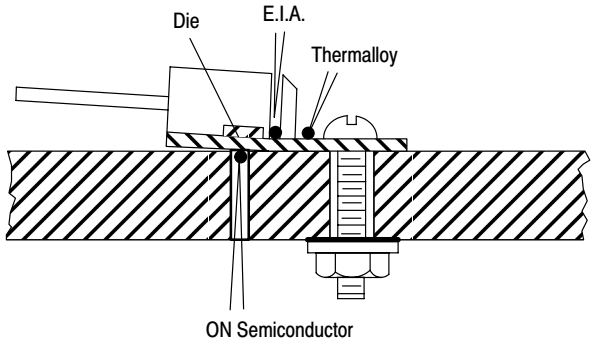
When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–204AA package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented".

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The ON Semiconductor fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15% to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in Figure B–1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, ON Semiconductor TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure.

B–1. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End



Three thermocouple locations are shown.

a) The ON Semiconductor location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b) The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c) The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in Figure B–1. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the ON Semiconductor location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the case temperature thermocouple readings become warmer. Thus the choice of reference point for the case temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The ON Semiconductor location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The ON Semiconductor location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1.0 mil/inch, has a finish better than 63 μin., and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application–oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

SECTION 6
LINEAR REGULATOR DESIGN EXAMPLE

As an illustration of the use of the material contained in the preceding sections, the following regulator design example is given.

Regulator Performance Requirements:

Output Voltage, V_O = +10 V ± 0.1 V
Output Current, I_O = 1.0 A, current limited
Load Regulation, ≤ 0.1% for I_O = 10 mA to 750 mA
Line Regulation, ≤ 0.1%
Output ripple, ≤ 2.0 mVpp
Max Ambient Temperature, $T_A \leq +70°C$
Supply will have common loads to a negative supply.

1. IC Regulator Selection

Study of the available regulators given in the selection guide reveals that the MC1723C would meet the regulation performance requirements. This regulator must be current boosted to obtain the required 1.0 A output current. A rough cost estimate shows that an MC1723C series pass element combination is the most economical approach.

2. Circuit Configuration

In Section 3, an appropriate circuit configuration is found. This is the MC1723C NPN boost configuration of Figure 3–4A.

3. Determination of Component Values

Using the equations given in Figure 3–4A, the values of C_{ref}, R_1, R_2, R_3 and R_{SC} are determined.

a) C_{ref} is chosen to be 0.1 μF for low noise operation.

b) $R_1 + R_2$ is chosen to be ≈ 10 k.

c) R_2 is then given by: $R_2 \approx \frac{7.0\ V}{V_O} (R_1 + R_2) = 0.7\ (10\ k) = 7.0\ k$

d) Since V_{ref} can vary by as much as ± 5% for the MC1723C, R_2 should be made variable by at least that much, so that V_O can be set to the required value of +10 V ± 0.1 V. R_2 is therefore chosen to consist of a 62 k resistor and a 2.0 k trimpot.

e) $R_1 = 10\ k - R_2 = 10\ k - 7.0\ k = 3.0\ k$

f) $R_{SC} \approx \frac{0.6\ V}{I_{SC}} = \frac{0.6\ V}{1.0\ A} = 0.6\ \Omega$; 0.56 Ω, 1.0 W chosen for R_{SC}.

g) $R_3 = R_1 \,||\, R_2 \cong 2.2\ k$

4. Determination of Input Voltage (V_{in})

There are two basic constraints on the input voltage: 1) the device limits for minimum and maximum V_{in} and, 2) the minimum input–output voltage differential. These limits are found on the device data sheet to be:

$$9.5\ V \le V_{in} \le 40\ V \text{ and } (V_{in} - V_O) \ge 3.0\ V$$

For the configuration of Figure 3–5A, $(V_{in} - V_O)$ is given by:

$$(V_{in} - V_O) = [V_{in} - (V_O + 2\phi)] \ge 3.0\ V, \text{ where } \phi = V_{BEon} \approx 0.6\ V$$

Note that $(V_{in} - V_O)$ is defined on the device data sheet to be the differential between the input and output pins. Since the base–emitter junction drops of Q1 and R_{SC} have been added to the circuit, they must be added to the minimum value of $(V_{in} - V_O)$. Therefore,

$$V_{in} \ge V_O + 2\phi + 3.0\ V = 10 + 1.2 + 3$$

$$V_{in} \ge 14.2\ V$$

This condition also satisfies the requirement for a minimum V_{in} of 9.5 V.

In order to simplify the design of the input supply (see Section 8), V_{in} is chosen to be 16 V average with a 3.0 Vpp ripple at full load and up to 25 V at no load. This assures that the input voltage is always above the required minimum value of 14.2 V. Now, the output ripple can be determined. The MC1723C has a typical ripple rejection ratio of –74 db, as given on its data sheet. With an input ripple of 3.0 Vpp, the output ripple would be less than 1.0 mVpp, which meets the regulator output ripple requirements.

5. Selection of the Series Pass Element (Q1)

The transistor type chosen for Q1 must have the following characteristics (see Section 4):

a) $V_{CEO} \ge V_{in(max)}$

b) $I_{C(max)} \ge I_{SC}$

c) $h_{fe} \ge \dfrac{I_{SC}}{I_O}$ @ $V_{CE} = V_{in} - V_O - \phi$, where $\phi = V_{BEon} \approx 0.6\ V$

d) $P_{D(max)} \ge V_{in}, \times I_{SC}$

e) θ_{JC} such to allow practical heatsinking

f) SOA such that it can withstand $V_{CE} = V_{in}$ @ $I_C = I_{SC}$

For this example:

$$V_{CEO} \ge 25\ V$$
$$I_{C(max)} \ge 1.0\ A$$
$$h_{fe} \ge 25 \text{ @ } V_{CE} = 5.0\ V \text{ @ } I_C = 1.0\ A$$
$$P_{D(max)} \ge 16\ W$$
$$\theta_{JC} = 1.52°C/W$$
$$SOA = 1.0\ A \text{ @ } 16\ V$$

A 2N3055 transistor is chosen as a suitable device for Q1 using the selection guide of Section 4 and the transistor data sheets (available from the device manufacturer).

6. Q1 Heatsink Calculation

$$T_J = T_A + P_D \theta_{JA} \quad \text{(Equation 15.1 from Section 15)}$$

where, $P_D = V_{in} \times I_{SC}$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ (Equation 6.2)

Solving for θ_{SA}:

$$\theta_{SA} = \left[\frac{T_J - T_A}{P_D} \right] - (\theta_{JC} + \theta_{CS}) \qquad (6.2)$$

From the 2N3055 data sheet, $T_J = 200°C$ and $\theta_{JC} = 1.52°C/W$. The transistor will be mounted with thermal grease directly to the heatsink. Therefore, θ_{CS} is found to be 0.1°C/W from Table 15–1.
Solving for Equation 6.2:

$$\theta_{SA} = \left[\frac{200°C - 70°C}{16\ V \times 1.0\ A} \right] - (1.52 + 0.1)\ °C/W$$

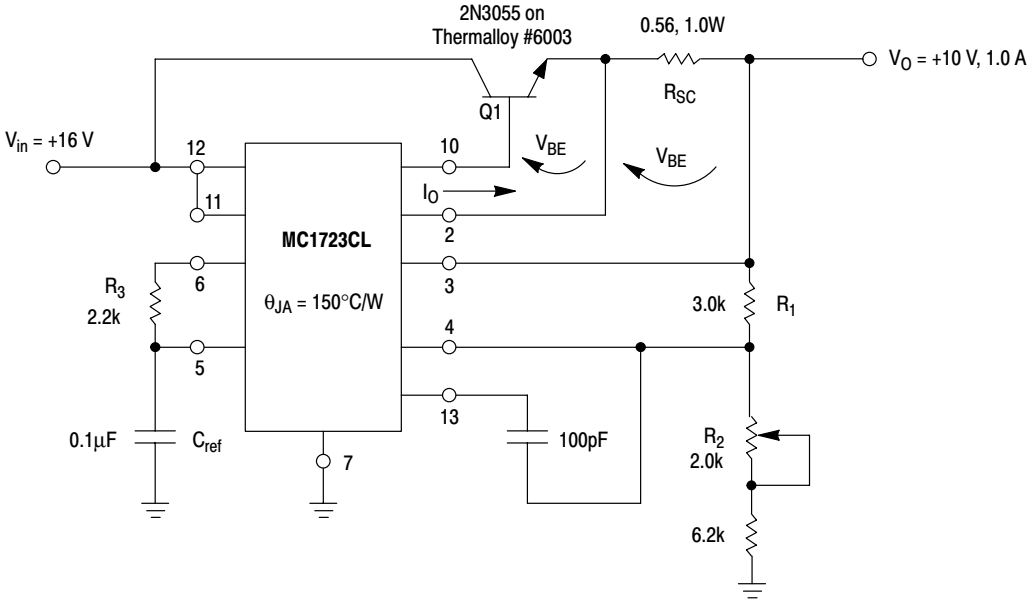
$$\leq 6.6°C/W$$

A commercial heatsink is now chosen from Table 15–2 or one custom designed using the methods given in Section 15. For this example, a Thermalloy #6003 heatsink, having a θ_{CS} of 6.2°C/W, was used.

7. Clamp Diode

Since the regulator can power a load which is also connected to a negative supply, a 1N4001 diode is connected to the output for protection. The complete circuit schematic is shown in Figure 6–1.

Figure 6–1. 10 V, 1.0 A Design Example



8. Construction Input Supply Design

The input supply is now designed using the information contained in Section 8 and the regulator circuit is constructed using the guidelines given in Section 5.

SECTION 7

LINEAR REGULATOR CIRCUIT TROUBLESHOOTING CHECKLIST

Occasionally, the designer's prototype regulator circuit will not operate properly. If problems do occur, the trouble can be traced to a design error in 99.9% of the cases. As a troubleshooting aid to the designer, the following guide is presented.

Of course, it would be difficult, if not impossible, to devise a troubleshooting guide which would cover all possible situations. However, the checklist provided will help the designer pinpoint the problem in the majority of cases. To use the guide, first locate the problem's symptom(s) and then carefully recheck the regulator design in the area indicated using the information contained in the referenced handbook section.

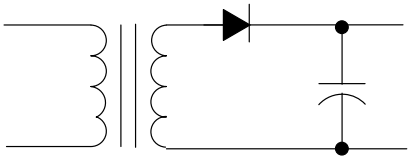
If, after carefully rechecking the circuit, the designer is not successful in resolving the problem, seek assistance from the factory by contacting the nearest ON Semiconductor Sales office.

Symptoms	Design Area to Check	Section
Regulator oscillates	1. Layout 2. Compensation capacitor too small 3. Input leads not bypassed 4. External pass element parasitically oscillating	5 3 5 5
Loss of regulation at light loads	1. Emitter–base resistor in "PNP" type boost configuration too large 2. Absence of 1.0 mA "minimum" load. (See load regulation test spec on device data sheet) 3. Improper circuit configuration	4 3
Loss of regulation at heavy loads	1. Input voltage too low [$V_{in(min)}$, $\|V_{in} - V_O\|_{min}$] 2. External pass element gain too low 3. Current limit too low 4. Line resistance between sense points and load 5. Inadequate heatsinking	2, 3 4 3 5 15
IC regulator or pass element fails after warm–up or at high T_A.	1. Inadequate heatsinking 2. Input Voltage Transient $V_{in(max)}$, V_{CEO}	15 2, 4, 5
Pass element fails during short circuit.	1. Insufficient pass element ratings SOA, $I_{C(max)}$ 2. Inadequate heatsinking	4 15
IC regulator fails during short circuit.	1. IC current or SOA capability exceeded 2. Inadequate heatsinking	2
IC regulator fails during power–up	1. Input voltage transient $V_{in(max)}$ 2. IC current or SOA capability exceeded as load (capacitor) is charged up.	2 2
IC regulator fails during power–down.	1. Regulator reverse biased	3
Output voltage does not come up during power–up or after short circuit	1. Out polarity reversal 2. Load has "latched–up" in some manner. (Usually seen with op amps, current sources, etc.)	3
Excessive 60 Hz or 120 Hz output ripple	1. Input supply filter capacitor ground loop	5

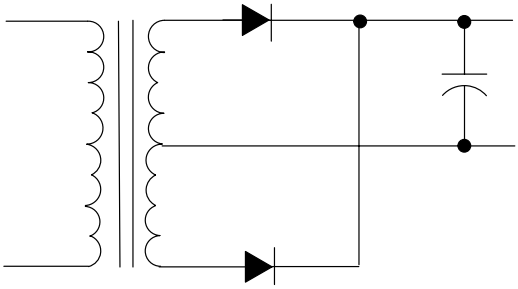
SECTION 8
DESIGNING THE INPUT SUPPLY

Most input supplies used to power series pass regulator circuits consist of a 60 Hz, single phase step–down transformer followed by a rectifier circuit whose output is smoothed by a choke or capacitor input filter. The type of rectifier circuit used can be either a half–wave, full–wave, or full–wave bridge type, as shown in Figure 8–1. The half–wave circuit is used in low current applications, while the full–wave is preferable in high–current, low output voltage cases. The full–wave bridge is usually used in all other high–current applications.

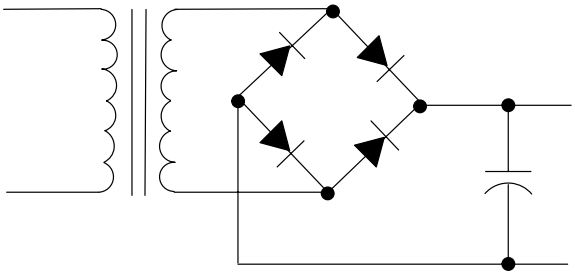
Figure 8–1. Rectification Schemes



(a) Half–Wave



(b) Full–Wave or Full–Wave Center Tap



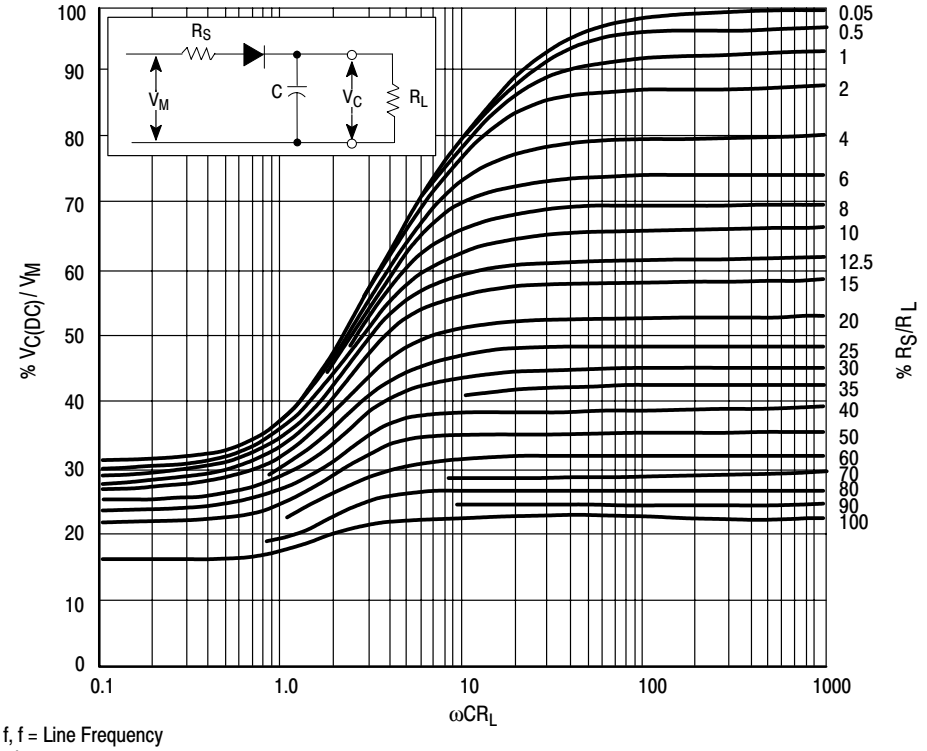
(c) Full–Wave Bridge

In this section, specification of the filter capacitor, rectifier and transformer ratings will be discussed. The specifications for the choke input filter will not be considered since the simpler capacitor input type is more commonly used in series regulated circuits. A detailed description of this type of filter can be found in the reference listed at the end of this section.

1. Design of Capacitor–Input Filters

The best practical procedure for the design of capacitor–input filters still remains based on the graphical data presented by Schade[1] in 1943. The curves shown in Figures 8–2 through 8–5 give all the required design information for half–wave and full–wave rectifier circuits. Whereas Schade originally also gave curves for the impedance of vacuum–tube rectifiers, the equivalent values for semiconductor diodes must be substituted. However, the rectifier forward drop often assumes more significance than the dynamic resistance in low–voltage supply applications, as the dynamic resistance can generally be neglected when compared with the sum of the transformer secondary–winding resistance plus the reflected primary–winding resistance. The forward drop may be of considerable importance, however, since it is about 1.0 V, which clearly cannot be ignored in supplies of 12 V or less.

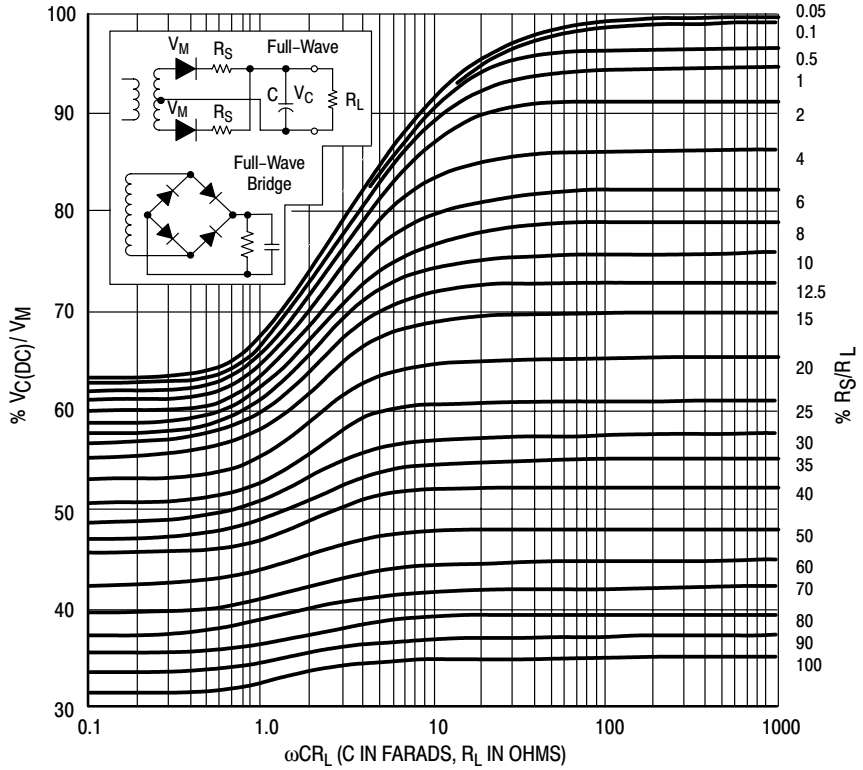
Figure 8–2. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half–Wave Capacitor–Input Circuits



$\omega = 2 \pi f$, f = Line Frequency
C in Farads
R_L in Ohms

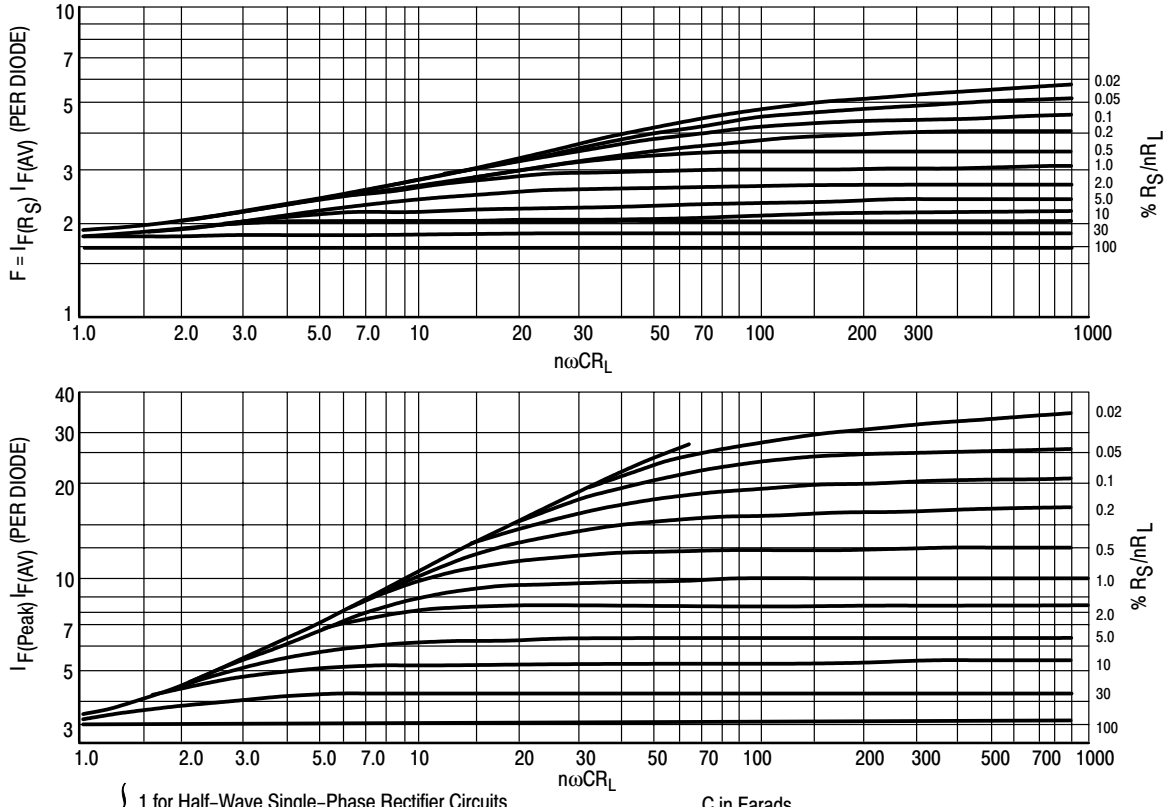
[1]From O. H. Schade, Proc. IRE, Vol. 31, p. 356, 1943.

Figure 8–3. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full–Wave Capacitor–Input Circuits



$\omega = 2\pi f$, f = Line Frequency

Figure 8–4. Relation of RMS and Peak–to–Average Diode Current in Capacitor–Input Circuits



n = { 1 for Half–Wave Single–Phase Rectifier Circuits; 2 for Full–Wave Single–Phase Rectifier Circuits

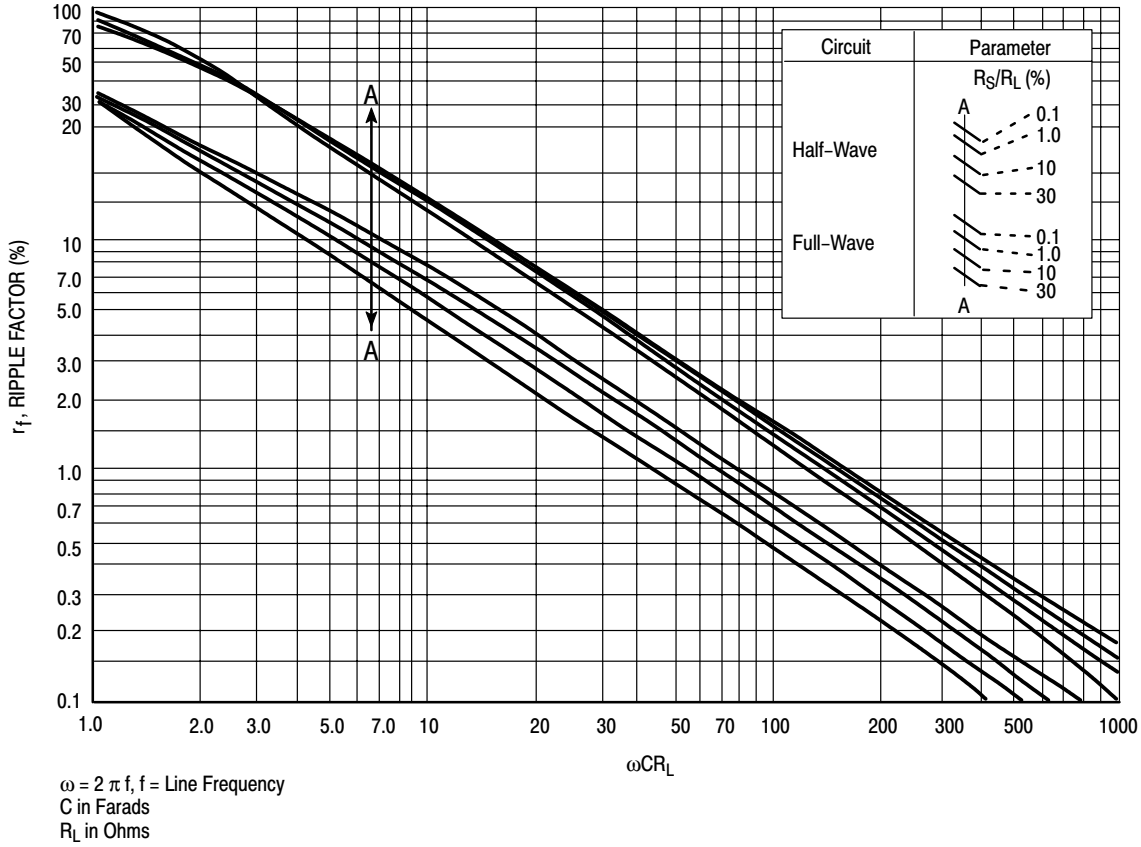
$\omega = 2\pi f$, where f = Line Frequency

C in Farads

R_L in Ohms

R_S = RMS Equivalent Source Resistance

Figure 8–5. Root–Mean–Square Ripple Voltage for Capacitor–Input Circuits



Returning to the above curves, the full–wave circuit will be considered. Figure 8–3 shows that a circuit must operate with $\omega CR_L \geq 10$ in order to hold the voltage reduction to less than 10% and $\omega CR_L \geq 40$ to obtain less than 2.0% reduction. However, it will also be seen that these voltage reduction figures require R_S/R_L, where R_S is now the total series resistance, to be about 0.1% which, if attainable, causes repetitive peak–to–average current ratios from 10 to 17 respectively, as can be seen from Figure 8–4. These ratios can be satisfied by many diodes; however, they may not be able to tolerate the turn–on surge current generated when the input–filter capacitor is discharged and the transformer primary is energized at the peak of the input waveform. The rectifier is then required to pass a surge current determined by the peak secondary voltage less the rectifier forward drop and limited only by the series resistance R_S. In order to control this turn–on surge, additional resistance must often be provided in series with each rectifier. It becomes evident, then, that a compromise must be made between voltage reduction on the one hand and diode surge rating and hence average current–carrying capacity on the other hand. If small voltage reduction, that is good voltage regulation, is required, a much larger diode is necessary than that demanded by the average current rating.

Surge Current

The capacitor–input filter allows a large surge to develop, because the reactance of the transformer leakage inductance is rather small. The maximum instantaneous surge current is approximately V_M/R_S and the capacitor charges with a time constant $\tau \approx R_S C_1$. As a rough — but conservative — check, the surge will not damage the diode if V_M/R_S is less than the diode I_{FSM} rating and τ is less than 8.3 ms. It is wise to make R_S as large as possible and not pursue tight voltage regulation; therefore, not only will the surge be reduced but rectifier and transformer ratings will more nearly approach the DC power requirements of the supply.

2. Design Procedure

A) From the regulator circuit design (see Section 6), we know:

$V_{C(DC)}$ = the required full load average dc output voltage of the capacitor input filter
$V_{Ripple(pp)}$ = the maximum no load peak–to–peak ripple voltage
V_m = the maximum no load output voltage
I_O = the full–load filter output current
f = the input ac line frequency

B) From Figure 8–5, we can determine a range of minimum capacitor values to obtain sufficient ripple attenuation. First determine r_f:

$$r_f = \frac{V_{Ripple(pp)}}{2\sqrt{2\,V_{C(DC)}}} \times 100\% \tag{8.1}$$

A range for ωCR_L can now be found from Figure 8–5.

C) Next, determine the range of R_S/R_L from Figure 8–2 or 8–3 using $V_{C(DC)}$ and the values for ωCR_L found in part B. If the range of ωCR_L values initially determined from Figure 8–5 is above $\simeq$10, R_S/R_L can be found from Figures 8–2 and 8–3 using the lowest ωCR_L value. Otherwise, several iterations between Figures 8–2 or 8–3 and 8–5 may be necessary before an exact solution for $R_S/R_L$and ωCR_L for a given r_f and $V_{C(DC)}/V_m$ can be found.

D) Once ωCR_L is found, the value of the filter capacitor (C) can be determined from:

$$C = \frac{\omega CR_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} \tag{8.2}$$

E) The rectifier requirements may now be determined:

1. Average current per diode;

$$I_{F(avg)} = I_O \text{ for half–wave rectification} = I_O/2 \text{ for full–wave rectification} \tag{8.3}$$

2. RMS and Peak repetitive rectifier current ratings can be determined from Figure 8–4.
3. The rectifier PIV rating is 2 V_m for the half–wave and full–wave circuits, V_m for the full wave bridge circuit. In addition, a minimum safety margin of 20% to 50% is advisable due to the possibility of line transients.
4. Maximum surge current, $I_{surge} = V_m/(R_S + ESR)$ (8.4)
where, ESR = minimum equivalent series resistance of filter capacitor from its data sheet.

F) Transformer Specification

1. Secondary leg RMS voltage, $V_S = \{V_m + (n)\ 1.0\}/\sqrt{2}$ (8.5)
where; n = 1 for half–wave and full–wave
n = 2 for full–wave bridge
2. Total resistance of secondary and any external resistors to be equal to R_S found from Figures 8–2, 8–3, and 8–4 (see Part C).
3. Secondary RMS current;

$$\text{half–wave} = I_{rms}; \quad \text{full–wave} = I_{rms}; \quad \text{full–wave bridge} = \sqrt{2}\,I_{rms} \tag{8.6}$$

where, I_{rms} = rms rectifier current (from part E.1 and E.2).
4. Transformer VA rating;

$$\text{half–wave} = V_S\,I_{rms}; \quad \text{full–wave} = 2\,V_S\,I_{rms}; \quad \text{full–wave bridge} = V_S\,I_{rms}(\sqrt{2}) \tag{8.7}$$

where, I_{rms} = rms rectifier current (from part E.1 and E.2) and,
V_S = secondary leg RMS voltage.

3. Design Example

A) Find the values for the filter capacitor, transformer rectifier ratings, given Full–Wave Bridge Rectification;

$$\begin{aligned} V_{C(DC)} &= 16\ V \\ V_{Ripple(pp)} &= 3.0\ V \\ V_M &= 25\ V \\ I_O &= 1.0\ A \\ f &= 60\ Hz \end{aligned}$$

B) Using Equation (8.1),

$$r_f = \frac{3}{2\sqrt{2}\,(16)} \times 100\% = 6.6\%$$

from Figure 8.5, $\omega CR_L \simeq 7$ to 15

C) Using $\omega CR_L = 10$, R_S/R_L is found from Figure 8–3 using,

$$\frac{V_{C(DC)}}{V_M} = \frac{16}{25} = 0.64 = 64\%$$

$$R_S/R_L = 20\% \text{ or } R_S = 0.2 \times R_L = 0.2 \left(\frac{V_{C(DC)}}{I_O}\right) = 0.2\ (16)$$

$$R_S = 3.2\ \Omega$$

D) From Equation (8.2), the filter capacitor size is found:

$$C = \frac{\omega CR_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} = \frac{10}{2\pi f(60)16} = 1658\ \mu F$$

E) The rectifier ratings are now specified:

1. $I_{F(avg)} = I_O/2 = 0.5$ A from Equation (8.3)
2. $I_{F(rms)} = 2 \times I_{F(AVG)} = 1.0$ A from Figure 8–4
3. $I_{F(Peak)} = 5.2 \times I_{F(AVG)} = 2.6$ A from Figure 8–4
4. PIV = V_M = 25 V (use 50 V for safety margin)
5. $I_{surge} = V_M/(R_S + ESR) \simeq 25/3.2 = 7.8$ A from Equation (8.4), neglecting capacitor ESR.

F) The transformer should have the following ratings:

1. $V_S = \{V_M + n(1.0)\}/\sqrt{2} = (25 + 2)/\sqrt{2} = 19$ VRMS {from Equation (8.5)}
2. Secondary Resistance should be 3.2 Ω
3. Secondary RMS current rating should be 1.4 A, (from Equation (8.6)).
4. From Equation (8.7), the transformer should have a 27 VA rating.

It should be noted that, in order to simplify the procedure, the above design does not allow for line voltage variations or component tolerances. The designer should take these factors into account when designing his input supply. Typical tolerances would be: line voltage = +10% to –15% and filter capacitors = +75% to –10%.

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1. O. H. Schade, Proc. IRE, Vol. 31, 1943.
2. ON Semiconductor Silicon Rectifier Manual, 1980.

SECTION 9

AN INTRODUCTION TO SWITCHING POWER SUPPLIES

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. Its performance and size advantages meet the needs of today's modern and compact electronic equipment and the increasing variety of components directed at these applications makes new designs even more practical.

This guide is intended to provide the designer with an overview of the more popular inverter circuits, their basic theory of operation, and some of the subtle characteristics involved in selecting a circuit and the appropriate components. Also included are valuable design tips on both the major passive and active components needed for a successful design. Finally, a complete set of selector guides to ON Semiconductor's Switchmode components is provided which gives a detailed listing of the industry's most comprehensive line of semiconductor products for switching power supplies.

Comparison with Linear Regulators

The primary advantages of a switching power supply are efficiency, size,and weight. It is also a more complex design, cannot meet some of the performance capabilities of linear supplies and generates a considerable amount of electrical noise. However switchers are being accepted in the industry, particularly where size and efficiency are of prime importance. Performance continues to improve and for most applications they are usually cost competitive down to the 20 W power level.

In the past the switcher's advantage versus the linear regulator was in the high power arena where passive components such as transformers and filters were small compared to the linear regulator at the same power level. However, active component count was high and tended to make the switcher less cost effective at low power levels. In recent years, Switchers have been significantly cost reduced because designers have been able to simplify the control circuits with new, cost effective integrated circuits and have found even lower cost alternatives in the passive component area.

A performance comparison chart of switching versus linear supplies is shown in Table 9–1. Switcher efficiencies run from 70% to 80% but occasionally fall to (60% to 65%) when linear post regulators are used for the auxiliary outputs. Some linear power supplies on the other hand, are operated with up to 50% efficiency but these are areas where line variations or hold–up time problems are minimal. Most linears operate with typical efficiencies of only 30%. The overall size reduction of a 20 kHz switcher is about 4:1 and newer designs in the 100 kHz to 200 kHz region end up at about 8:1 (versus a linear). Other characteristics such as static regulation specs are comparable, while ripple and load transient response are usually worse. Output noise specs can be somewhat misleading. Very often a 500 mV switching spike at the output may be attenuated considerably at the load itself due to the series inductance of the connecting cables and the additional filter capacitors found in many logic circuits. In the future, the noise generated at higher switching frequencies (100 kHz to 500 kHz) will probably be easier to filter and the transient response will be faster. Hold–up time is greater for switchers because it is easier to store energy in high voltage capacitors (200 V to 400 V) than in the lower voltage (20 V to 50 V) filter capacitors common to linear power supplies. This is due to the fact that the physical size of a capacitor is dependent on its CV product while energy storage is proportional to CV^2.

Table 9–1. 20 kHz Switcher versus Linear Performance

Parameter	Switcher	Linear
Efficiency	75%	30%
Size	2.0 W/in^3	0.5 W/in^3
Weight	40 W/lb	10 W/lb
Line and Load Regulation	0.1%	0.1%
Output Ripple V_{pp}	50 mV	5.0 mV
Noise V_{pp}	50 mV to 200 mV	—
Transient Response	1.0 ms	20 μs
Hold–Up Time	20 ms to 30 ms	1.0 ms to 2.0 ms

Basic Configurations

A switching power supply is a relatively complex circuit as is shown by the four basic building blocks of Figure 9–1. It is apparent here that the heart of the supply is really the high frequency inverter. It is here that the work of chopping the rectified line at a high frequency (20 kHz to 200 kHz) is done. It is here also that the line voltage is transformed down to the correct output level for use by logic or other electronic circuits. The remaining blocks support this basic function. The 60 Hz input line is rectified and filtered by one block and after the inverter steps this voltage down, the output is again rectified and filtered by another. The task of regulating the output voltage is left to the control circuit which closes the loop from the output to the inverter. Most control circuits generate a fixed frequency internally and utilize pulse width modulation techniques to implement the desired regulation. Basically, the on–time of the square wave drive to the inverter is controlled by the output voltage. As load is removed or input voltage increases,the slight rise in output voltage will signal the control circuit to deliver shorter pulses to the inverter and conversely as the load is increased or input voltage decreases, wider pulses will be fed to the inverter.

The inverter configurations used in today's switchers actually evolved from the buck and boost circuits shown in Figures 9–2a and 9–2b. In each case the regulating means and loop analysis will remain the same but a transformer is added in order to provide electrical isolation between the line and load. The forward converter family which includes the push–pull and half bridge circuits evolved from the buck regulator (Figure 9–2a). And the newest switcher, the flyback converter, actually evolved from the boost regulator. The buck circuit interrupts the line and provides a variable pulse width square wave to a simple averaging LC filter. In this case, the first order approximation of the output voltage is $V_{out} = V_{in} \times$ duty cycle and regulation is accomplished by simply varying the duty cycle. This is satisfactory for most analysis work and only the transformer turns ratio will have to be adjusted slightly to compensate for IR drops, diode drops, and transistor saturation voltages.

Operation of the boost circuit is more subtle in that it first stores energy in a choke and then delivers this energy plus the input line to the load. However, the flyback regulators which evolved from this configuration delivers only the energy stored in the choke to the load. This method of operation is actually based on the buck boost model shown in Figure 9–2c. Here, when the switch is opened, only the stored inductive energy is delivered to the load. The true boost circuit can also regulate by stepping up (or boosting) the input voltage whereas the buck–boost or flyback regulator can step the input voltage up or down. Analysis of the boost regulator begins by dealing with the choke as an energy storage element which delivers a fixed amount of power to the load: $P_O = 1/2\ L\ If_O$ where, I = the peak choke current; $f_O =$ the operating frequency; and, L = the inductance.

Because it delivers a fixed amount of power to the load regardless of load impedance (except for short circuits), the boost regulator is the designer's first choice in photoflash and capacitive–discharge (CD) automotive ignition circuits to recharge the capacitive load. It also makes a good battery charger. For an electronic circuit load, however, the load resistance must be known in order to determine the output voltage:

$$V_O = \sqrt{P_O R_L} = I \sqrt{\frac{Lf_O R_L}{2}}$$ where, R_L = the load resistance.

In this case, the choke current is proportional to the on–time or duty cycle of the switch and regulation for fixed loads simply involves varying the duty cycle as before. However, the output also depends on the load which was not the case with buck regulators and results in a variation of loop gain with load.

Figure 9–1. Functional Block Diagram — Switching Power Supply

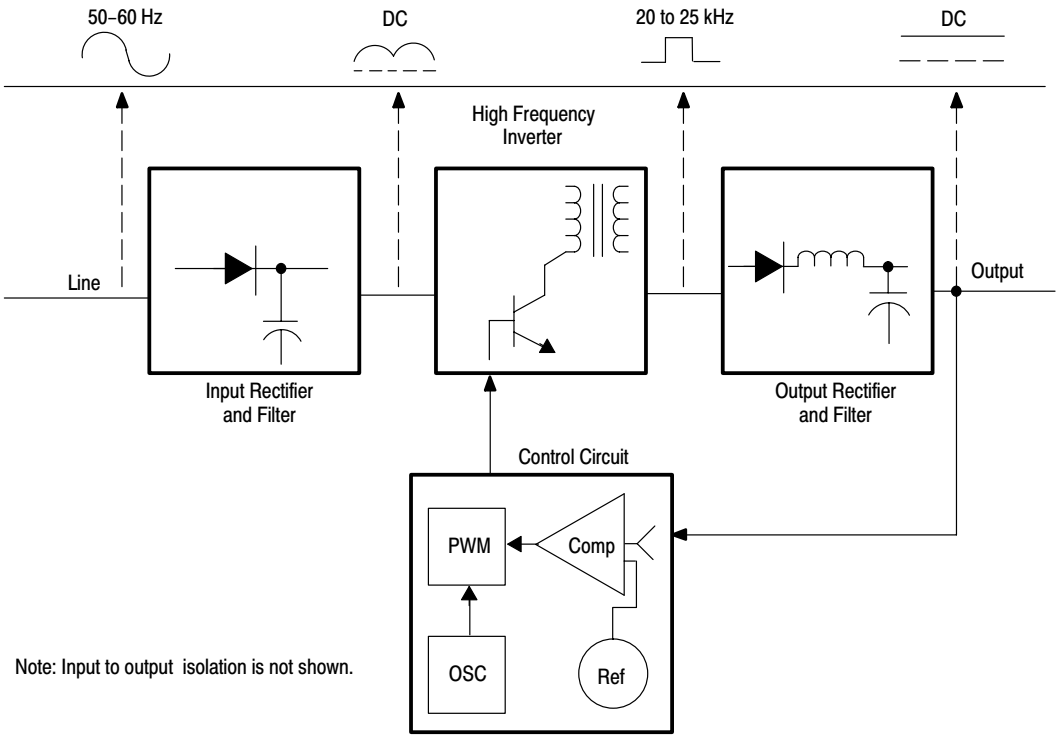
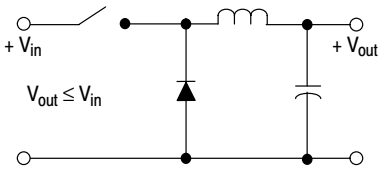
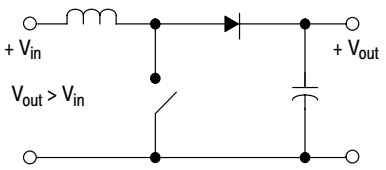


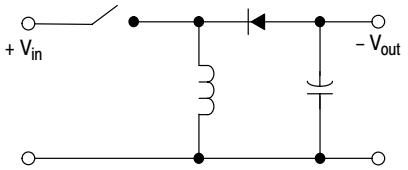
Figure 9–2. Nonisolated DC–DC Converters



(a) Buck (Step–Down)



(b) Boost (Step–Up)



(c) Buck–Boost Regulator which Resembles the Flyback Regulator (Step–Up or Down)

For both regulators, transient response or responses to step changes in load are very difficult to analyze. They lead to what is termed a “load dump” problem. This requires that energy already stored in the choke or filter be provided with a place to go when load is abruptly removed. Practical solutions to this problem include limiting the minimum load and using the right amount of filter capacitance to give the regulator time to respond to this change.

The Future

The future offers a lot of growth potential for switchers in general and low power switchers (20 W to 100 W) in particular. The latter are responding to the growth in microprocessor based equipment as well as computer peripherals. Today’s configurations have already been challenged by the sine wave inverter which reduces noise and improves transistor reliability but does effect a cost penalty. Also, a trend to higher switching frequencies to reduce size and cost even further has begun. The latest bipolar designs operate efficiently up to 100 kHz and the FET seems destined to own the 200 kHz to 500 kHz range.

At this time there are a lot of safety and noise specifications. Originally governed only by MIL specs and the VDE in Europe, now both UL and the FCC have released a set of specifications that apply to electronic systems which often include switchers (see Table 9–2). It seems probable, however, that system engineers or power supply designers will be able to add the necessary line filters and EMI shields without evoking a significant cost penalty in the design.

The most optimistic note concerning switchers is in the component area. Switching power supply components have actually evolved from components used in similar applications. And it is very likely that newer and more mature products specifically for switchers will continue to appear over the next several years. The ultimate effect of this evolution will be to further simplify, cost reduce and increase the reliability of these designs.

Table 9–2. SMPS Specifications

Specification	Area
UL 478, VDE 0730, VDE 0806	Safety
VDE 0871, VDE 0875	EMI
MIL–STD–217D	Reliability
MIL–STD–461A	EMI
DOD–STD–1399	Harmonic Content
FCC Class A & B	EMI
CSA C22.2, IEC 380	Safety

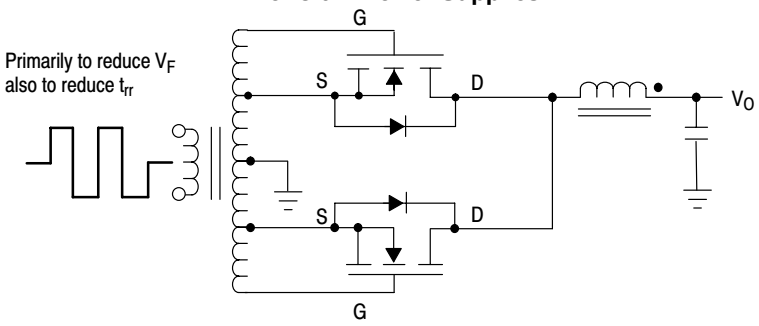
The synchronous rectifier is one example of a new component developed specifically for low voltage switchers. As requirements for 2.0 V and 3.0 V supplies emerge for use by fine geometry VLSI chips, the only way to maintain decent conversion efficiency is to develop lower forward drop rectifiers. The differences in 3.0 V and 5.0 V rectifier requirements are shown in Table 9–3. At this time, ON Semiconductor offers low V_F Schottky and area efficient TMOS III FETs for this task and is considering a variety of additional technology options. The direct approach involves using low V_F Schottkys or pinch rectifiers which will feature V_Fs of 0.3 V to 0.4 V. The indirect approach involves using FETs or bipolar transistors and slightly more complex circuitry like that shown in Figure 9–3. Both transistors will feature V_Fs of 0.2 V and, in addition, the bipolar will have high EBOs (30 V) and high gain (100) with a recovery time of 100 ns.

And for designers who are not satisfied with the relatively low frequency limitations of square wave switchers, there is the SRPS. The series resonant power supply topology seems to offer the possibility of working in the 1.0 MHz region. If components like the relatively exotic power transformer can be cost reduced, then it will be possible for this topology to become dominant in the market. The features generally associated with this type of power supply are listed in Table 9–4 and a typical half bridge circuit is shown in Figure 9–4. In a design now being studied in ON Semiconductor’s advanced products laboratory, standard FETs, Schottkys and ultrafast rectifiers all appear to work very well at 1.0 MHz.

Table 9–3. Synchronous Rectifier Requirements

Output Voltage	Rectifier Characteristics	
	V_F	V_R
5.0 V	0.5 V–1.0 V	30 V–60 V
3.0 V	0.3 V–0.6 V	20 V–40 V

Figure 9–3. Synchronous Rectifiers for 3.0 V Power Supplies

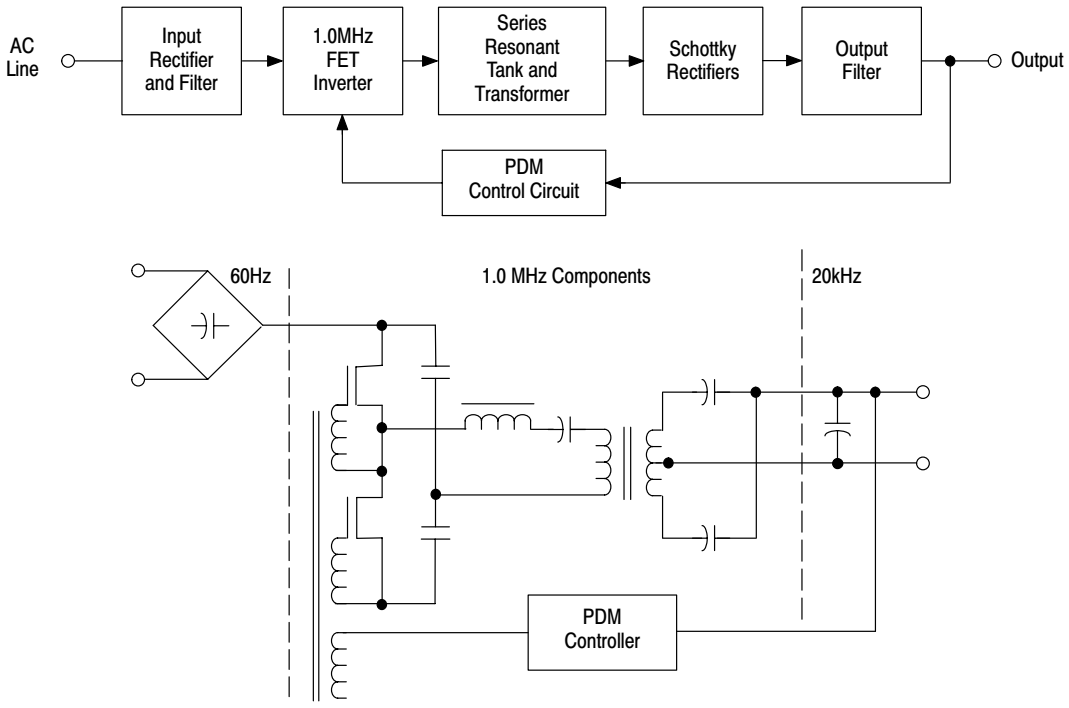


Note: The FET must be operated below V_F of the diode in order to gain the t_{rr} advantage.

Table 9–4. SRPS Features

Feature	Description
High Frequency	Today's line operated designs use sine waves in the 500 kHz to 1.0 MHz range.
Small Size	The ferrite transformer and polypropylene coupling capacitor are smaller than those found in lower frequency square wave designs.
Low Noise	Switching occurs at zero crossings which reduces component stress and lowers EMI.
Efficient	Because switching losses are reduced, efficiency is high (typically 80%).
High Peak to Average Current Ratios	Current ratings of the transistors and rectifiers are twice as high as similar flyback designs.
Special Control Circuit	PDM (density) rather than PWM (width) control is used and requires a control IC with a programmable VCO.
Market	The SRPS is expected to own 15% of the power supply market by 1990.

Figure 9–4. SRPS Block Diagram



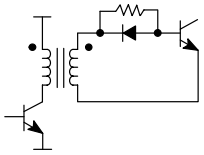
SECTION 10
SWITCHING REGULATOR TOPOLOGIES

FET and Bipolar Drive Considerations

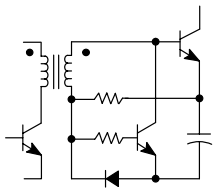
There are probably as many base drive circuits for bipolars as there are designers. Ideally, the transistor would like just enough forward drive (current) to stay in or near saturation and reverse drive that varies with the amount of stored base charge such as a low impedance reverse voltage. Many of today's common drive circuits are shown in Figure 10–1. The fixed drive circuits of Figure 10(a), (b) and (c) tend to emphasize economy, while the Baker clamp and proportional drive circuits of Figure 10(d) and (e) emphasize performance over cost.

FET drive circuits are another alternative. The standard that has evolved at this time is shown in Figure 10–2A. This transformer coupled circuit will produce forward and reverse voltages applied to the FET gate which vary with the duty cycle as shown. For this example, a V_{GS} rating of 20 V would be adequate for the worst case condition of high logic supply (12 V) and minimum duty cycle. And yet, minimum gate drive levels of 10 V are still available with duty cycles up to 50%. If wide variations in duty cycle are anticipated, it might be wise to consider using a semi–regulated logic supply for these situations. Finally, one point that is not obvious when looking at the circuit is that FETs can be directly coupled to many ICs with only 100 mA of sink and source capability and still switch efficiently at 20 kHz. However, to achieve switching efficiently at higher frequencies, 1.0 A to 2.0 A of drive may be required on a pulsed basis in order to quickly charge and discharge the gate capacitances. A simple example will serve to illustrate this point and also show that the Miller effect, produced by C_{DG}, is the predominant speed limitation when switching high voltages (see Figure 10–2B). A FET responds instantaneously to changes in gate voltage and will begin to conduct when the threshold is reached (V_{GS} = 2.0 V to 3.0 V) and be fully on with V_{GS} = 7.0 V to 8.0 V. Gate waveforms will show a porch at a point just above the threshold voltage which varies in duration depending on the amount of drive current available and this determines both the rise and fall times for the drain current.

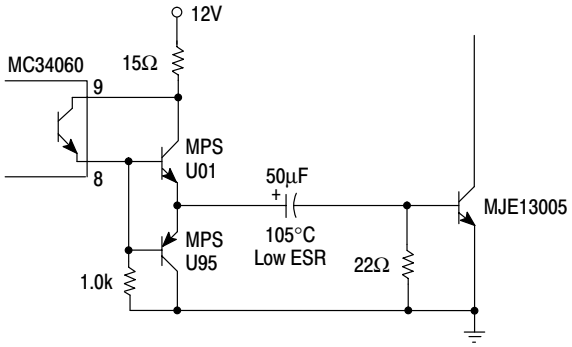
Figure 10–1. Typical Bipolar Base Drive Circuits



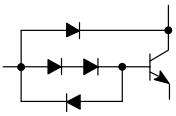
(a) Fixed Drive, Turn–Off Energy Stored in Transformer



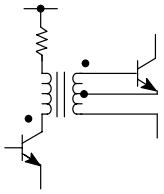
(b) Fixed Drive, Turn–Off Energy Stored in Capacitor



(c) Direct Drive

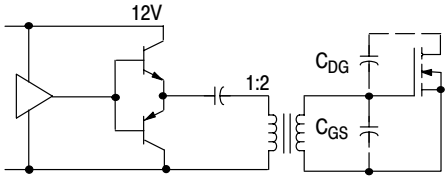


(d) Standard Baker Clamp

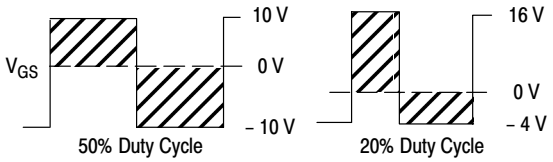


(e) Proportional Base Drive

Figure 10–2A. Typical Transformer Coupled FET Drive

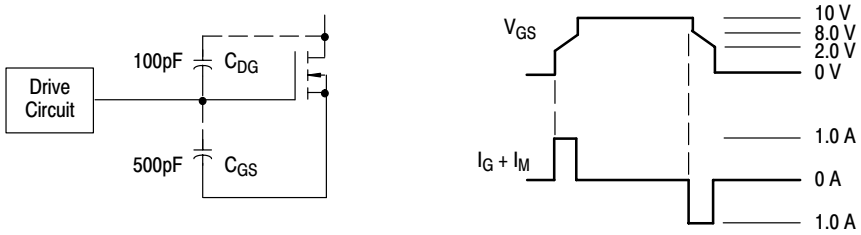


Wave Forms



V_{GS} Wave Forms

Figure 10–2B. FET Drive Current Requirements



1. Miller Current for 30 ns:
$I_M = C_{DG}\, dv/dt$

$$= 100\ pF \times \frac{300\ V}{30\ ns} = 1.0\ A$$

2. Gate Cap Current for 30 ns:
$I_G = C_{GS}\, dv/dt$

$$= 500\ pF \times \frac{6.0\ V}{30\ ns} = 0.1\ A$$

To estimate drive current requirements, two simple calculations with gate capacitances can be made:

1. $I_M = C_{DG}dv/dt$ and,
2. $I_G = C_{GS}dv/dt$

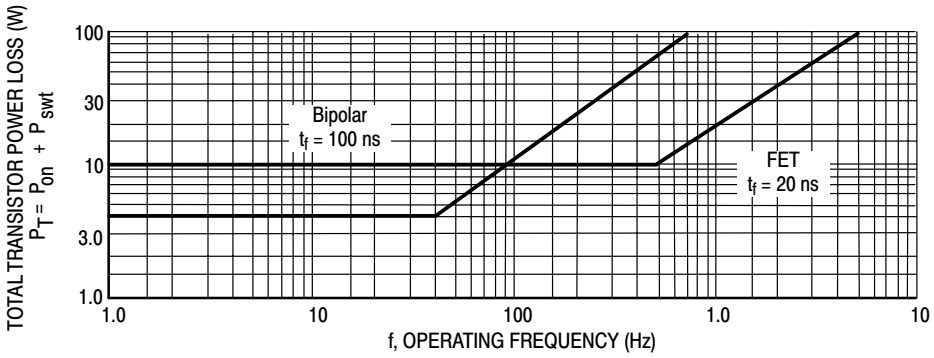
I_M is the current required by the Miller Effect to charge the drain–to–gate capacitance at the rate it is desired to move the drain voltage (and current). And I_G is usually the lesser amount of current required to charge the gate–to–source capacitance through the linear region (2.0 V to 8.0 V). As an example, if 30 ns switching times are desired at 300 V, where C_{DG} = 100 pF and C_{GS} = 500 pF, then:

1. $I_M = 100\ pF \times 300\ V/30\ ns = 1.0\ A$ and,
2. $I_G = 500\ pF \times 6.0\ V/30\ ns = 0.1\ A$

This example shows the direct proportion of drive current capability to speed and also illustrates that for most devices, C_{DG} will have the greatest effect on switching speed and that C_{GS} is important only in estimating turn–on and turn–off delays.

Aside from its unique drive requirements, a FET is very similar to a bipolar transistor. Today's 400 V FETs compete with bipolar transistors in many switching applications. They are faster and easier to drive, but do cost more and have higher saturation, or more accurately, "on" voltages. The performance or efficiency tradeoffs are analyzed using Figure 10–3, where typical power losses for switching transistors versus frequency are shown. The FET (and bipolar) losses were calculated at 100°C rather than 25°C because on resistance and switching times are highest here and 100°C is typical of many applications. These curves are asymptotes of the actual device performance, but are useful in establishing the "breakpoint" of various devices, which is the point where saturation and switching losses are equal.

Figure 10–3. Typical Switching Losses at 300 V and 5.0 A (T_J = 100°C)



Control Circuits

Over the years, a variety of control ICs for SMPS have been introduced. The voltage mode controllers diagramed in Table 10–1 still dominate this market. The basic regulating function is performed in the pulse width modulator (PWM) section. Here, the dc feedback signal is compared to a fixed frequency sawtooth waveform. The result is a variable duty cycle pulse train which, with suitable buffer or interface circuits, can be used to drive the power switching transistor. Some ICs provide only a single output while others provide a phase splitter or flip–flop to alternately pulse two output channels. Additionally, most ICs provide an error amplifier and reference section shown as a means to process, compare and amplify the feedback signal.

Features required by a control IC vary to some extent because of the particular needs of a designer and on the circuit configuration chosen. However, most of today's current generation ICs have evolved with the following capabilities or features:

- Programmable (to 500 kHz) Fixed Frequency Oscillator
- Linear PWM Section with Duty Cycle from 0% to 100%
- On Board Error Amplifiers
- On Board Reference Regulator
- Adjustable Deadtime
- Under Voltage (low V_{CC}) Inhibit
- Good Output Drive (100 mA to 200 mA)
- Option of Single or Dual Channel Output
- Uncommitted Output Collector and Emitter or Totem Pole Drive Configuration
- Soft–Start
- Digital Current Limiting
- Oscillator Sync Capability

It is primarily the cost differences in these parts that determine whether all or only part of these features will be incorporated. Most of these are evident to the designer who has already started comparing competitive device data sheets.

In addition to the control circuits listed in Table 10–2, ON Semiconductor also has two dc converter control chips, the μA78S40 and the MC34063A. These chips feature an on–board 40 V, 2.0 A switching transistor and operate by dropping pulses from a fixed frequency, fixed duty cycle oscillator depending on load demand.

Today there is a demand for simple, low cost, single control ICs. These ICs, like ON Semiconductor's MC34060A and MC34063A components, are used to run the low–power flyback type configurations and are usually part of a three chip rather than a single chip system. The differences in these two approaches are illustrated in Figure 10–6.

When it is necessary to drive two or more power transistors, drive transformers are a practical interface element and are driven by the conventional dual channel ICs. In the case of a single transistor converter, however, it is usually more cost effective to directly drive the transistor from the IC. In this situation, an

optocoupler is commonly used to couple the feedback signal from the output back to this control IC. And the error amplifier in this case is nothing more than a programmable zener like ON Semiconductor's TL431.

Overvoltage Protection

Linear and switching power supplies can be protected from overvoltage with a crowbar circuit. For linear supplies, the pass transistor can fail shorted, allowing high line transformer voltage to the load. For switching power supplies, a loose or disconnected remote sense lead can allow high voltage to the load.

Table 10–1. Basic SM Control ICs

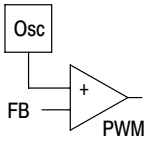
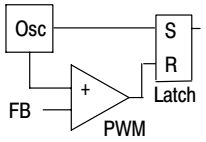
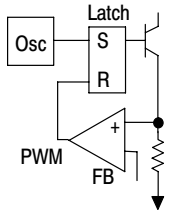
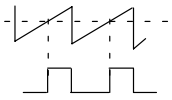
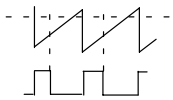
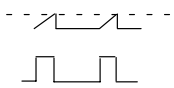
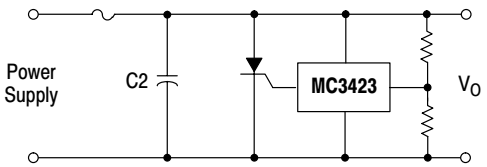
Control Technique	Type A Voltage Mode	Type B Voltage Mode w/Latch	Type C Current Mode
Schematic			
Single Channel Parts	MC34060A	—	UC3842 MC34129
Dual Channel Parts	TL494/594	SG3525A/27A SG3526	—
Features	Low Cost	Digital Current Limiting, Good Noise Immunity	Designed for Flyback, Inherent Feed Forward
PWM Waveforms Output			

Table 10–2. Control Circuits

Overvoltage Protection (OVP)		Over/Undervoltage Protection (O/UVP)	Undervoltage Sense MPU/MCU Reset
Standard	High Performance		
TL431	MC3423 TL431A	MC3425 MC34161	MC34064–5 MC34164–3 MC34164–5

The list of available circuits is shown in Table 10–2 and a typical 0 V application is shown in Figure 10–4. This crowbar circuit ignores noise spikes but will fire the SCR when a valid overvoltage condition is detected. The SCR will discharge C2 and either blow the fuse or cause the power supply to shut down.

Figure 10–4. Crowbar Circuit



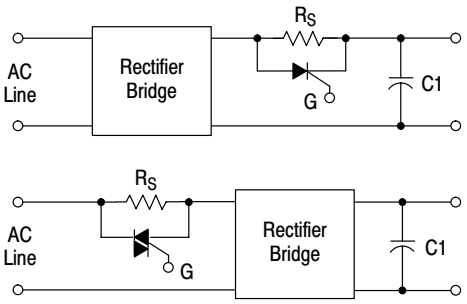
For further information, see the MC3423 data sheet.

Surge Current Protection

Many high current PWM switching supplies operate directly off the ac line. They have very large capacitive input filters with high inrush surge currents. The line circuit breaker and the rectifier bridge must be protected during turn–on.

Surge current limiting can be accomplished by adding R_S and an SCR short after charging C1, as shown in Figure 10–5, or by phase controlling the line voltage with a Triac.

Figure 10–5. Surge Current Limiting for a Switching Power Supply



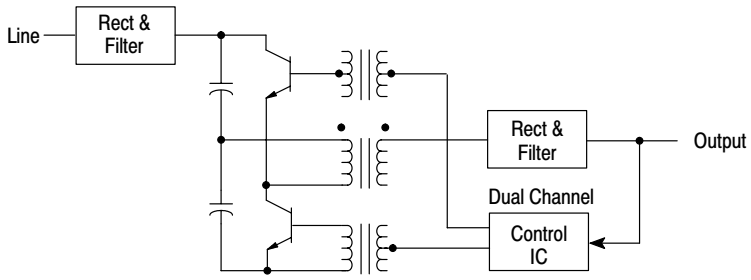
Transformer Design

With respect to transformer design, many of today's designers would say don't try it. They'd advise using a consultant or winding house to perform this task and with good reason. It takes quite a bit of time to develop a feel for this craft and be able to use both experience and intuition to find solutions to second and third order problems. Because of these subtle problems, most designers find that after the first paper design is done, as many as four or five lab iterations may be necessary before the transformer meets the design goals. However, there is a considerable design challenge in this area and a great deal of satisfaction can be obtained by mastering it.

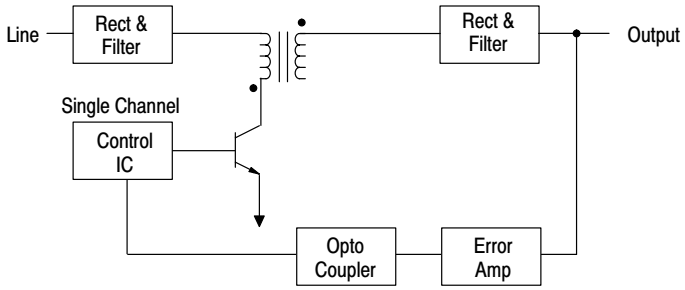
This component design, as do all others, begins by requesting all available literature from the appropriate manufacturers and then following this up with phone calls when specific questions arise. A partial list of companies is shown in Table 10–3. Designs below 20 W generally use pot cores, but for 20 W and above, E cores are preferred. E cores expose the windings to air so that heat is not trapped inside and make it easier to bring out connections for several windings. Remember that flyback designs require lower permeability cores than the others. The classic approach is to consult manufacturers charts like the one shown in Figure 10–8 and then to pick a core with the required power handling ability. Both E and EC (E cores with a round center leg) are popular now and they are available from several manufacturers. EC cores offer a performance advantage (better coupling) but standard E cores cost less and are also used in these applications. Another approach that seems to work equally well is to do a paper design of the estimated windings and turns required. Size the wire for 500 circular mils (CM) per amp and then find a core that has the required window area for this design. Now, before the windings are put on, it is a good idea to modify the turns so that they fit on one layer or an integral number of layers on that bobbin. This involves checking the turns per inch of the wire against the bobbin length. The primary generally goes on first and then the secondaries. If the primary hangs over an extra half layer, try reducing the turns or the wire size. Conversely, if the secondary does not take up a full layer, try bifilar winding (parallel) using wire half the size originally chosen (i.e., 3 wire sizes smaller, like 23 versus 20). This technique ultimately results in the use of foil for the higher current (20 A) low voltage windings. Most windings can be separated with 3 mil mylar (yellow) tape but for good isolation, cloth is recommended between primary and secondary.

Finally, once a mechanical fit has been obtained, it is time for the circuit tests. The isolation voltage rating is strictly a mechanical problem and is one of the reasons why cloth is preferred over tape between the primary and secondary. The inductance and saturating current level of the primary are inherent to the design, and should be checked in the circuit or other suitable test fixture. Such a fixture is shown in Figure 10–7 where the transistor and diode are sized to handle the anticipated currents. The pulse generator is run at a low enough duty cycle to allow the core to reset. Pulse width is increased until the start of saturation is observed (I_{sat}). Inductance is found using L = E/(di/dt).

Figure 10–6. Control Circuit Topologies



(a) Single Chip System — Drive Transformer Isolation



(b) Three Chip System — Opto Coupler Isolation

In forward converters, the transformer generally has no gap in order to minimize the magnetizing current (I_M). For these applications the core should be chosen large enough so that the resulting LI product insures that I_M at operating voltages is less than I_{sat}. For flyback designs, a gap is necessary and the test circuit is useful again to evaluate the effect of the gap. The gap will normally be quite large, $Lg >> L_m/u$,

where, Lg = gap length
L_m = magnetic path length, and
u = permeability.

Under this stipulation, the gap directly controls the LI parameters and doubling it will decrease L by two and increase I_{sat} by two until fringing effects occur. Gaps of 5 mils to 20 mils are common. Again, the anticipated switching currents must be less than I_{sat} when the core is gapped for the correct inductance.

Table 10–3. Partial List of Core (C) and Transformer (T) Manufacturers

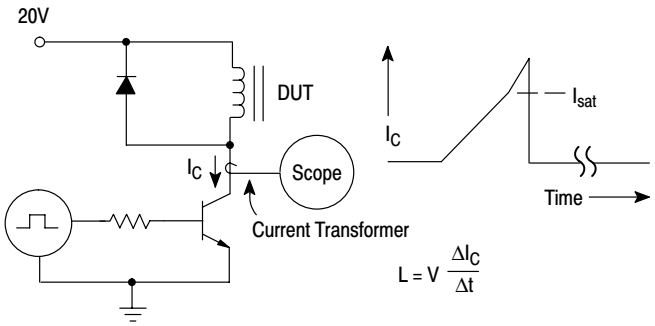
Company	Location	Code
Ferroxcube Inc.	Sauggerties, NY	C
Indiana General	Keasby, NJ	C
Stackpole	St. Marys, PA	C
TDK	El Segundo, CA	C
Pulse Engineering	San Diego, CA	T
Coilcraft	Cary, IL	T

Transformer tests in the actual supply are usually done with a high voltage dc power supply on the primary and with a pulse generator or other manual control for the pulse width (such as using the control IC in the open loop configuration). Here the designer must recheck three areas:

1. Core saturation
2. Correct amount of secondary voltage
3. Transformer heat rise

If problems are detected in any of these areas, the ultimate fix may be to redesign using the next larger core size. However, if problems are minimal, or none exist, it is possible to stay with the same core or even consider using the next smaller size.

Figure 10–7. Simple Coil Tester



Filter Capacitor Considerations

In today's 20 kHz switchers, aluminum electrolytics still predominate. The good news is that most have been characterized, improved, and cost reduced for this application. The input filter requires a voltage rating that depends on the peak line voltage; i.e., 400 V to 450 V for a 220 V switcher. If voltage is increased beyond this point, the capacitor will begin to act like a zener and be thermally destroyed from high leakage currents if the rating is exceeded for enough time. In doubler circuits, voltage sharing of the two capacitors in series can be a problem. Here extra voltage capability may be needed to make up for the imbalances caused by different values of capacitance and leakage current. A bleeder resistor is normally used here not only for safety but to mask the differences in leakage current. The RMS current rating is also an important consideration for input capacitors and is an example of improvements offered by today's manufacturers. Earlier "lytics" usually lacked this rating and often overheated. Large capacitors that were not needed for performance were used just to reduce this heating. However, today's devices offer lower thermal resistance, improved connection to the foil and good RMS ratings. A partial list of manufacturers that supply both high voltage input and the lower voltage output capacitors for switchers is shown in Table 10–4. Most of the companies offer not only the standard 85°C components, but devices with up to 125°C ratings which are required because of the high ambient temperatures (55° to 85°C) that many switchers have to operate in, many times without the benefit of fans.

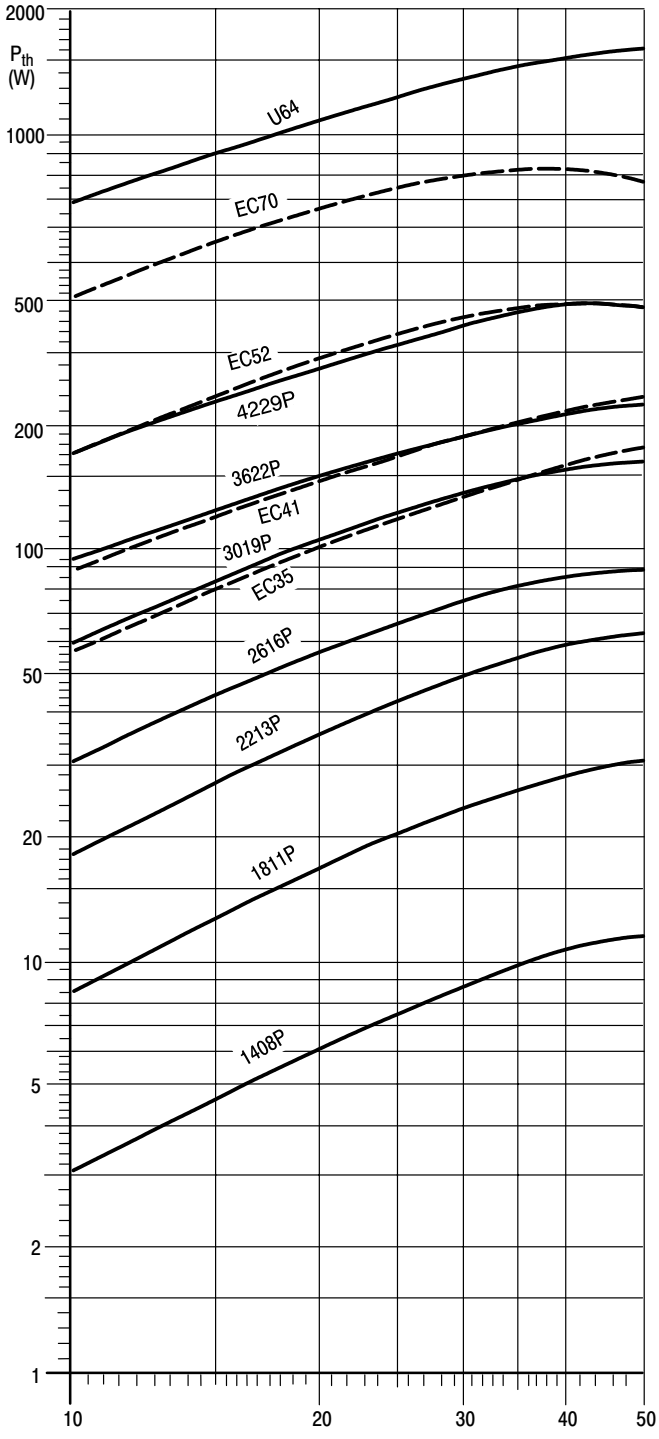
Table 10–4. Partial List of Capacitor Companies

Company (U.S.)	Location
MEPCO/Electra	Columbia, SC
Cornell–Dublier	Sanford, NC
Sangamo	Pickens, SC
Mallory	Indianapolis, IN

For output capacitors the buzz word is low ESR (equivalent series resistance). It turns out that for most capacitors even in the so–called "low ESR" series, the output ripple depends more on this resistance than on the capacitor value itself. Although typical and maximum ESR ratings are now available on most capacitors designed for switchers, the lead inductance generally is not specified except for the ultra–high frequency four terminal capacitors from some vendors. This parameter is responsible for the relatively high switching spikes that appear at the output. However, at this point in time, most designers find it less costly and more effective to add a high frequency noise filter rather than use a relatively expensive capacitor with low equivalent series inductance (ESL).

These LC noise or spike filters are made using small powdered iron toroids (1/2″ to 1″ OD) with distributed windings to minimize interwinding capacitance. And the output is bypassed using a small 0.1 μF ceramic or a 10 μF to 50 μF tantalum or both. Larger powered iron toroids are often used in the main LC output filter although the higher permeability ferrite EC and E cores with relatively large gaps can also be used. Calculations for the size of this component should take into account the minimum load so that the choke will not run "dry" as stated earlier.

Figure 10–8. Core Selection for Bridge Configurations (Reprinted from Ferroxcube Design Manual)



Note: Power handling decreases by a factor of 2 in forward and by 4 in flyback configurations.

SECTION 11
SWITCHING REGULATOR COMPONENT DESIGN TIPS

Transistors

The initial selection of a transistor for a switcher is basically a problem of finding the one with voltage and current capabilities that are compatible with the application. For the final choice performance and cost tradeoffs among devices from the same or several manufacturers have to be weighed. Before these devices can be put in the circuit, both protective and drive circuits will have to be designed.

ON Semiconductor's first line of devices for switchers were trademarked "Switchmode" transistors and introduced in the early 70's with data sheets that provided all the information that a designer would need including reverse bias safe operating area (RBSOA) and performance at elevated temperature (100°C). The first series was the 2N6542 through 2N6547, TO–204 (TO–3) and was followed by the MJE13002 through MJE13009 series in a plastic TO–220 package. Finally, high voltage (1.0 kV) requirements were met by the metal MJ8500 thru MJ8505 series and the plastic MJE8500 series. The Switchmode II series is an advanced version of Switchmode I that features faster switching. Switchmode III is a state of the art bipolar with exceptional speed, RBSOA, and up to 1.5 kV blocking capacity. Here, device cost is somewhat higher, but system costs may be lowered because of reduced snubber requirements and higher operating frequencies. A similar argument applies to ON Semiconductor TMOS Power FETs. These devices make it possible to switch efficiently at higher frequencies (200 kHz to 500 kHz) but the main selling point is that they are easier to drive. This latter point is the one most often made to show that systems savings are again quite possible even though the initial device cost is higher.

Table 11–1. ON Semiconductor High Voltage Switching Transistor Technologies

Family	Typical Device	Typical Fall Time	Approximate Switching Frequency
SWITCHMODE I	2N6545 MJE13005 MJE12007	200 ns to 500 ns	20 k
SWITCHMODE II	MJ13081	100 ns	100 k
SWITCHMODE III	MJ16010	50 ns	200 k
TMOS	MTP5N40	20 ns	500 k

Table 11–2 is a chart of the transistor voltage requirements for the various off–line converter circuits. As illustrated, the most stringent requirement for single transistor circuits (flyback and forward) is the blocking or V_{CEV} rating. Bridge circuits, on the other hand, turn on and off from the dc bus and their most critical voltage is the turn–on or $V_{CEO(sus)}$ rating.

Table 11–2. Power Transistor Voltage Chart

Line Voltage	Circuit			
	Flyback, Forward or Push–Pull		Half or Full–Bridge	
	V_{CEV}	$V_{CEO(sus)}$	$V_{CEO(sus)}$	V_{CEV}
220 120	850 kV to 1.0 kV 450	450 250	450 250	450 250

Most switchmode transistor load lines are inductive during turn–on and turn–off. Turn–on is generally inductive because the short circuit created by output rectifier reverse recovery times is isolated by leakage inductance in the transformer. This inductance effectively snubs most turn–on load lines so that the rectifier recovery (or short circuit) current and the input voltage are not applied simultaneously to the transistor. Sometimes primary interwinding capacitance presents a small current spike but usually turn–on transients are not a problem. Turn–off transients due to this same leakage inductance, however, are almost always a problem. In bridge circuits, clamp diodes can be used to limit these voltage spikes. If the resulting inductive load line exceeds the transistor's reverse bias switching capability (RBSOA) then an RC network may also be added across the primary to absorb some of this transient energy. The time constant of this network should equal the anticipated switching time of the transistor (50 ns to 500 ns). Resistance values of 100 Ω to 1000 Ω in this RC network are generally appropriate. Trial and error will indicate how low the resistor has to be to provide the correct amount of snubbing. For single transistor converters, the circuits shown in Figure 11–1 are generally used.

Here slightly different criteria are used to define the R and C snubber values:

$$C = \frac{I\, t_f}{V}$$

where; I = the peak switching current

t_f = the transistor fall time

V = the peak switching voltage (Approximately twice the DC bus)

also, $R = t_{on}/C$ (it is not necessary to completely discharge this capacitor in order to obtain the desired effects of this circuit)

where, t_{on} = the minimum on–time or pulse width

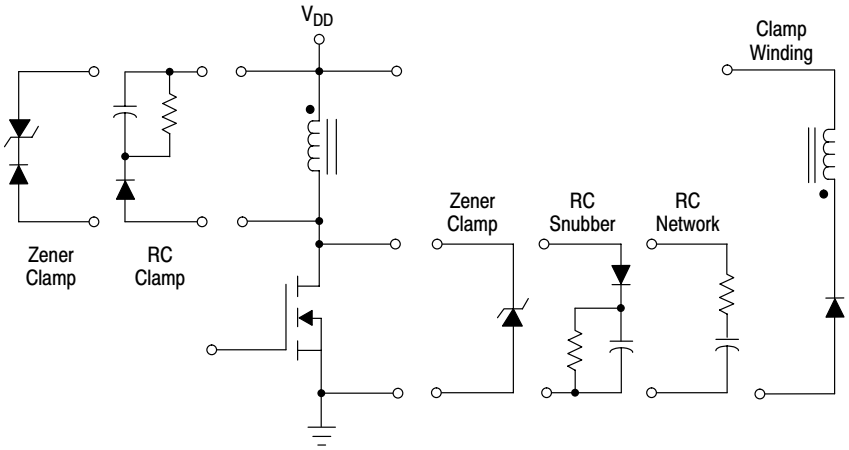
and, $P_R = \frac{CV^2f}{2}$

where, P_R = the power rating of the resistor

and, f = the operating frequency.

In most of today's designs snubber elements are small or nonexistent and voltage spikes from energy left in the leakage inductance a more critical problem depending on how good the coupling is between the primary and clamp windings and how fast the clamp diode turns on. FETs often have to be slowed down to prevent self destruction from this spike.

Figure 11–1. Protection Circuits for Switching Transistors



Zener and Mosorb Transient Suppressors

If necessary, protection from voltage spikes may be obtained by adding a zener and rectifier across the primary as shown in Figure 11–1. Here ON Semiconductor's 5.0 W zener lines with ratings up to 200 V, and 10 W TO–220 Mosorbs with ratings up to 250 V can provide the clamping or spike limiting function. If the zener must handle most of the power, its size can be estimated using:

$$PZ = \frac{L_L I^2 f}{2}$$

where, P_Z = the zener power rating
and, L_L = the leakage inductance (measured with the clamp winding or secondary shorted)
I = peak collector current
f = operating frequency

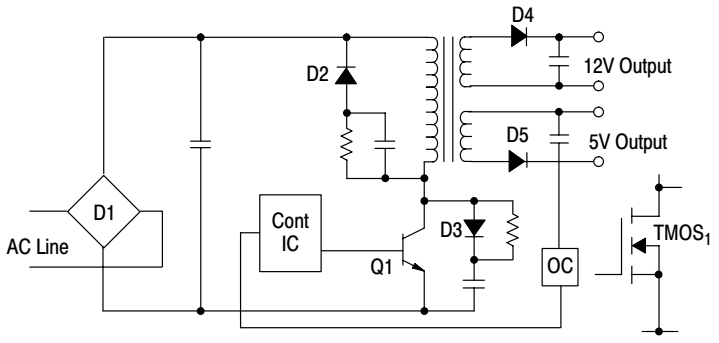
Distinction is sometimes made between devices trademarked Mosorb (by ON Semiconductor, Inc.), and standard zener/avalanche diodes used for reference, low–level regulation and low–level protection purposes. It must be emphasized that Mosorb devices are, in fact, zener diodes. The basic semiconductor technology and processing are identical. The primary difference is in the applications for which they are designed. Mosorb devices are intended specifically for transient protection purposes and are designed, therefore, with a large effective junction area that provides high pulse power capability while minimizing the total silicon use. Thus, Mosorb pulse power ratings begin at 600 W — well in excess of low power conventional zener diodes which in many cases do not even include pulse power ratings among their specifications.

MOVs, like Mosorbs, do have the pulse power capabilities for transient suppression. They are metal oxide varistors (not semiconductors) that exhibit bidirectional avalanche characteristics, similar to those of back–to–back connected zeners. The main attributes of such devices are low manufacturing cost, the ability to absorb high energy surges (up to 600 joules) and symmetrical bidirectional "breakdown" characteristics. Major disadvantages are: high clamping factor, an internal wear–out mechanism and an absence of low–end voltage capability. These limitations restrict the use of MOVs primarily to the protection of insensitive electronic components against high energy transients in applications above 20 V, whereas, Mosorbs are best suited for precise protection of sensitive equipment even in the low voltage range the same range covered by conventional zener diodes.

Rectifiers

Once components for the inverter section of a switcher have been chosen, it is time to determine how to get power into and out of this section. This is where the all–important rectifier comes into play. (See Figure 11–2.) The input rectifier is generally a standard recovery bridge that operates off the ac line and into a capacitive filter. For the output section, most designers use Schottkys for efficient rectification of the low voltage, 5.0 V output windings and for the higher voltage, 12 V to 15 V outputs, the more economical fast recovery or ultrafast diodes are used.

Figure 11–2. Switchmode Power Supply Flyback or Boost Design



D1 — Bridge Rectifier — Line Voltage
D2 — Clamp Diode — HV/Fast–Ultrafast
D3 — Snubber Diode — HV/Fast–Ultrafast
D4 — Output Rectifier — Fast/Ultrafast
D5 — Output Rectifier — Schottky

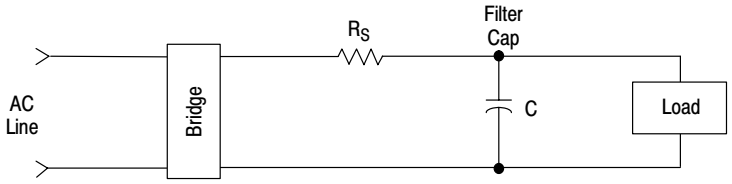
For the process of choosing an input rectifier, it is useful to visualize the circuit shown in Figure 11–3. To reduce cost, most earlier approaches of using choke input filters, soft start relays (Triacs), or SCRs to bypass a large limiting resistor have been abandoned in favor of using small limiting resistors or thermistors and a large bridge. The bridge must be able to withstand the surge currents that exist from repetitive starts at peak line. The procedure for finding the right component and checking its fit is as follows:

1. Choose a rectifier with 2 to 5 times the average I_O required.
2. Estimate the peak surge current (I_p) and time (t) using:

$$I_p = \frac{1.4\ V_{in}}{R_S} \quad t = R_S C$$

Where V_{in} is the RMS input voltage; R_S is the total series resistance; and C is the filter capacitor size.

Figure 11–3. Choosing Input Rectifiers



3. Compare this current pulse to the sub cycle surge current rating (I_S) of the diode itself. If the curve of I_S versus time is not given on the data sheet, the approximate value for I_S at a particular pulse width (t) may be calculated knowing:
   - I_{FSM} — the single cycle (8.3 ms) surge current rating and using.
   - $I^2\sqrt{t}$ = K, which applies when the diode temperature rise is controlled by its thermal response as well as power (i.e., $T = K'P\sqrt{t}$ for t < 8.0 ms).

   This gives:

$$I_S 2\sqrt{t} = I2_{FSM}\ \sqrt{8.3\ ms} \quad \text{or,} \quad I_S = I_{FSM}\ \left(\frac{8.3\ ms}{t}\right)^{1/4}, \text{ t is in milliseconds.}$$

4. If $I_S < I_P$, consider either increasing the limiting resistor (R_S) or utilizing a larger diode.

In the output section where high frequency rectifiers are needed, there are several types available to the designer. In addition to the Schottky (SBR) and fast recovery (FR), there is also an ultrafast recovery (UFR). Comparative performance for devices with similar current ratings is shown in Table 11–3. The obvious point here is that lower forward voltage improves efficiency and lower recovery times reduce turn–on losses in the switching transistors, but the tradeoff is higher cost. As stated earlier, Schottkys are generally used for 5.0 V outputs and fast recovery and ultrafast devices for 12 V outputs and greater. The ultrafast is competing both with the Schottky where higher breakdown is needed and with the fast recovery in those applications where performance is more important than cost. Ten years ago Schottkys were very fragile and could fail short from either excessive dv/dt (1.0 V to 5.0 V per nanosecond) or reverse avalanche. Since that time, ON Semiconductor has incorporated a “guard ring” or internal zener which minimizes these earlier problems and reduces the need for RC snubbers and other external protective networks.

Table 11–3. ON Semiconductor Rectifier Product Portfolio

Parameter	Schottky	Ultrafast	Fast Recovery	Standard Recovery
Forward Voltage (V_F)	0.5 V to 0.6 V	0.9 V to 1.0 V	1.2 V to 1.4 V	1.2 V to 1.4 V
Reverse Recovery Time (t_{rr})	<10 ns	25 ns to 100 ns	150 ns	1.0 μs
t_{rr} Form	Soft	Soft	Soft	Soft

DC Blocking Voltage (V_R)	20 V to 60 V	50 V to 1000 V	50 V to 1000 V	50 V to 1000 V
Cost Ratio	3:1	3:1	2:1	1:1

SECTION 12
BASIC SWITCHING POWER SUPPLY CONFIGURATIONS

The implementation of switching power supplies by the non–specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback and Forward Converter Switching Power Supplies (50 W to 250 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ variation: $\delta_{(max)}$ = 0.4)
- Maximum Transistor working current:

$$I_w = \frac{2.0\ P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{5.5\ P_{out}}{V_{in}} \quad \text{(Flyback)}$$

$$= \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{2.25\ P_{out}}{V_{in}} \quad \text{(Forward)}$$

- Maximum transistor working voltage: $V_w = 2 \times V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Flyback Configuration

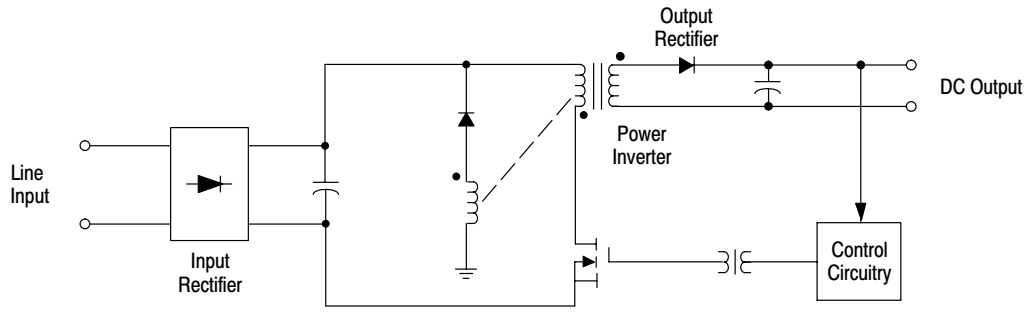


Table 12–1. Flyback and Forward Converter Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V	120 V
MOSFET Requirements: Max Working Current (I_w) Max Working Voltage (V_w)	 2.25 A 380 V	 1.2 A 750 V	 4.0 A 380 V	 2.5 A 750 V	 8.0 A 380 V	 4.4 A 750 V	 11.4 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N90 —	 MTM7N45 — MTH7N45	 MTM4N90 — —	 MTM15N45 — —
Input Rectifiers: Max Working Current (I_w) Recommended Types	 0.4 A MDA104A	 0.25 A MDA106A	 0.4 A MDA206	 0.5 A MDA210	 2.35 A MDA970	 1.25 A MDA210	 4.6 A MDA3506
Output Rectifiers: Recommended types for Output Voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MUR3010PT MUR1615CT MUR1615CT MUR 440, MUR840A		 MBR3035PT MUR3010PT MUR1615CT MUR1615CT MUR840A		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902						

Flyback and Forward Converters

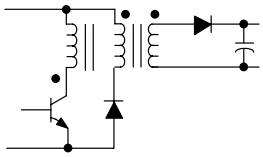
To take advantage of the regulating techniques discussed earlier and also provide isolation, a total of seven popular configurations have evolved and are listed below. Each circuit has a practical power range or capability associated with it as follows:

Circuit	Power Range	Parts Cost
DC Converter	5.0 W	$ 4.00
Converter w/30 V Transformer	10 W	7.00
Blocking OSC	20 W	10.00
Flyback	50 W	15.00
Forward	100 W	20.00
Half–Bridge	200 W	30.00
Full–Bridge	500 W	75.00

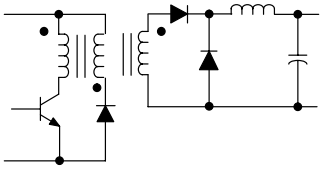
First to be discussed will be the low power (20 W to 200 W) converters which are dominated by the single transistor circuits shown in Figure 12–1. All of these circuits operate the magnetic element in the unipolar rather than bipolar mode. This means that transformer size is sacrificed for circuit simplicity.

The flyback (alternately known as the “ringing choke”) regulator stores energy in the primary winding and dumps it into the secondary windings, see Figure 12–1(a). A clamp winding is usually present to allow energy stored in the leakage reactance to return safely to the line instead of avalanching the switching transistor. The operating model for this circuit is the buck–boost discussed earlier. The flyback is the lowest cost regulator because output filter chokes are not required since the output capacitors feed from a current source rather than a voltage source. It does have higher output ripple than the forward converters because of this. However, it is an excellent choice when multiple output voltages are required and does tend to provide better cross regulation than the other types. In other words changing the load on one winding will have little effect on the output voltage of the others.

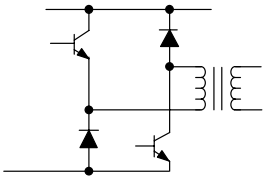
Figure 12–1. Low Power Popular (20 to 200 W) Converter Configurations



(a) Flyback (Clamp Winding is Optional)



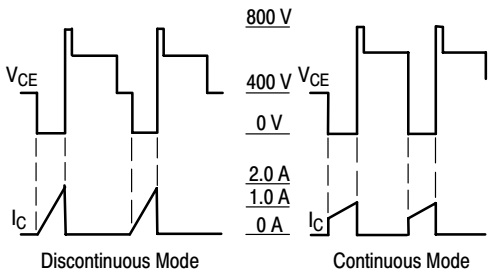
(b) Forward (Clamp Winding is Necessary)



(c) Two Transistor Forward or Flyback (Clamp Winding is not Needed)

A 120/220 Vac flyback design requires transistors that block twice the peak line plus transients or about 1.0 kV. ON Semiconductor's MJE13000 and 16000A series with ratings of 750 V to 1000 V are normally used here. These bipolar devices are relatively fast (100 ns) and are typically used in the 20 kHz to 50 kHz operating frequency range. The recent availability of 900 V and 1000 V TMOS FETs allows designers to operate in the next higher range (50 kHz to 80 kHz) and some have even gone as high as 300 kHz with square wave designs and FETs. Faster 1.0 kV bipolar transistors are also planned in the future and will provide another design alternative. The two transistor variations of this circuit, Figure 12–1(c), eliminate the clamp winding and add a transistor and diode to effectively clamp peak transistor voltages to the line. With this circuit a designer can use the faster 400 V to 500 V FET transistors and push operating frequencies considerably higher. There is a cost penalty here over the single transistor circuit due to the extra transistor, diodes and gate drive circuitry.

Figure 12–2. Flyback Transistor Waveforms

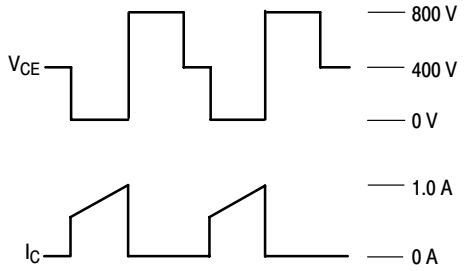


A subtle variation in the method of operation can be applied to the flyback regulator. The difference is referred to as operation in the discontinuous or continuous mode and the waveform diagrams are shown in Figure 12–2. The analysis given in the earlier section on boost regulators dealt strictly with the discontinuous mode where all the energy is dumped from the choke before the transistor turns on again. If the transistor is turned on while energy is still being dumped into the load, the circuit is operating in the continuous mode. This is generally an advantage for the transistor in that it needs to switch only half as much peak current in order to deliver the same power to the load. In many instances, the same transformer transformer may be used with only the gap reduced to provide more inductance. Sometimes the core size will need to be increased to support the higher LI product (2 to 4 times) now required because the inductance must increase by almost 10 times to effectively reduce the peak current by two. In dealing with the continuous mode, it should also be noted that the transistor must now turn on from 500 V to 600 V rather than 400 V level because there no longer is any deadtime to allow the flyback voltage to settle back down in the input voltage level. Generally, it is advisable to have $V_{CEO(sus)}$ ratings comparable to the turn–on requirements except for SMIII where turn–on up to V_{CEV} is permitted.

The flyback converter stands out from the others in its need for a low inductance, high current primary. Conventional E and pot core ferrites are difficult to work with because their permeability is too high even with relatively large gaps (50 to 100 milli–inches). The industry needs something better that will provide permeabilities of 60 to 120 instead of 2000 to 3000 for this application.

The single transistor forward converter is shown in Figure 12–1(b). Although it initially appears very similar to the flyback, it is not. The operating model for this circuit is actually the buck regulator discussed earlier. Instead of storing energy in the transformer and then delivering it to the load, this circuit uses the transformer in the active or forward mode and delivers power to the load while the transistor is on. The additional output rectifier is used as a freewheeling diode for the LC filter and the third winding is actually a reset winding. It generally has the same turns as the primary, (is usually bifilar wound) and does clamp the reset voltage to twice the line. However, its main function is to return energy stored in the magnetizing inductance to the line and thereby reset the core after each cycle of operation. Because it takes the same time to set and reset the core, the duty cycle of this circuit cannot exceed 50%. This also is a very popular low power converter and like the flyback is practically immune from transformer saturation problems. Transistor waveforms shown in Figure 12–3 illustrate that the voltage requirements are identical to the flyback. For the single transistor versions, 400 V turn–on and 1.0 kV blocking devices like the MJE13000 and MJE16000 transistors are required. The two transistor circuit variations shown in Figure 12–1(b) again adds a cost penalty but allows a designer to use the faster 400 V to 500 V devices. With this circuit, operation in the discontinuous mode refers to the time when the load is reduced to a point where the filter choke runs “dry.” This means that choke current starts at and returns to zero during each cycle of operation. Most designers prefer to avoid this type of mode because of higher ripple and noise even though there are no adverse effects on the components themselves. Standard ferrite cores work fine here and in the high power converters as well. In these applications, no gap is used as the high permeability (3000) results in the desirable effect of very low magnetizing current levels. And, zeners or RC clamps may be used to reset the core in lieu of the clamp winding to lower the voltage stress on the switching transistors.

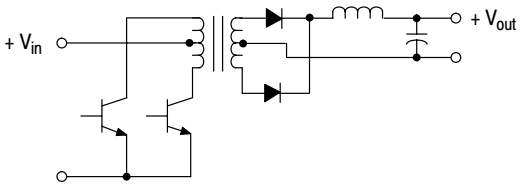
Figure 12–3. Forward Converter Transistor Waveforms



Push–Pull and Bridge Converters

The high power circuits shown in Figures 12–4 to 12–7 all operate the magnetic element in the bipolar or push–pull mode and require 2 to 4 inverter transistors. Because the transformers operate in this mode they tend to be almost half the size of the equivalent single transistor converters and thereby provide a cost advantage over their counterparts at power levels of 200 kW to 1.0 kW.

Figure 12–4. Push–Pull Converter (200 W to 1.0 kW)



The push–pull converter shown in Figure 12–4 is one of the oldest converter circuits around. Its early use was in low voltage inverters such as the 12 Vdc to 120 Vdc power source for recreational vehicles and in dc to dc converters. Because these converters are free running rather than driven and operate from low voltages, transformer saturation problems are minimal. In the high voltage off–line switchers, saturation problems are common and were difficult to solve. The transistors are also subjected to twice the peak line voltage which requires the use of high voltage (1.0 kV) transistors. Both of these drawbacks have tended to discourage designers of off–line switchers from using this configuration until current mode control ICs were introduced. Now these circuits are being looked at with renewed interest.

Push–Pull Switching Power Supplies (100 W to 500 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)}$ = 0.8
- Maximum transistor working current:

$$I_w = \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum transistor working voltage: $V_w = 2 \times V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Push–Pull Configuration

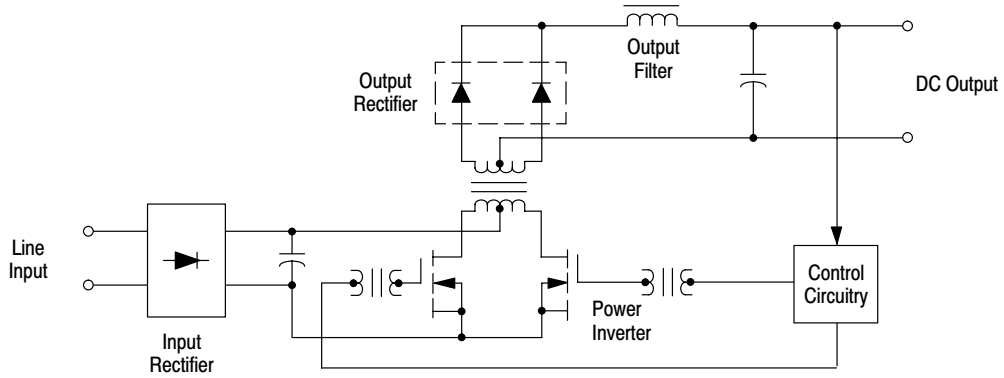


Table 12–2. Push–Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_w) Max Working Voltage (V_w)	 1.2 A 380 V	 0.6 A 750 A	 2.9 A 380 V	 1.6 A 750 V	 5.7 A 380 V	 3.1 A 750 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM2N50 MTP2N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N94 —	 MTM7N45 — MTH7N45	 MTM4N90 — —
Input Rectifiers: Max Working Current (I_w) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.35 A MDA970–5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

Half–Bridge/Full–Bridge Switching Power Supplies (100 W to 500 W/500 W to 1000 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)}$ = 0.8
- Maximum working current:

$$I_w = \frac{2\ P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{2.8\ P_{out}}{V_{in}} \quad \text{(Half–Bridge)}$$

$$= \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}} \quad \text{(Full–Bridge)}$$

- Maximum transistor working voltage: $V_w = V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Half–Bridge Configuration

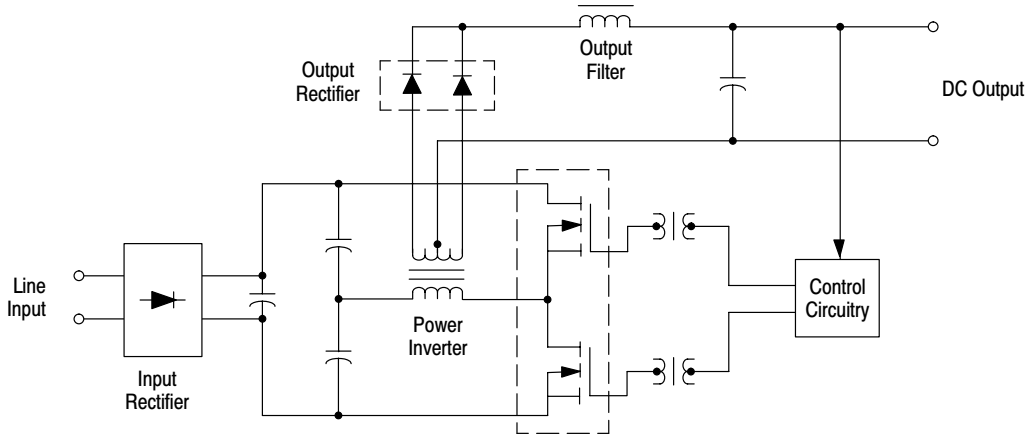


Table 12–3. Half–Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_w) Max Working Voltage (V_w)	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM5N35 MTP3N40 —	 MTM2N45 MTP2N45 —	 MTM8N40 — MTH8N40	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_w) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970–5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

Half and Full–Bridge

The most popular high power converter is the half–bridge (Figure 12–6). It has two clear advantages over the push–pull and became the favorite rather quickly. First, the transistors never see more than the peak line voltage and the standard 400 V fast switchmode transistors that are readily available may be used. And second, and probably even more important, transformer saturation problems are easily minimized by use of a small coupling capacitor (about 2.0 μF to 5.0 μF) as shown above. Because the primary winding is driven in both directions, a full–wave output filter, rather than half, is now used and the core is actually utilized more effectively. Another more subtle advantage of this circuit is that the input filter capacitors are placed in series across the rectified 220 V line which allows them to be used as the voltage doubler elements on a 120 V line. This still allows the inverter transformer to operate from a nominal 320 V bus when the circuit is connected to either 120 V or 220 V. Finally, this topology allows diode clamps across each transistor to contain destructive switching transients. The designer's dream, of course, is for fast transistors that can handle a clamped inductive load line at rated current. And a few (like the MJE16000 series from ON Semiconductor) are beginning to appear on the market. With the improved RBSOA that these transistors feature, less snubbing is required and this improves both the cost and efficiency of these designs.

Figure 12–5. Half–Bridge Converter with Split Windings

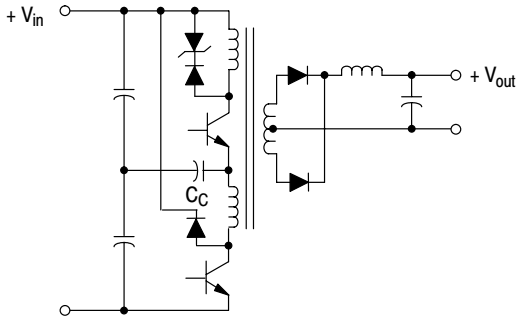
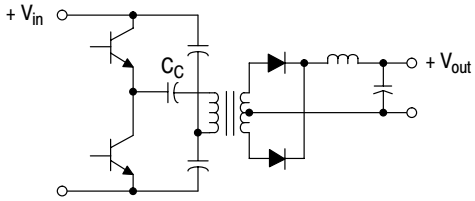


Figure 12–6. Half–Bridge Converter (200 W to 1.0 kW)



Basic Full–Bridge Configuration

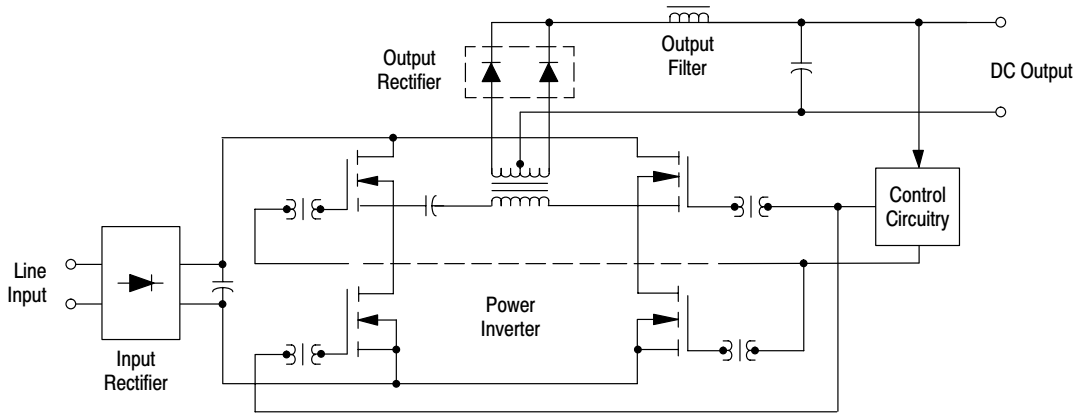


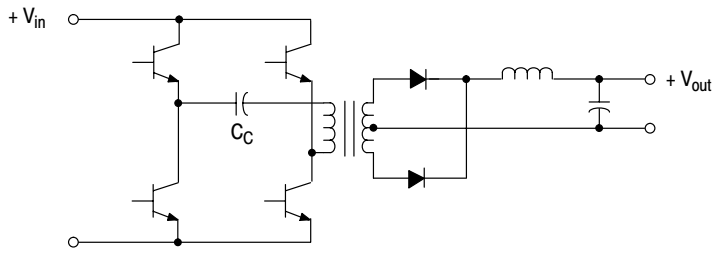
Table 12–4. Full–Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Curren (I_w) Max Working Voltage (V_w)	 5.7 A 190 V	 3.1 A 380 V	 8.6 A 190 V	 4.7 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM8N20 MTP8N20 —	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 MTP4N45 MTH7N45	 MTM15N20 MTP12N20 MTH15N20	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_w) Recommended Types	 4.6 A MDA3506	 2.5 A MDA3510	 7.0 A	 3.8 A	 9.25 A	 5.0 A
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		 MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT		 MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

*More than one device per leg, matched.

The effective current limit of today's low cost TO–218 discrete transistors (250 mil die) is somewhere in the 10 A to 20 A area. Once this limit is reached, the designer generally changes to the full–bridge configurations shown in Figure 12–7. Because full line rather than half is applied to the primary winding, the power out can be almost double that of the half–bridge with the same switching transistors. Power Darlington transistors are a logical choice for higher power control with current, voltage and speed capabilities allowing very high performance and cost effective designs. Another variation of the half–bridge is the split winding circuit, shown in Figure 12–5. A diode clamp can protect the lower transistor but a snubber or zener clamp must still be used to protect the top transistor from switching transients. Because both emitters are at an ac ground point, expensive drive transformers can now be replaced by lower cost capacitively–coupled drive circuits.

Figure 12–7. Full–Bridge Converter (200 W to 1.0 kW)



SECTION 13
SWITCHING REGULATOR DESIGN EXAMPLES

In addition to the application materials in this data book, ON Semiconductor publishes several application notes which contain basic information on the design of power supplies using a variety of ON Semiconductor Analog ICs. AN920 describes in detail the principles of operation of the MC34063A and μA78S40 Switching Regulator Subsystems. Several converter design examples and numerous applications circuits with test data are included in this application note. The circuit techniques described in this note are also applicable to the MC34163 and MC34165 Power Switching Regulators.

Operating details of the MC34129 Current Mode Switching Regulator Controller, and examples of its use with ON Semiconductor SENSEFET™ products, are provided in AN976. The application note AN983 focuses on a 400 W half-bridge power supply design which uses the TL494 PWM control circuit. The TL594 can be used in this same application.

Essentially all of the data sheets for newer power supply control and supervisory circuits include extensive applications information with test conditions and performance results. Many data sheets also include printed circuit board layouts for some key applications so that the designer can evaluate the integrated circuits in an actual power supply. This data book presents all data sheets in their entirety so that the applications information is readily available for each device.

SECTION 14

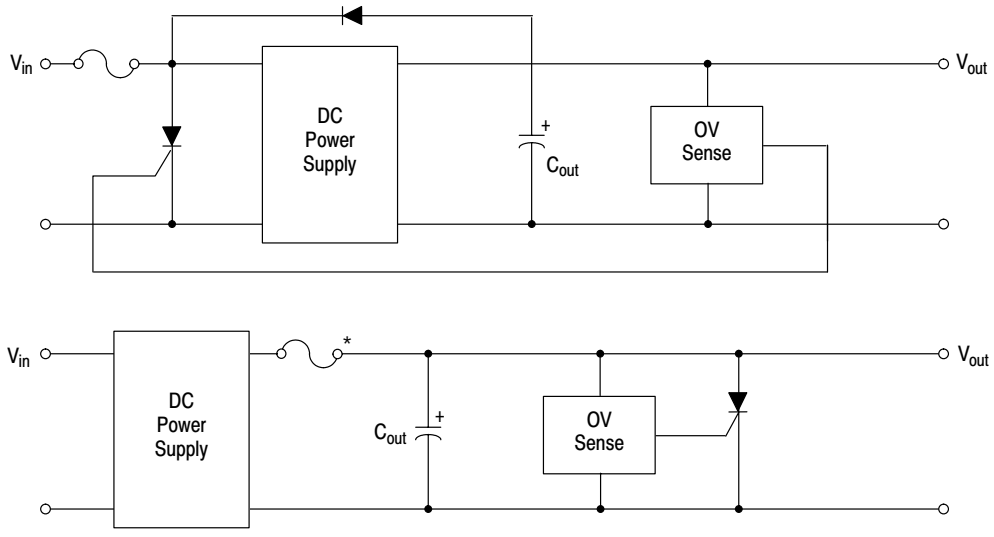
POWER SUPPLY SUPERVISORY AND PROTECTION CONSIDERATIONS

The use of SCR crowbar overvoltage protection (OVP) circuits has been, for many years, a popular method of providing protection from accidental overvoltage stress for the load. In light of the recent advances in LSI circuitry, this technique has taken on added importance. It is not uncommon to have several hundred dollars worth of electronics supplied from a single low voltage supply. If this supply were to fail due to component failure or other accidental shorting of higher voltage supply busses to the low voltage bus, several hundred dollars worth of circuitry could literally go up in smoke. The small additional investment in protection circuitry can easily be justified in such applications.

A. The Crowbar Technique

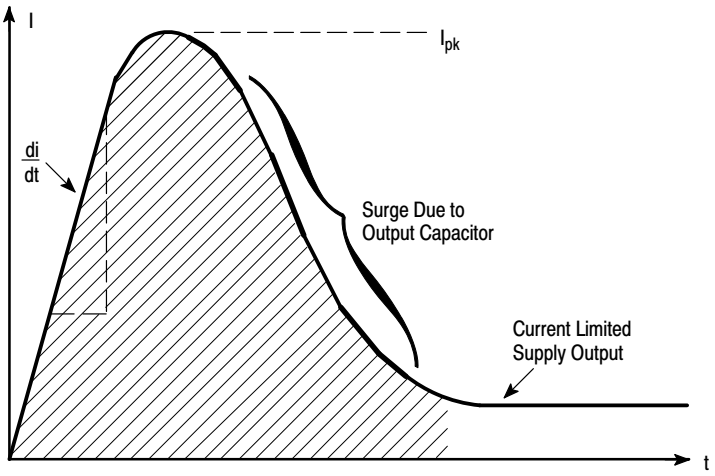
One of the simplest and most effective methods of obtaining overvoltage protection is to use a “crowbar” SCR placed across the equipment’s dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the dc supply when an overvoltage condition is detected. Typical circuit configurations for this circuit are shown on Figure 14–1. This method is very effective in eliminating the destructive overvoltage condition. However, the effectiveness is lost if the OVP circuitry is not reliable.

Figure 14–1. Typical Crowbar OVP Circuit Configurations



*Needed if supply not current–limited.

Figure 14–2. Crowbar SCR Surge Current Waveform



B. SCR Considerations

Referring to Figure 14–1, it can easily be seen that, when activated, the crowbar SCR is subjected to a large current surge from the filter and output capacitors. This large current surge, illustrated in Figure 14–2, can cause SCR failure or degradation by any one of three mechanisms: di/dt, peak surge current, or I2 t. In many instances the designer must empirically determine the SCR and circuit elements which will result in reliable and effective OVP operation. To aid in the selection of devices for this application, ON Semiconductor has characterized several devices specifically for crowbar applications. A summary of these specifications and a selection guide for this application is shown in Table 14–1. This significantly reduces the amount of empirical testing that must be done by the designer. A good understanding of the factors that influence the SCR's di/dt and surge current capability will greatly simplify the total circuit design task.

Table 14–1. Crowbar SCRs

Device Type**	Peak Discharge Current*	di/dt*
MCR67	300 A	75 A/μs
MCR68	300 A	75 A/μs
MCR69	750 A	100 A/μs
MCR70	850 A	100 A/μs
MCR71	1700 A	200 A/μs

* tw = 1.0 μs, exponentially decaying

** All devices available with 25, 50, and 100 V ratings

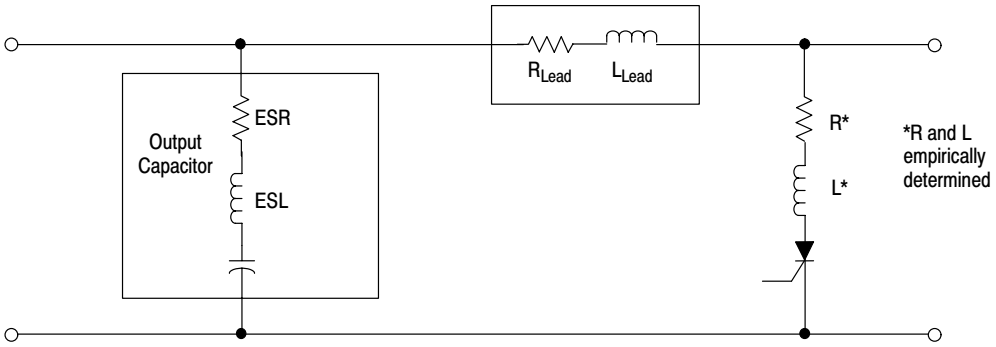
1. di/dt — As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities, depending upon the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum di/dt in phase control SCRs of less than 50 A rms rating might be 200 A/μs, assuming a gate current of five times IGT and <1.0 μs rise time. If having done this, a di/dt problem still exists, the designer can also decrease the di/dt of the current saveform by adding inductance in series with

the SCR, as shown in Figure 14–3. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage, and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current — If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance, see Figure 14–3) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

Figure 14–3. Circuit Elements Affecting SCR Surge & di/dt



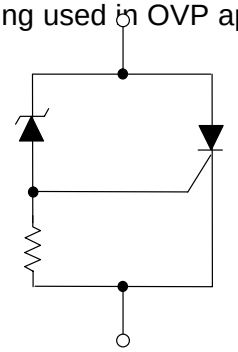
(For additional information on SCRs in crowbar applications refer to *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, ON Semiconductor AN789).

C. The Sense and Drive Circuit

In order to maximize the crowbar SCR's di/dt capability, it should receive a fast rise time high–amplitude gate–drive signal. This must be one of the primary factors considered when selecting the sensing and drive circuitry. Also important is the sense circuitry's noise immunity.

Noise immunity can be a major factor in the selection of the sense circuitry employed. If the sensing circuit has low immunity and is operated in a noisy environment, nuisance tripping of the OVP circuit can occur on short localized noise spikes, which would not normally damage the load. This results in excessive system down time. There are several types of sense circuits presently being used in OVP applications. These can be classified into three types: zener, discrete, and "723."

Figure 14–4. The Zener Sense Circuit



NO!

1. The Zener Sense Circuit — Figure 14–4 shows the use of a zener to trigger the crowbar SCR. This method is NOT recommended since it provides very poor gate drive and greatly decreases the SCR's di/dt handling capability, especially since the SCR steals its own very necessary gate drive as it turns on. Additionally, this method does not allow the trip point to be adjusted except by zener replacement.

2. The Discrete Sense Circuit — A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 14–5. While overcoming the disadvantages of the zener sense circuit, this technique requires many components and is more costly. In addition, this method is not particularly noise immune and often suffers from nuisance tripping.

3. The “723” Sense Circuit — By using an integrated circuit voltage regulator, such as the industry standard “723” type, a considerable reduction in component count can be achieved. This is illustrated in Figure 14–6. Unfortunately, this technique is not noise immune, and suffers an additional disadvantage in that it must be operated at voltages above 9.5 V.

Figure 14–5. The Discrete Sense Circuit

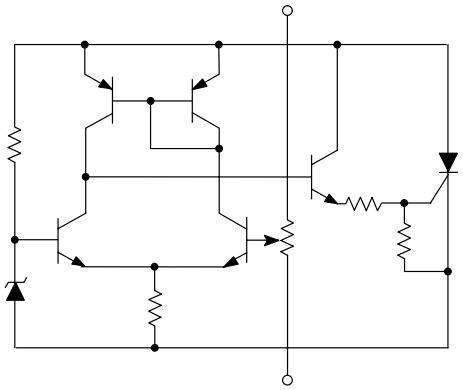
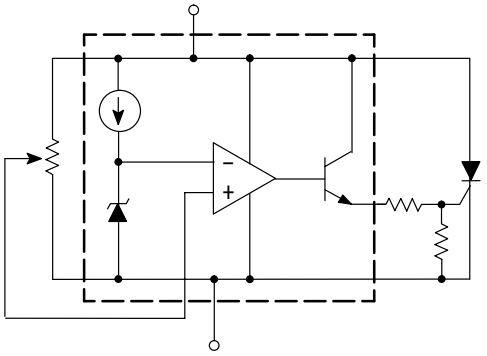


Figure 14–6. The “723” Sense Circuit



4. The MC3423 — To fill the need for a low cost, low complexity method of implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, an IC has been developed for use as an OVP sense and drive circuit, the MC3423.

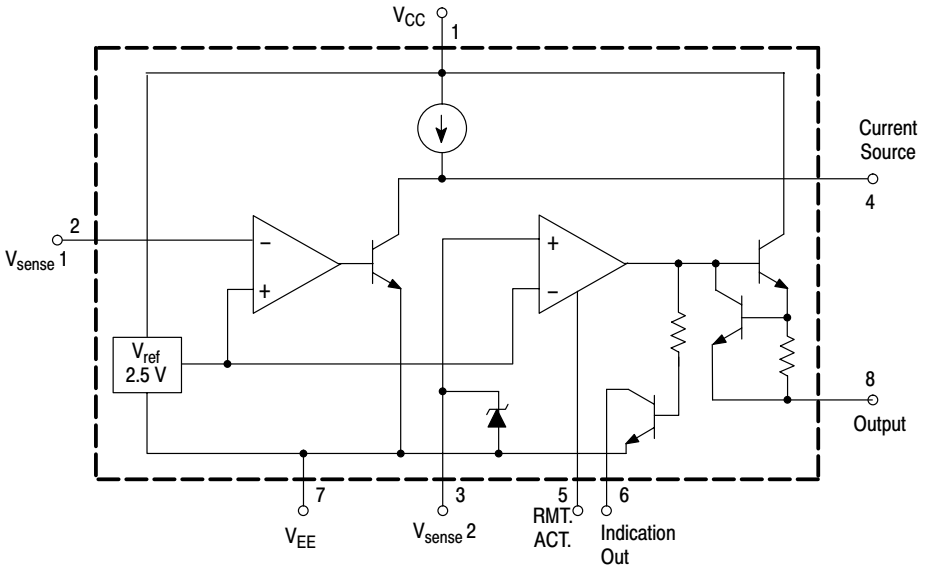
The MC3423 was designed to provide output currents of up to 300 mA with a 400 mA/μs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its features include:

1. Operation off 4.5 V to 40 V supply voltages.
2. Adjustable low temperature coefficient trip point.
3. Adjustable minimum overvoltage duration before actuation to reduce nuisance tripping in noisy environments.
4. Remote activation input.
5. Indication output.

5. Block Diagram — The block diagram of the MC3423 is shown in Figure 14–7. It consists of a stable 2.6 V reference, two comparators and a high current output. This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on Pin 3 or by a TTL/5.0 V CMOS high logic level on the remote activation input, Pin 5.

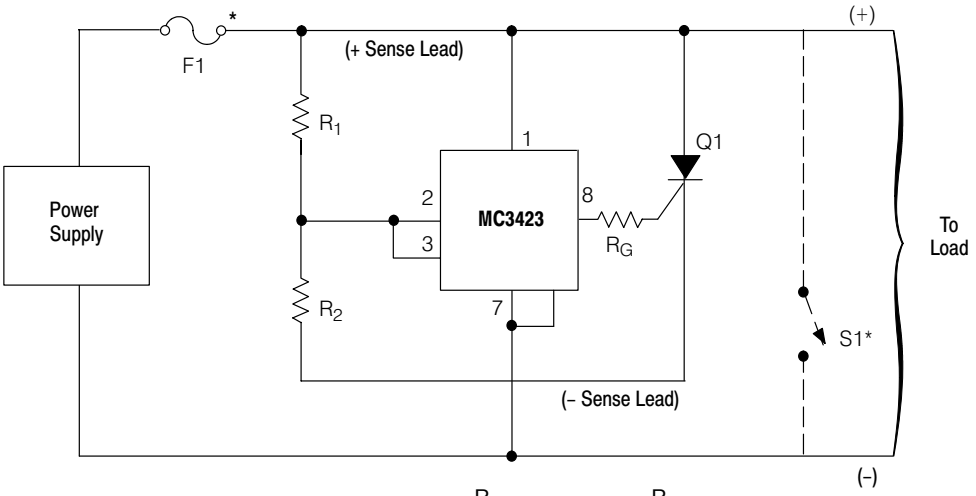
The circuit also has a comparator–controlled current source which can be used in conjunction with and external timing capacitor to set a minimum overvoltage duration (0.5 μs to 1.0 ms) before actuation occurs. This feature allows the OVP circuit to operate in noisy environments without nuisance tripping.

Figure 14–7. MC3423 Block Diagram



6. Basic Circuit Configuration — The basic circuit configuration of the MC3423 OVP is shown in Figure 14–8. In this circuit the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R_1 and R_2. Their values can be determined by the equations given in Figure 14–8 or by the graph shown in Figure 14–9. The switch (S1) shown in Figure 14–8 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current–limited supply is used a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

Figure 14–8. MC3423 Basic Circuit Configuration



$$V_{trip} = V_{ref} \left(1 + \frac{R_1}{R_2}\right) \approx 2.6\ V \left(1 + \frac{R_1}{R_2}\right)$$

$R_2 \leq 10\ k\Omega$ for minimum drift

*Needed if supply is not current–limited

7. MC3423 Programmable Configuration — In many instances, MC3423 OVP will be used in a noisy environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load,

MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 14–10 is used.

Here a capacitor is connected from Pin 3 and Pin 4 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition (t_D) which is necessary to trip the OVP. The value of C_D can be found from Figure 14–11. The circuit operates in the following manner: when V_{CC} rises above the trip point set by R_1 and R_2, the internal current source begins charging the capacitor, C_D, connected to Pins 3 and 4. If the overvoltage condition remains present long enough for the capacitor voltage, V_{CD} to reach V_{ref}, the output is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

8. Indication Output — An additional output for use as an indicator of OVP activation is provided by the MC3423. This output (Pin 6) is an open–collector transistor which saturates when the MC3423 OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 14–10. This output can be used to clock an edge triggered flip–flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

Figure 14–9. R_1 versus Trip Voltage for the MC3423 OVP

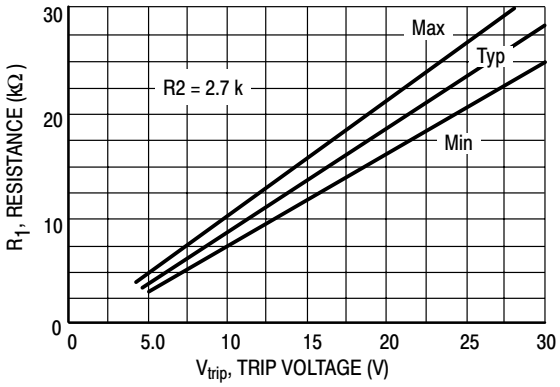
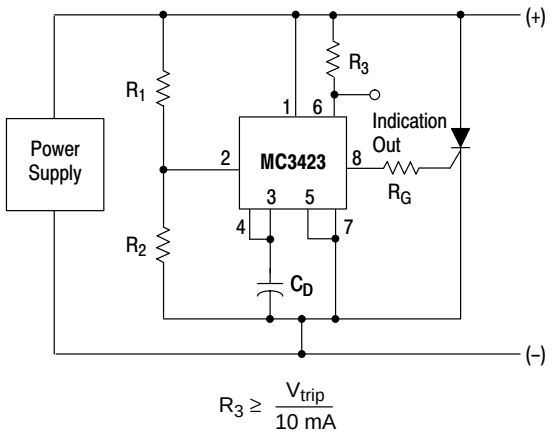


Figure 14–10. MC3423 Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping



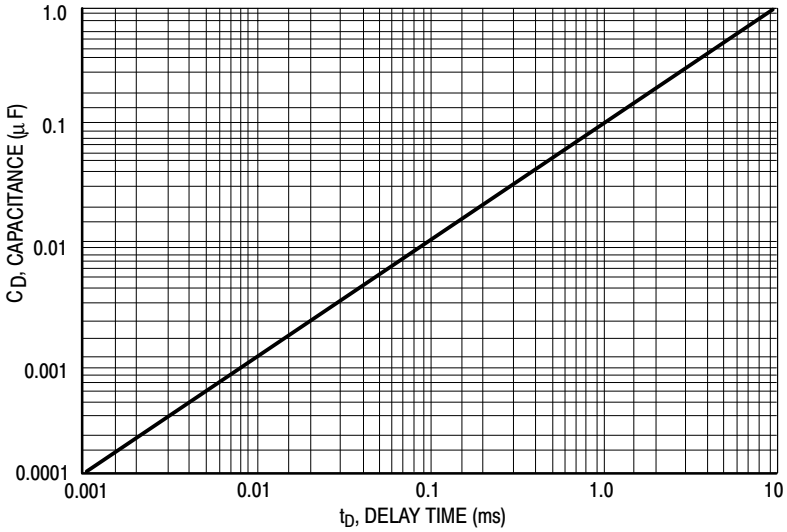
9. Remote Activation Input — Another feature of the MC3423 is its Remote Activation Input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.7 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present.

This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the Indication Output of one MC3423 can be used to activate another MC3423, if a single transistor inverter is used to interface the former's Indication Output to the latter's Remote Activation Input.

D. MC3425 Power Supply Supervisory Circuit

In addition to the MC3423 a second IC, the MC3425 has been developed. Similar in many respects to the MC3423, the MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 14–12. The Overvoltage (OV) and Undervoltage (UV) Input Comparators are both referenced to an internal 2.5 V regulator. The UV Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_{HRH} = 12.5 \times 10^{-6} R_H$.

Figure 14–11. C_D versus Minimum Overvoltage Duration, t_D for The MC3423 OVP



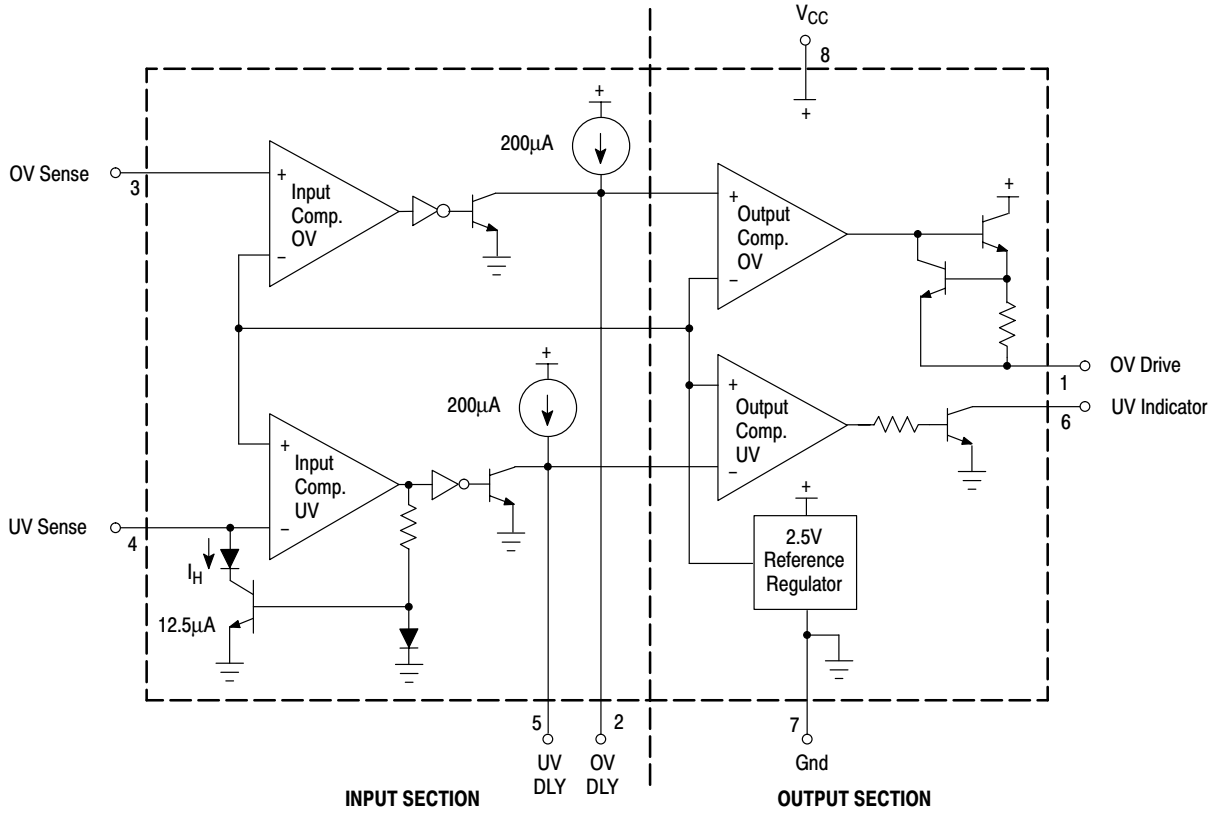
Separate Delay pins (OV DLY, UV DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non–inverting inputs of the OV and UV Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 14–13 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non–inverting input is less than the inverting input. The sink current $I_{DLY(sink)}$ capability of the Delay pins is ≥1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

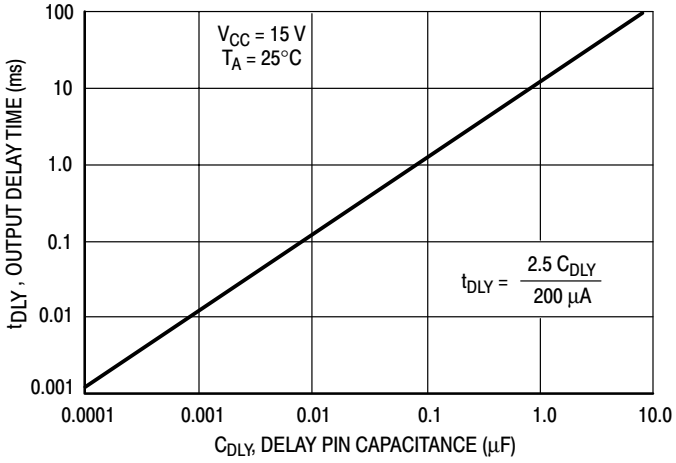
The Overvoltage Drive Output is a current–limited emitter–follower capable of sourcing 300 mA at a turn–on slew rate of 2.0 A/μs, ideal for driving crowbar SCRs. The Undervoltage Indicator Output is an open–collector NPN transistor, capable of sinking 30 mA to provide sufficient drive for LEDs, small relays or shutdown circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded. The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic devices.

Figure 14–12. Block Diagram



Note: All voltages and currents are nominal.

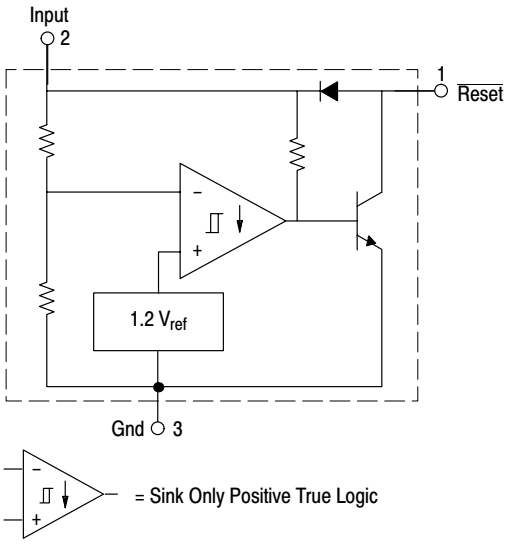
Figure 14–13. Output Delay Time versus Delay Capacitance



E. MC34064 and MC34164 Series

The MC34064 and MC34164 series are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits, taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.



Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment. The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.

REFERENCES

1. *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, ON Semiconductor AN789. **(Out of Print)**
2. *Semiconductor Considerations for DC Power Supply SCR Crowbar Circuits*, Henry Wurzburg, Third National Sold–State Power Conversion Conference, June 25, 1976.
3. *Is a Crowbar Enough?* Willis C. Pierce Jr., Hewlett–Packard, Electronic Design 20, Sept. 27, 1974.
4. *Transient Thermal Response — General Data and Its Use*, Bill Roehr and Brice Shiner, ON Semiconductor AN569. **(Out of Print)**

SECTION 15
HEATSINKING

A. The Thermal Equation

A necessary and primary requirement for the safe operation of any semiconductor device, whether it be an IC or a transistor, is that its junction temperature be kept below the specified maximum value given on its data sheet. The operating junction temperature is given by:

$$T_J = T_A + P_D \theta_{JA} \quad (15.1)$$

where: T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
θ_{JA} = thermal resistance from junction–to–ambient air (°C/W)

The junction–to–ambient thermal resistance (θ_{JA}) in Equation (15.1), can be expressed as a sum of thermal resistances as shown below:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (15.2)$$

where: θ_{JC} = junction–to–case thermal resistance
θ_{CS} = case–to–heatsink thermal resistance
θ_{SA} = heatsink–to–ambient thermal resistance

Equation (15.2) applies only when an external heatsink is used. If no heatsink is used, θ_{JA} is equal to the device package θ_{JA} given on the data sheet.

θ_{JC} depends on the device and its package (case) type, while θ_{SA} is a property of the heatsink and θ_{CS} depends on the type of package/heatsink interface employed. Values for θ_{JC} and θ_{SA} are found on the device and heatsink data sheets, while θ_{CS} is given in Table 15–1.

Table 15–1. θ_{CS} For Various Packages & Mounting Arrangements

	θ_{CS}			
	Metal–to–Metal*		Using an Insulator*	
Case	Dry	With Heatsink Compound	With Heatsink Compound	Type
TO–204	0.5°C/W	0.1°C/W	0.36°C/W 0.28°C/W	3 mil MICA Anodized Aluminum
TO–220	1.2°C/W	1.0°C/W	1.6°C/W	2 mil MICA

*Typical values; heatsink surface should be free of oxidation, paint, and anodization

Examples showing the use of Equations (15.1) and (15.2) in thermal calculations are as follows:

Example 1: Find required heatsink θ_{SA} for an MC7805CT, given:

$$T_{J(max)} \text{ (desired)} = +125°C$$
$$T_{A(max)} = +70°C$$
$$P_D = 2.0 \text{ W}$$

Mounted directly to heatsink with silicon thermal grease at interface:

1. From MC7805CT data sheet, θ_{JC} = 5°C/W
2. From Table 15–1. θ_{CS} = 1.6°C/W
3. Using Equation (15.1) and (15.2), solve for θ_{SA}:

$$\theta_{SA} = \frac{(T_J - T_A)}{P_D} - \theta_{CS} - \theta_{JC}$$

$$\theta_{SA} = \frac{(125 - 70)}{2} - 5.0 - 1.6 \ (\leq 20.9°C/W \text{ required})$$

Example 2: Find the maximum allowable T_A for an unheatsinked MC78L15CT, given:

$$T_{J(max)} \text{ (desired)} = +125°C$$

$$P_D = 0.25 \text{ W}$$

1. From MC78L15CT data sheet, θ_{JA} = 200°C/W
2. Using Equation (15.1), find T_A:

$$T_A = T_j - P_D \theta_{JA}$$
$$= 125 - 0.25 \ (200)$$
$$= +75°C$$

B. Selecting a Heatsink

Usually, the maximum ambient temperature, power being dissipated, the $T_{J(max)}$, and θ_{JC} for the device being used are known. The required θ_{SA} for the heatsink is then determined using Equations (15.1) and (15.2), as in Example 1. The designer may elect to use a commercially available heatsink, or if packaging or economy demands it, design his own.

1. Commercial Heatsinks

As an aid in selecting a heatsink, a representative listing is shown in Table 15–2. This listing is by no means complete and is only included to give the designer an idea of what is available.

Table 15–2. Commercial Heatsink Selection Guide

TO–204AA (TO–3)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
0.3–1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0–3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0–5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3–3–2
5.0–7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver — V3–5–2
7.0–10	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA μP Staver — V1–3, V1–5, V3–3, V3–5, V3–7
10–25	Thermalloy — 6013, 6014, 6015, 6103, 6104, 6105, 6117

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Table 15–2. Commercial Heatsink Selection Guide (continued)

TO–204AA (TO–5)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
12 to 20	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A–5
20 to 30	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5–5
30 to 50	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver — F5–5, F6–5
	Wakefield — 204, 205, 208 Thermalloy — 1115, 1129, 2205, 2207, 2209, 2210, 2211, 2226, 2230, 2257, 2260, 2262 Staver — F1–5, F5–5

TO–204AB	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
5.0 to 10	IERC H P3 Series Staver — V3–7–225, V3–7–96
10 to 15	Thermalloy — 6030, 6032, 6034 Staver — V4–3–192, V–5–1
20 to 30	Wakefield — 295 Thermalloy — 6025, 6107
15 to 20	Thermalloy — 6106 Staver — V4–3–128, V6–2

TO–226AA (TO–92)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
46	Staver F5–7A, F5–8
50	IERC AUR
57	Staver F5–7D
65	IERC RU
72	Staver F1–8, F2–7
80 to 90	Wakefield 292
85	Thermalloy 2224
DUAL–IN–LINE–PACKAGE ICs	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LIC
60	Wakefield — 650, 651

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Staver Co., Inc.: 41–51 N. Saxon Ave., Bay Shore, NY 11706
IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W. Valley View Ln. Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

2. Custom Heatsink Design

Custom heatsinks are usually either forced air cooled or convection cooled. The design of forced air cooled heatsinks is usually done empirically, since it is difficult to obtain accurate air flow measurements. On the other hand, convection cooled heatsinks can be designed with fairly predictable characteristics. It must be emphasized, however, that any custom heatsink design should be thoroughly tested in the actual equipment configuration to be certain of its performance. In the following sections, a design procedure for convection cooled heatsinks is given.

Obviously, the basic goal of any heatsink design is to produce a heatsink with an adequately low thermal resistance, θ_{SA}. Therefore, a means of determining θ_{SA} is necessary in the design. Unfortunately, a precise calculation method for θ_{SA} is beyond the scope of this book.* However, a first order approximation can be calculated for a convection cooled heatsink if the following conditions are met:

1. The heatsink is a flat rectangular or circular plate whose thickness is smaller than its length or width.
2. The heatsink will not be located near other heat radiating surfaces.
3. The aspect ratio of a rectangular heatsink (length:width) is not greater than 2:1.
4. Unrestricted convective air flow.

For the above conditions, the heatsink thermal resistance can be approximated by:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(Fchc + \in Hr)} \quad (°C/W) \tag{15.3}$$

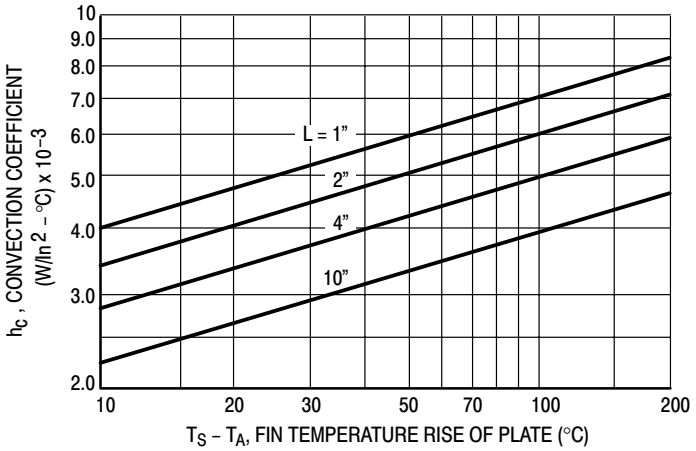
where: A = area of the heatsink surface
η = heatsink effectiveness
F_c = convective correction factor
h_c = convection heat transfer coefficient
$\in$ = emissivity
H_r = normalized radiation heat transfer coefficient

The convective heat transfer coefficient, h_c, can be found from Figure 15–1. Note that it is a function of the heatsink fin temperature rise ($T_S - T_A$) and the heatsink significant dimension (L). The fin temperature rise ($T_S - T_A$) is given by:

$$T_S - T_A = \theta_{SA} P_D \tag{15.4}$$

where: T_S = heatsink temperature
T_A = ambient temperature
θ_{SA} = heatsink–to–ambient thermal resistance
P_D = power dissipated

Figure 15–1. Convection Coefficient (h_c)



*If greater precision is desired, or more information on heat flow and heatsinking is sought, consult the references list at the end of this section.

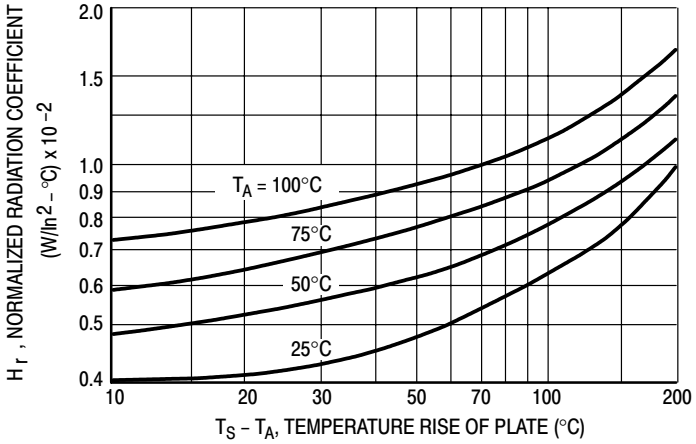
The significant heatsink dimension (L) is dependent on the heatsink shape and mounting place and is given in Table 15–3. The convective correction factor (F_c) is likewise dependent on shape and mounting plane of the heatsink and is also given in Table 15–3.

Table 15–3. Significant Dimension (L) and Correction Factor (F_c) for Convection Thermal Resistance

Surface	Significant Dimension L		Correction Factor F_c	
	Position	L	Position	F_c
Rectangular Plane	Vertical	Height (max 2 ft)	Vertical Plane	1.0
	Horizontal	$\frac{\text{length} \times \text{width}}{\text{length} + \text{width}}$	Horizontal Plane both surfaces exposed	1.35
Circular Plane	Vertical	π / 1 $\times$ diameter	Top only exposed	0.9

The normalized radiation heat transfer coefficient (H_r) is dependent on the ambient temperature (T_A) and the heatsink temperature rise ($T_S - T_A$) given by Equation (15.4). H_r can be determined from Figure 15–2.

Figure 15–2. Normalized Radiation Coefficient (H_r)



The emissivity ($\in$) can be found in Table 15–4 for various heatsink surfaces.

Table 15–4. Typical Emissivities of Common Surfaces

Surface	Emissivity ($\in$)
Alodine on Aluminum	0.15
Aluminum, Anodized	0.7 to 0.9
Aluminum, Polished	0.05
Copper, Polished	0.07
Copper, Oxidized	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85 to 0.91
Oil Paints (any color)	0.92 to 0.96
Varnish	0.89 to 0.93

Finally, the heatsink efficient (η) can be found from the nomograph of Figure 15–3. Use of the nomograph is as follows:

a) Find $h_T = Fchc + \in H_r$ from Figures 15–1, 15–2 and Tables 15–3 and 15–4, and locate this point on the nomograph.

b) Draw a line from h_T through chosen heatsink fin thickness (x) to find α.

c) Determine D for the heatsink shape as given in Figure 15–4 and draw a line from this point through α, which was found in (b), to determine η.

d) If power dissipating element is not located at heatsink's center of symmetry, multiply η by 0.7 (for vertically mounted plates only).

Note that in order to calculate θ_{SA} from Equation (15.3), it is necessary to know the heatsink size. Therefore, in order to arrive at a suitable heatsink design, a trial size is selected, its θ_{SA} evaluated, and the original size reduced or enlarged as necessary. This process is iterated until the smallest heatsink is obtained that has the required θ_{SA}. The following design example is given to illustrate this procedure.

Figure 15–3. Fin Effectiveness Nomogram for Symmetrical Flat, Uniformly Thick Fins

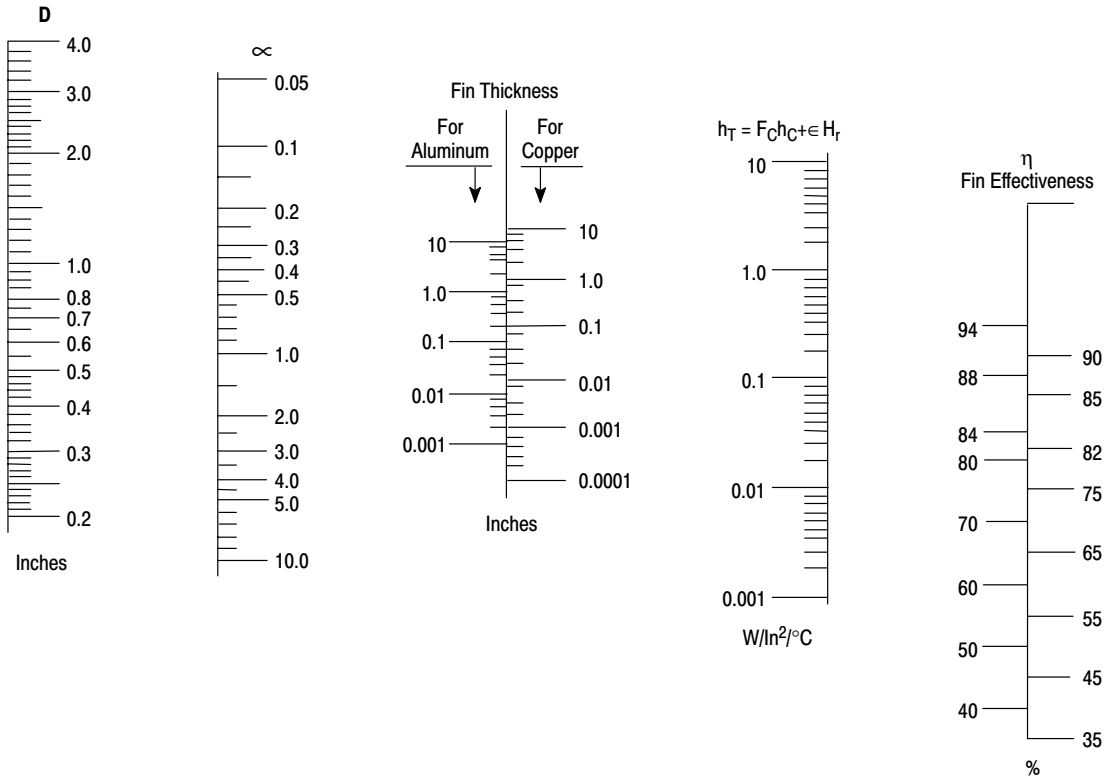


Figure 15–4. Determination of D for Use in η Nomograph of Figure 15–3

Heatsink Design Example

Design a flat rectangular heatsink for use with a horizontally mounted power device on a PC board, given the following:

1. Heatsink θ_{SA} = 25°C/W
2. Power to be dissipated, P_D = 2.0 W
3. Maximum ambient temperature, T_A = 50°C
4. Heatsink to be constructed from 1/8″ (0.125″) thick anodized aluminum.
   a) First, a trial heatsink is chosen: 2″ × 3″ (experience will simplify this selection and reduce the number of necessary iterations.)
   b) The factors in Equation (15.3) are evaluated by using the Figures and Tables given:

$$A = 2'' \times 3'' = 6 \text{ sq. in.}$$
$$L = 6/5'' = 1.2 \text{ in. (from Table 15–3)}$$
$$T_S - T_A = 50°C \text{ (from Figure 15–4)}$$
$$h_c = 5.8 \times 10^{-3} \text{ W/in}^2 - °C \text{ (from Figure 15–1)}$$
$$F_c = 0.9 \text{ (from Table 15–3)}$$
$$H_r = 6.1 \times 10^{-3} \text{ W/in}^2 - °C \text{ (from Figure 15–2)}$$
$$\in = 0.9 \text{ (from Table 15–4)}$$
$$h_T = Fchc + H_{r\in} = 10.7 \times 10^{-3} \text{ W/in}^2 - °C$$
$$\alpha = 0.13 \text{ (from Figure 15–3)}$$
$$D = 1.77 \text{ (from Figure 15–4)}$$
$$\eta > 0.94 \simeq 1 \text{ (from Figure 15–3)}$$

   c) Using Equation (15.3), find θ_{SA}:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(Fchc + \in H_r)} = 16.66°C/W < 25°C/W$$

   d) Since 2″ × 3″ is too large, try 2″ × 2″. Following the same procedure, θ_{SA} is found to be 25°C/W, which exactly meets the design requirements.

SOIC MINIATURE IC PLASTIC PACKAGE

Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(typ)}$$

where: $P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature,
$T_{J(max)}$ = maximum operating junction temperature as listed in the maximum ratings section,
T_A = desired operating ambient temperature,
$R_{\theta JA}$ (typ) = typical thermal resistance junction–to–ambient.

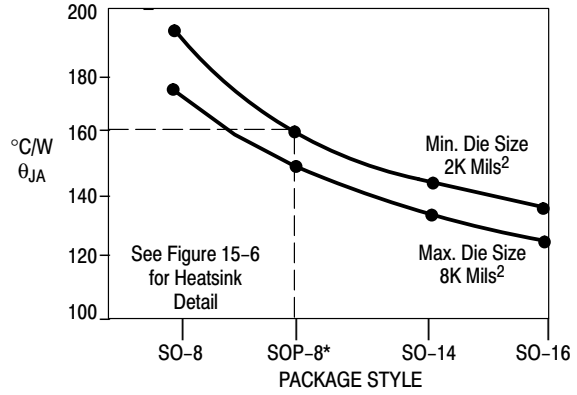
Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 – 40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

THERMAL CHARACTERISTICS OF SOIC PACKAGES

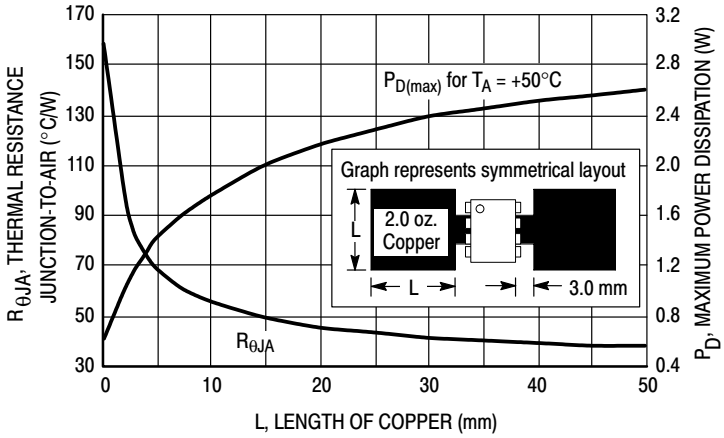
Measurement specimens are solder mounted on a Philips SO test board #7322–078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.

Figure 15–5. Thermal Resistance, Junction–to–Ambient (°C/W)



Data taken using Philips SO test board #7322–078, 80873
*SOP–8 using standard SO–8 footprint — minimum pad size

Figure 15–6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



SOP–8 and SOP–16L Packaged Devices

Several families of voltage regulators and power control ICs have been introduced in surface mounted packages which were developed by the Analog IC Division. The SOP–8 and SOP–16L packages have external dimensions which are identical to the standard SO–8 and SO–16L surface mount devices, but the center four leads of the packages are all connected to the leadframe die flag. This internal modification decreases the package thermal resistance and therefore increases its power dissipation capability. This advantage is fully realized when the package is mounted on a printed circuit board with a single pad for the four center leads. This large area of copper then acts as an external heat spreader, efficiently conducting heat away from the package.

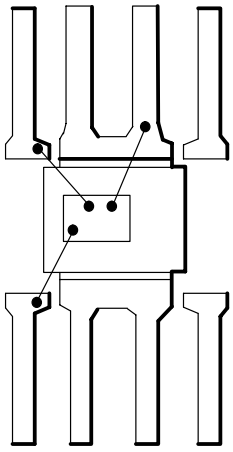
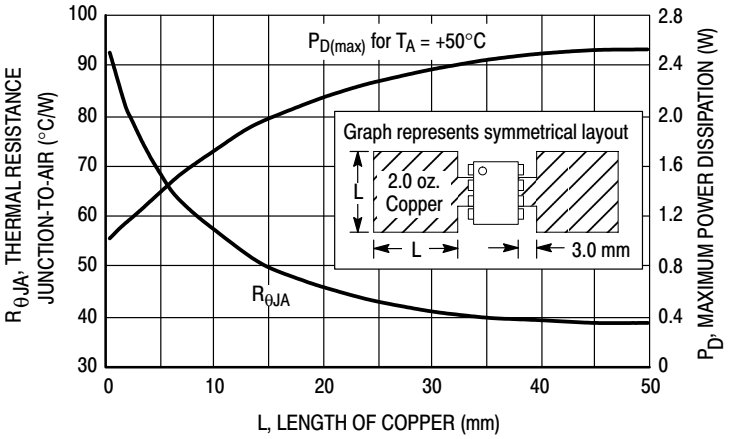


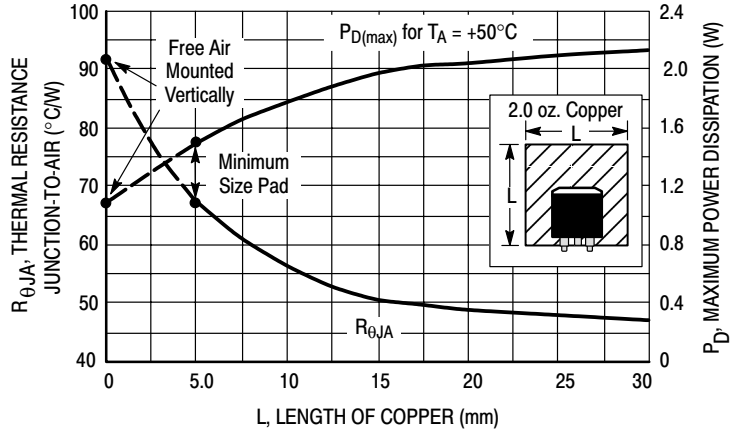
Figure 15–7. SOP–16L Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



THERMAL CHARACTERISTICS OF DPAK AND D^{2}PAK PACKAGE

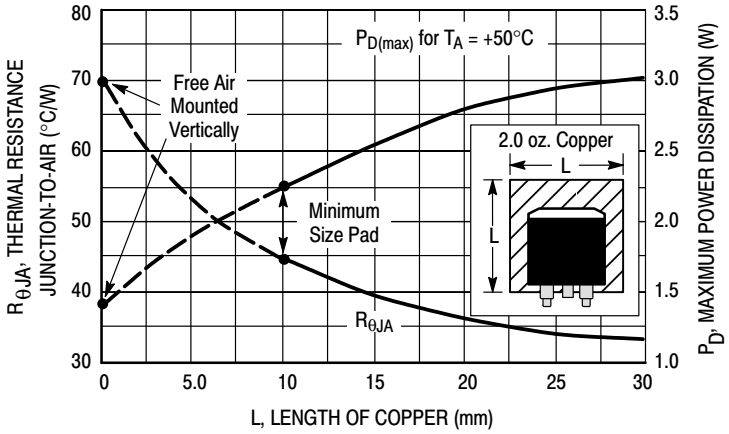
The evaluation was performed using an active device (4900 square mils) mounted on 2.0 ounce copper foil epoxied to a GIO type printed circuit board. Measurements were made in still air and no auxiliary thermal conduction aids were used. The size of a square copper pad was varied, and all measurements were made with the unit mounted as shown in Figure 15–8. The curve shown in Figure 15–8 is a plot of junction–to–air thermal resistance versus the length of the square copper pad in millimeters. This shows that when the DPAK is mounted on a 10 mm $\times$ 10 mm square pad of 2.0 ounce copper it has a thermal resistance which is comparable to a TO–220 device mounted vertically without additional heatsinking.

Figure 15–8. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



The thermal characteristics of the D^{2}PAK are shown in Figure 15–9. The device was mounted on 2.0 oz. copper on an FR4–type P.C. board. The maximum power dissipation was measured with a junction temperature of 150°C.

Figure 15–9. 3–Pin and 5–Pin D^{2}PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



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