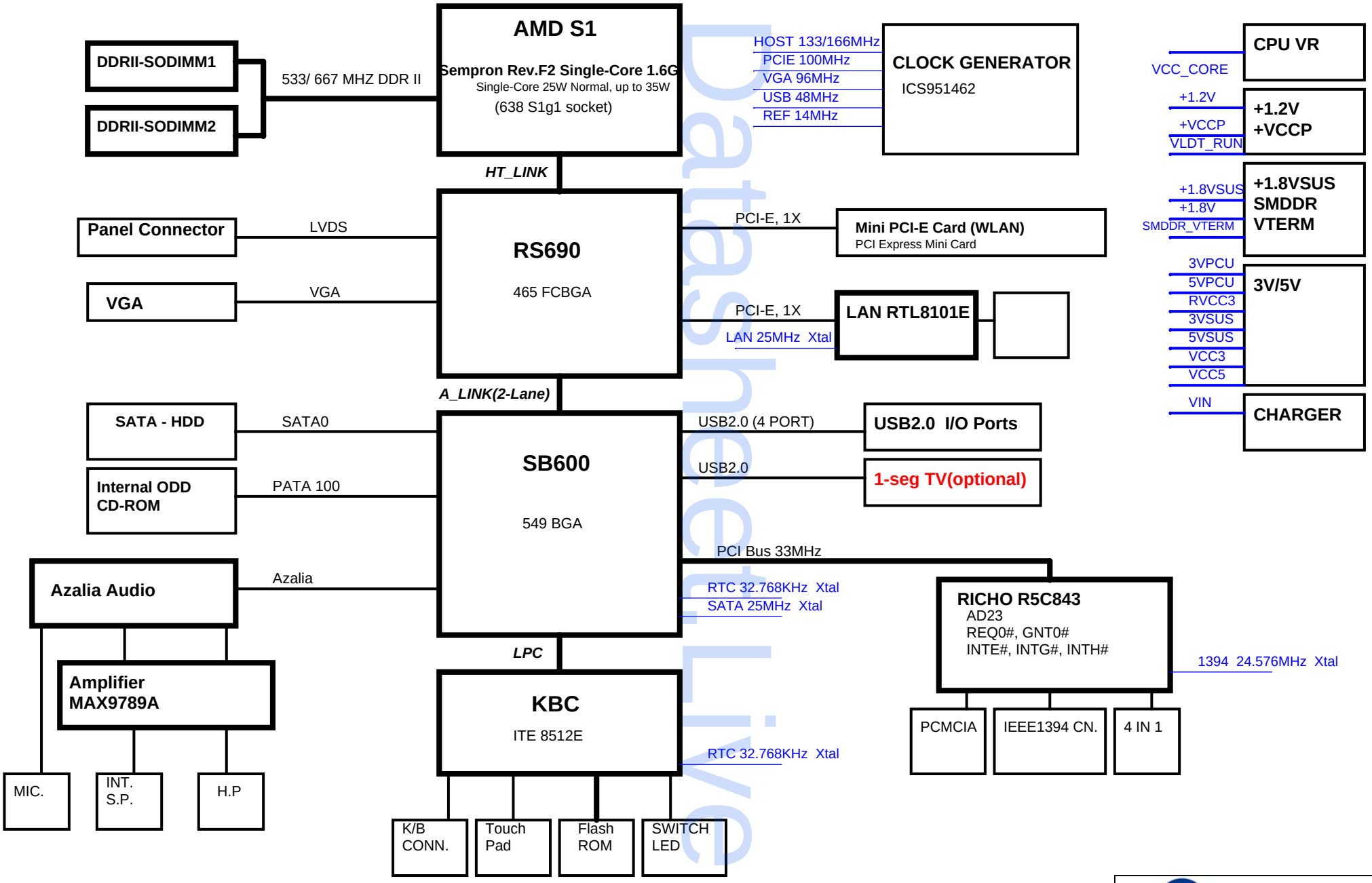
ES23 BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	Block Diagram	D

Date: Friday, October 26, 2007 Sheet 1 of 37

Voltage Rails

Power	Voltage	ON S0~S2	ON S3	ON S4	ON S5	Ctl Signal
15VPCU	15V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
RVCC3	3V	V	V	V		RVCC_ON
RVCC1.8	1.8V	V	V	V		RVCC_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VLDT_RUN	1.2V	V				VLDT_ON

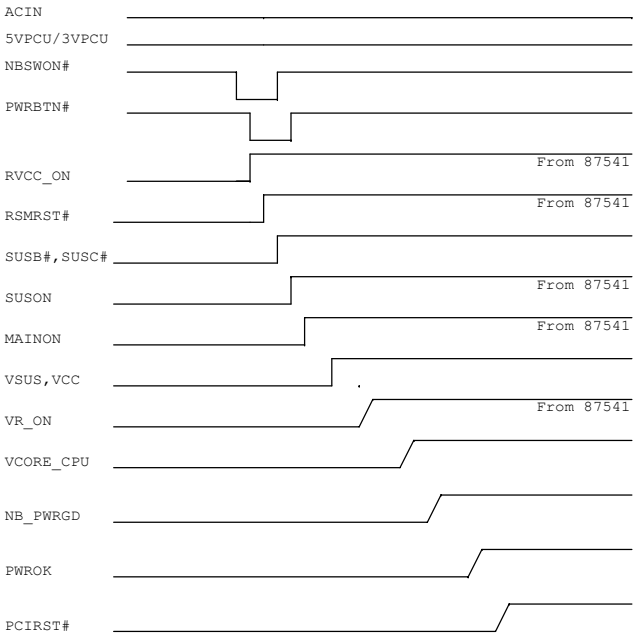
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

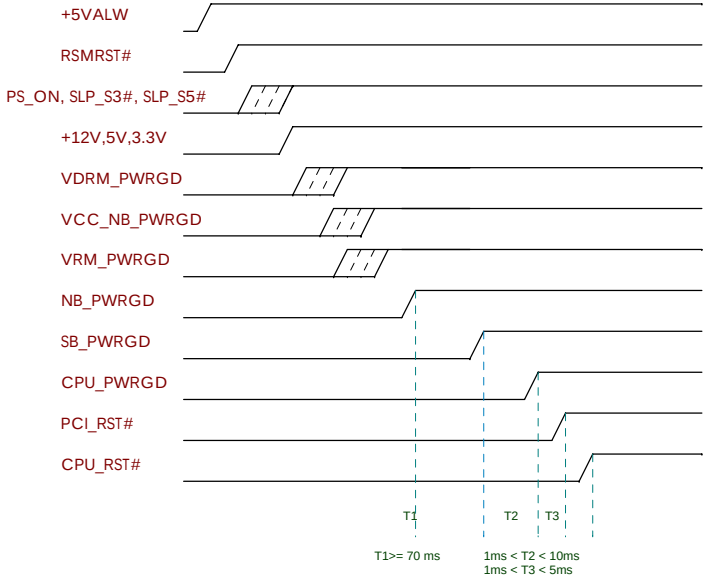
PCI DEVICES IRQ ROUTING

ES2 PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
R5C843	AD23	REQ0# / GNT0#	INT E/F/G

Power On Sequence

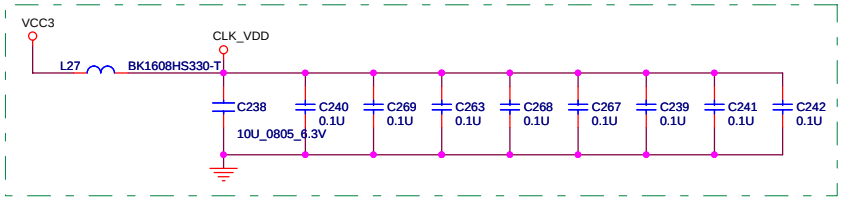


BONEFISH POWER UP SEQUENCE

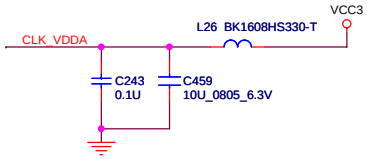


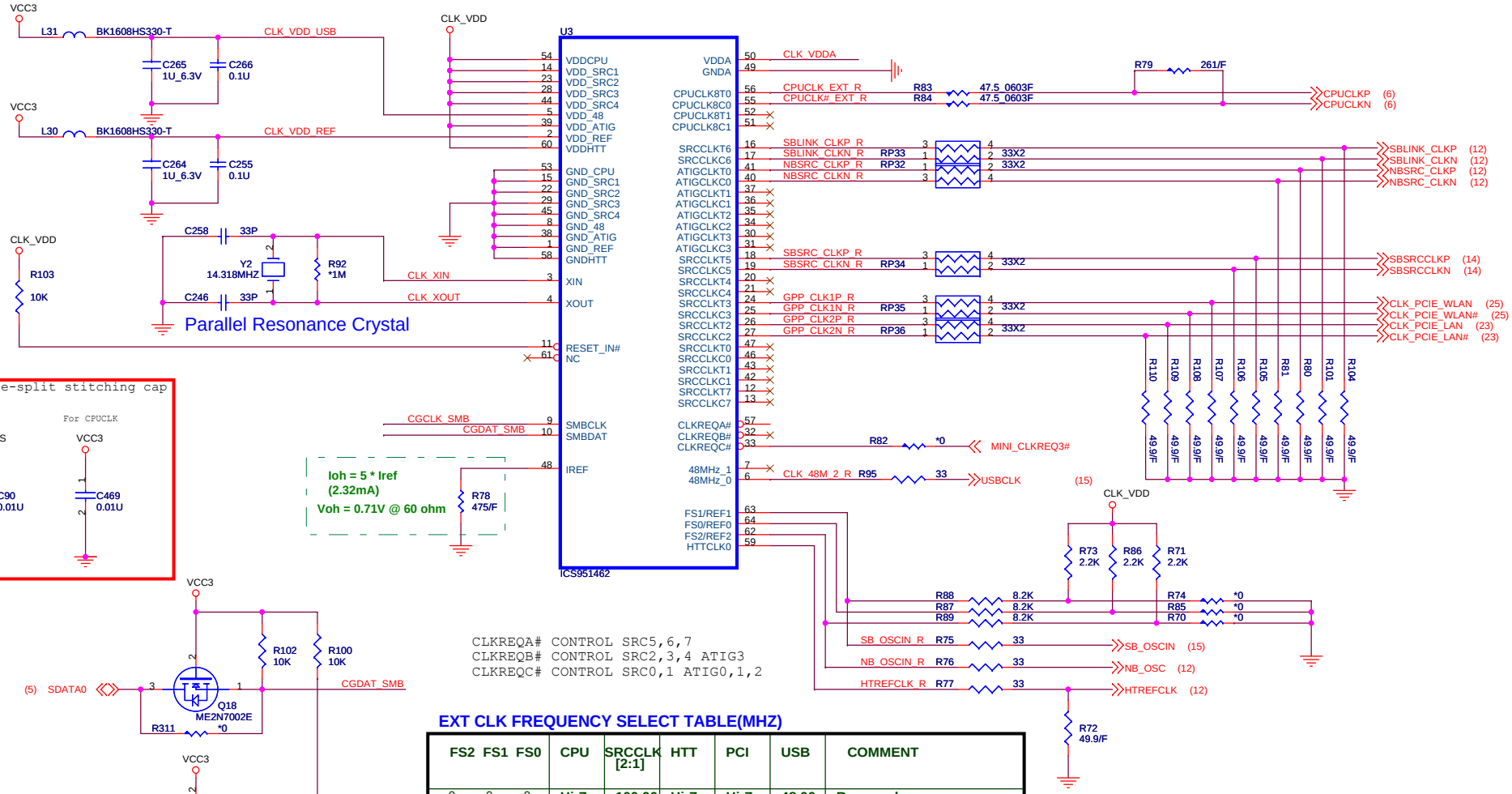
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	System information	D
Date: Friday, October 26, 2007	Sheet 2 of 37	



Put Decoupling Caps close to Clock Fen. power pin

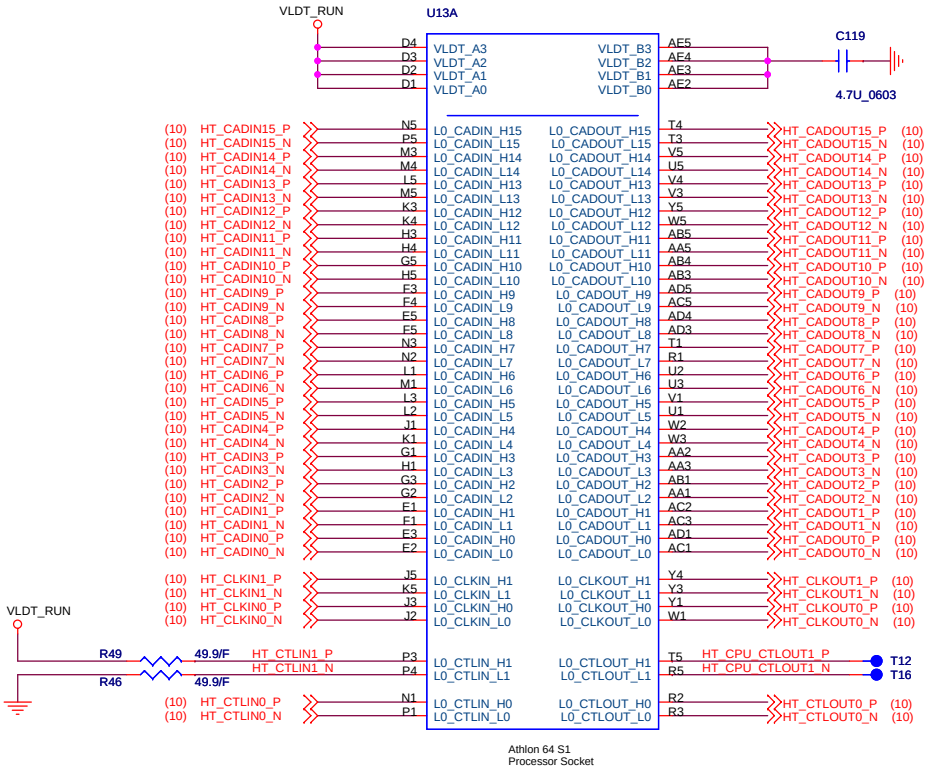


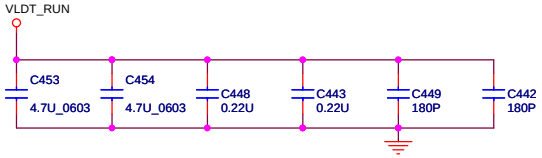


CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation





Quanta Computer Inc.

PROJECT : ES2

Size	Document Number	Rev
	ATHLON64 HT I/F	D

Date: Friday, October 26, 2007 Sheet 4 of 37

Processor DDR2 Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"

1.8VSUS

R48 2K/F

CPU_M_VREF

C142 0.1U

C149 1000P_16V

R44 2K/F

R189 39.2F

R188 39.2F

T8

SMDDR_VTERM

U13B

W17 MEMVREF

VTT_SENSE Y10 VTT_SENSE

M_ZN AE10 MEMZN

M_ZP AE10 MEMZP

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

(8,9) M_A_CS#3 V19 MA0_CS_L3
(8,9) M_A_CS#2 J22 MA0_CS_L2
(8,9) M_A_CS#1 V22 MA0_CS_L1
(8,9) M_A_CS#0 T19 MA0_CS_L0

MA0_CLK_H2 Y16 M_CLKOUT1 (8)
MA0_CLK_L2 AA16 M_CLKOUT1# (8)
MA0_CLK_H1 E16 M_CLKOUT0 (8)
MA0_CLK_L1 F16 M_CLKOUT0# (8)

(8,9) M_B_CS#3 Y26 MB0_CS_L3
(8,9) M_B_CS#2 J24 MB0_CS_L2
(8,9) M_B_CS#1 W24 MB0_CS_L1
(8,9) M_B_CS#0 U23 MB0_CS_L0

MB0_CLK_H2 AF18 M_CLKOUT4 (8)
MB0_CLK_L2 AF17 M_CLKOUT4# (8)
MB0_CLK_H1 A17 M_CLKOUT3 (8)
MB0_CLK_L1 A18 M_CLKOUT3# (8)

(8,9) M_CKE3 H26 MB_CKE1
(8,9) M_CKE2 J23 MB_CKE0
(8,9) M_CKE1 J20 MA_CKE1
(8,9) M_CKE0 J21 MA_CKE0

MB0_ODT1 W23 M_ODT3 (8,9)
MB0_ODT0 W26 M_ODT2 (8,9)
MA0_ODT1 V20 M_ODT1 (8,9)
MA0_ODT0 U19 M_ODT0 (8,9)

(8,9) M_A_A[0..15]

M_A_A15 K19 MA_ADD15
M_A_A14 K20 MA_ADD14
M_A_A13 V24 MA_ADD13
M_A_A12 K24 MA_ADD12
M_A_A11 L20 MA_ADD11
M_A_A10 R19 MA_ADD10
M_A_A9 L19 MA_ADD9
M_A_A8 L22 MA_ADD8
M_A_A7 L21 MA_ADD7
M_A_A6 M19 MA_ADD6
M_A_A5 M20 MA_ADD5
M_A_A4 M24 MA_ADD4
M_A_A3 M22 MA_ADD3
M_A_A2 N22 MA_ADD2
M_A_A1 N21 MA_ADD1
M_A_A0 R21 MA_ADD0

MB_ADD15 J25 M_B_A15
MB_ADD14 J26 M_B_A14
MB_ADD13 W25 M_B_A13
MB_ADD12 L23 M_B_A12
MB_ADD11 L25 M_B_A11
MB_ADD10 U25 M_B_A10
MB_ADD9 L24 M_B_A9
MB_ADD8 M26 M_B_A8
MB_ADD7 L26 M_B_A7
MB_ADD6 N23 M_B_A6
MB_ADD5 N24 M_B_A5
MB_ADD4 N25 M_B_A4
MB_ADD3 N26 M_B_A3
MB_ADD2 P24 M_B_A2
MB_ADD1 P26 M_B_A1
MB_ADD0 T24 M_B_A0

(8,9) M_A_BS#2 K22 MA_BANK2
(8,9) M_A_BS#1 R20 MA_BANK1
(8,9) M_A_BS#0 T22 MA_BANK0

MB_BANK2 K26 M_B_BS#2 (8,9)
MB_BANK1 T26 M_B_BS#1 (8,9)
MB_BANK0 U26 M_B_BS#0 (8,9)

(8,9) M_A_RAS# T20 MA_RAS_L
(8,9) M_A_CAS# U20 MA_CAS_L
(8,9) M_A_WE# U21 MA_WE_L

MB_RAS_L U24 M_B_RAS# (8,9)
MB_CAS_L V26 M_B_CAS# (8,9)
MB_WE_L U22 M_B_WE# (8,9)

DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

To SODIMM socket B (Far)

U13C

(8) M_B_DQ[0..63]

M_B_DQ63 AD11 MB_DATA63
M_B_DQ62 AF11 MB_DATA62
M_B_DQ61 AF14 MB_DATA61
M_B_DQ60 AE14 MB_DATA60
M_B_DQ59 Y11 MB_DATA59
M_B_DQ58 AB11 MB_DATA58
M_B_DQ57 AC12 MB_DATA57
M_B_DQ56 AF13 MB_DATA56
M_B_DQ55 AF15 MB_DATA55
M_B_DQ54 AF16 MB_DATA54
M_B_DQ53 AC18 MB_DATA53
M_B_DQ52 AF19 MB_DATA52
M_B_DQ51 AD14 MB_DATA51
M_B_DQ50 AC14 MB_DATA50
M_B_DQ49 AE18 MB_DATA49
M_B_DQ48 AD18 MB_DATA48
M_B_DQ47 AD20 MB_DATA47
M_B_DQ46 AC20 MB_DATA46
M_B_DQ45 AF23 MB_DATA45
M_B_DQ44 AE24 MB_DATA44
M_B_DQ43 AE20 MB_DATA43
M_B_DQ42 AE20 MB_DATA42
M_B_DQ41 AD22 MB_DATA41
M_B_DQ40 AC22 MB_DATA40
M_B_DQ39 AE25 MB_DATA39
M_B_DQ38 AD26 MB_DATA38
M_B_DQ37 AA25 MB_DATA37
M_B_DQ36 AA26 MB_DATA36
M_B_DQ35 AE24 MB_DATA35
M_B_DQ34 AD24 MB_DATA34
M_B_DQ33 AA23 MB_DATA33
M_B_DQ32 AA24 MB_DATA32
M_B_DQ31 G24 MB_DATA31
M_B_DQ30 G23 MB_DATA30
M_B_DQ29 D26 MB_DATA29
M_B_DQ28 C26 MB_DATA28
M_B_DQ27 G26 MB_DATA27
M_B_DQ26 G25 MB_DATA26
M_B_DQ25 E24 MB_DATA25
M_B_DQ24 F23 MB_DATA24
M_B_DQ23 C24 MB_DATA23
M_B_DQ22 B24 MB_DATA22
M_B_DQ21 C20 MB_DATA21
M_B_DQ20 B20 MB_DATA20
M_B_DQ19 C25 MB_DATA19
M_B_DQ18 D24 MB_DATA18
M_B_DQ17 A21 MB_DATA17
M_B_DQ16 D20 MB_DATA16
M_B_DQ15 D18 MB_DATA15
M_B_DQ14 C18 MB_DATA14
M_B_DQ13 D14 MB_DATA13
M_B_DQ12 C14 MB_DATA12
M_B_DQ11 A20 MB_DATA11
M_B_DQ10 A19 MB_DATA10
M_B_DQ9 A16 MB_DATA9
M_B_DQ8 A15 MB_DATA8
M_B_DQ7 A13 MB_DATA7
M_B_DQ6 D12 MB_DATA6
M_B_DQ5 E11 MB_DATA5
M_B_DQ4 G11 MB_DATA4
M_B_DQ3 B14 MB_DATA3
M_B_DQ2 A14 MB_DATA2
M_B_DQ1 A11 MB_DATA1
M_B_DQ0 C11 MB_DATA0

MA_DATA63 AA12 M_A_DQ63
MA_DATA62 AB12 M_A_DQ62
MA_DATA61 AA14 M_A_DQ61
MA_DATA60 AB14 M_A_DQ60
MA_DATA59 W11 M_A_DQ59
MA_DATA58 Y12 M_A_DQ58
MA_DATA57 AD13 M_A_DQ57
MA_DATA56 AB13 M_A_DQ56
MA_DATA55 AD15 M_A_DQ55
MA_DATA54 AB15 M_A_DQ54
MA_DATA53 AB17 M_A_DQ53
MA_DATA52 Y17 M_A_DQ52
MA_DATA51 Y14 M_A_DQ51
MA_DATA50 W14 M_A_DQ50
MA_DATA49 W16 M_A_DQ49
MA_DATA48 AD17 M_A_DQ48
MA_DATA47 Y18 M_A_DQ47
MA_DATA46 AD19 M_A_DQ46
MA_DATA45 AD21 M_A_DQ45
MA_DATA44 AB21 M_A_DQ44
MA_DATA43 AB18 M_A_DQ43
MA_DATA42 AA18 M_A_DQ42
MA_DATA41 AA20 M_A_DQ41
MA_DATA40 Y20 M_A_DQ40
MA_DATA39 AA22 M_A_DQ39
MA_DATA38 Y22 M_A_DQ38
MA_DATA37 W21 M_A_DQ37
MA_DATA36 W22 M_A_DQ36
MA_DATA35 AA21 M_A_DQ35
MA_DATA34 AB22 M_A_DQ34
MA_DATA33 AB24 M_A_DQ33
MA_DATA32 Y24 M_A_DQ32
MA_DATA31 H22 M_A_DQ31
MA_DATA30 H20 M_A_DQ30
MA_DATA29 E22 M_A_DQ29
MA_DATA28 E21 M_A_DQ28
MA_DATA27 J19 M_A_DQ27
MA_DATA26 H24 M_A_DQ26
MA_DATA25 F22 M_A_DQ25
MA_DATA24 F20 M_A_DQ24
MA_DATA23 C23 M_A_DQ23
MA_DATA22 B22 M_A_DQ22
MA_DATA21 F18 M_A_DQ21
MA_DATA20 E18 M_A_DQ20
MA_DATA19 F20 M_A_DQ19
MA_DATA18 D22 M_A_DQ18
MA_DATA17 C19 M_A_DQ17
MA_DATA16 G18 M_A_DQ16
MA_DATA15 G17 M_A_DQ15
MA_DATA14 C17 M_A_DQ14
MA_DATA13 F14 M_A_DQ13
MA_DATA12 E14 M_A_DQ12
MA_DATA11 H17 M_A_DQ11
MA_DATA10 E17 M_A_DQ10
MA_DATA9 E15 M_A_DQ9
MA_DATA8 H15 M_A_DQ8
MA_DATA7 E13 M_A_DQ7
MA_DATA6 C13 M_A_DQ6
MA_DATA5 H12 M_A_DQ5
MA_DATA4 H11 M_A_DQ4
MA_DATA3 G14 M_A_DQ3
MA_DATA2 H14 M_A_DQ2
MA_DATA1 F12 M_A_DQ1
MA_DATA0 G12 M_A_DQ0

(8) M_B_DM[0..7]

M_B_DM7 AD12 MB_DM7
M_B_DM6 AC16 MB_DM6
M_B_DM5 AE22 MB_DM5
M_B_DM4 AB26 MB_DM4
M_B_DM3 E25 MB_DM3
M_B_DM2 A22 MB_DM2
M_B_DM1 B16 MB_DM1
M_B_DM0 A12 MB_DM0

MA_DM7 Y13 M_A_DM7
MA_DM6 AB16 M_A_DM6
MA_DM5 Y19 M_A_DM5
MA_DM4 AC24 M_A_DM4
MA_DM3 E24 M_A_DM3
MA_DM2 E19 M_A_DM2
MA_DM1 C15 M_A_DM1
MA_DM0 E12 M_A_DM0

(8) M_B_DQS[0..7]

M_B_DQS0 M_B_DQS7 AE12 MB_DQS_H7
M_B_DQS1 M_B_DQS#7 AE12 MB_DQS_L7
M_B_DQS2 M_B_DQS6 AE16 MB_DQS_H6
M_B_DQS3 M_B_DQS#6 AD16 MB_DQS_L6
M_B_DQS4 M_B_DQS5 AF21 MB_DQS_H5
M_B_DQS5 M_B_DQS#5 AF22 MB_DQS_L5
M_B_DQS6 M_B_DQS4 AC25 MB_DQS_H4
M_B_DQS7 M_B_DQS#4 AC26 MB_DQS_L4
M_B_DQS3 F26 MB_DQS_H3
M_B_DQS#3 F26 MB_DQS_L3
M_B_DQS2 A24 MB_DQS_H2
M_B_DQS#2 A23 MB_DQS_L2
M_B_DQS1 D16 MB_DQS_H1
M_B_DQS#1 C16 MB_DQS_L1
M_B_DQS0 C12 MB_DQS_H0
M_B_DQS#0 B12 MB_DQS_L0

MA_DQS_H7 W12 M_A_DQS7 M_A_DQS0
MA_DQS_L7 W13 M_A_DQS#7 M_A_DQS1
MA_DQS_H6 Y15 M_A_DQS6 M_A_DQS2
MA_DQS_L6 W15 M_A_DQS#6 M_A_DQS3
MA_DQS_H5 AB19 M_A_DQS5 M_A_DQS4
MA_DQS_L5 AB20 M_A_DQS#5 M_A_DQS5
MA_DQS_H4 AD23 M_A_DQS4 M_A_DQS6
MA_DQS_L4 AC23 M_A_DQS#4 M_A_DQS7
MA_DQS_H3 G22 M_A_DQS3
MA_DQS_L3 G21 M_A_DQS#3 M_A_DQS#0
MA_DQS_H2 C22 M_A_DQS2 M_A_DQS#1
MA_DQS_L2 C21 M_A_DQS#2 M_A_DQS#2
MA_DQS_H1 G16 M_A_DQS1 M_A_DQS#3
MA_DQS_L1 G15 M_A_DQS#1 M_A_DQS#4
MA_DQS_H0 G13 M_A_DQS0 M_A_DQS#5
MA_DQS_L0 H13 M_A_DQS#0 M_A_DQS#6
M_A_DQS#7

(8) M_A_DQS[0..7]

(8) M_A_DQS#[0..7]

DDR: DATA
Athlon 64 S1
Processor Socket

To SODIMM socket A (near)

(8) M_A_DQ[0..63]

(8) M_A_DM[0..7]

SMDDR_VTERM

C77 4.7U_0603
C456 4.7U_0603
C75 4.7U_0603
C80 4.7U_0603
C451 0.22U
C438 0.22U
C83 0.22U
C452 0.22U
C76 1000P_16V
C439 1000P_16V
C445 1000P_16V
C444 1000P_16V
C84 180P
C455 180P
C81 180P
C78 180P

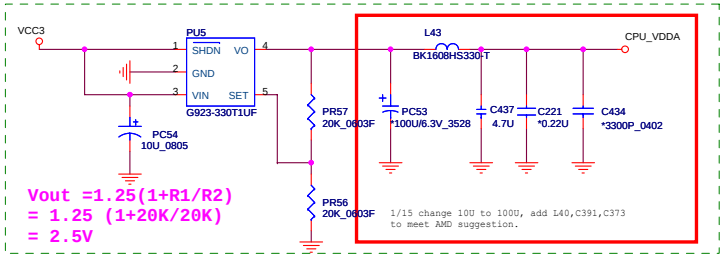
Quanta Computer Inc.

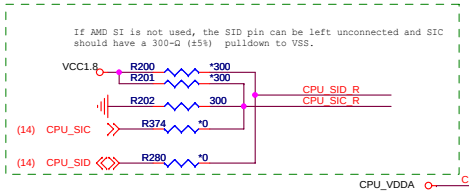
PROJECT : ES2

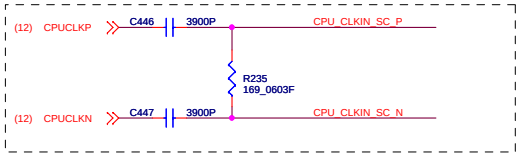
Size	Document Number	Rev
	ATHLON64 DDRII MEMORY I/F	D

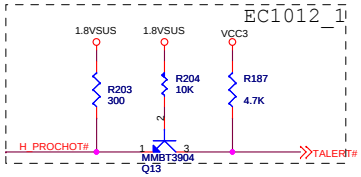
Date: Friday, October 26, 2007 Sheet 5 of 37

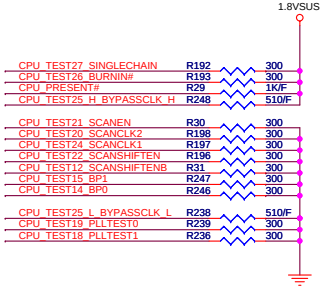
ATHLON Control and Debug

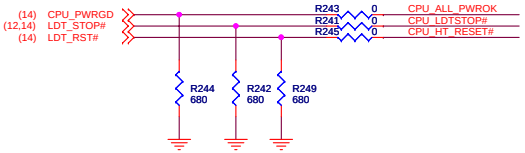


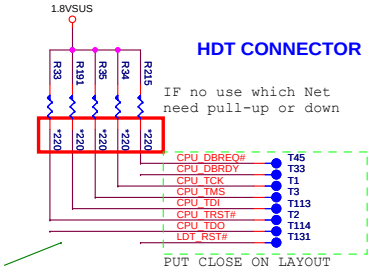






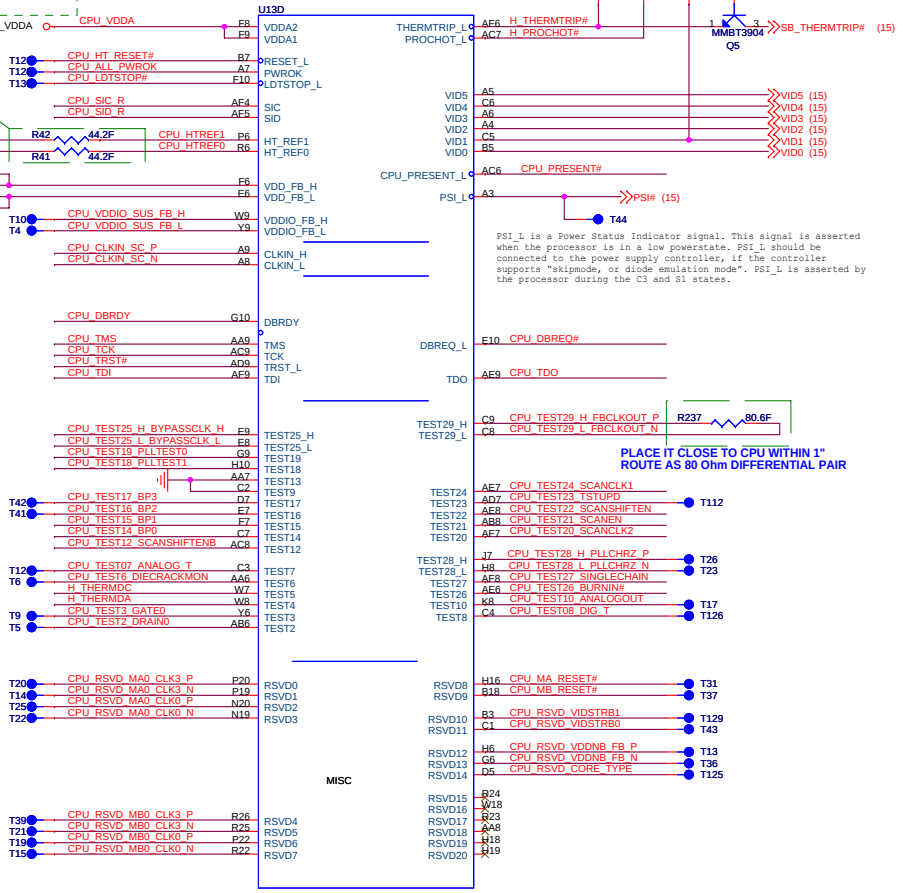




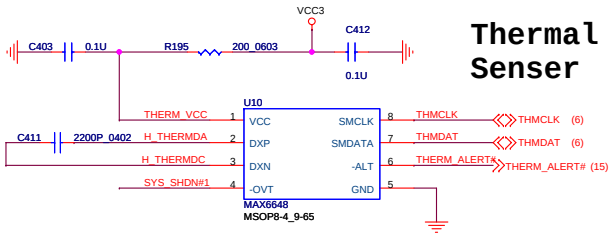


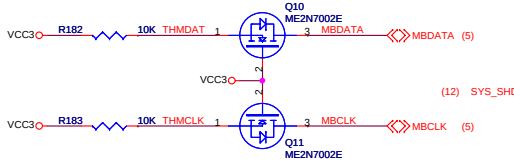
HDT CONNECTOR

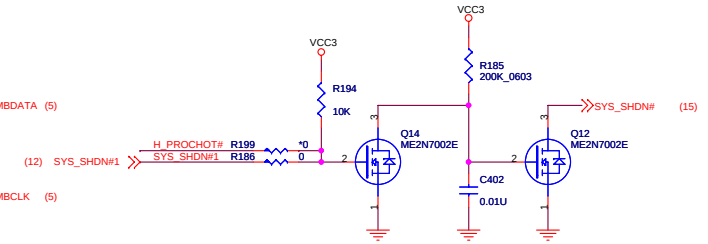
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.



Thermal Senser

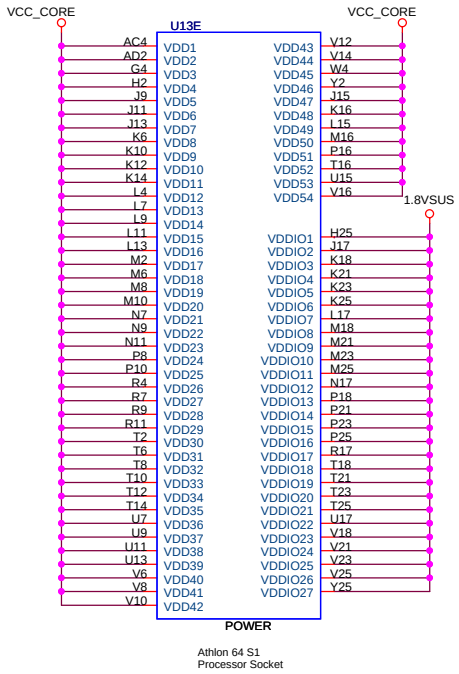


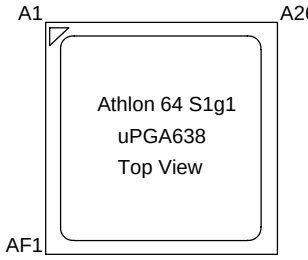


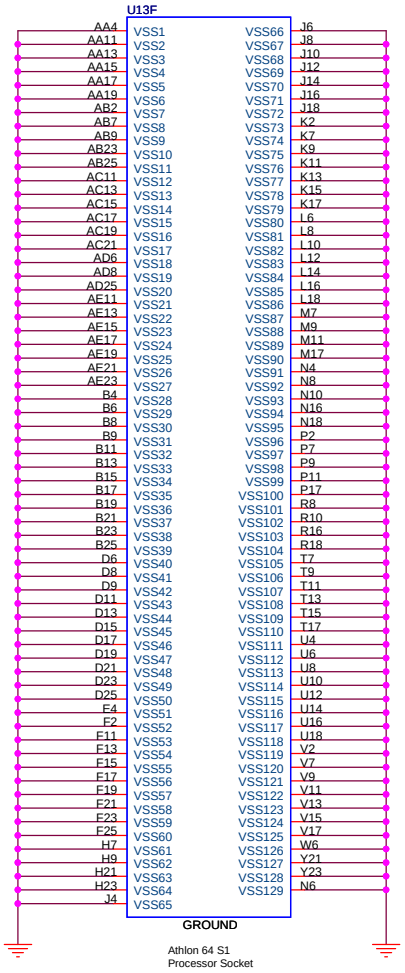


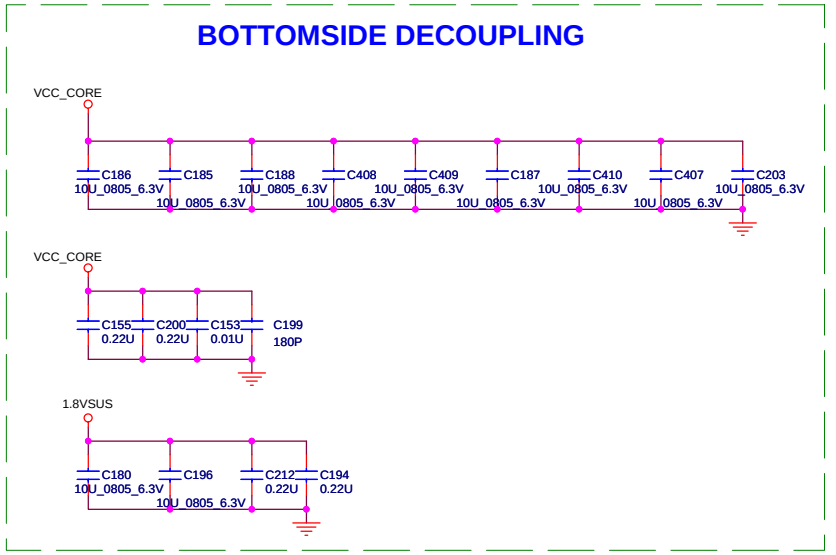
Quanta Computer Inc.
PROJECT : ES2
Size
Document Number
ATHLON64 CTRL & DEBUG
Rev D
Date: Tuesday, November 13, 2007
Sheet 6 of 37

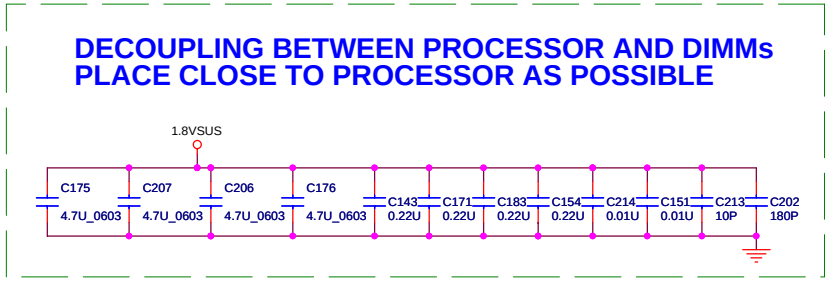
PROCESSOR POWER AND GROUND

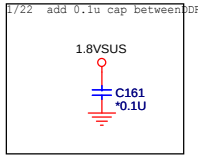








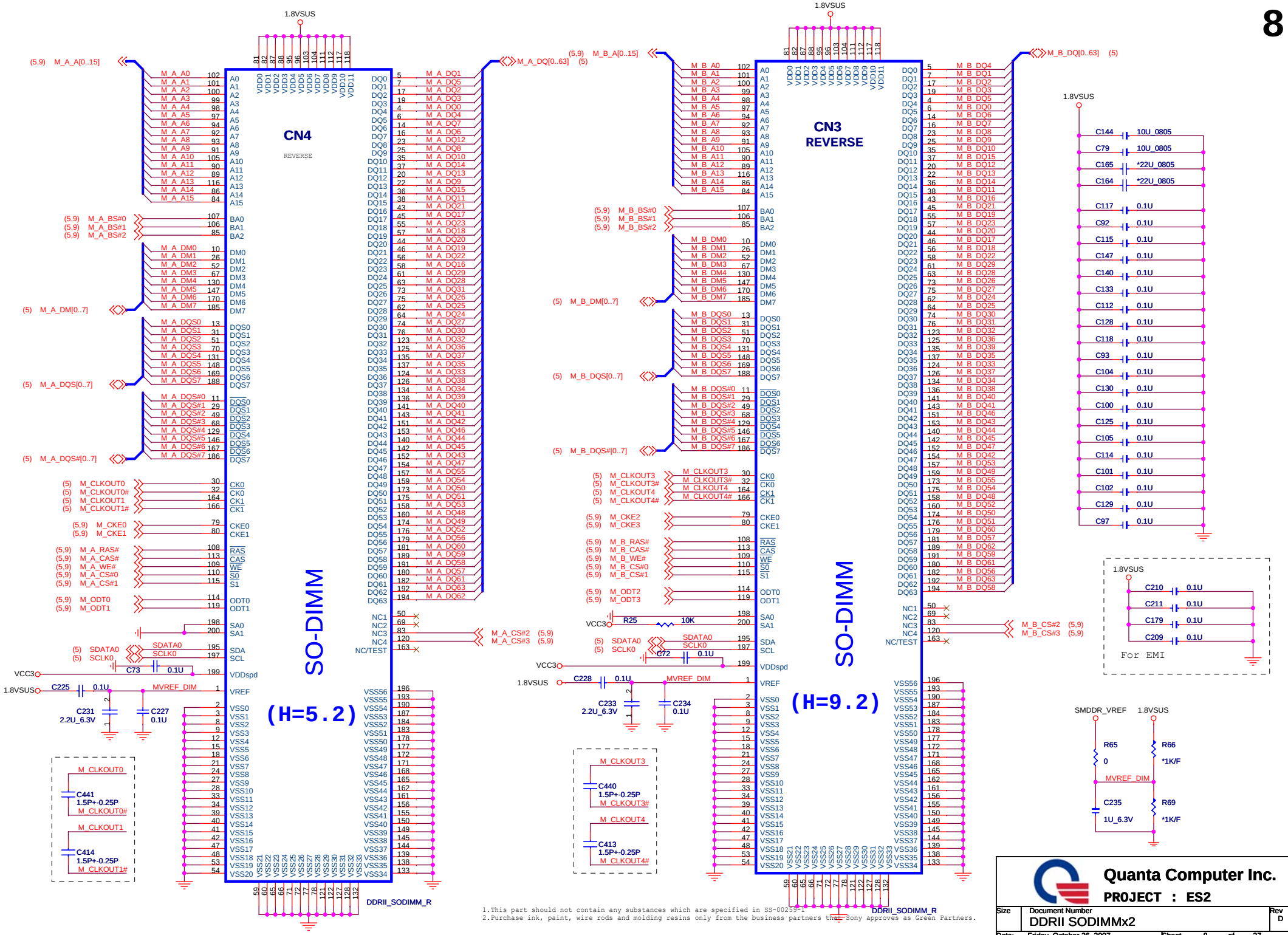




Turion64 X2 TL-50 Rev.F2 (TMDTL50HAX4CT) AJDTL50VG26

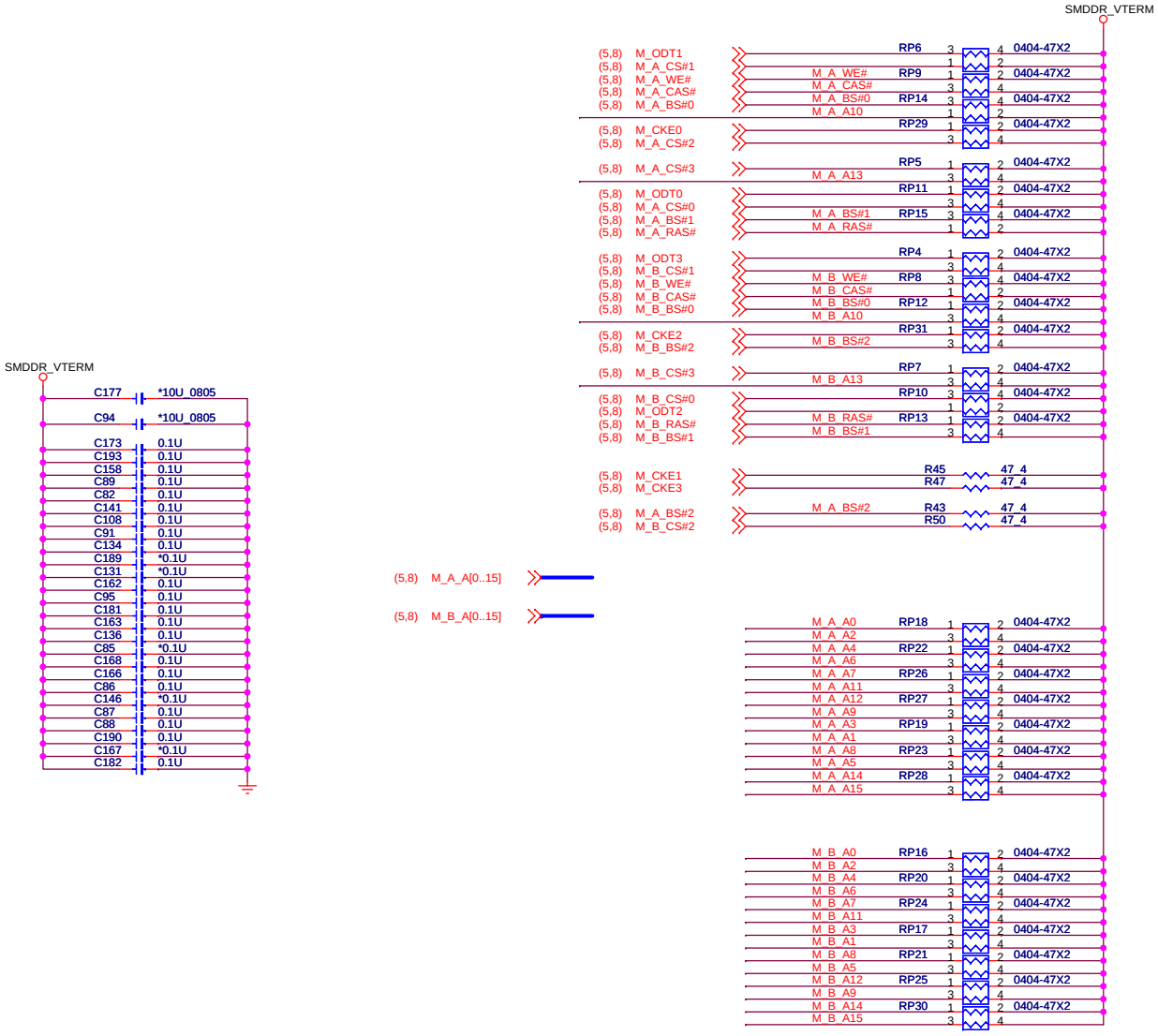
Sempron-64 Single core Rev.F2 (SMS3200HAX4CM) AJ03200VG11

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: ATHLON64 PWR & GND	Rev: D
Date: Friday, October 26, 2007	Sheet 7 of 37	

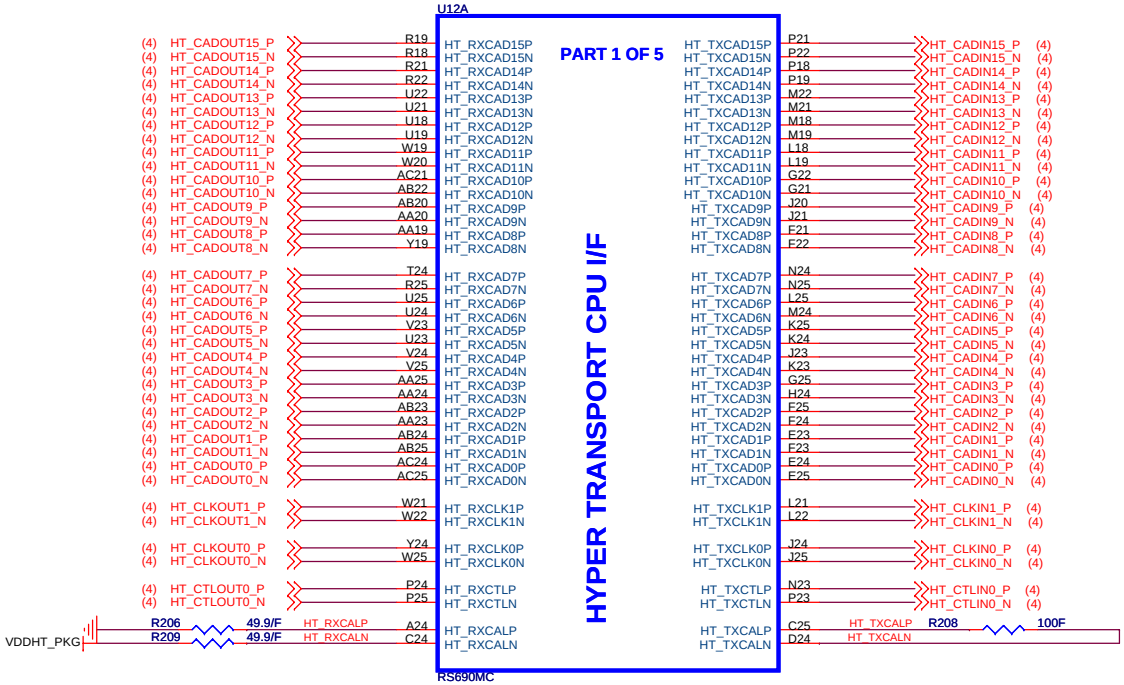


1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

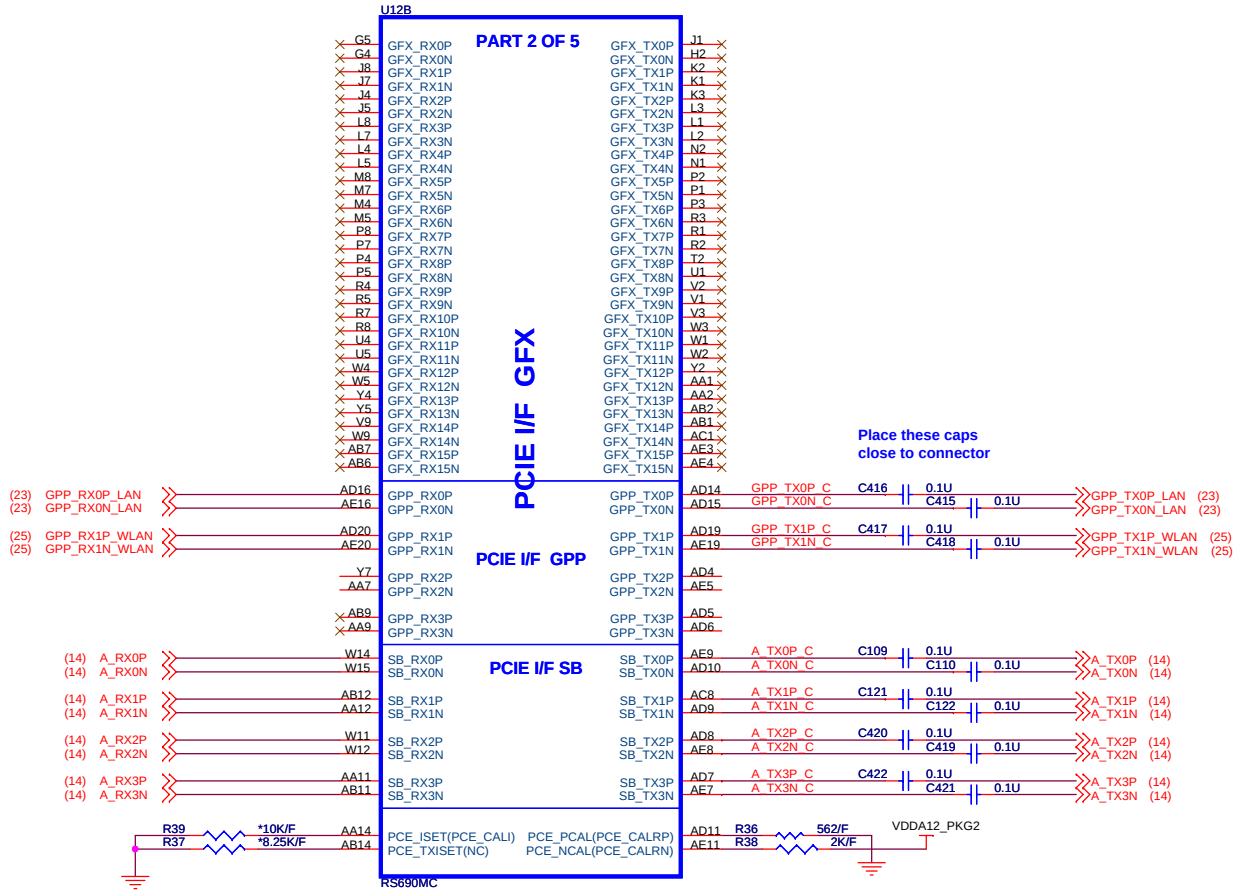
Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: DDRII SODIMMx2	Rev: D
Date: Friday, October 26, 2007	Sheet 8 of 37	



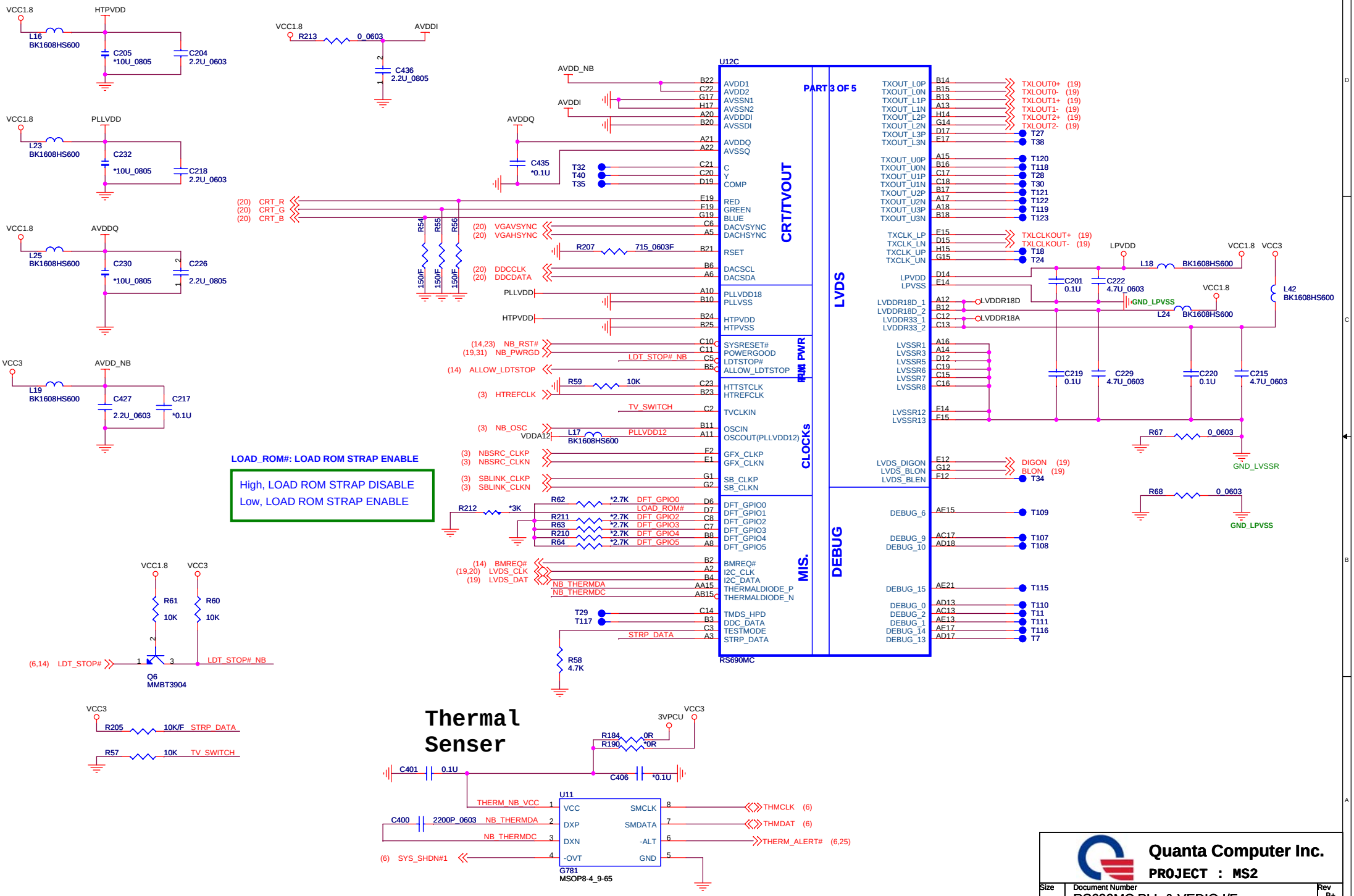
Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: DDRII TERMINATION	Rev: D
Date: Friday, October 26, 2007	Sheet 9 of 37	



Quanta Computer Inc.		
PROJECT : MS2		
Size	Document Number: RS690MC HT LINK I/F	Rev: B+
Date: Friday, October 26, 2007	Sheet 10 of 37	



Quanta Computer Inc.		
PROJECT : MS2		
Size	Document Number: RS690MC PCIE LINK I/F	Rev: B+
Date: Friday, October 26, 2007	Sheet 11 of 37	

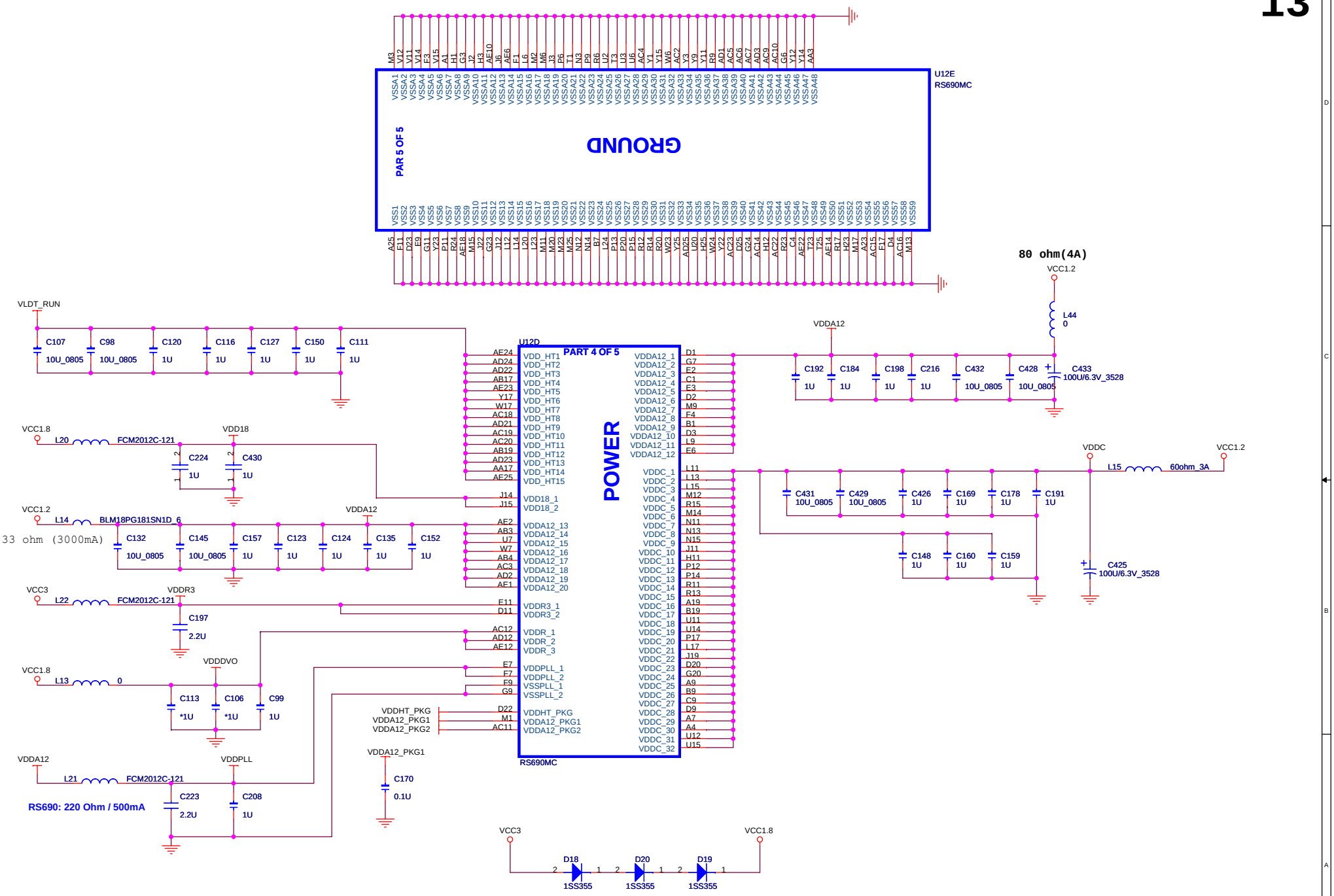


Quanta Computer Inc.

PROJECT : MS2

Size	Document Number	Rev
	RS690MC PLL & VEDIO I/F	B+

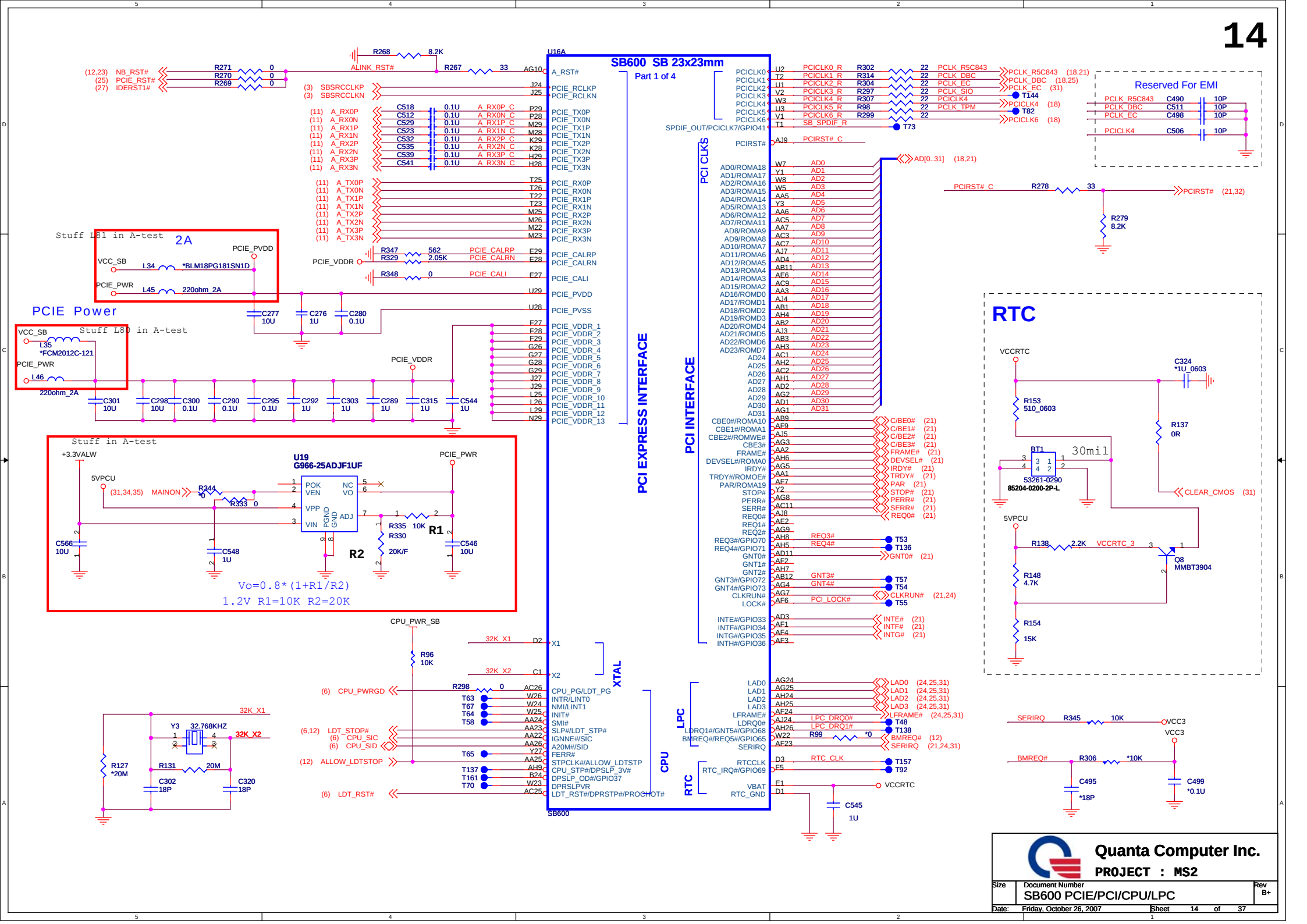
Date: Tuesday, November 13, 2007 Sheet 12 of 37

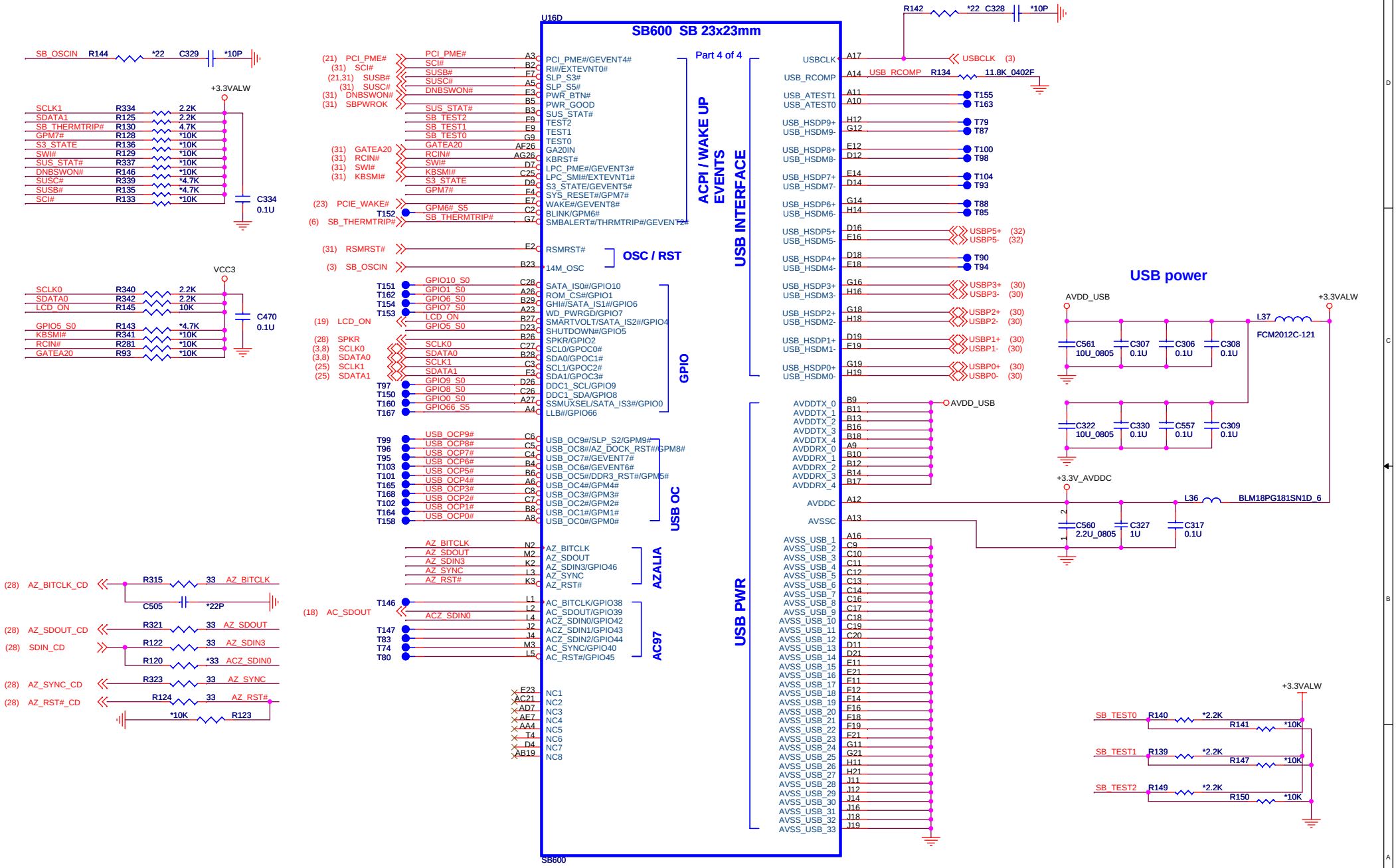


C107	C98	C120	C116	C127	C150	C111
10U_0805	10U_0805	1U	1U	1U	1U	1U
C192	C184	C198	C216	C432	C428	C433
1U	1U	1U	1U	10U_0805	10U_0805	100U/6.3V_3528
C431	C429	C426	C169	C178	C191	
10U_0805	10U_0805	1U	1U	1U	1U	
C148	C160	C159				
1U	1U	1U				
C425						
100U/6.3V_3528						
C132	C145	C157	C123	C124	C135	C152
10U_0805	10U_0805	1U	1U	1U	1U	1U
C113	C106	C99				
*1U	*1U	1U				
C223	C208					
2.2U	1U					

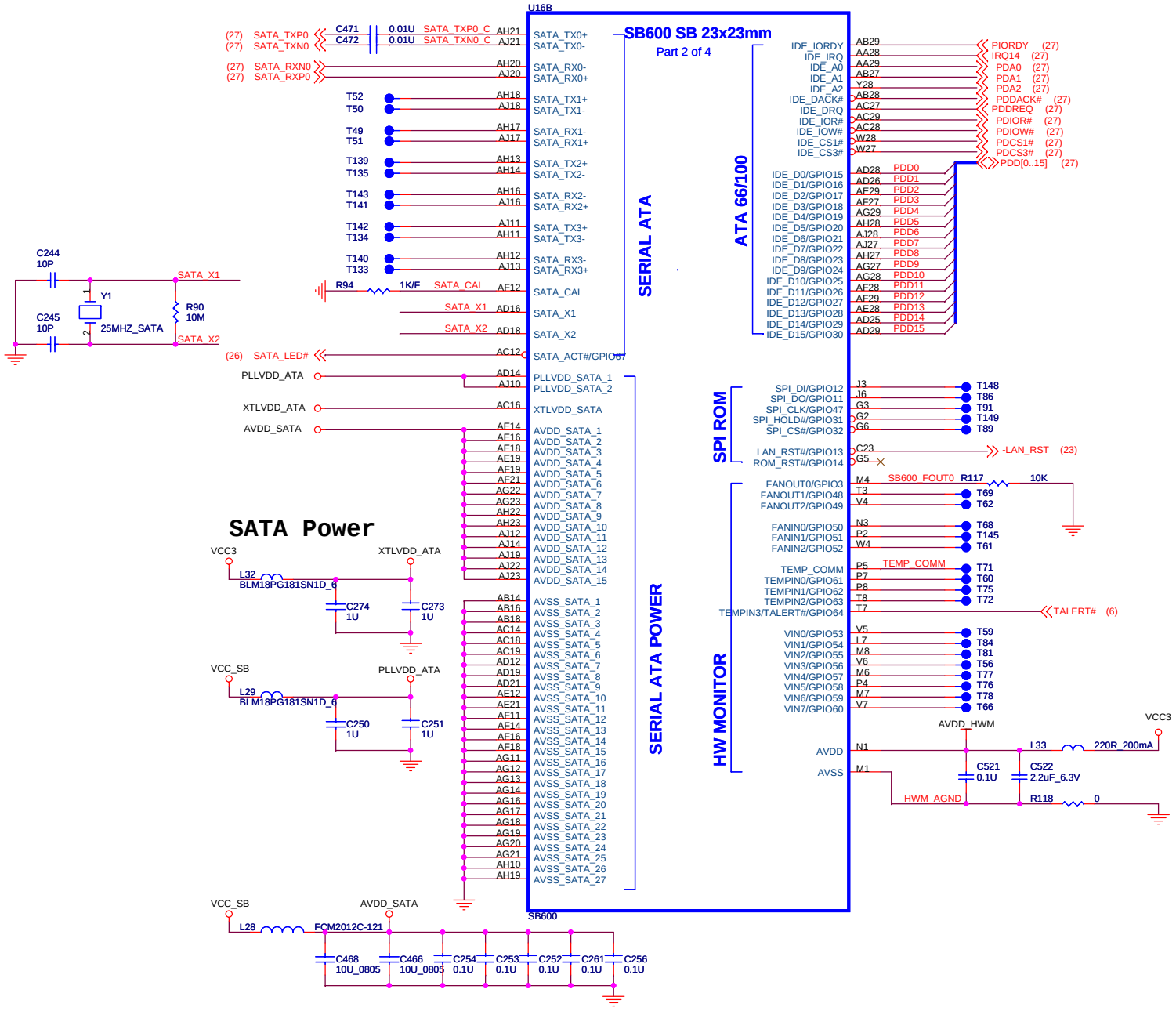
Quanta Computer Inc.
PROJECT : MS2

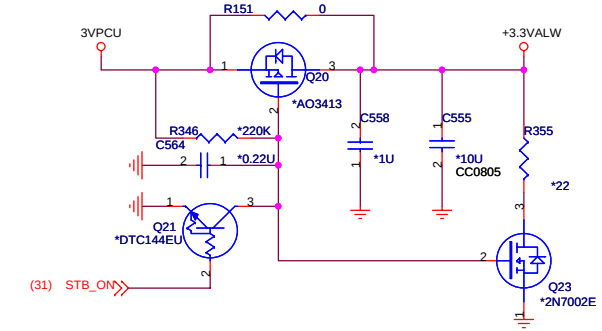
Size	Document Number	Rev
	RS690MC POWER	B+
Date: Friday, October 26, 2007	Sheet 13 of 37	

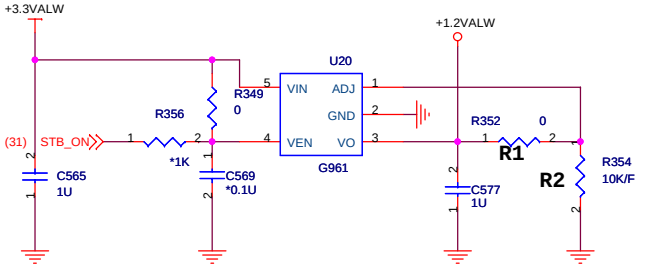

SB600 SB 23x23mm
Part 1 of 4
U16A
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
SB600
PCIE Power
Stuff L81 in A-test
2A
Stuff L80 in A-test
Stuff in A-test
U19
G966-25ADJF1UF
Vo=0.8*(1+R1/R2)
1.2V R1=10K R2=20K
RTC
Reserved For EMI
Quanta Computer Inc.
PROJECT : MS2
SB600 PCIE/PCI/CPU/LPC
Friday, October 26, 2007



Quanta Computer Inc.			
PROJECT : MS2			
Size	Document Number		Rev
	SB600 ACPI/GPIO/USB/AC97		B+
Date: Friday, October 26, 2007	Sheet 15 of 37		

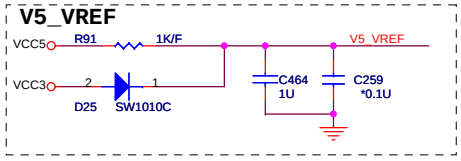

U16B
SB600 SB 23x23mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA Power
SB600
SATA_X1
SATA_X2
25MHZ_SATA
SATA_CAL
SATA_LED#
PLLVDD_ATA
XTLVDD_ATA
AVDD_SATA
VCC3
VCC_SB
AVDD_HWM
HWM_AGND
LAN_RST
TEMP_COMM
TALERT#
SB600_FOUT0





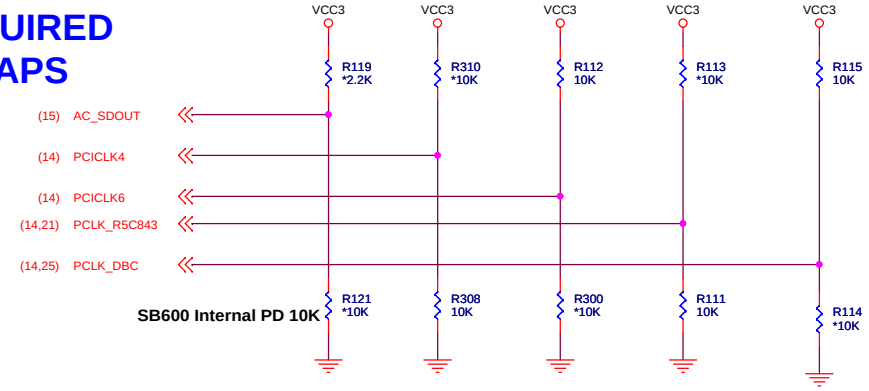
1.2V R1= 0 R2=10K

Vo=1.2*(1+R1/R2)



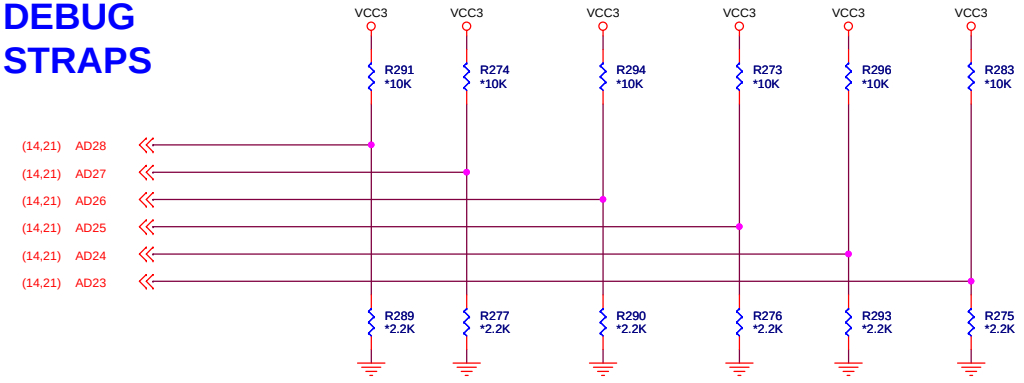
Quanta Computer Inc.
PROJECT : MS2
Size
Document Number
SB600 POWER/DECOUPLING
Rev
B+
Date: Friday, October 26, 2007
Sheet 17 of 37

REQUIRED STRAPS



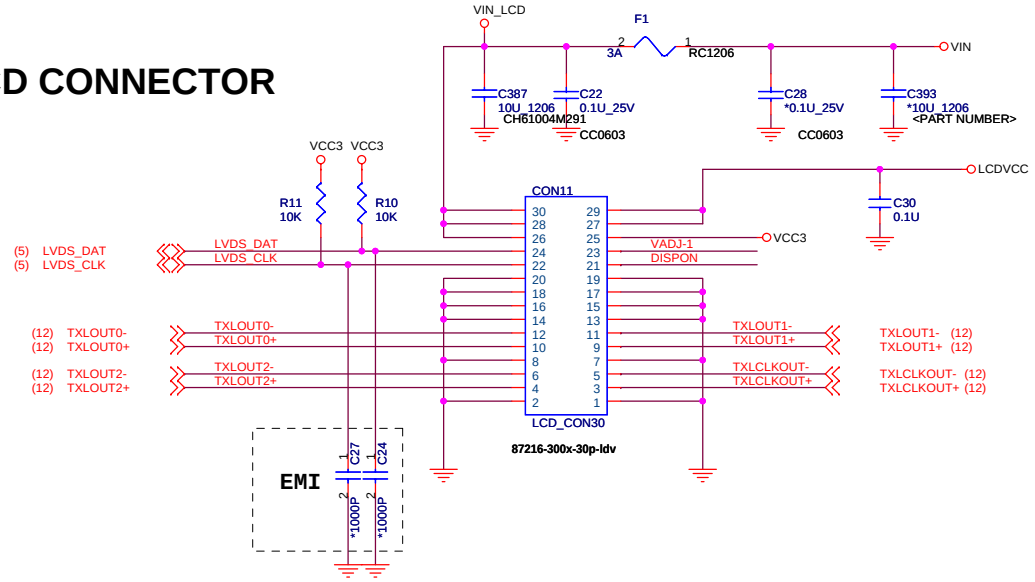
	AC_SDOUT	PCICLK4	PCICLK6	PCLK_R5C843 PCI_CLK0	PCLK_DBC PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

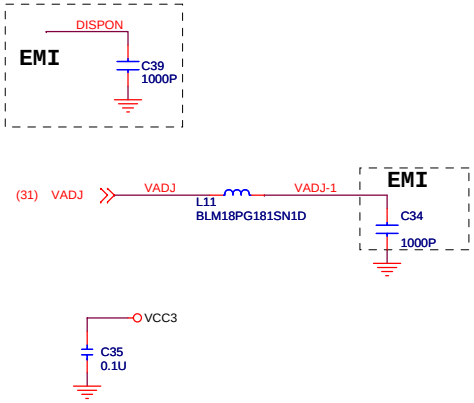
DEBUG STRAPS



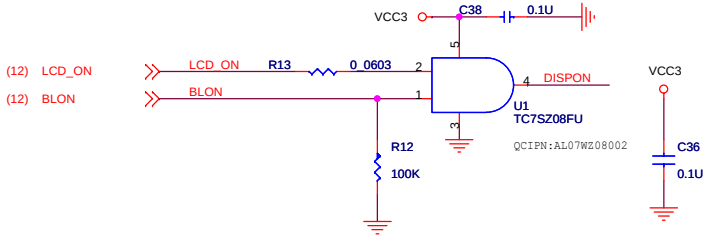
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

LCD CONNECTOR

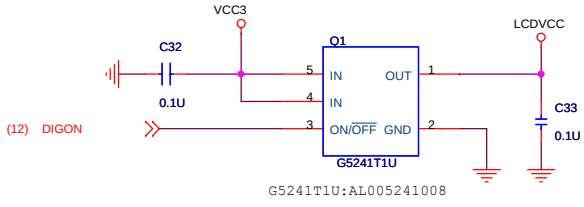




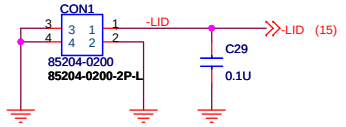
BACKLIGHT CONTROL



PANEL VCC CONTROL



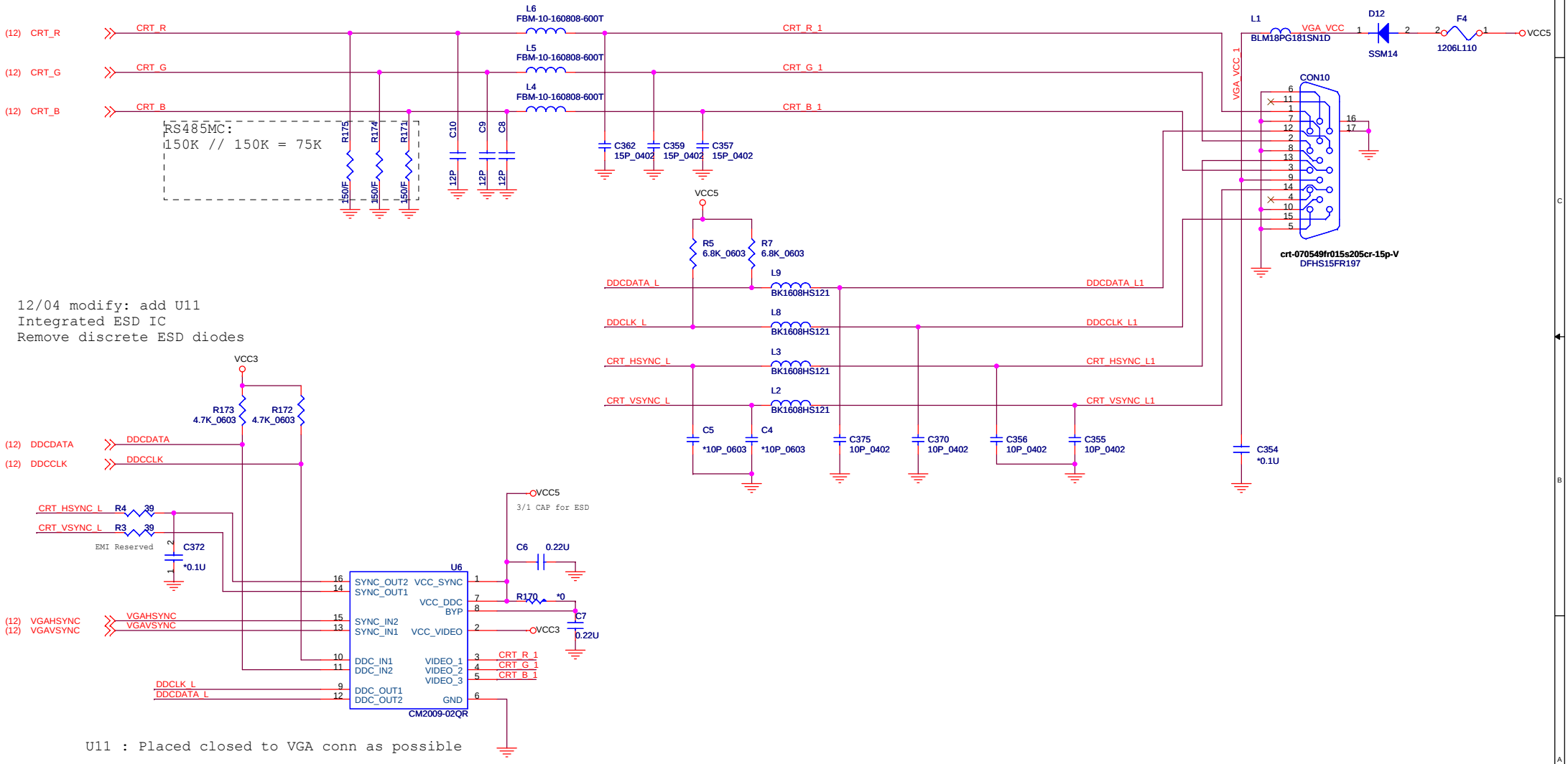
LID



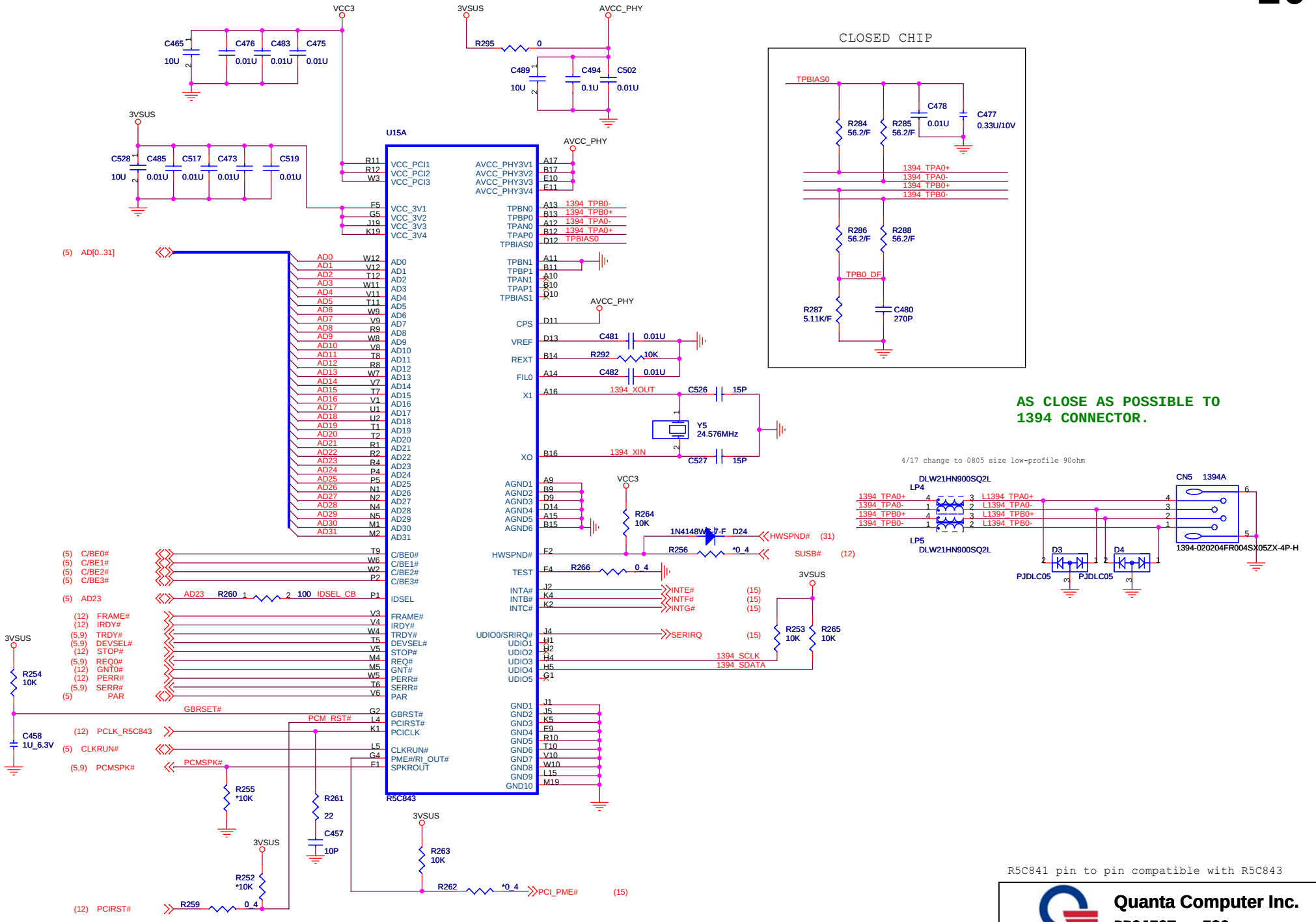
Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	LCD PANEL	D
Date: Friday, October 26, 2007	Sheet 19 of 37	

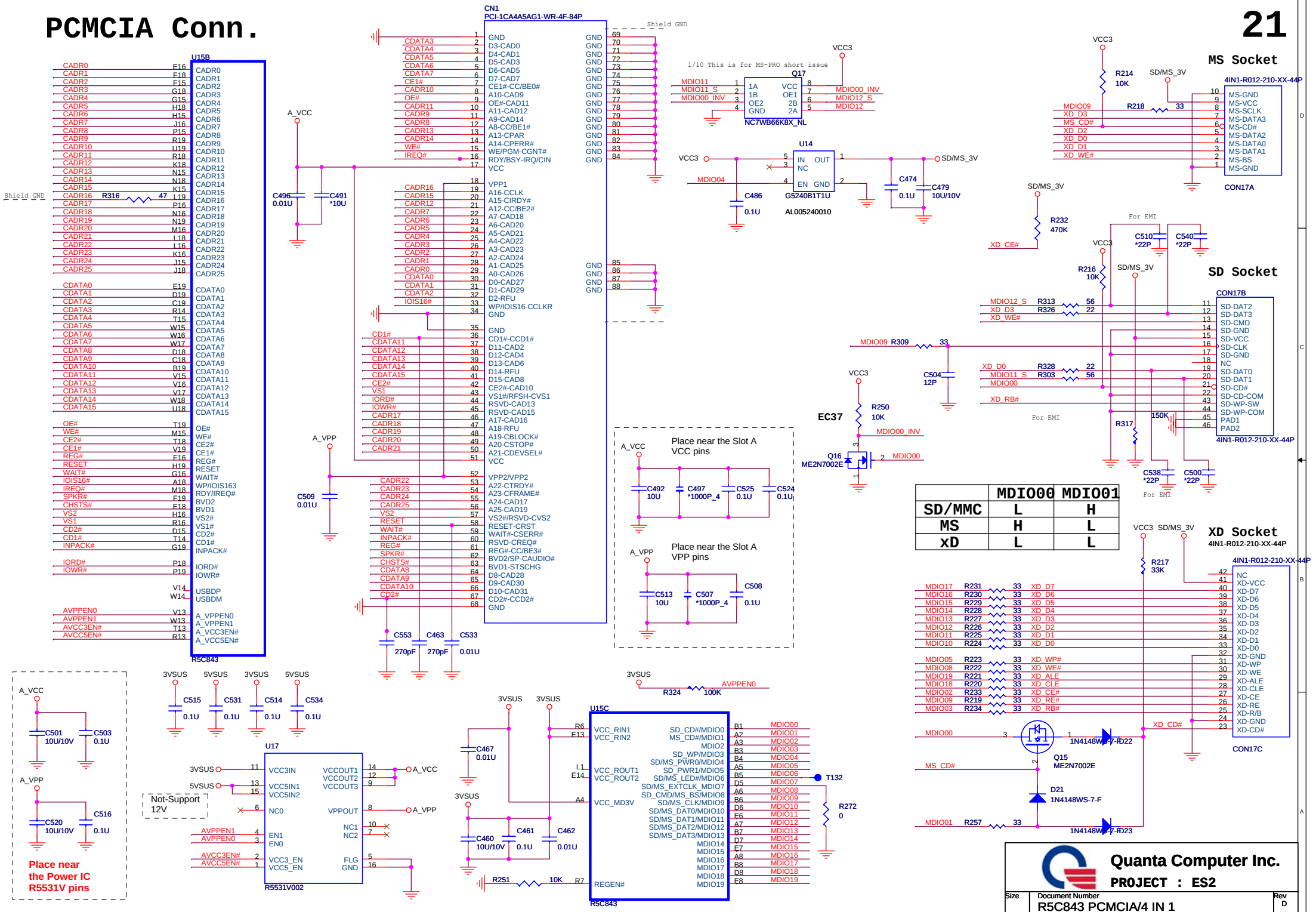
CRT



Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: CRT	Rev: D
Date: Friday, October 26, 2007	Sheet 20 of 37	


U15A
R5C843
VCC3
3VSUS
AVCC_PHY
CLOSED CHIP
TPBIAS0
1394_TPA0+
1394_TPA0-
1394_TPB0+
1394_TPB0-
TPB0_DF
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.
4/17 change to 0805 size low-profile 90ohm
DLW21HN900SQ2L
LP4
LP5
CN5 1394A
1394-020204FR004SX05ZX-4P-H
PJDLC05
D3
D4
Y5 24.576MHz
1394_XOUT
1394_XIN
HWSPND#
SUSB#
SERIRQ
1394_SCLK
1394_SDATA
PCI_PME#
PCIRST#
PCLK_R5C843
CLKRUN#
PCMSPK#
PCM_RST#
GBRSET#
IDSEL_CB
R5C841 pin to pin compatible with R5C843
Quanta Computer Inc.
PROJECT : ES2
Document Number
R5C843 PCI/1394
Rev D
Date: Friday, October 26, 2007
Sheet 21 of 37

PCMCIA Conn.



	MDIO00	MDIO01
SD/MMC	L	H
MS	H	L
xD	L	L

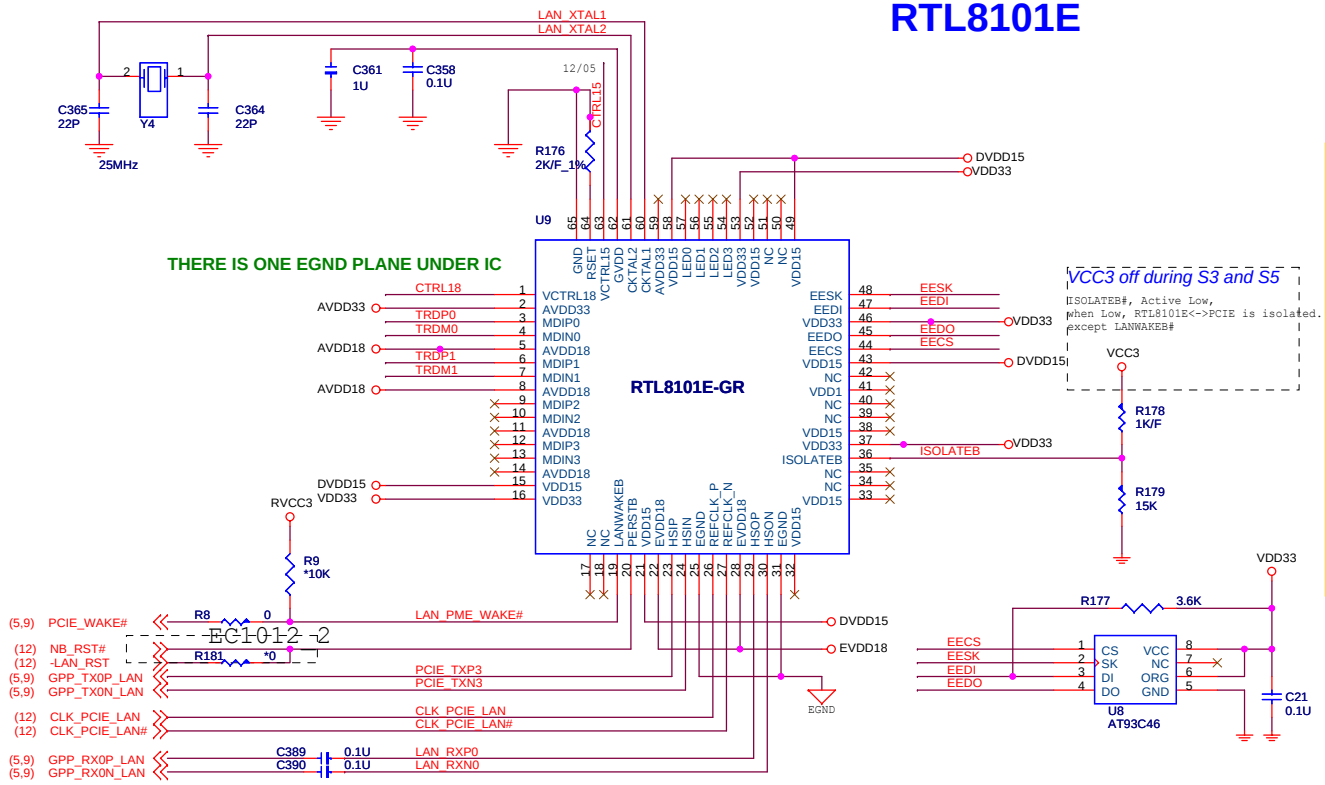
Quanta Computer Inc.

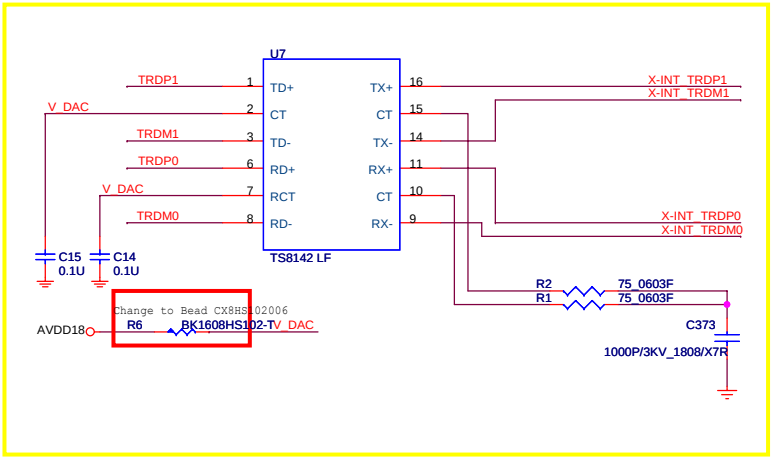
PROJECT : ES2

Size	Document Number	Rev
	R5C843 PCMCIA/4 IN 1	D

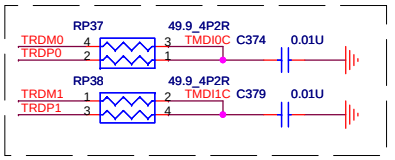
Date: Friday, October 26, 2007 Sheet 22 of 37

RTL8101E

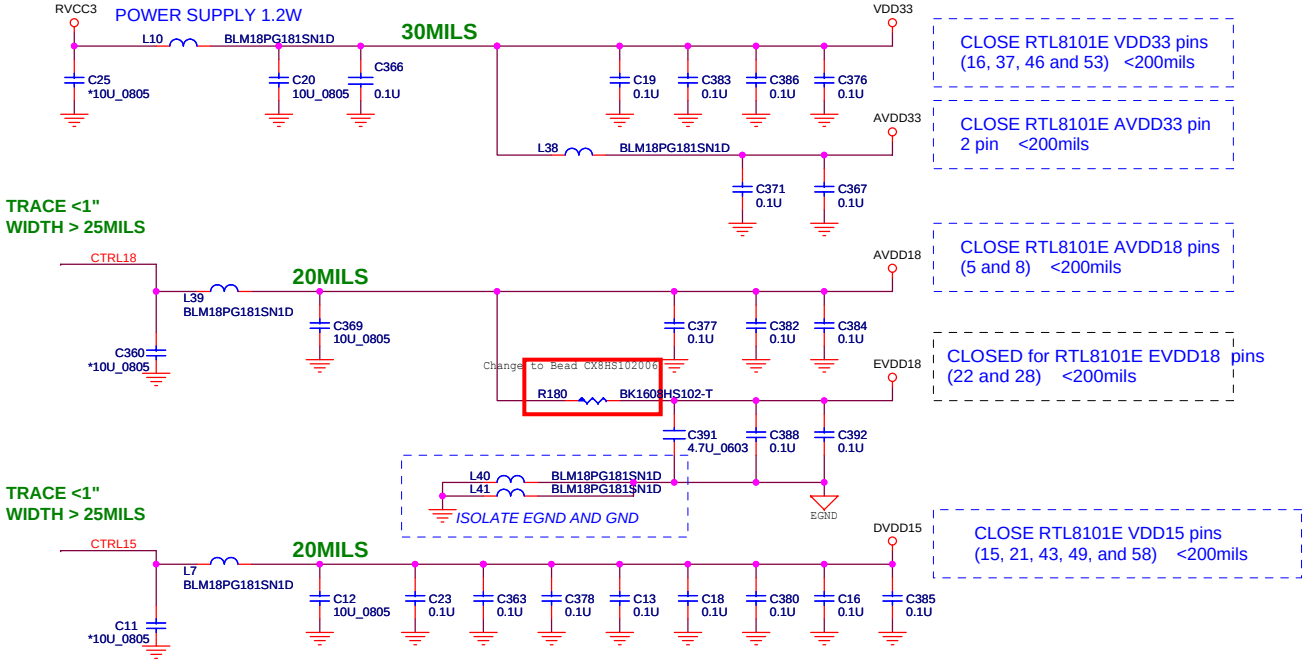




These parts only for RTL8101E application



POWER SUPPLY



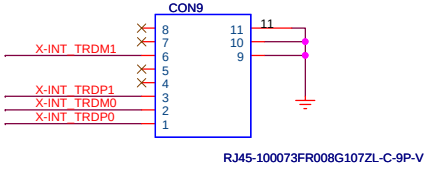
CLOSE RTL8101E VDD33 pins (16, 37, 46 and 53) <200mils

CLOSE RTL8101E AVDD33 pin 2 pin <200mils

CLOSE RTL8101E AVDD18 pins (5 and 8) <200mils

CLOSED for RTL8101E EVDD18 pins (22 and 28) <200mils

CLOSE RTL8101E VDD15 pins (15, 21, 43, 49, and 58) <200mils

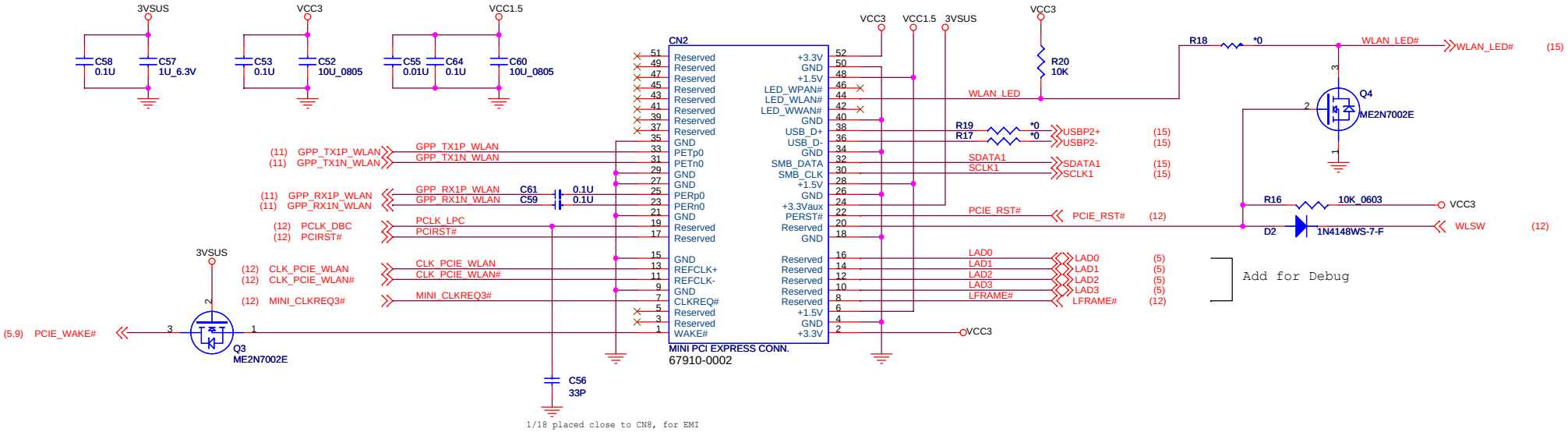


RTL8101E P/N:AL08101E005

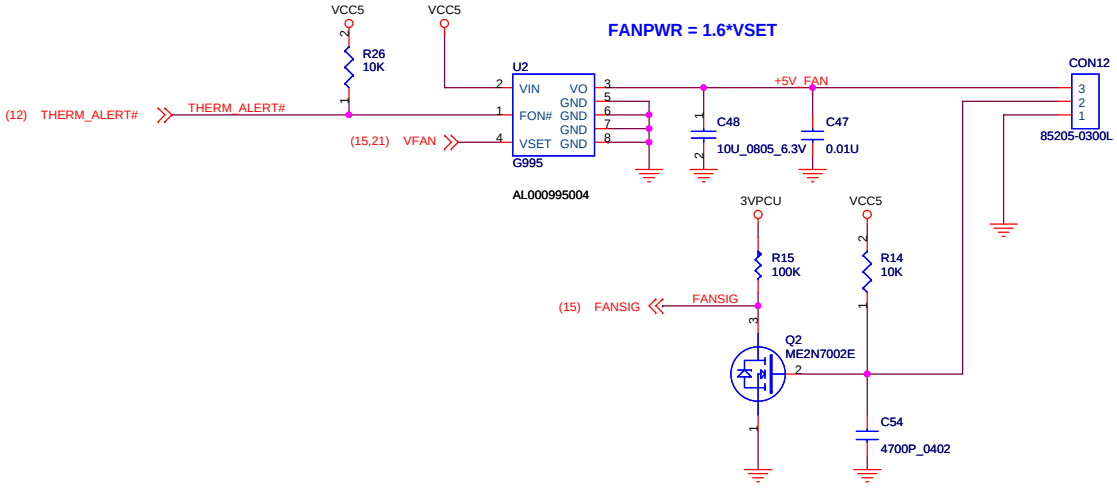
RTL8101E is 10/100 Base, RTL8111B is Giga Base
RTL8101E and RTL8111B are pin to pin compatible

Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: LAN RTL8101E	Rev: D
Date: Friday, October 26, 2007	Sheet 23 of 37	

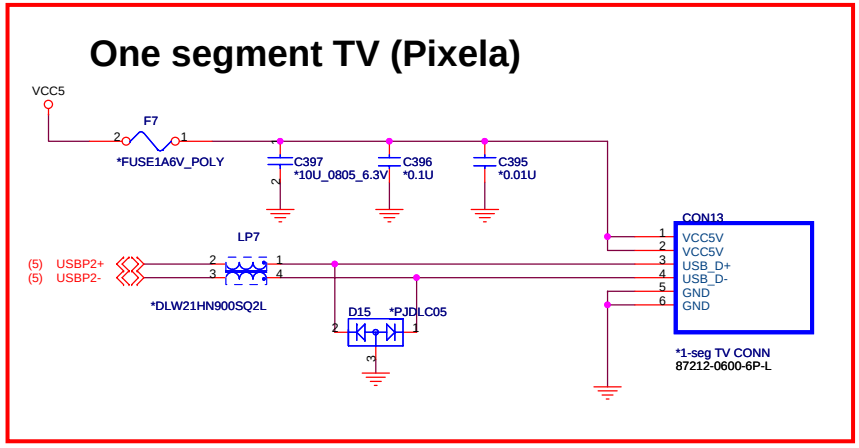
Mini PCI-E Card
WLAN



FAN CONN



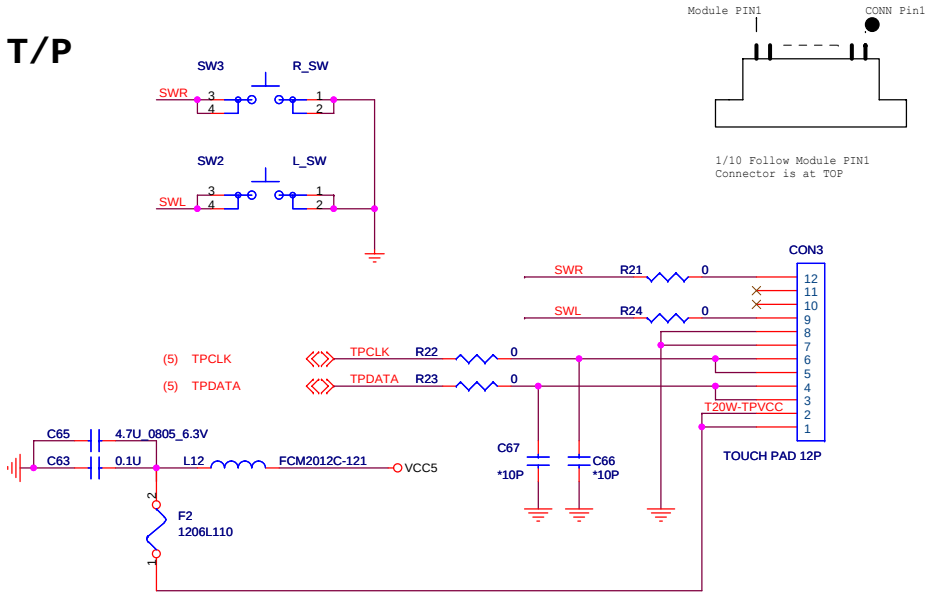
One segment TV (Pixela)

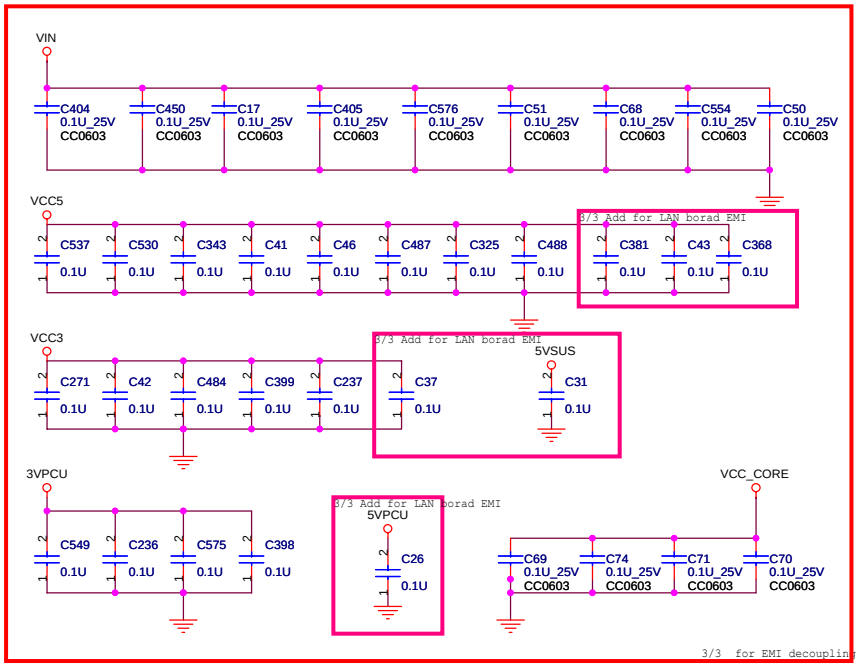


Quanta Computer Inc.
PROJECT : ES2

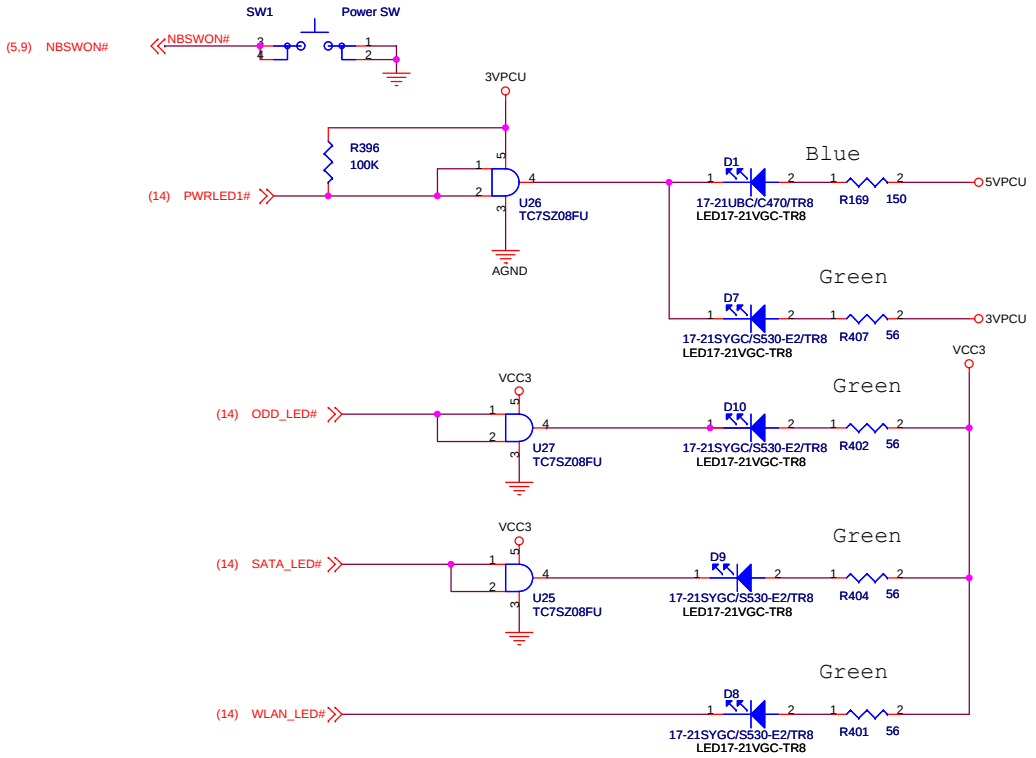
Size	Document Number	Rev
	FAN / MINI PCIE / 1-seg TV	D
Date: Friday, October 26, 2007	Sheet 24 of 37	

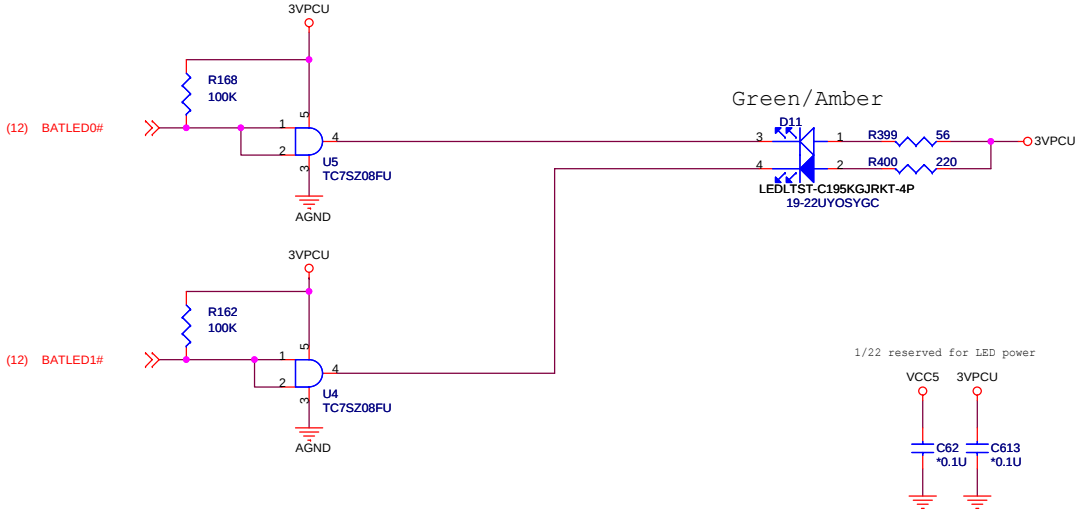
T/P





SYSTEM LEDs





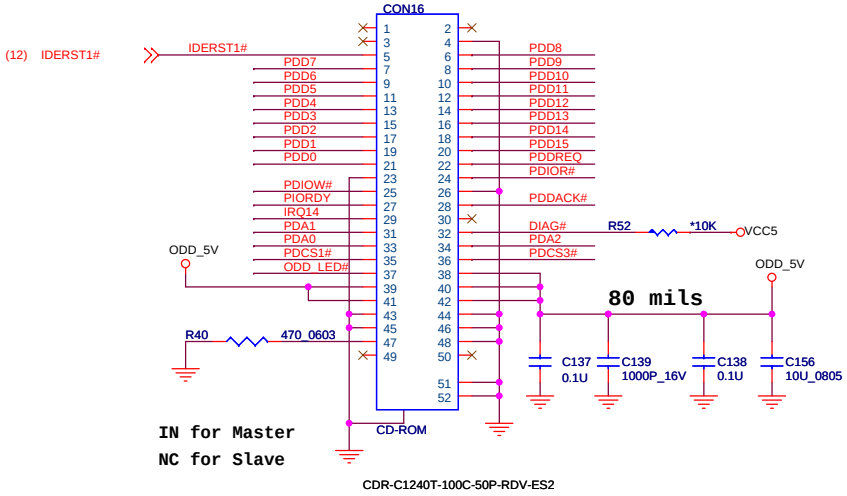
POWER LED	BATT LED	Wireless LED	HDD LED	ODD LED	POWER SWITCH
D14	D18	D15	D16	D17	D7

Quanta Computer Inc.
PROJECT : ES2

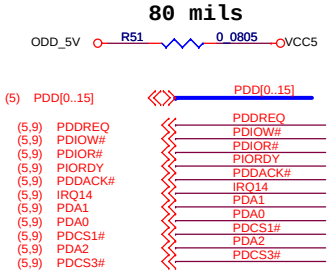
Size	Document Number	Rev
	LEDs / TP CONNECTOR	A
Date: Friday, October 26, 2007	Sheet 25 of 37	

CD-ROM CONNECTOR

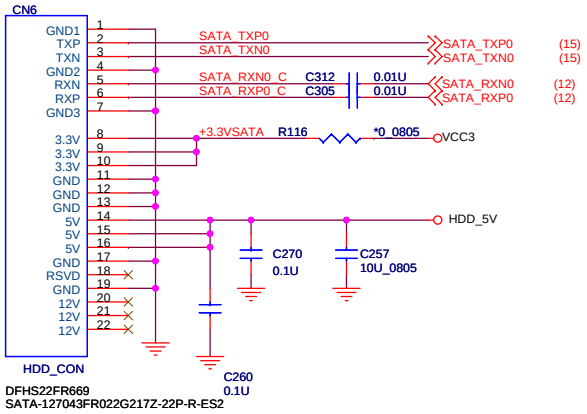
SMT TYPE CNN

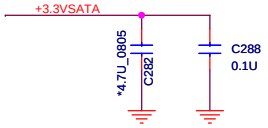


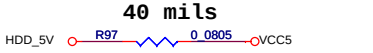
CDR-C1240T-100C-50P-RDV-ES2

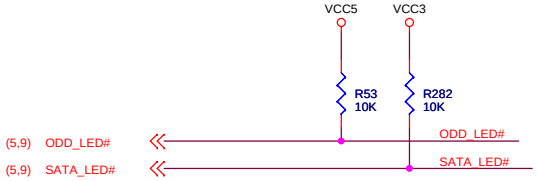


SATA HDD









Quanta Computer Inc.

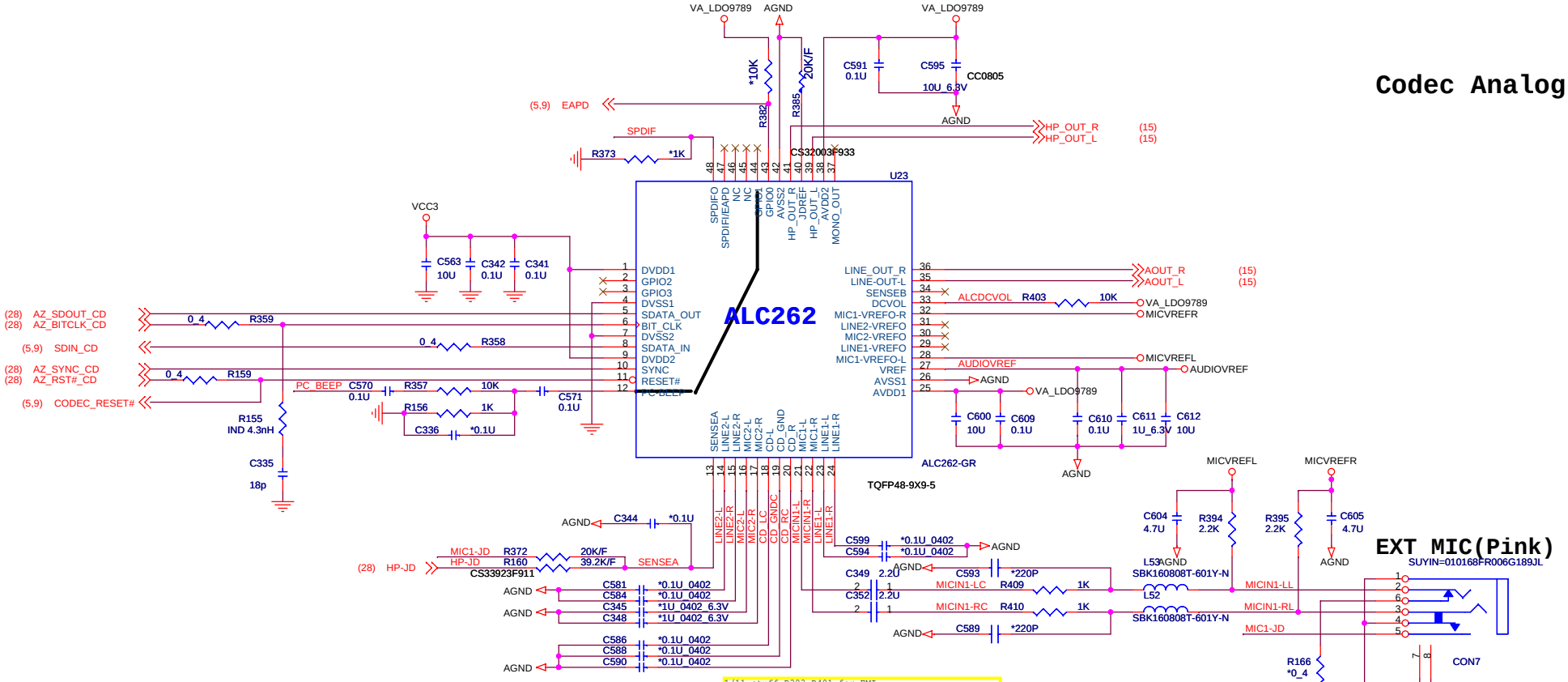
PROJECT : ES2

Size	Document Number	Rev
	ODD/SATA HDD	D

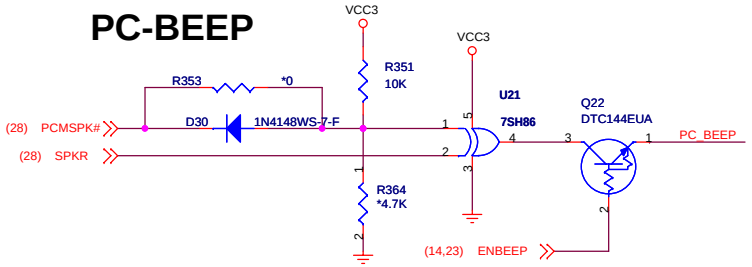
Date: Friday, October 26, 2007 Sheet 26 of 37

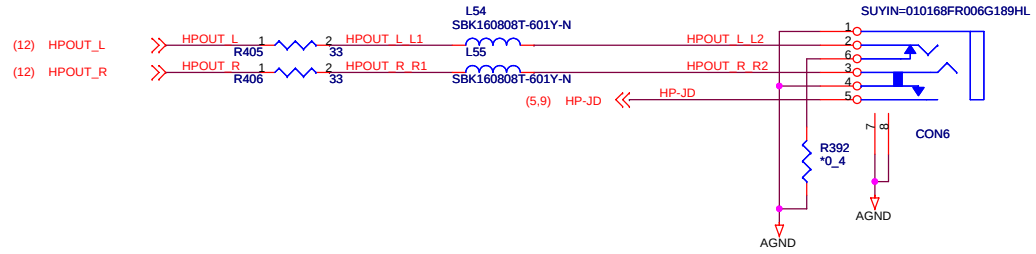
Aucio Codec

Codec Analog Power

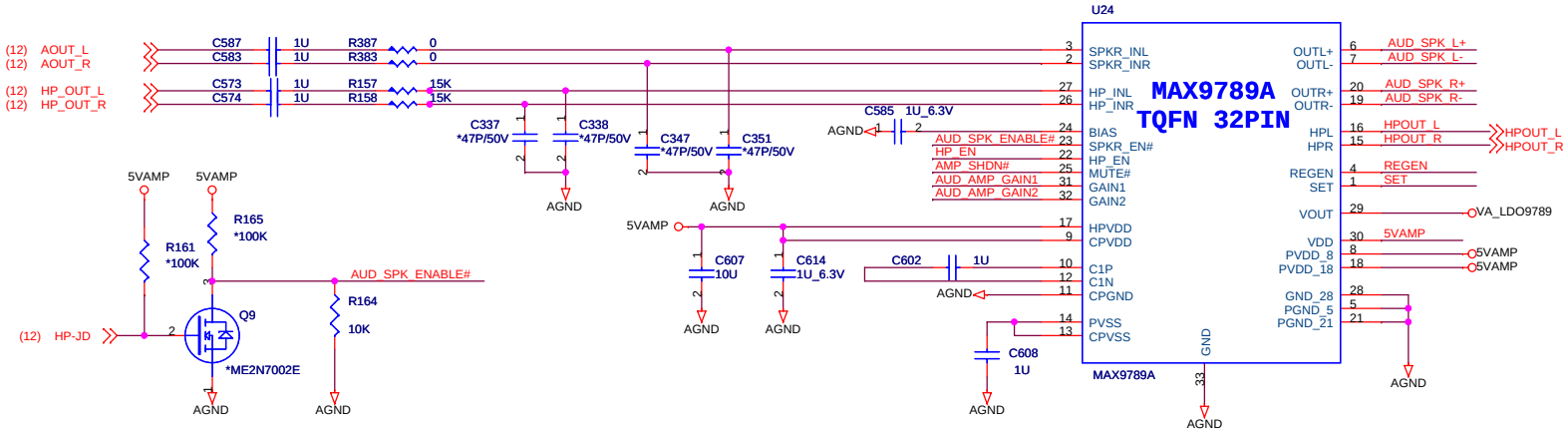


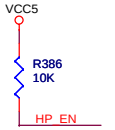
PC-BEEP



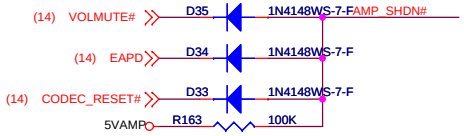


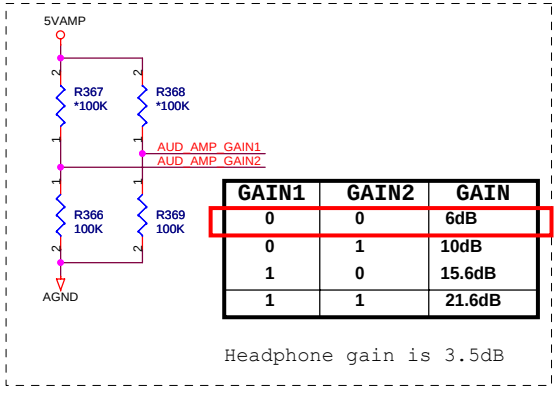
Quanta Computer Inc.			
PROJECT : ES2			
Size	Document Number		Rev
	AUDIO ALC262 MIC/HP		D
Date: Friday, October 26, 2007	Sheet 27 of 37		





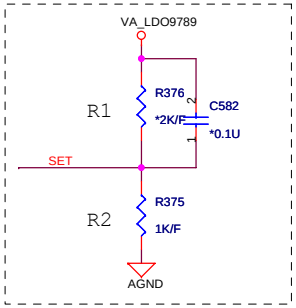
Head phone AMP always ON





GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

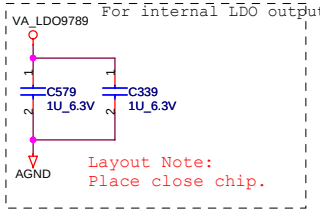
Headphone gain is 3.5dB

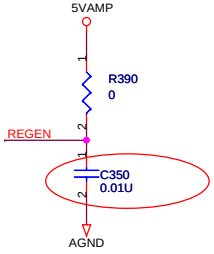


V_LDO_OUT=Vset(1+R1/R2) =3.6V
Vset=1.21V

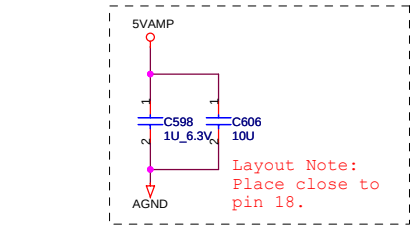
When SET connected to GND, V_LDO_OUT = 4.75V

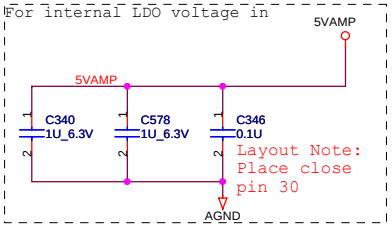
V_LDO_OUT= fix 4.75V
Iout(max) = 120mA, Drop V = 150mV
V_LDO_OUT(actual) = 4.75V - 2% = 4.655V
V_LDO_OUT(worst_case) = 4.655 - 150mV = 4.505V

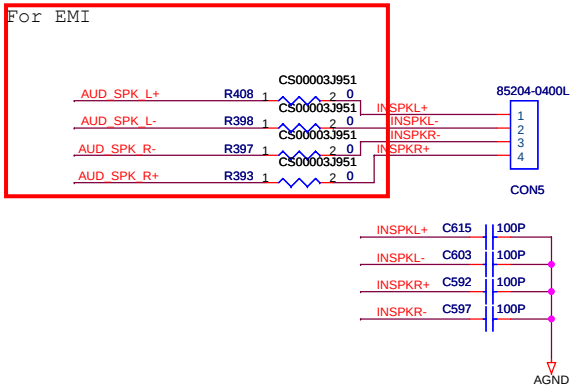


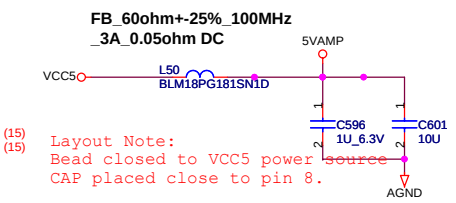


Enable Internal LDO









F5 1206L110 5VSUS → USBVCC5 40 mils
F6 1206L110 5VSUS → USBVCC7 40 mils
80 mils
F3 1206L110 5VSUS → USBVCC1 40 mils
F8 1206L110 → USBVCC3 40 mils
C424 0.1U, C126 0.1U, C423 150U/6.3V CH71511MJ86
USBVCC5 150u to 100u: C3 0.1U, C353 100U/6.3V_3528
USBVCC7 150u to 100u: C49 0.1U, C394 100U/6.3V_3528

D16 PJDLC05, LP2 DLW21HN900SQ2L
(5) USBP0+ (5) USBP0-
USBVCC1 → C96 *47P, C103 *47P → CON14 USB usb-020173mr004s582zl-c2-4p-l-h

D17 PJDLC05, LP3 DLW21HN900SQ2L
(5) USBP3+ (5) USBP3-
USBVCC3 → C172 *47P, C195 *47P → CON15 USB usb-020173mr004s582zl-c2-4p-l-h

D13 PJDLC05, LP6 DLW21HN900SQ2L
(5) USBP5- (5) USBP5+
USBVCC5 → C1 *47P, C2 *47P → CON8 USB
Vertical Type

D14 PJDLC05, LP1 DLW21HN900SQ2L
(5) USBP1- (5) USBP1+
USBVCC7 → C40 *47P, C45 *47P → 85204-0400L CON2
To USB wire

1/11 stuff LP11,LP10,LP9,LP0 for EMI

PAD2 *EMIPAD142X91, PAD8 *EMIPAD142X91, PAD5 *EMIPAD142X91, PAD6 *EMIPAD142X91, PAD9 *EMIPAD142X91
PAD7 *EMIPAD138X98, PAD4 *EMIPAD142X91, PAD3 *EMIPAD142X91, PAD1 *EMIPAD142X91, PAD12 *EMIPAD177X106

H5 H-C307D118P2, H3 H-C307D118P2, H6 h-tc307be335x40HC307D118P2, H4 H-C307D118P2, H8 H-C307D118PT
H10 H-C307D118P2, H14 h-tc307be283x30HC307D118P2, H15 h-tc307be307x33HC307D118P2, H18 H-C307D118P2, H22 H-C307D118P2
H21 H-C307D118P2, H26 H-C307D118P2, H23 H-C307D118P2, H24 H-C307D118P2

(31) MX[7..0]
(31) MY[15..0]
CON4 88502-2401-24P-L
KeyBoard Connector
Bot contact???

CP1 220Px4: MY15 MY13 MY12 MY0
CP2 220Px4: MY2 MY11 MY14 MY10
CP3 220Px4: MY9 MY8 MY7 MY6
CP4 220Px4: MY5 MY3 MY1 MY4
CP5 220Px4: MX5 MX6 MX0 MX3
CP6 220Px4: MX7 MX1 MX4 MX2

3VPCU
RP2 10KX8: MY4 MY1 MY3 MY5 → MY9 MY8 MY7 MY6
RP3 10KX8: MX2 MX4 MX1 MX7 → MX5 MX6 MX0 MX3
RP1 10KX8: MY10 MY14 MY11 MY2 → MY15 MY13 MY12 MY0

H16 H-C315D177P2, H17 H-C315D177P2, H19 H-C315D177P2, H20 H-C315D177P2

4/11 for 1-seg TV
H13 H-TC39BC256D39P2, H11 H-TC39BC256D39P2

NPTH hole
H25 h-c95d95n, H2 h-c95d95n, H27 H-C98D98N

PAD11 *PAD-C236NPT, PAD10 *PAD-C236NPT
2/12 for ME copper contact

H12 H-TC39BC295D39P2, H9 H-TC39BC295D39P2
1/11 for USB wire GND
H7 h-tc217bc307d118p2

H1 H-C405D244P2

Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	KEYBOARD/USB/SCREW	A
Date: Friday, October 26, 2007	Sheet 29 of 37	

Layout Note:
Place all capacitors close to IT8512.

(For PLL Power)

3VPCU
C331 0.1U
C297 0.1U
C333 0.1U
C310 0.1U
C296 0.1U
C326 0.1U
C313 1000P/16V_4
C314 0.1U
L47 BK1608HS121-T
L51 BK1608HS121-T
C332 0.1U

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

C550 *10P
PCLK_EC
R336 *22
C323 0.1U
VCC3 3VPCU VCCRTC

T166 T159 T156

HWPG (37)
VOLMUTE# (29)
SUSC# (15)
NB_PWRGD (12,19)
RSMRST# (15)
VRON (33)
SBPWROK (15)
MAINON (14,34,35)
SUSON (34,35,37)
RVCC_ON (35)
CHG- (36)

SMBUS
MY16 R319 10K 3VPCU
MY17 R318 10K
MBCLK R362 10K
MBDATA R363 10K
HWPG R320 *10K
NBSWON# R152 10K
WLSW R126 *10K
-LID R331 10K

Pull Up for Low Active Pin

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

8Mbit , SPI
3VPCU
R389 10K
R381 10K
U22 W25X80
8512_SCE# 8512_SCK 8512_SI 8512_SO
R384 47
R388 47
R370 15
C580 0.1U

16M SST P/N:AKE28FP0K07

8M Winbond P/N:AKE3GFP0N08

Use 8Mbit in A-test

IT8512

LAD0 LAD1 LAD2 LAD3 LPCRST#/WUI4/GPD2 LPCCLK LFRAME#
LPCPD#/WUI6/GPE6
GA20/GPB5 SERIRQ ECSMI#/GPD4 ECSCI#/GPD3 WRST# KBRST#/GPB6 PWUREQ#/GPC7
LPC
D32 D28 D27 D29 1SS355
GATEA20 SERIRQ KBSMI# SCI# PCURST# RCIN#

GPC0/CRX GPB2/CTX
CIR
T169

GPIO

SM BUS
SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2 SMCLK2/GPF6 SMDAT2/GPF7
MBCLK MBDATA D31 1SS355 MBCLK (6,38) MBDATA (6,38) DNBSWON# (15)
BAT_TYPE
RF_LED WLAN_LED# (26)

PS/2
PS2CLK0/GPF0 PS2DAT0/GPF1 PS2CLK1/GPF2 PS2DAT1/GPF3 PS2CLK2/GPF4 PS2DAT2/GPF5
VCC5 10K 10K R338 R343
TPCLK (26) TPDATA (26)

PWM
PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/GPA6 PWM7/GPA7
PWRLED1# (26) HWSPND# (21) ENBEEP (28) REFON (38) WLSW (25) SWI# (15)
D26 1SS355
TACH0/GPD6 TACH1/GPD7
FANSIG (25) BAT/AC- (36)
TMR0/WUI2/GPC4 TMR1/WUI3/GPC6
STB_ON (17)

WAKE UP
PWRSW/GPE4 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1
NBSWON# SUSB# ACIN (36)
WUI5/GPE5 RING#/PWRFAIL#/LPCRST#/GPB7

UART
TXD/GPB1 RXD/GPB0
T106 T105
BATLED0# (26) BATLED1# (26)

A/D D/A
ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/GPI4 ADC5/GPI5 ADC6/GPI6 ADC7/GPI7
MTEMPV MBATV -PCUHOLD
MTEMPV (36,38) MBATV (38)
DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3 DAC4/GPJ4 DAC5/GPJ5
CC-SET (36) VFAN (25) VADJ (19)

CLOCK
CK32KE CK32K
PMUX2 PMUX1

FLASH
R361 10K 8512_SCK
R360 *100K 8512_SO 8512_SI 8512_SCE#
FLRST#/WUI7/GPG0/TM FLCLK/SCK FLAD3/GPG6 FLAD2/SO FLAD1/SI FLAD0/SCE# FLFRAME#/GPG2

KBMX
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15
(30) MY[15..0]
(30) MX[7..0]
KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

VSS VSS VSS VSS VSS VSS VSS AVSS
R332 0

IT8512 U18
AJ085120F01

Y6 32.768KHZ
C568 18P CC0603
C567 18P CC0603

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

DNBSWON# HWPG SUSC#
C316 *39P C285 *39P C572 *39P

3VPCU
Q7 DTA124EU
(26) NBSWON# NBSWON#
(36) ACIN 1SS355 D5
(15,21) SUSB# 1SS355 D6
-PCUHOLD
R327 100K

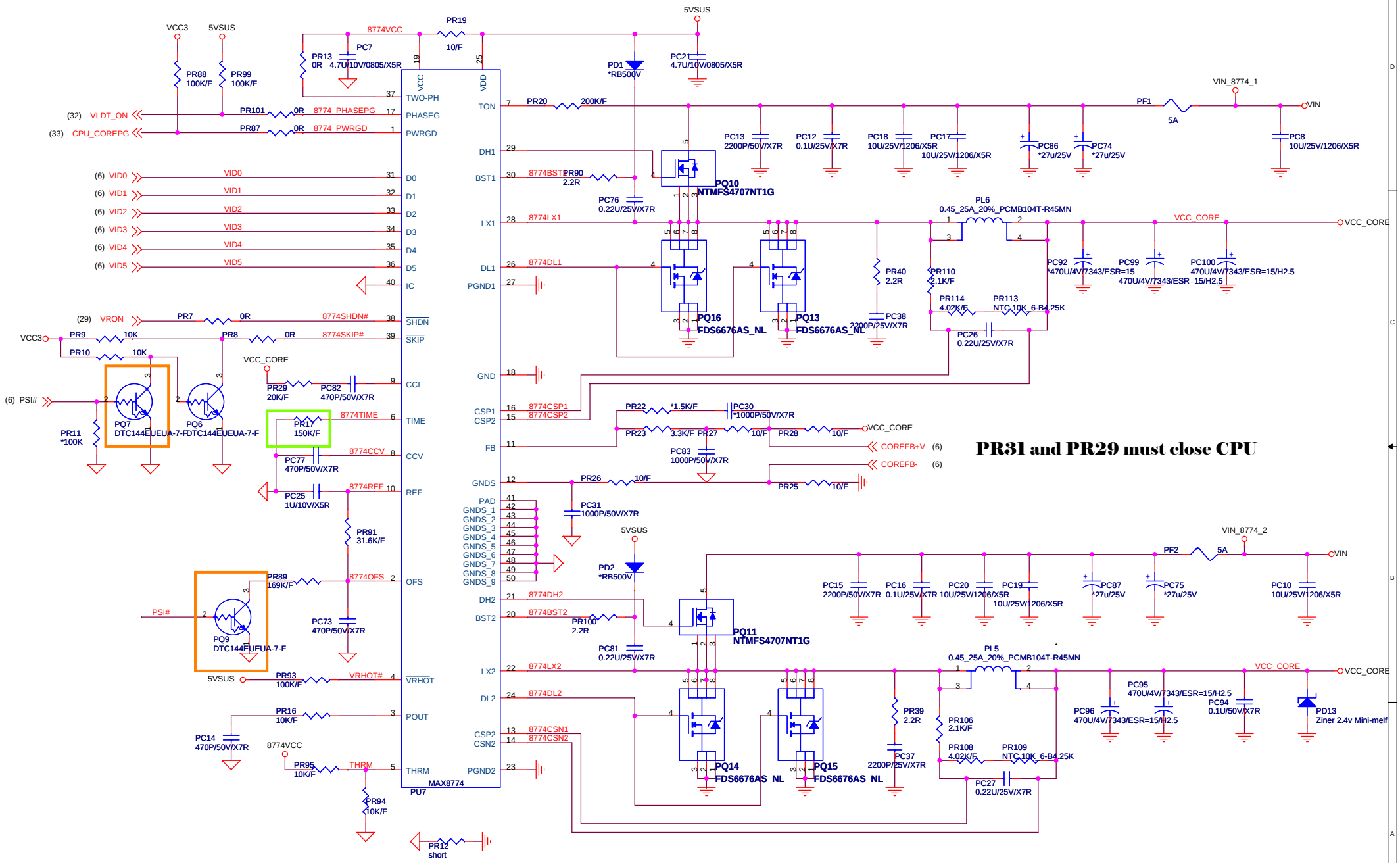
Please reserve this connector
for serial debug port & KBS download usage.
UART_TXD T96
UART_RXD T98

R258 *0
(14) CLEAR_CMOS

Quanta Computer Inc.
PROJECT : MS2

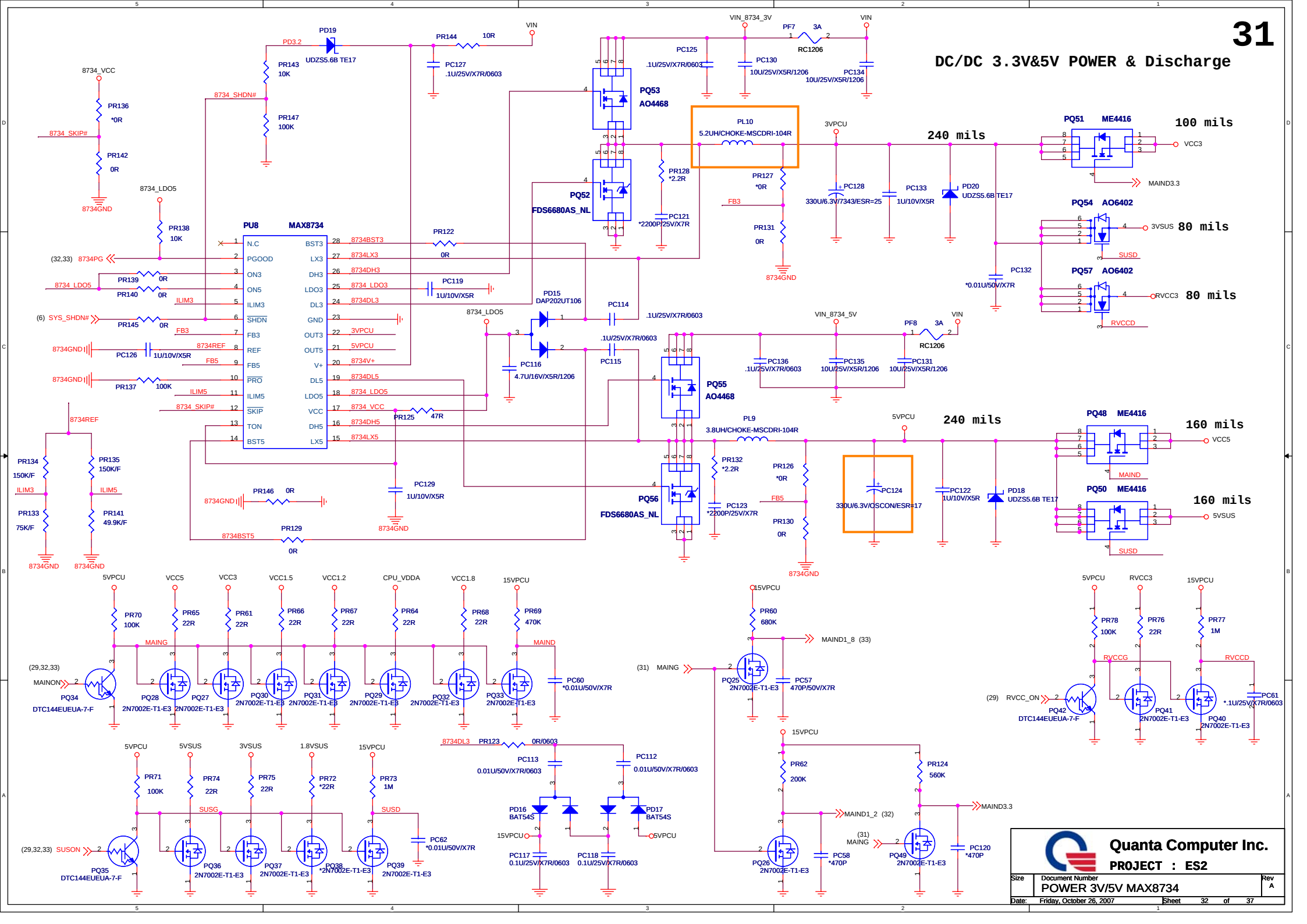
Size	Document Number	Rev
	EC ITE8512	B+

Date: Friday, October 26, 2007 Sheet 30 of 37



Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: POWER CPU CORE MAX8774	Rev: A
Date: Friday, October 26, 2007	Sheet 31 of 37	

DC/DC 3.3V&5V POWER & Discharge

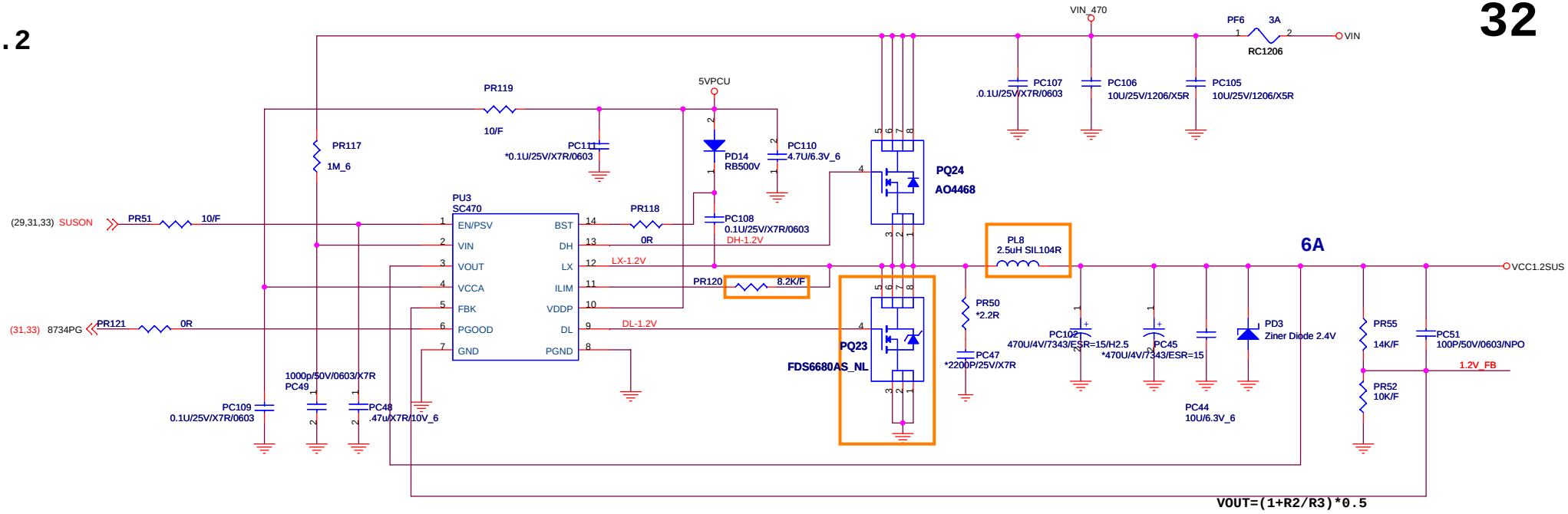


Quanta Computer Inc.
PROJECT : ES2

Size	Document Number	Rev
	POWER 3V/5V MAX8734	A

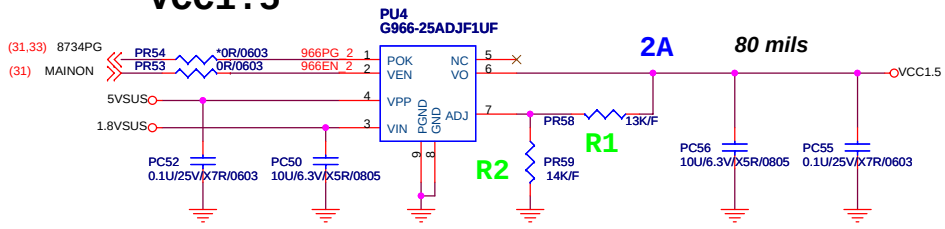
Date: Friday, October 26, 2007 Sheet 32 of 37

VCC1.2

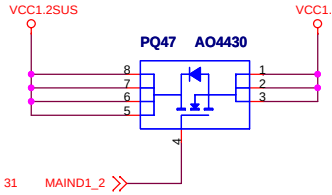


VOUT=(1+R2/R3)*0.5

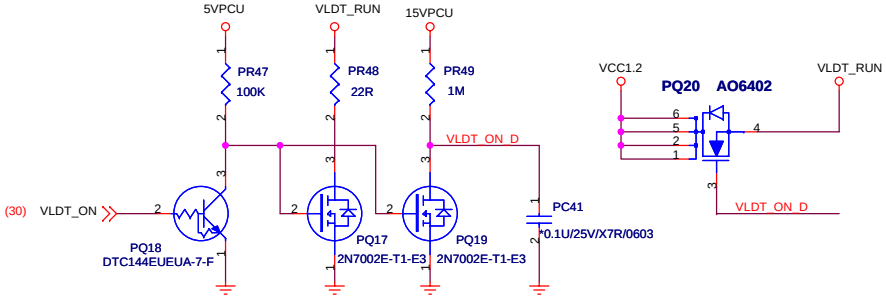
VCC1.5



Vout =0.8*(1+R1/R2)
= 0.8* (1+13K/14K)
= 1.54V

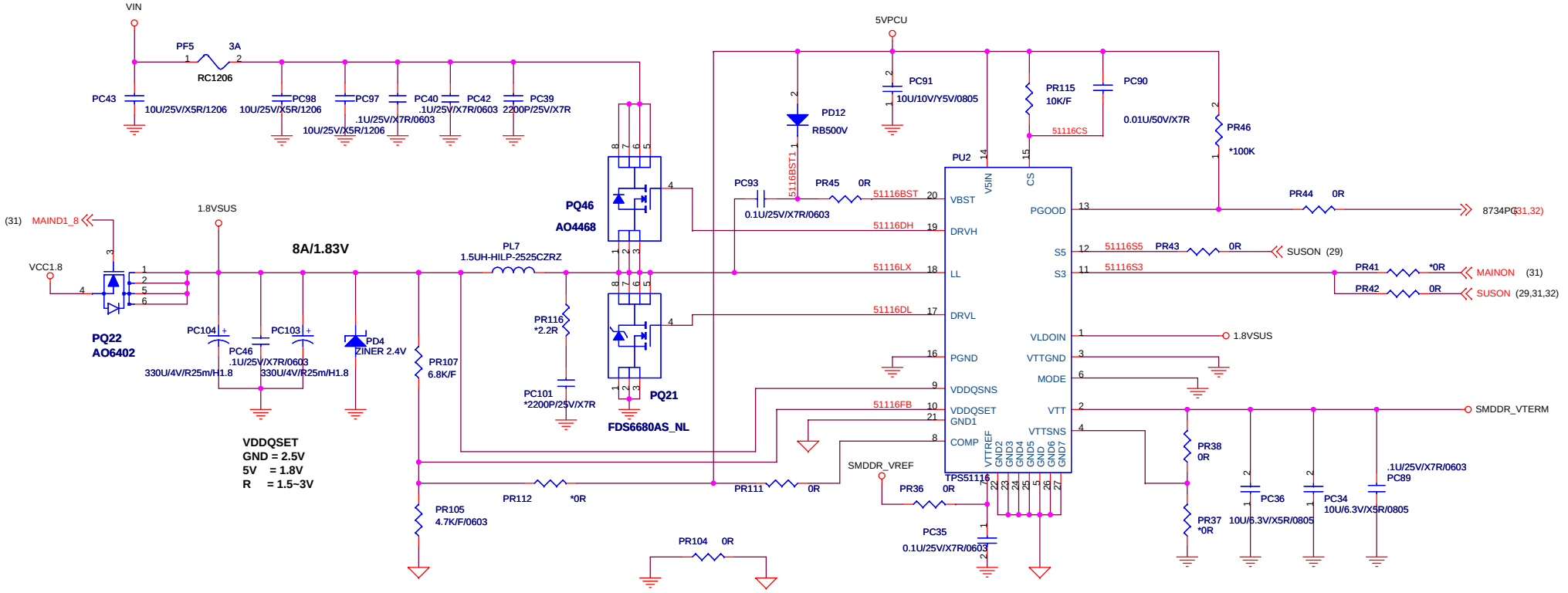


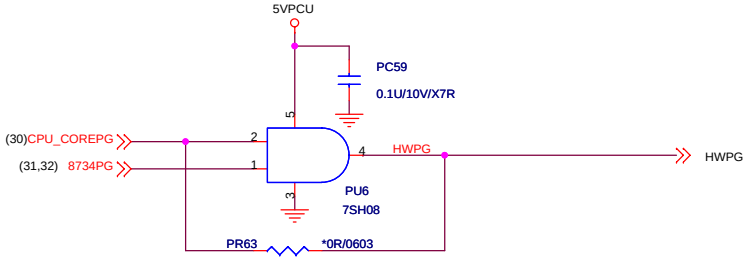
VLDT_RUN



Quanta Computer Inc. PROJECT : ES2		
Size	Document Number POWER 1.2V/1.5V/2.5V	Rev A
Date: Friday, October 26, 2007	Sheet 33 of 37	

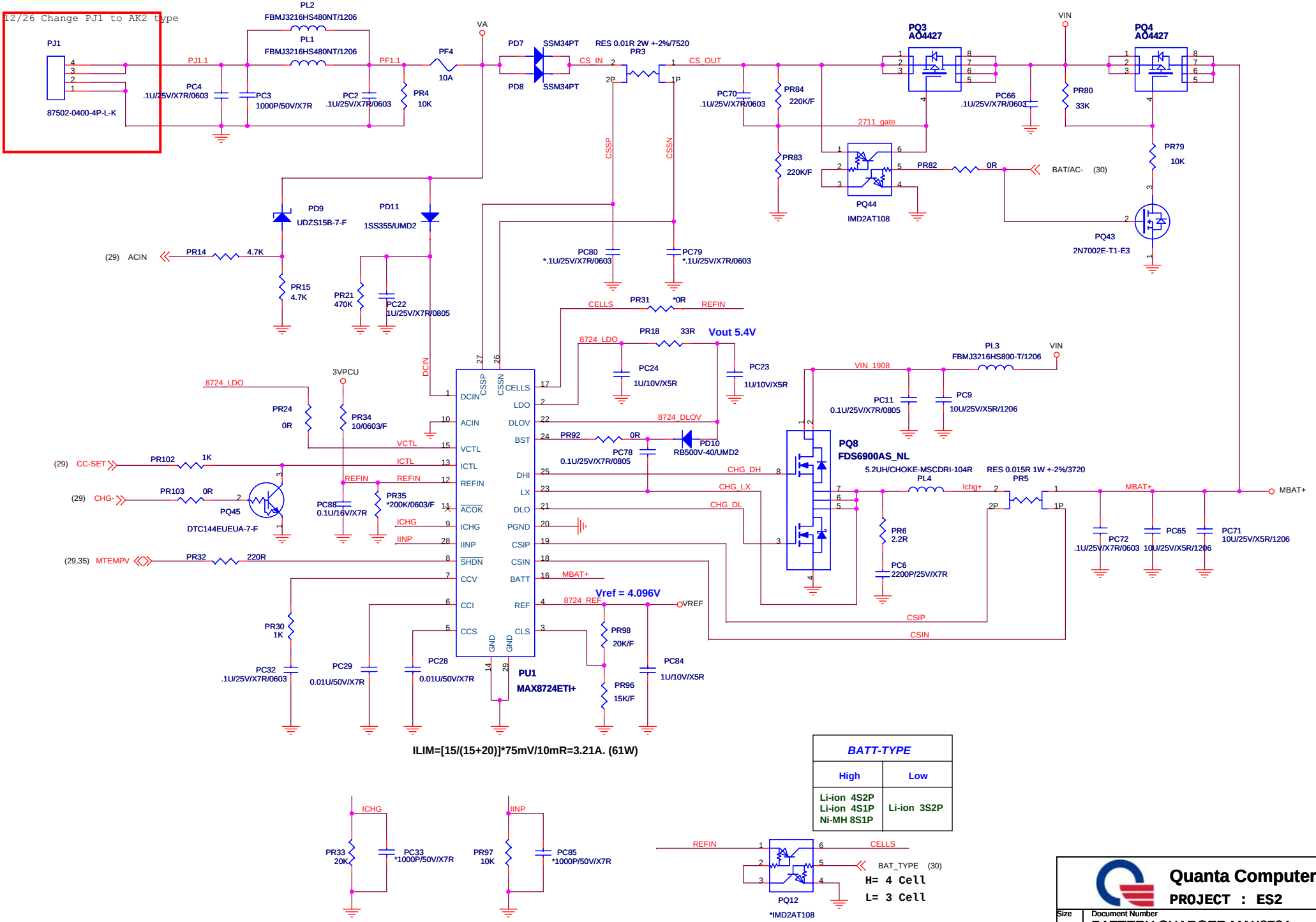
1.8VSUS & VTERM(DDR2) & VCC1.8





Quanta Computer Inc.		
PROJECT : ES2		
Size	Document Number: POWER 1.8VSUS/DDR VTERM	Rev: A
Date: Friday, October 26, 2007	Sheet 34 of 37	

Battery Charger



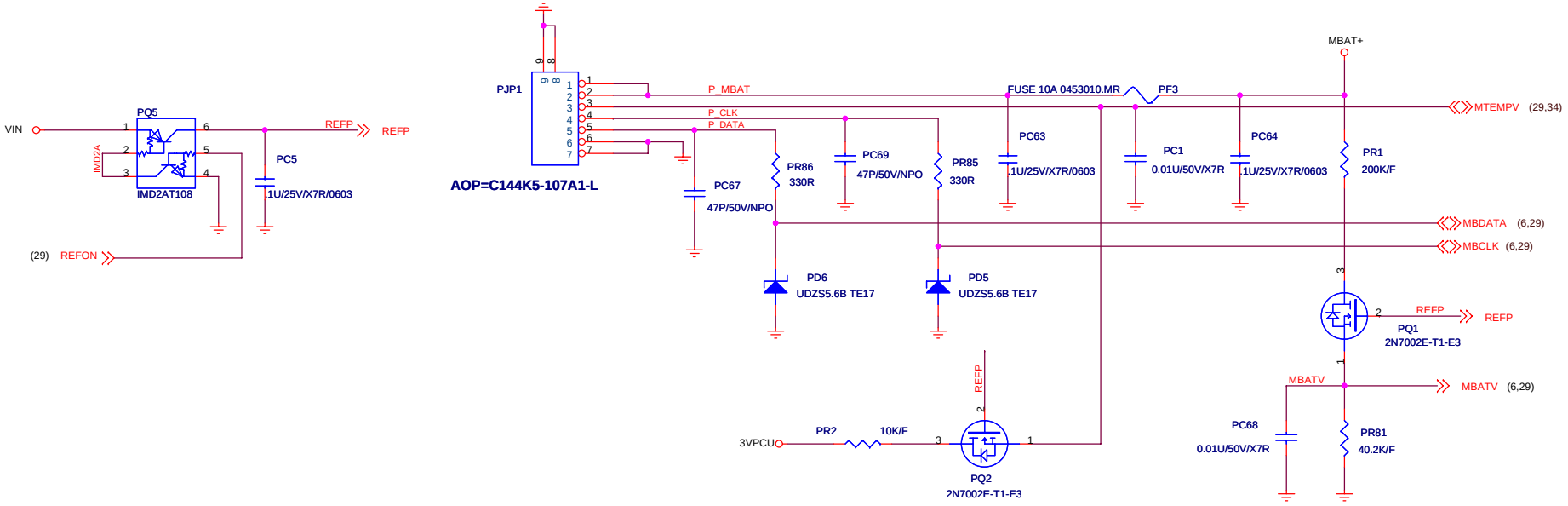
BATT-TYPE	
High	Low
Li-ion 4S2P Li-ion 4S1P Ni-MH 8S1P	Li-ion 3S2P

Quanta Computer Inc.

PROJECT : ES2

Size	Document Number	Rev
	BATTERY CHARGER MAX8724	A
Date: Friday, October 26, 2007	Sheet 35 of 37	

Battery Connector



MTEMPV voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :

16.8V*40.2/(200+40.2)= 2.812V

12.0V*40.2/(200+40.2)= 2.008V

8.0V*40.2/(200+40.2)= 1.34V

EC1012_1 PAGE 6 add message circuit
EC1012_2 PAGE23 add lan_RST

Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Friday, October 26, 2007	Sheet 37 of 37	