

AN4105

Flyback Converter Design Guide with SPS

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PD division

Understanding the Basic Operation

The purpose of this note is to provide an understanding of power circuits that are used in the SMPS.

1. The Transformer

1.1 The Need for a Transformer

There are three reasons for needing a transformer in the power conversion circuit.

The first is for safety. For a power source, a large voltage, applied between the ground and rectified voltages, can cause an electric shock. However, after isolating the primary and secondary sides with a transformer and grounding the output voltage GND, and then connecting it to an electronic mechanism, the electronic mechanism would be safe to touch.

The second reason is for voltage conversion. For example, if a DC/DC converter (Buck Converter), Figure 1 (b), switching at 50kHz is used to obtain 5V from 100V, the control circuit must control a short time of around 1 μ s, which is not an easy task. Even if this was possible, the internal voltage and current of each element increases, greatly reducing efficiency. The problem aggregates if the output current is large. In such case, as shown in the circuit diagram of figure 1(b), using a transformer to lower the voltage to 10V and then controlling the time of around 10 μ s is beneficial in aspects of cost and efficiency.

The third is for potential fluctuations. For example, though all control in a 1000V electronic mechanism occurs at the 5V power source on the GND side, a transformer is absolutely required if power is needed for either current sensing at the 1000V side terminal or for other controls. If the isolation voltage between the windings is sufficient, a 1000V potential difference is maintained between the first and secondary windings and power can be delivered. Furthermore, a transformer is absolutely required if the power GND has a sudden potential fluctuation like the half-bridge converter gate-drive power source.

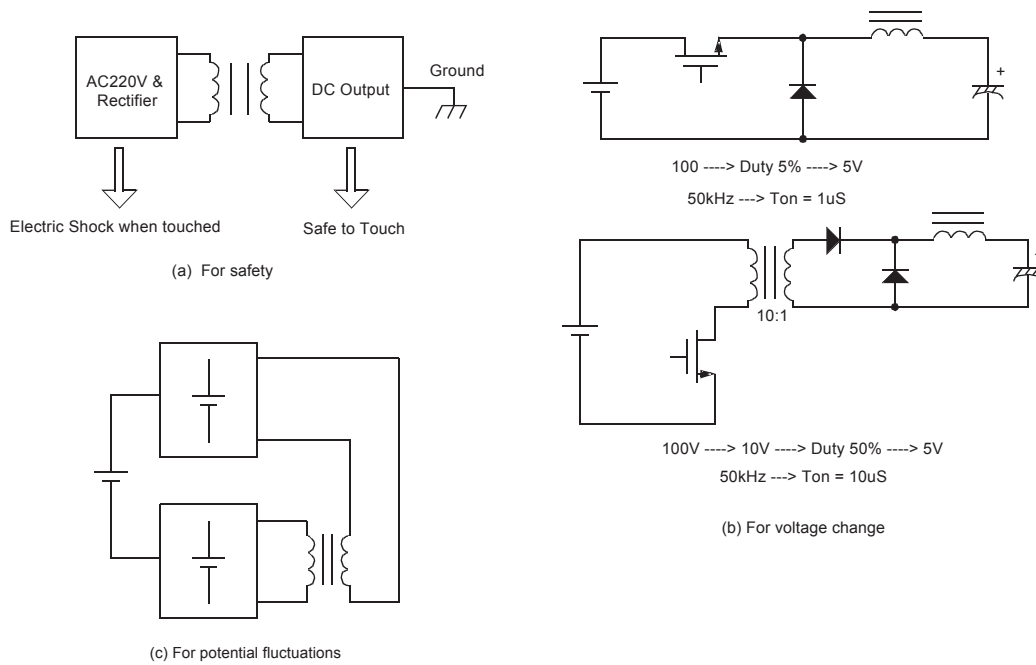


Figure 1. Need for transformer

1.2 The ideal transformer

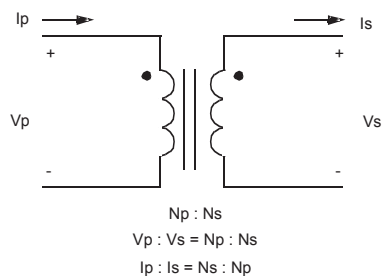


Figure 2. Ideal Transformer

The transformer is a circuit device that uses induction coupling between the windings to deliver power or electric signals. If necessary, it can isolate the primary and the secondary sides and raise or lower the voltage. The ideal transformer that describes the transformer concept is shown in the circuit diagram of Figure 2. An ideal transformer is an imaginary transformer that satisfies the following three conditions.

- i) The coupling coefficient between each coil is 1. (The leakage flux is 0.)
- ii) The coil loss is 0.
- iii) The inductance of each coil is infinite.

The input/output voltage ratio of an ideal transformer is proportional to the winding ratio, and polarity corresponds to the direction of the dot. The current ratio is proportional to the inverse winding ratio and current direction is such that if current enters from one side, it leaves at another. Then, the sum of NI that flows into the dot is 0. (The dot, indicating the coil polarity, is placed to make the flux direction in the transformer core uniform when current flows into the dot.) Furthermore, in the case of an ideal transformer, if the path of the secondary side windings is cut off, the current on the primary side becomes 0.

1.3 The actual transformer

There is significant difference between the actual and ideal transformer.

- i) The coupling coefficient between each coil is finite. Especially, when a gap is placed in the core as in the flyback trans, the coupling coefficient becomes even smaller. (There is a leakage flux.)
- ii) There are transformer losses such as iron loss (hysteresis loss), Eddy Current loss and coil resistance loss etc.
- iii) The inductance of each coil is finite. Especially, when a gap is placed in the core as in the flyback trans, the inductance becomes even smaller.

Even if the secondary side was opened, the current flows to the primary side because of iii) above. This means that energy is not stored in an ideal transformer, but is stored in an actual transformer. The magnetizing inductance considers exactly this energy storage phenomena. The circuit below represents a transformer, which includes the magnetizing inductance, and is also called a total coupling transformer. The equivalent circuit below (Figure 4) is sufficient for understanding the above explanation so this should be enough for our discussion on the transformer and will end here. A detailed equivalent circuit and short description are placed in the next figure as reference.

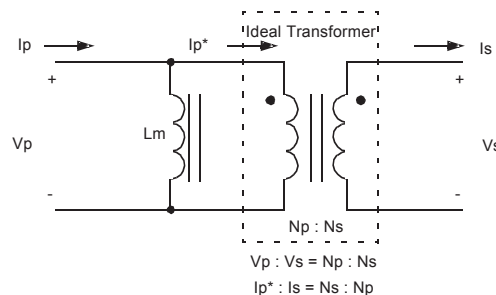
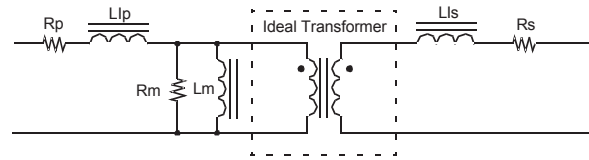


Figure 3. Complete Coupling Transformer



- Rp: primary side winding resistance
- Rs: secondary side winding resistance
- Llp: primary side leakage inductance
- Lls: secondary side leakage inductance
- Lm: magnetizing inductance
- Rm: transformer core loss resistance

Figure 4. Actual transformer equivalent circuit

2. Basic Operation of the Flyback Converter

2.1 Continuous Conduction Mode(CCM)

When the inductor current operates always greater than zero within one switching cycle, this is called the Continuous Conduction Mode. CCM stands for the Continuous Conduction Mode. The following is a short explanation of the operating wave forms (Figure 6).

1) $t_0 \sim t_1 = T_{ON}$

The MOSFET is turned on at t_0 . Just before, the inductor current flowed through D and D turns off when MOSFET turns on. Because MOSFET turns on, V_{DS} becomes zero and V_D becomes $(V_O + V_i/n)$. In this interval, V_i is applied to L_m so that I_{Lm} increases in a straight line with the following slope. The output voltage V_O can be viewed as the DC voltage.

$$\text{Slope} = \frac{V_i}{L_m}$$

When energy flow is examined, the input power source supplies energy to L_m during this interval. Therefore, because the L_m energy increases and output terminal separates from the input terminal, C_O supplies the output current during this interval.

2) $t_1 \sim t_2 = T_{OFF}$

The MOSFET is turned off at t_1 . The inductor current that flowed to the MOSFET starts flowing through D the instant the MOSFET turns off. When D turns on, V_{DS} becomes $(V_i + nV_O)$. During this interval $-nV_O$ voltage is applied to L_m so that I_{Lm} decreases in a straight line with the following slope.

$$\text{Slope} = \frac{nV_O}{L_m}$$

When the energy flow is examined, the inductor energy is delivered to the output during this interval. Namely, the amount of L_m energy that is reduced is the amount of energy delivered to the output. When the MOSFET turns on again at t_2 , one switching cycle will end.

3) Relationship of Input and Output

The colored areas, A and B, in the diagram of the Figure 6 must be equal because the average voltage of the inductor or transformer in steady state is always 0 so

$$V_i T_{ON} = n V_O T_{OFF}$$

$$\frac{n V_O}{V_i} = \frac{T_{ON}}{T_{OFF}} = \frac{D}{D-1}$$

The input and output currents become

$$I_i = D I_{Lm, AVG}$$

$$I_O = n(1 - D) I_{Lm, AVG}$$

making the input and output powers equal. An ideal wave form appears in the equivalent circuit below because the effect of leakage inductance is not considered, but, in actuality, much ringing is produced because of this effect.

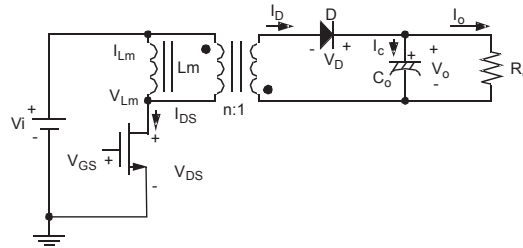


Figure 5. Basic topology of flyback converter

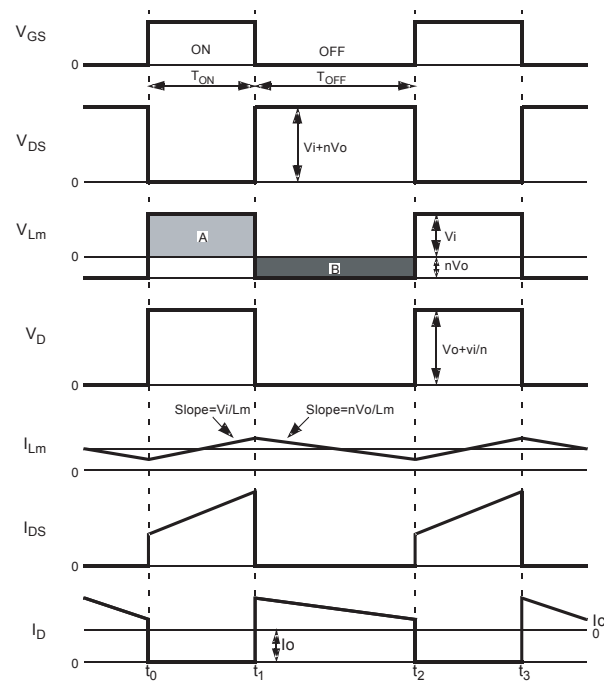


Figure 6. Operating waveform (continuous current)

2.2 Discontinuous Conduction Mode(DCM)

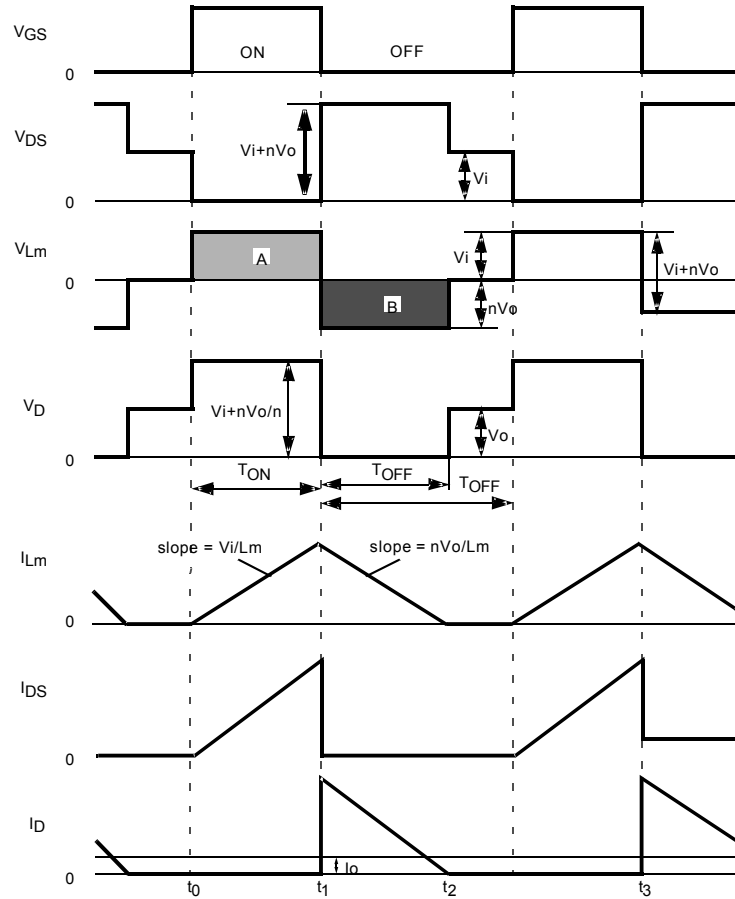


Figure 7. The operating wave forms (discontinuous current)

The appearance of the interval in which the inductor current becomes zero during one switching cycle, is called a Discontinuous Conduction Mode. DCM stands for the Discontinuous Conduction Mode. As shown in the above wave form, the voltage wave form, applied to the inductor, becomes somewhat complex in the discontinues conduction mode. If the concept of T_{OFF} was used, the equation is simplified but actually difficult to calculate. Three input and output relationships of a converter are derived by using T_{OFF} * and the fact that the average inductor voltage is zero and again by using I_O .

The boundary condition of DCM and CCM becomes

$$I_i + I_O = \frac{V_i}{2L_m} T_{ON}$$

The following input/output relationship in DCM is derived by using the fact that the colored areas A and B in the diagram of Figure 7 must always be equal because the average inductor (or transformer) voltage always becomes zero in steady state.

$$V_i T_{ON} = n V_O T_{OFF}^*$$

$$\frac{V_O}{V_i} = \frac{T_{ON}}{T_{OFF}^*} = \frac{D^*}{1 - D^*}$$

When the above equation is derived again using IO and the fact that input and output power are equal, it becomes the following.

$$V_O = \frac{(V_i T_{ON})^2}{2 \frac{I_O}{n} L_m (T_{ON} + T_{OFF}) + V_i}$$

The equation below is often used to represent the input power.

$$P_{IN} = \frac{1}{2} L_m I_{Lm, (peak)}^2 f_{sw}$$

Flyback Converter Design

Most SMPS used in power sources are equipped with a flyback converter. The purpose of this section is to establish the design concept of the flyback converter.

1. Selection of the Operating Point

1.1 Determination of the winding ratio

The coil ratio of the flyback converter transformer is an important variable that affects the voltage and current amounts of the primary side switching device and of the secondary side rectified diode and the number of windings and current amount of the transformer itself. Among the frequently written about design concepts, there is a concept of operating it at maximum duty when the input voltage is minimum. For simplified calculation, assume that it changes as below and we will look at the coil winding dependent voltage and current of each device.

- AC input voltage: 85V~265V
- DC rectified voltage: 100V~400V
- Output voltage: 50V
- Inductor current: Continuous Conduction Mode

The input power of the DC source is the product of the DC voltage and average input current. Furthermore, using wide duty to deliver equal average current reduces the actual efficiency of the current. In the case of a small operating with narrow duty, increases the effective current on the primary side making the MOSFET and primary side coil heat to increase. The primary side is inverse of the secondary side. The voltage becomes inverse of the current.

It is a relationship in which the voltage reduces and current increases. In addition, it is best to decide n based on the device used, but if the primary side MOSFET pressure is on the small side (for example, 600V level), make the n small or if the pressure is sufficiently large (for example, 800V level), make the n large. If n increases, not only does primary side current of the switching device reduce, but, also, the secondary side rectified diode pressure reduces. The bigger the output voltage and more number of secondary side outputs, it could be advantageous to increase n . Discussions about the MOSFET internal pressure and Avalanche Energy will be held at another time.

1.2 Determination of the Operating Current Mode

As explained previously, there are two types of operating current mode in the flyback converter - the continuous conduction mode and discontinuous conduction mode. An appropriate design method, following the overall operating conditions, will be examined by reviewing the advantages and disadvantages of the two operating modes, herein.

Characteristics of the Discontinuous Conduction Mode

In the flyback converter design, if a discontinuous conduction is made even at minimum input and maximum output, then a discontinuous conduction is made of all input conditions. It is advantageous in many aspects to express the flyback converter input power in discontinuous conduction mode as,

$$P_I = \frac{1}{2} L_m I_P^2 f_{sw}$$

Regardless of the changes in the input voltage, this indicates that the input current is limited by the peak value of the current flowing through the transformer primary side MOSFET. When SPS is used, it can execute an over-current protection feature for all the input current to prevent the output current from flowing over a fixed value without requiring separate, additional circuit. As compared to the continuous conduction mode having an average current value, the discontinuous conduction mode operation in all cases, requiring the use of thicker coils due to rise in effective current doesn't bring an advantage in view of the transformer. Furthermore, there is no advantage because the primary side MOSFET heat increases from the large effective current.

The gain from operating in the discontinuous conduction mode is that a slow secondary side rectified diode (low price) can be used. Furthermore, the discontinuous conduction mode has a fixed operating current has this gain at the low frequency where core loss is not a problem (because minimum number of coils can be wound) and turn-on loss is not a serious problem because of low input amount (because Eddy Current losses such as skin effect and proximity effect etc. do not arise significantly).

Characteristics of the Continuous Conduction Mode

From the transformer's point of view the advantage of operating through the continuous conduction mode is that thinner coils can be used because coil's effective current decreased even though there were a lot of coils. Furthermore, the primary side MOSFET heating reduces due to the small effective current, which is advantageous, the bigger the amount of input average current. However, in continuous conduction, the reverse recovery current, depending on the secondary side rectified diode reverse recovery time (t_{rr}), brings large internal pressure increase and loss to diode end terminals. Therefore, within the allowable cost range, a diode with a minimum t_{rr} must be used.

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<p> V_{DS} $nV_O = 67V$ $V_i = 100V$ V_D $V_i/n = 75V$ $V_O = 50V$ $V_{DS} = 167V$ $V_D = 125V$ </p>	<p> V_{DS} $nV_O = 67V$ $V_i = 400V$ V_D $V_i/n = 267V$ $V_O = 50V$ $V_{DS} = 467V$ $V_D = 317V$ </p>	<ul style="list-style-type: none"> - Voltage applied to switching device is small. - effective current of switching device and primary side winding is large. - Voltage applied to the rectified diode is large. - Output voltage ripple is small. - Control must be done through short turn-on time.
<p> V_{DS} $nV_O = 100V$ $V_i = 100V$ V_D $V_i/n = 50V$ $V_O = 50V$ $V_{DS} = 200V$ $V_D = 100V$ </p>	<p> V_{DS} $nV_O = 100V$ $V_i = 400V$ V_D $V_i/n = 200V$ $V_O = 50V$ $V_{DS} = 500V$ $V_D = 250V$ </p>	<p>Intermediate Design Method</p>
<p> V_{DS} $nV_O = 150V$ $V_i = 100V$ V_D $V_i/n = 33V$ $V_O = 50V$ $V_{DS} = 250V$ $V_D = 83V$ </p>	<p> V_{DS} $nV_O = 150V$ $V_i = 400V$ V_D $V_i/n = 133V$ $V_O = 50V$ $V_{DS} = 550V$ $V_D = 183V$ </p>	<ul style="list-style-type: none"> - Voltage applied to switching device is small. - Voltage applied to switching device is large. - effective current of switching device and primary side winding is small. - Voltage applied to the rectified diode is small. - Output voltage ripple is large. - Control must be done through long turn-on time.

Table 1. Voltage rating of switching device in primary side and diode in secondary side according to winding ratio

Appropriate Trade-Off

As can be understood from the above, discontinuous conduction is advantageous in terms of cost and efficiency if the inputs amount is small and precise control of the input power through the primary side switch (MOSFET) current is required. On the other hand, if the input amount is large and switching turn on loss could be a major problem, a continuous conduction mode design would be more advantageous. Therefore, an appropriate trade off is required fitting the characteristics of the system to be designed.

2. Transformer Design

2.1 Selection of the Core

The maximum power (transformer) that the core can deliver or the maximum energy (inductor) that it can store depends on the shape and size of the core. Generally, because the minimum number of coils to be wound reduces (or can apply a larger voltage) as the effective cross-sectional area (A_c) gets bigger, more power can be delivered. Also, if the window area (A_w) on which the coils can be wound gets bigger, more number of coils (more voltage can be applied) and thicker coils (more current flow) can be wound, which allows that much more power to be delivered. The product of A_w and A_c is called the Area Product (AP). In case of the transform, the maximum power that can be delivered is proportional to the exponential of AP. The latest transformer design theories include designs which depend almost entirely on the AP.

From a wider perspective, the fly back converter transformer (herein, the flyback trans) is a coupled inductor so it's common to design it following inductor design methods. Equation a) below, a calculation method based on whether or not the core is saturated, is comparatively appropriate at low frequency and equation b), limited by core loss, is appropriate at high frequency. After calculating the area product using both equations, the equation that gives the higher value must be used. The equation below is derived ignoring the core loss (iron loss) and assuming that all losses are wire losses.

$$AP = \left(\frac{L I_P I_{RM} 10^4}{420 K B_{MAX}} \right)^{1.31} [\text{cm}^2] \quad \text{a)}$$

L and B_{MAX} are in H and Tesla units, respectively, and K is listed in the next table. In the above equation the current density (J) per unit area of wire is obtained from the current by the relationship below which assumes that the inductor Hot Spot temperature increases to 30°C more than its surrounding.

$$J_{30} = 420 AP^{-0.24} [\text{A}/\text{cm}^2]$$

If actually the operating frequency increases making the flux shift band the saturation flux density, the core losses become too big. The following equation, derived from the transformer loss of 50% iron and 50% wire, must be used.

$$AP = \left(\frac{L \Delta I_m I_{RMS} 10^4}{K_H f_{SW} + K_E f_{SW}^2} \right)^{1.58} (K_H f_{SW} + K_E f_{SW}^2)^{0.66} [\text{cm}^4] \quad \text{b)}$$

though most ferrite cores sold in the market have Hysteresis Coefficient k_H of 4×10^{-5} and Eddy Current Coefficient k_E of 4×10^{-10} , few errors are generated. The current density relationship used here assumes that the hot spot temperature increases 15°C more than its surroundings (iron loss increasing the remaining 15°C). The following equation is used.

$$J_{30} = 297AP^{-0.24} \text{ [A/cm}^2\text{]}$$

Next is a description of K . Like the table below, K is the product of the Window Utilization Factor K_U and Primary Area Factor K_P .

K_U is the percentage of how much the cross sectional area of the copper, used for the windings, takes up of the entire window area. K_U makes the isolation pressure between the primary and secondary sides follow the safety standards and becomes about 0.4 as shown in the table below if a general bobbin is used. Because this parameter is related to the transformer shape and winding method, one should know the K_U of the transformer that one usually uses. It greatly varies depending especially on how much of the safety standards are followed.

K_P is the percentage of how much area the primary winding takes up of the entire winding.

It is 1 for the inductor because it has no secondary side windings and usually 0.5 for the flyback trans type coupled inductor, which has the highest efficiency when the primary and secondary winding areas are equal. However, when there is more secondary side windings, it can have a lower value.

Three parameters J , K_U , K_P depend on the designer's experience when obtaining AP from the above equations a) and b). Precisely knowing the values of these three parameters within one's application reduces the number of trial/error when designing the flyback trans, quickly and effectively.

Table 2. K factor

	K_U	K_P	$K = K_U K_P$
Continuous Buck, Boost Inductor	0.7	1.0	.7
Discontinuous Buck, Boost Inductor	0.7	1.0	0.7
Continuous Flyback Transformer	0.4	0.5	0.2
Discontinuous Flyback Transformer	0.4	0.5	0.2

2.2 Determination of the Number of Windings

For the transformer, the equation for the minimum number of windings can be determined with the applied voltage and maximum turn on time, but the same equation can also be derived from the relationship between L and I_p . When AP was obtained by equation a) above, N is calculated from

$$N_{\text{MIN}} = \frac{L I_p}{B_{\text{MAX}} A_C} 10^4$$

$$N_{\text{MIN}} = \frac{L \Delta I_m}{\Delta B_m A_C} 10^4$$

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2.3 The coils

The coil cross sectional area must be obtained from the number of windings, determined by the equations above, the effective current calculated and the current density equation that one used. Just divide the effective current by the current density. This determines the coil thickness if Eddy Current loss is not a serious problem, but if the coil becomes thicker, the problem of Eddy current loss cannot be avoided. Using twisted thin coil strands (Litz wire) instead of a thick wire can reduce the Eddy current loss, but K_u becomes smaller

2.4 Determination of the Gap

It is not easy to calculate precisely the actual required gap. If the gap, calculated from the equation below based on the Fringing Effect of the surrounding flux, was used, it is common to calculate a L value larger than what is required.

$$l_g = \frac{u_o u_r N^2 A_c}{L} 10^{-2} [\text{cm}]$$

Therefore, the gap must be controlled to obtain the required L value.

Internal Block Diagram and Basic Operation of SPS

1. Block Diagram of SPS

A block diagram of the SPS internals is presented below. As revealed by the below diagram, the internal is composed of the MOSFET (Sense FET or Mirror FET) equipped with current sensing feature and control IC. On the inside only the current sensing between the IC and MOSFET and gate operating circuit are connected by bonding wire, and, on the outside, five terminals extend out.

The IC internals can be divided into large sections-the UVLO, reference voltage, oscillator (OSC), PWM block, protection circuits and gate operating circuits. The operation of each block is as follows.

1.1 UVLO (Under Voltage Lock Out)

To guarantee stable operation of the control circuit, the UVLO circuit stops the control circuit when V_{cc} voltage is lower than the fixed level (10V) and starts it when V_{cc} is above the fixed level (15V). Once the control circuit starts operating, the V_{cc} must become lower than the fixed level (10V) for UVLO to stop the circuit. The Figure 9 and Figure 10 are the UVLO block diagram and its start-up waveform. The critical turn on / off voltage are fixed internally at 15V and 10V, respectively.

A 5V hysteresis makes the IC start-up simple. The IC was designed to consume a small amount of current (start up current, lower than 300 μ A) before starting. If it started operating after C_{CC} charges to 15V, it can continue operating until the V_{CC} voltage discharges to 10V by designing to allow only a small amount of current lower than 1mA to flow in through the start up resistor. The IC can continue operating if it receives its operating current through the line connected to the V_{CC} by increasing the output voltage during this time. By doing this, during normal operation, the current dissipation due to the SMPS start up resistor can be reduced.

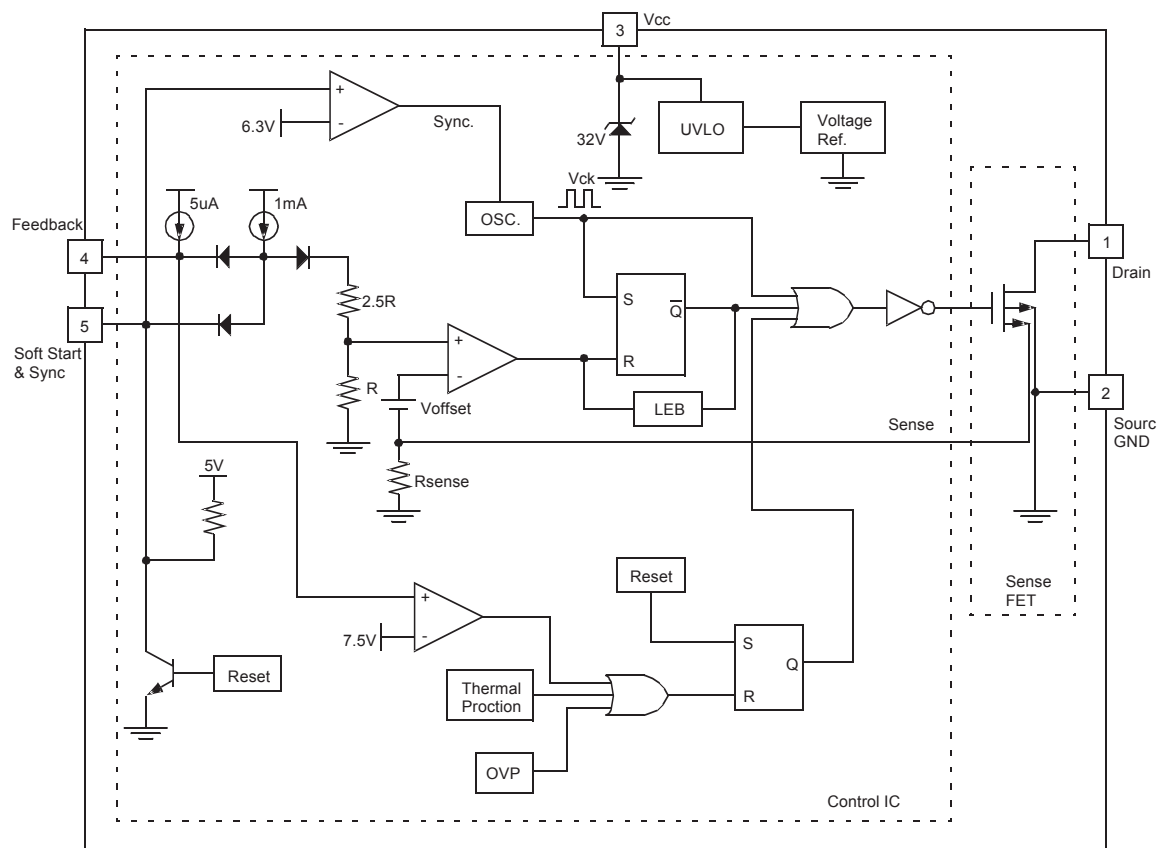


Figure 8. Internal block diagram of SPS

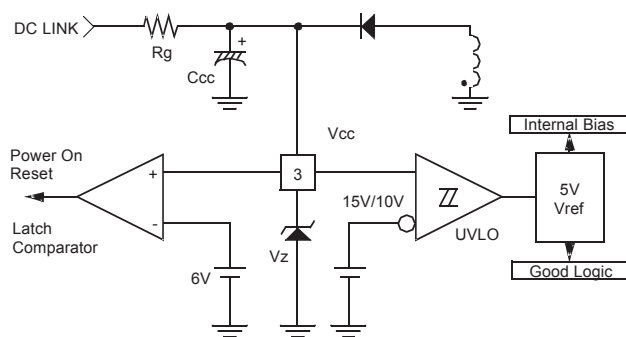


Figure 9. UVLO block diagram

The gate operating circuit maintains at low state during UVLO, thereby maintaining the Sense-FET at turn off.

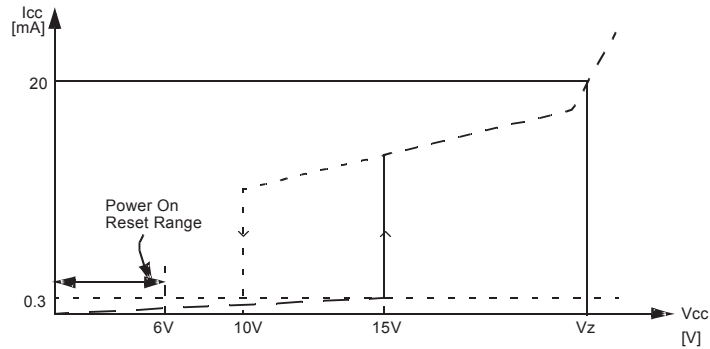


Figure 10. Start-up waveform

1.2 Feedback Control Circuit

Basically, the SPS has the current control (Current Mode PWM). Essentially, the control circuit was made to operate such that the MOSFET current becomes proportional to the feedback voltage. By doing this, the MOSFET current can be limited at every cycle and other characteristics can be gained such as good line regulation of the output voltage related to the input voltage change.

Furthermore, good control characteristics can be gained even in the wide synchronized frequency range like a monitor.

As shown in the diagram of Figure 11, the internal oscillator oscillates at the fixed frequency, synchronized to an external signal and turns on the MOSFET. The feedback comparator repeats its operation to turn it off again when the MOSFET current becomes a fixed value proportional to V_{fb} . The MOSFET turn-off operation is as follows. $V_{fb}^* = V_{fb}/3.5$ and a current proportional to the drain current flow to the Sense - FET sense terminal making V_{sense} proportional to the drain current. When V_{sense} becomes greater than V_{fb} , the output of the feedback comparator output becomes high, turning off the MOSFET.*

As shown in the circuit below, if the error amp in the control circuit is eliminated and, instead, a terminal with a current source is placed as a feedback terminal, it becomes a most appropriate circuit with good control characteristics for the Off line SMPS feedback circuit which always uses a photocoupler due to the isolation pressure between the primary and secondary sides. The C_{fb} for better noise characteristics and photocoupler CE terminal can be attached parallel to the feedback terminal, but, if an error amp is equipped as was in KA3842, a resistor and condenser to give feedback to the error amp must be installed additionally to obtain the same functions produced by the diagram of Figure 11. Fine control the V_{fb} to control the output voltage. As a widely used error amplifier at the output side, the Shunt Regulator, KA431, is also an appropriate IC for this type of characteristics. Considering the cost, a Zener diode can be used to configure the output feedback circuit.

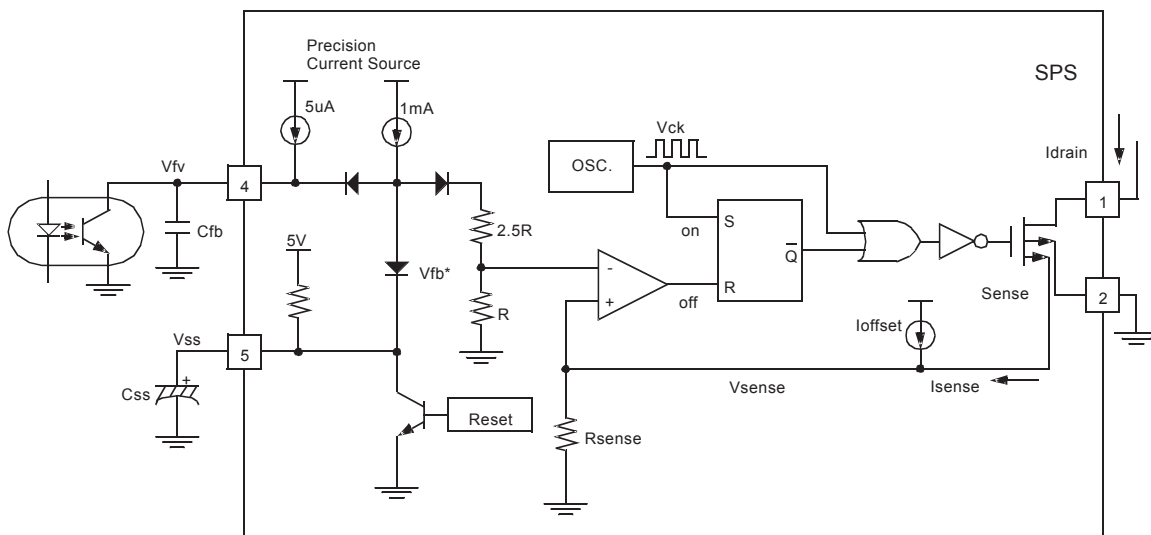


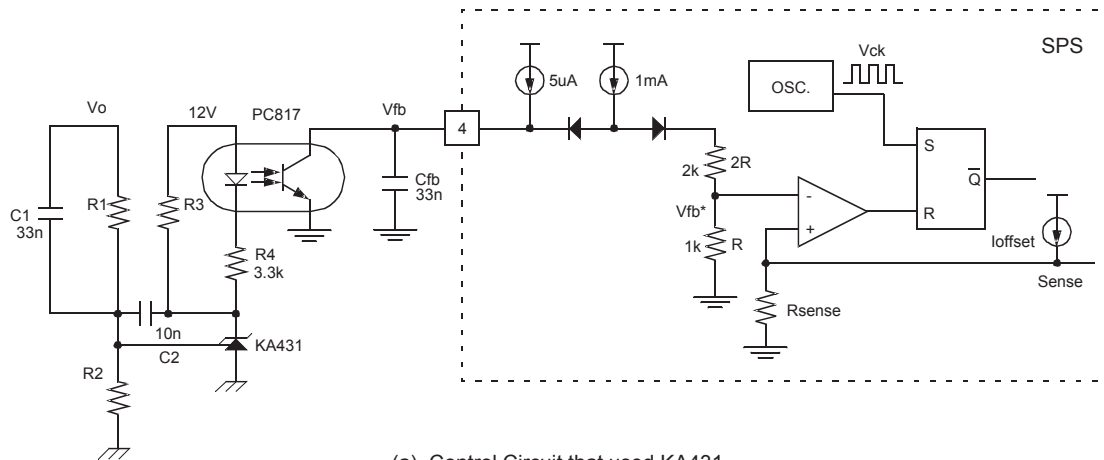
Figure 11. SPS feedback circuit appropriate for the off-line SMPS (current mode PWM)

1.3 Example of the SPS Control Circuit

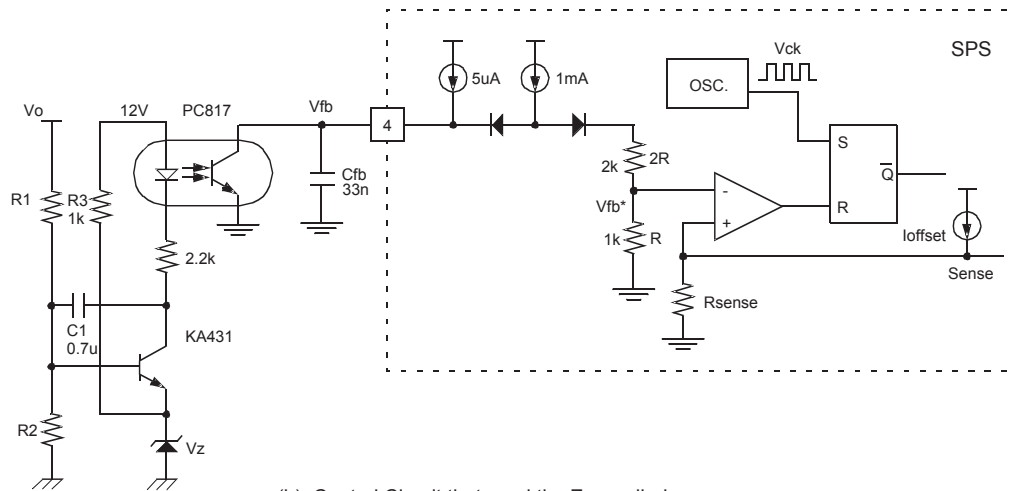
The following diagram (Figure 12) represents the SPS control circuit. The (a) design uses the KA431 and (b) uses the Zener diode. Though differences among the diodes exist and constant voltage characteristics are slightly poorer, a design using the Zener diode is cost advantageous.

C1, in the diagram (a) below, together with R1 produces a zero point to compensate the pole formed by SPS internal resistor 3.5k Ohms and Cfb. There would be no safety problems if the zero point did not exist but was only added to improve the dynamic response; C1 could be taken out, as done in diagram (b). C2 sufficiently increases the loop gain at low frequency, improving the output voltage load regulation due to load fluctuations. The R3, through KA431 bias resistor, can make the photodiode current even almost zero. The R4 can limit the maximum current of the photodiode, the maximum current being $(12-2.5-2)/3.3k$ about 2.3mA, where the 2.5 is KA431's saturation voltage and 2 is the photodiode's voltage drop. The Cfb should be determined by considering the shut-down delay time, to be mentioned later.

The R3 in diagram b) flows a fixed current to the Zener diode to stabilize the Zener voltage.



(a). Control Circuit that used KA431



(b). Control Circuit that used the Zener diode

Figure 12. SPS feedback control circuit

1.4 Soft Start

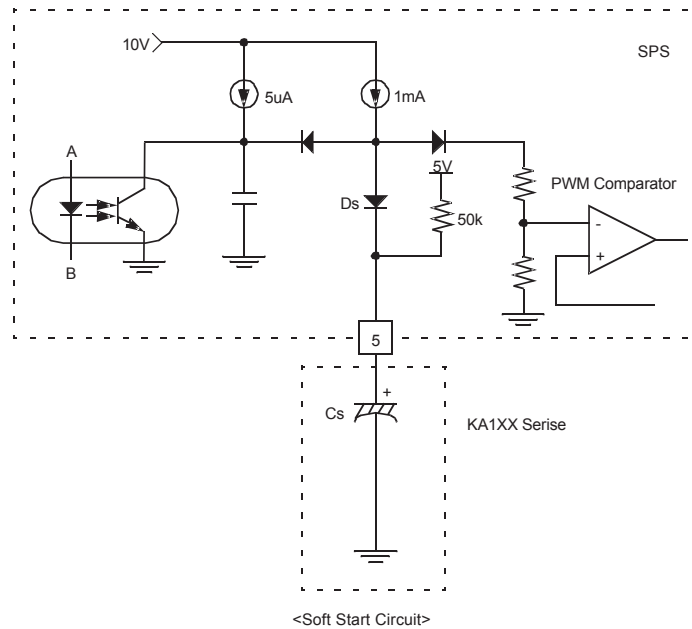


Figure 13. Soft start circuit

Generally, the output voltage increases with a fixed time constant at start up due to the capacitive load component existing at the output side of SMPS. Because of this, at start up, the feedback signal applied to the PWM comparator's inverting terminal becomes the maximum value of 1V because the feedback loop looks open. During this time, the drain current maintains at a peak value (I_{PEAK}) delivering maximum- allowable power to the secondary load side. Generally if the SMPS pushes in maximum power to the secondary side for a fixed time initially, this puts serious stress on the entire circuit. To avoid such operation, soft start function is required.

The Fairchild Power Switch adopts the soft start circuit, as in the Figure 13. When the operation starts, the soft start capacitor, Cs, starts to charge through 1mA current source and 5V, 50kΩ. When Cs voltage reaches above 3V, the diode Ds turns off and no more current flows in from the 1mA current source so charging to 5V must be done through the 50kΩ. Ultimately, the PWM comparator inverting terminal voltage becomes 1/3 the Cs potential and slowly starts to increase until the diode Ds turns off. Because of this, the maximum drain current value slowly increases following the inverting terminal voltage.

When Cs voltage becomes greater than 3V, diode Ds turns off, and the inverting terminal voltage does not follow the Cs voltage any further, but, instead, follows the output voltage feedback signal. In Shut-down or protection circuit operation, the capacitor C must be discharged, to enable it to charge from 0V at restart.

1.5 Synchronization

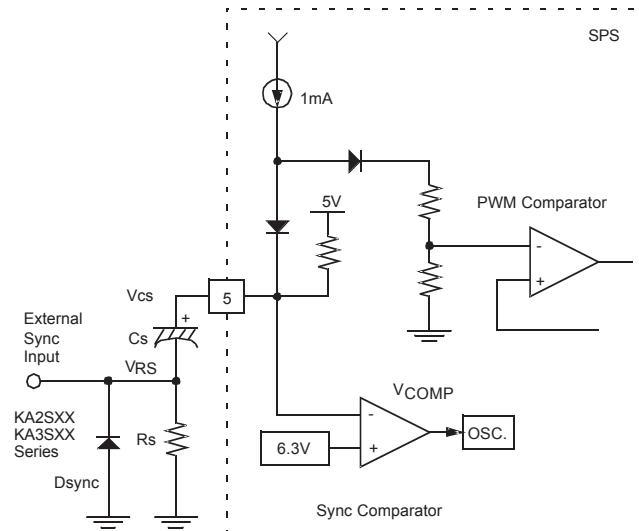


Figure 14. Synchronization circuit

The Sync, among the features of the Monitor SMPS, is a feature that is different from general SMPS. It synchronizes the SMP switching frequency with the sync frequency to prevent noise from appearing at the monitor display. It is common to use the flyback signal at monitor display horizontal scanning as an external sync frequency. Essentially, by precisely synchronizing the switching and horizontal scanning and combining the display noise due to switching to the far left of the monitor display, it prevents the noise from being visible.

Synchronization of the switching frequency based on external sync signal is executed as follows. The external sync signal, applied to the resistor R_s , does not drop below $-0.6V$ because of the diode, D_{sync} . After initial soft start finishes, the C_s voltage continues to remain at $5V$ until the external sync signal enters at which point it shows the shape of V_{RS} loaded to DC $5V$. The sync comparator compares V_{CS} with $6.3V$ and produces the comparator output waveform (V_{comp}) like in the diagram of Figure 15. When the IC internal timing capacitor C_t reaches the High Threshold during charging, it discharges following the oscillator internal discharge command. Then, when it reaches the Low Threshold, it starts to charge. The oscillator output waveform V_{ck} becomes low when C_t recharges and High when it discharges. This oscillator output signal is applied to the S/R Latch Set terminal.

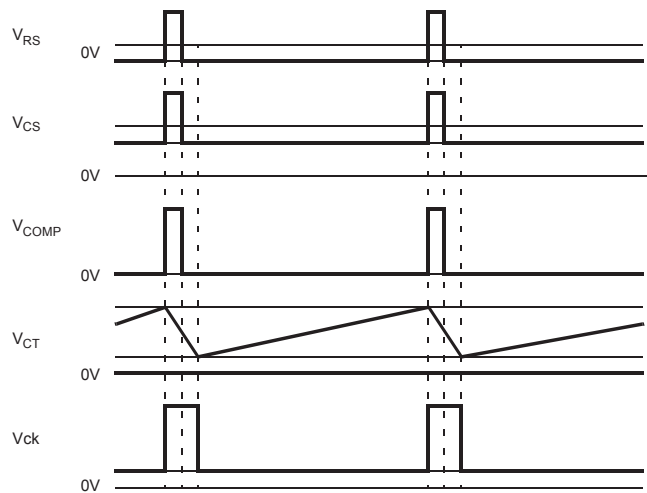


Figure 15. Synchronous circuit operation

If there is no external sync signal, C_t oscillates at the existing frequency (20kHz), but, if there is a sync signal, the Set signal becomes High because the V_{CT} charges to High Threshold following to the external sync signal, as Figure 15. Ultimately, the Set signal that determines the switching frequency is synchronized to the external sync signal frequency.

The following is the reason for limiting the Set signal's High Duration to within 5% of the full cycle. As the set signal drops to low, the gate turns on. As the switch turns on at this time, the switching noise appears on the screen. In SPS the set signal becomes high the sync is synchronized simultaneously with the horizontal scanning flyback time. Because the high duration is 5% of the full cycle, the starting of the horizontal scanning as the set signal drops to low turns on the switch. Therefore, the switch turn-on noise hides behind the display.

2. SPS Protection Circuit

Because the SPS has few self protective circuits not requiring additional external components, reliability is obtained without cost increase. After starting the protection circuit, it can completely stop the SMPS operation (Latch Mode Protection) until the power is turned off and connected again and can make the control voltage restart above ULVO when the latch released below ULVO (Auto Restart Mode Protection). As ordered items, these two operations can be selected by the user at the IC or can be selected by fine controlling the circuit number. The following are each of its functions and application methods.

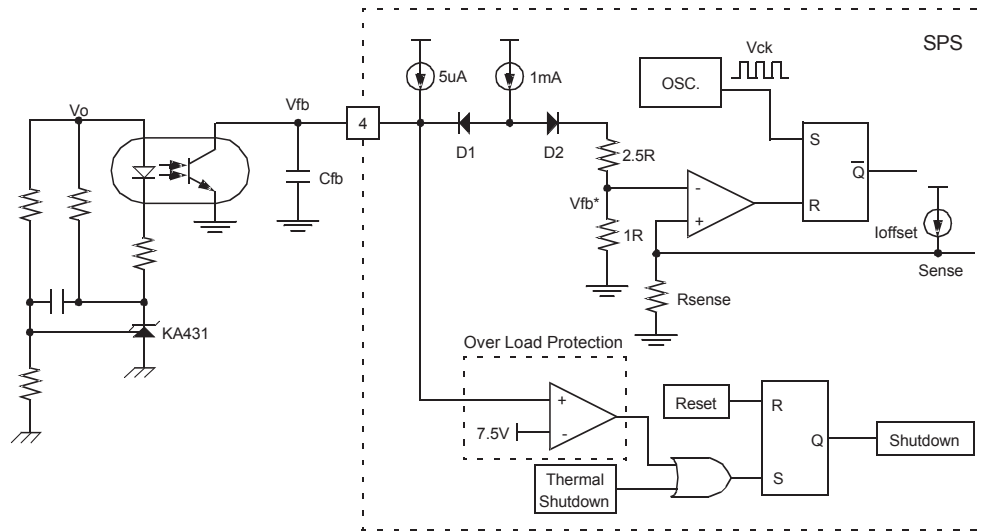


Figure 16. Over load protection circuit diagram

2.1 Over Load Protection

An overload and a load short circuit will be distinguished here. This is when a load suddenly becomes greater than the set load during normal operation. Essentially, the SPS overload protection circuit is a feature that makes the operation stop by itself when 110W flow out the SMPS output, designed to a maximum of 100W. If such a protective circuit is adopted, an operation, unwanted by the protective circuit, may be generated even at transient conditions. Therefore, SPS takes measures for this. In SPS, when it recognizes an overload, it waits for a specified time to determine whether the load is a transient or an overload, and then the protection circuit is made to operate. Because a transient state returns to normal state after a fixed time, the protection circuit was made not to function during that time. The above operations are carried out as follows.

Because the SPS has current control, it cannot have flows above the set maximum current so the maximum input power is limited to a specific voltage. Therefore, if the output consumes more than this power, the V_o (shown in the diagram of Figure 16) becomes smaller than the set voltage and KA431 can draw only the given minimum current. As a result, the photocoupler secondary current becomes almost zero. If all the current flows through the SPS 1mA current, the internal resistor ($2.5R + R = 3k$) then V_{fb} becomes about 3V and from that point on the 5 μ A source current starts to charge the C_{fb} . Because the photocoupler secondary current becomes almost zero, V_{fb} continues to increase and when it becomes 7.5V, the SPS shuts down.

The delay time to shutdown is time needed to charge C_{fb} to 4.5V through 5 μ A and can be easily decided. When C_{fb} is 10nF(103) and 0.1 μ F(104), t_2 is about 9.0mS and 90mS, respectively. With such times, it does not shut down for just an average transient. Just blindly making C_{fb} large, when a longer delay time is needed, can become a problem because C_{fb} is an important parameter that determines the SMPS response rate (Dynamic Response). In this case, the C_d series-connected to the Zener diode can be used as shown Figure 17(a). When V_{fb} is below 3V, a low C_{fb} makes the SMPS dynamic response good and above 3.9V, a large C_d can extend the delay time to shut-

down to what is desired. However, if good dynamic response is not required and transient is not significant, then it is better not to operate it, always having to add two components, as shown in Figure 17.

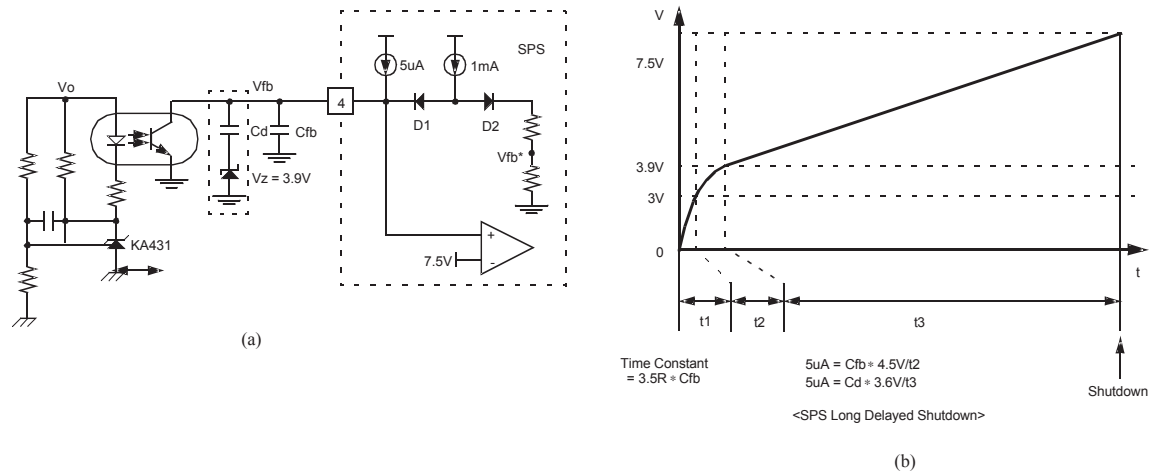
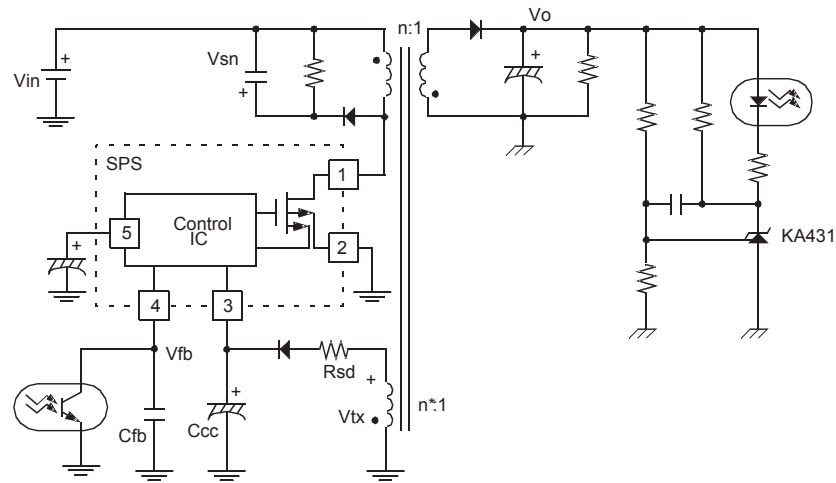


Figure 17. Long delayed shutdown

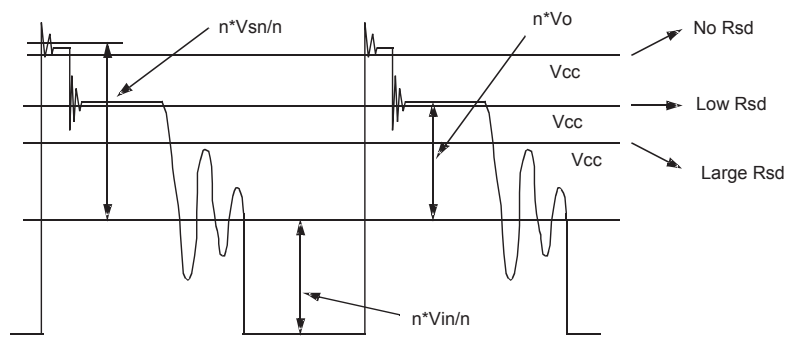
2.2 Output Short Circuit Protection

Even though the input current becomes maximum, when the output terminal is short-circuited, the output power does not maximize because an output short circuit means that its voltage is becoming almost zero. If the input current is limited to a value lower than the specified value when the output voltage is almost zero, it operates in the continuous conduction mode having very small duty and, though the input and output powers not very large, the output current has large movement. In this case, the output short circuit protection operates differently from the overload protection in 2.1.

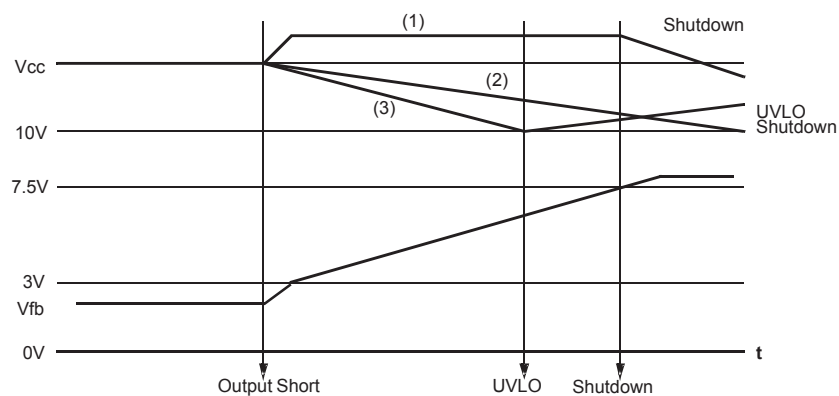
When the output voltage short circuits a relatively large winding, a situation is created in which the MOSFET current becomes much greater than I_{PEAK} because the magnetic inductor was unable to reset due to low transformer coil voltage at turn-off. Essentially, this occurs because the current left during SPS minimum turn on time at the magnetic inductor could not reduce by that amount during the remaining turn-off time. Even though it is a large current, it does not overstrain one MOSFET but greatly overstrains the secondary coils and the rectified diode.



(a) Flyback Converter



(b) Flyback Converter Control Winding Voltage and Rsd Dependent Vcc



(c) Vcc and Vfb waveforms Depending on the Relative Size of Cfb at output short circuit

Figure 18. Output short circuit protection circuit operation of the flyback converter (latch mode or intermittent mode operations)

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Most flyback or forward converters were designed to receive control power through the transformer support coils. Furthermore, it is common to make this voltage proportional to the output voltage as in diagram (a) on the next page. This is not so difficult because, for a flyback converter, the coil voltage when the switch turns off is proportional to the output voltage and, for a forward converter, the transformer average voltage at turn off is proportional to the output voltage. In this type of SMPS, by deciding well on the circuit number, the protection circuit can be operated through either latch mode or intermittent mode at output short circuit.

The change of V_{cc} depending on the magnitude of R_{sd} is shown in diagram (b) of Figure 18. When R_{sd} is zero, V_{cc} follows V_{tx} maximum value, proportional to $(n \cdot V_{sn}/n) V_{sn}$, which is proportional to the transformer maximum current, so that if the output short circuits, the V_{cc} rather increases, and after a specified delay time, the protection circuit operates and enters the latch mode. When R_{sd} becomes appropriately large, the V_{cc} can be made appropriately smaller than $n \cdot V_o$. If the output short circuits in such a case, the V_{cc} starts to reduce from that moment, but, if the C_{cc} is sufficiently large, V_{cc} maintains a voltage higher than UVLO's low critical voltage (10V) until V_{fb} becomes 7.5V (as in diagram (c)(2)) and the latch mode protection starts. If C_{cc} is sufficiently small, the V_{cc} approaches the UVLO's low critical voltage (10V) before V_{fb} becomes 7.5V as in diagram (c)(3), and instead of the protection circuit, the UVLO operates, stopping the switching. In such a case, if V_{cc} becomes greater than the ULVO's high critical voltage (15V), the intermittent mode operates again. R_{sd} , C_{cc} and C_{fb} have effects even at start and off power so they should be carefully considered when deciding on these values. (Refer to application circuit related to start up). Our experiments have indicated that 10-20 Ohms is most appropriate for R_{sd} .

2.3 Fast Protection Circuit without Delay

Because SPS overlapped various protection operations at the feedback circuit, the unavoidably delayed protection operates in preparation for a transient. Therefore, protection range must be restricted or fast protection requires additional circuits. The latch mode or intermittent mode is possible for this protection (Figure 19). Using T_r to force the feedback photodiode current to increase and maintaining the primary V_{fb} below 0.3V, the SPS stops the switching and can be made to operate as a protection circuit. Depending on the magnitude of the photodiode current, the protection circuit could be made to operate sufficiently fast. In such a case, when T_r is turned off, it becomes an intermittent mode protection circuit, which re-enters normal operation. Also, it possible to use this circuit as an output enable circuit.

A fast latch mode protection can be operated by adding one photocoupler, as shown in the Figure 19. When output terminal latch mode T_r turns on, a large current flows to the PC2 photodiode and a large current also flows to the primary photo T_r , suddenly increasing the V_{fb} , executing the fast latch mode protection without time delay.

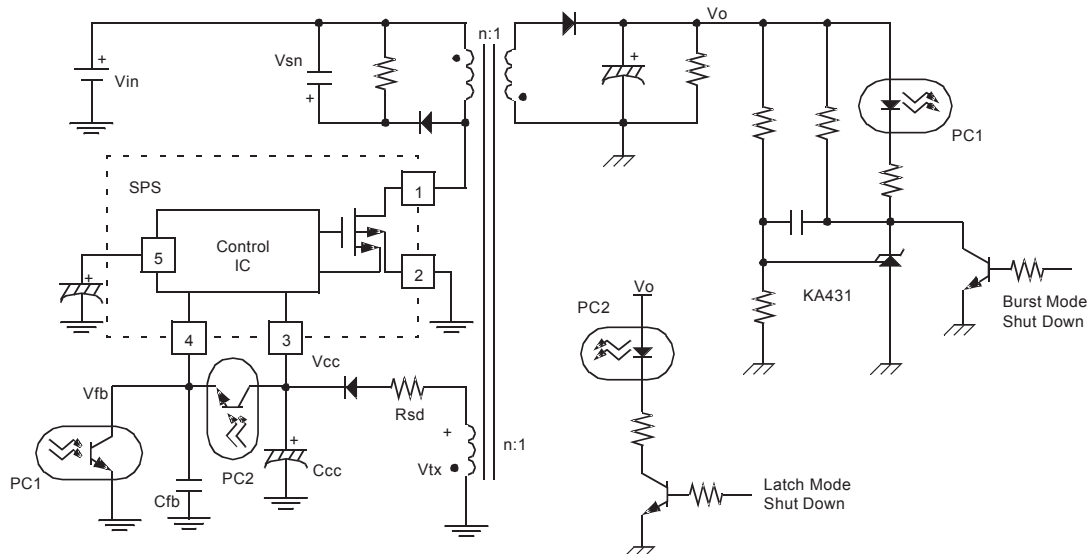


Figure 19. SPS fast protection circuit without delay

2.4 Over Voltage Protection

SPS has a self protection feature which functions even when malfunctions such as open or short circuit in the feedback circuit exists. From the primary side view, when the feedback terminal short circuits, its voltage becomes zero and is unable to start switching. Even if it opens, the protection circuit operates like the overload protection circuit. If the feedback terminal looks open possible due to either a malfunction in the primary feedback circuit or a no soldering etc., the primary side switches with the set maximum current until the protection circuit operates and causes the secondary voltage to become much greater than the rated voltage, which is common. If there was no protection circuit in such a case, the fuse would blow or, more serious, it could lead to a fire. To a lesser degree, there is a good possibility the ICs, without a regulator, directly connected to the secondary output, could be destroyed (especially, TTL IC etc., digital IC). Even in such a case, the SPS protection circuit operates, which is exactly the overvoltage protection circuit (protection against feedback malfunction). In this situation, the output voltage greatly increases so the Vcc voltage should be made proportional to the output voltage. In SPS IC, the protection circuit is made to operate when Vcc is over 25V. During normal operation, Vcc voltage must be maintained reasonably lower than 25V.

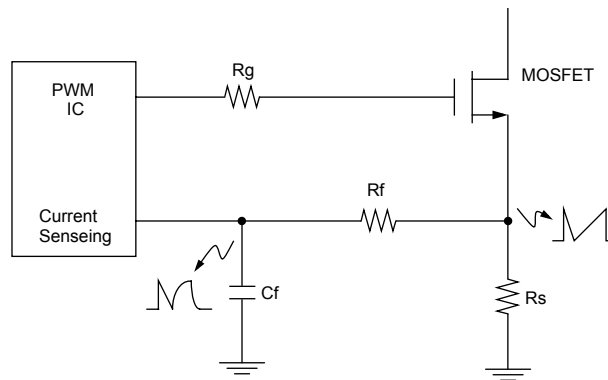
MOSFET Gate Operating Current: As shown in the diagram, MOSFET Gate Operating current also flows through the current sensing resistor. This diagram shows the current flow path.

3.3 Measures against the Leading Edge Noise and their Advantages and Disadvantages

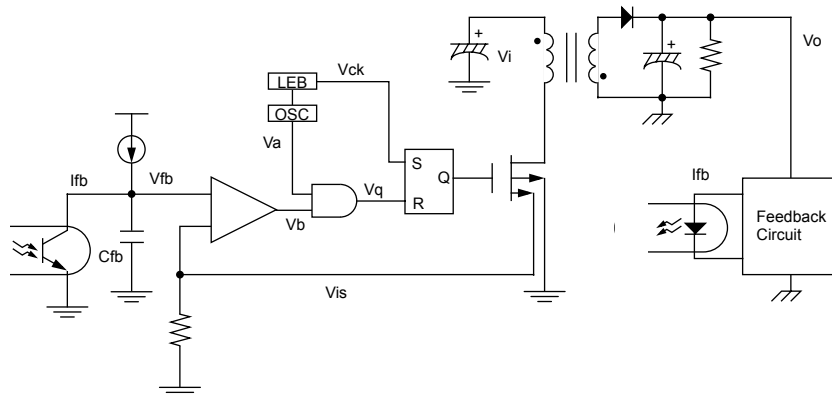
Among the measures against current sensing noise directly after turn-on the most commonly used method is the use of the RC filter. As shown by the diagram on the next page, if a RC filter is used, not only is the noise eliminated, but the current sensing signal is distorted so that accurate current sensing becomes difficult, which is a disadvantage. Furthermore, a large RC value means a bigger chip, making it difficult to install on the IC. If the method, shown in the bottom diagram on the next page, is used, the above disadvantage could be overcome. The problem noise arises just after turn-on, so if a circuit is inserted that ignores the current sensing noise for a fixed time just after turn-on, like the moving waveform, it could be made to operate normally regardless of the noise. Even though there are methods similar to this depending on the location of on the circuit to nullify the current sensing, the basic idea is to maintain turn-on during minimum turn-on time (the smallest turn-on time that cannot be turned off one turn-on starts). Duty ratio control lower than this time is done through non-linear control method. As a concept relative to the linear control, the non-linear control range is very wide, but, at low load, the method in the last diagram that executes in the control circuit is as follows. For example, it is controlled such that if load conditions require turn-on time of 400ns when the minimum turn-on time is 500ns, one switching cycle turns-on at 800ns and another stops to make the average turn-on time of the two cycles equal 400ns. In this case, the switching frequency becomes half of the linear control switching frequency and improves the efficiency at low load so that minimum input power can be reduced. The Motorola MC34063 (Fairchild KA34063, DC/DC converter) are examples of nonlinear control ICs that control through these methods.

3.4 Burst Mode Operation

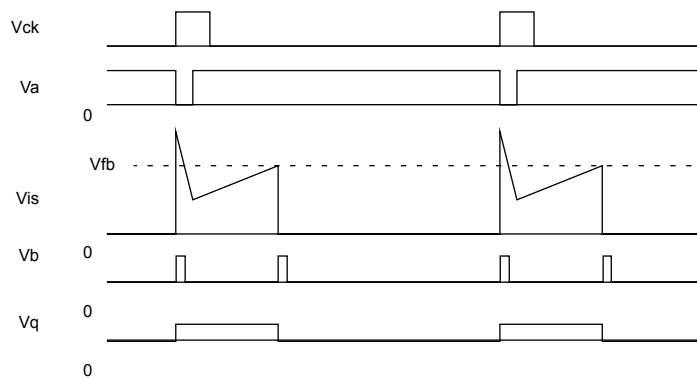
The aforementioned method can be viewed as one method of Burst Mode Operation. The Burst Mode Operation is one of the most useful methods to improve the SMP efficiency at low load and to reduce the standby input power of household appliances etc. The Burst Mode Operation is a method to reduce the switching frequency at low load for high efficiency. However, some SMPS designers wrongly believe that the Burst Mode operation is burst oscillation (known mostly in RCC (Ringing Choke Conversion)), which can bring about reliability problems. Such Burst Mode Operation can be divided largely into two methods of which one lowers the switching frequency equally and the other switches at normal frequency for a fixed time and stops the control IC operation for a fixed time (comparatively a long time). Even though in the first method the control IC continues to consume power, a large ripple is not produced in the output voltage. The second method can be a useful method to reduce the minimum input power at standby because the standby power greatly reduced when the IC was stopped. Actually, it is used often to reduce DC/DC converter standby consumption power in handphone's standby mode. However, the disadvantage is that the output voltage ripple gets bigger. Presently, Europe restricts the household appliance standby input power to lower than 5W, but, in time, it has been determined that they will restrict it to lower than 3W. In that case, the Burst Mode Operation will be a useful, powerful method used to satisfying the standby input power



(a) Noise Elimination by using the RC Filter



(b) Internal Block Diagram for Leading Edge Blanking



(c) Noise Elimination & the Wave forms by using the Leading Edge Blanking

Figure 21. Leading edge blanking

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