

SN54HCT574, SN74HCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS177E – MARCH 1984 – REVISED AUGUST 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 22$ ns
- ± 6 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Bus-Structured Pinout

description/ordering information

These octal edge-triggered D-type flip-flops feature 3-state outputs designed specifically for bus driving. The 'HCT574 devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

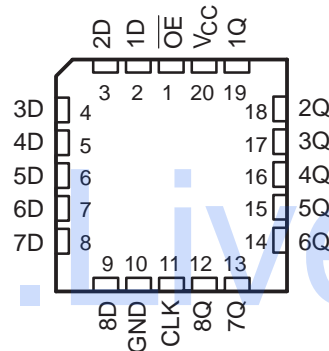
The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54HCT574 . . . J OR W PACKAGE
SN74HCT574 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT574 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 20	SN74HCT574N	SN74HCT574N
	SOIC – DW	Tube of 25	SN74HCT574DW	HCT574
		Reel of 2000	SN74HCT574DWR	
	SOP – NS	Reel of 2000	SN74HCT574NSR	HCT574
	SSOP – DB	Reel of 2000	SN74HCT574DBR	HT574
	TSSOP – PW	Tube of 70	SN74HCT574PW	HT574
Reel of 2000		SN74HCT574PWR		
Reel of 250		SN74HCT574PWT		
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54HCT574J	SNJ54HCT574J
	CFP – W	Tube of 85	SNJ54HCT574W	SNJ54HCT574W
	LCCC – FK	Tube of 55	SNJ54HCT574FK	SNJ54HCT574FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54HCT574, SN74HCT574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS177E – MARCH 1984 – REVISED AUGUST 2003

description/ordering information (continued)

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND	± 70 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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SCLS177E – MARCH 1984 – REVISED AUGUST 2003

recommended operating conditions (see Note 3)

		SN54HCT574			SN74HCT574			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V			0.8			V
V _I	Input voltage	0		V _{CC}	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time	500			500			ns
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
		I _{OH} = -6 mA		3.98	4.3		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		V	
		I _{OL} = 6 mA			0.17	0.26		0.4			0.33
I _I	V _I = V _{CC} or 0		5.5 V		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0		5.5 V		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0		5.5 V			8		160		80	μA
ΔI _{CC} †	One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC}		5.5 V		1.4	2.4		3		2.9	mA
C _i			4.5 V to 5.5 V		3	10		10		10	pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HCT574		SN74HCT574		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	4.5 V		30		20		24	MHz
		5.5 V		33		22		27	
t _w	Pulse duration, CLK high or low	4.5 V		16		24		20	ns
		5.5 V		14		22		18	
t _{su}	Setup time, data before CLK↑	4.5 V		20		30		25	ns
		5.5 V		17		27		23	
t _h	Hold time, data after CLK↑	4.5 V		5		5		5	ns
		5.5 V		5		5		5	

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SCLS177E – MARCH 1984 – REVISED AUGUST 2003

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	30	36		20		24	MHz	
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		30	36		54		45	ns
			5.5 V		25	32		48		41	
t_{en}	\overline{OE}	Any Q	4.5 V		26	30		45		38	ns
			5.5 V		23	27		41		34	
t_{dis}	\overline{OE}	Any Q	4.5 V		23	30		45		38	ns
			5.5 V		22	27		41		34	
t_t		Any Q	4.5 V		10	12		18		15	ns
			5.5 V		9	11		16		14	

switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT574		SN74HCT574		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	30	36		20		24	MHz	
			5.5 V	33	40		22		27		
t_{pd}	CLK	Any Q	4.5 V		40	53		80		66	ns
			5.5 V		35	47		71		60	
t_{en}	\overline{OE}	Any Q	4.5 V		34	47		71		59	ns
			5.5 V		29	39		94		78	
t_t		Any Q	4.5 V		18	42		63		53	ns
			5.5 V		16	38		57		48	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per flip-flop	No load	93	pF

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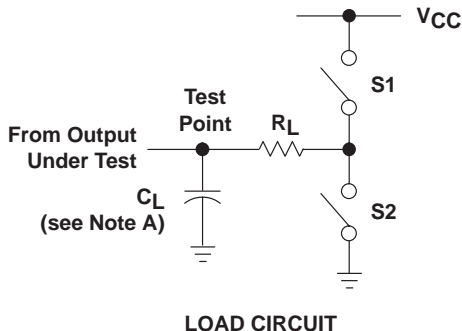


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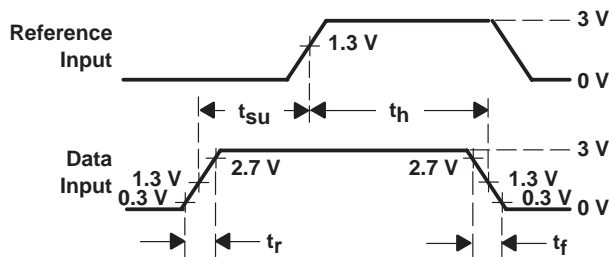
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SCLS177E – MARCH 1984 – REVISED AUGUST 2003

PARAMETER MEASUREMENT INFORMATION



PARAMETER	R_L	C_L	S1	S2
t_{en}	t_{PZH}	50 pF or 150 pF	Open	Closed
	t_{PZL}		Closed	Open
t_{dis}	t_{PHZ}	50 pF	Open	Closed
	t_{PLZ}		Closed	Open
t_{pd} or t_t	--	50 pF or 150 pF	Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74HCT574DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HCT574N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74HCT574NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74HCT574NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74HCT574PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT574PWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

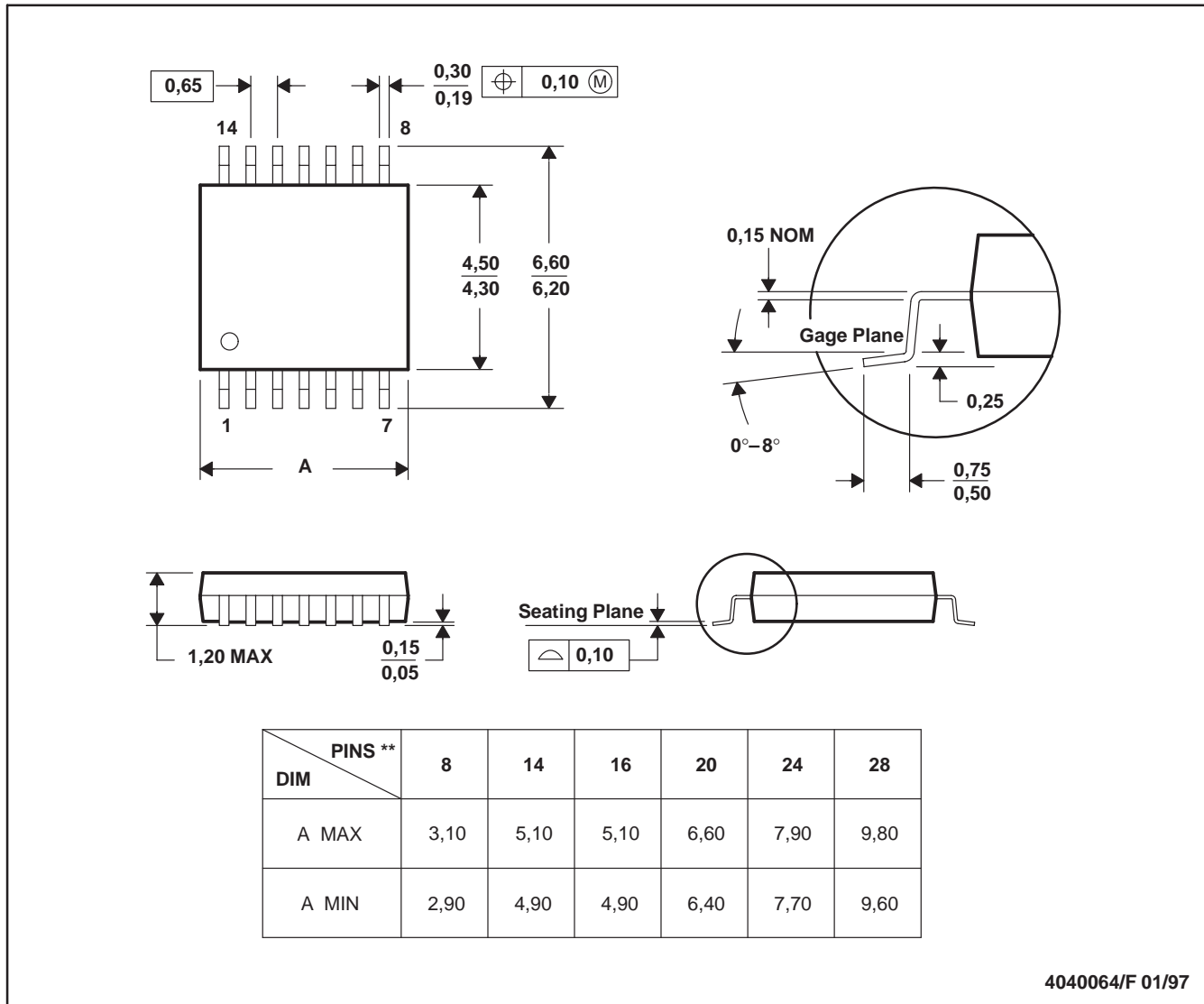


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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View ROHS Compliant Devices

clear gif

SN74HCT574, Status: ACTIVE

View RoHS Compliant Devices

Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs



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<input type="checkbox"/> Features	<input type="checkbox"/> Samples	<input type="checkbox"/> Technical Documents
<input type="checkbox"/> Quality & Pb-Free Data	<input type="checkbox"/> Pricing/Packaging	<input type="checkbox"/> Applications Notes
<input type="checkbox"/> Related Products	<input type="checkbox"/> Inventory	<input type="checkbox"/> Simulation Models
<input type="checkbox"/> Tools & Software	<input type="checkbox"/> Symbols/Footprints	<input type="checkbox"/> Reference Designs



Refine Your Selection

- Logic: D-Type (3-State) Flops

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet



Download Datasheet

SN54HCT574, SN74HCT574 (Rev. E) (sn74hct574.pdf, 387 KB)
19 Aug 2003 [Download](#)

	SN74HCT574
Voltage Nodes(V)	5
Vcc range(V)	4.5 to 5.5
Input Level	TTL
Output Level	CMOS
Output Drive(mA)	-6/6
No. of Outputs	8
Static Current	0.08
th(ns)	5
tpd max(ns)	41
tsu(ns)	23
Logic	True
	Samples
	Inventory

Product Information

Features Save this to your personal library

Operating Voltage Range of 4.5 V to 5.5 V
 High-Current 3-State Noninverting Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
 Low Power Consumption, 80-µA Max I_{CC}
 Typical t_{pd} = 22 ns
 ±6-mA Output Drive at 5 V
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A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Pricing/Packaging/CAD Design Tools/Samples


			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74HCT574DBR	ACTIVE	-40 to 85	0.33 1KU	SSOP (DB) 20	View	2000	<input type="checkbox"/>	Purchase Samples
SN74HCT574DBRE4	ACTIVE	-40 to 85	0.33 1KU	SSOP (DB) 20	View	2000	<input type="checkbox"/>	Purchase Samples
SN74HCT574DW	ACTIVE	-40 to 85	0.33 1KU	SOIC (DW) 20	View	25	<input type="checkbox"/>	Purchase Samples
SN74HCT574DWR	ACTIVE	-40 to 85	0.33 1KU	SOIC (DW) 20	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74HCT574DWRE4	ACTIVE	-40 to 85	0.33 1KU	SOIC (DW) 20	View	2000	<input type="checkbox"/>	Request Free Samples
SN74HCT574N	ACTIVE	-40 to 85	0.36 1KU	PDIP (N) 20	View	20	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74HCT574N3	OBSOLETE	-40 to 85		PDIP (N) 20	View		<input type="checkbox"/>	Not Available
SN74HCT574NE4	ACTIVE	-40 to 85	0.36 1KU	PDIP (N) 20	View	20	<input type="checkbox"/>	Request Free Samples
SN74HCT574NSR	ACTIVE	-40 to 85	0.33 1KU	SO (NS) 20	View	2000	<input type="checkbox"/>	Purchase Samples
SN74HCT574NSRE4	ACTIVE	-40 to 85	0.33 1KU	SO (NS) 20	View	2000	<input type="checkbox"/>	Purchase Samples
SN74HCT574PW	ACTIVE	-40 to 85	0.33 1KU	TSSOP (PW) 20	View	70	<input type="checkbox"/>	Purchase Samples
SN74HCT574PWE4	ACTIVE	-40 to 85	0.33 1KU	TSSOP (PW) 20	View	70	<input type="checkbox"/>	Purchase Samples
SN74HCT574PWLE	OBSOLETE	-40 to 85		TSSOP (PW) 20	View		<input type="checkbox"/>	Not Available
SN74HCT574PWR	ACTIVE	-40 to 85	0.33 1KU	TSSOP (PW) 20	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74HCT574PWRE4	ACTIVE	-40 to 85	0.33 1KU	TSSOP (PW) 20	View	2000	<input type="checkbox"/>	Request Free Samples
SN74HCT574PWT	ACTIVE	-40 to 85	0.66 1KU	TSSOP (PW) 20	View	250	<input type="checkbox"/>	Purchase Samples
SN74HCT574PWTE4	ACTIVE	-40 to 85	0.66 1KU	TSSOP (PW) 20	View	250	<input type="checkbox"/>	Purchase Samples

Inventory

	TI Inventory Status			Reported Distributor Inventory			
SN74HCT574DBR	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 31 Jan	10 Weeks	None Reported View Distributors			
SN74HCT574DBRE4	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 31 Jan	10 Weeks	None Reported View Distributors			
SN74HCT574DW	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

View all Distributors

Choose a Region



	0*	>10k 30 Jan	9 Weeks	Americas	Arrow	>1k	<input type="text"/>
				DigiKey	>1k	<input type="text"/>	
				Newark InOne	>1k	<input type="text"/>	
				Europe	Abacus Polar	>1k	<input type="text"/>
				Arrow Northern Europe	>1k	<input type="text"/>	
				Arrow Southern Europe	>1k	<input type="text"/>	
				EBV Elektronik	>1k	<input type="text"/>	
				Spoerle	>1k	<input type="text"/>	

SN74HCT574DWR As of 9:11 AM GMT, 29 Nov 2005 As of 9:11 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 30 Jan	9 Weeks	Americas	DigiKey	579	<input type="text"/>
				Europe	Abacus Polar	>1k	<input type="text"/>
				Arrow Southern Europe	>1k	<input type="text"/>	
				Avnet-SILICA	>1k	<input type="text"/>	

SN74HCT574DWRE4 As of 9:11 AM GMT, 29 Nov 2005 As of 9:11 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 30 Jan	9 Weeks	None Reported View Distributors			

SN74HCT574N As of 9:11 AM GMT, 29 Nov 2005 As of 9:11 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	8889*	1111 28 Dec	10 Weeks	Americas	Avnet	>1k	<input type="text"/>
				DigiKey	299	<input type="text"/>	
				Newark InOne	293	<input type="text"/>	
				Asia	P&S	315	<input type="text"/>
				Europe	Abacus Polar	200	<input type="text"/>
				Arrow Northern Europe	>1k	<input type="text"/>	
				Arrow Southern Europe	171	<input type="text"/>	
				Avnet-SILICA	>1k	<input type="text"/>	
				EBV Elektronik	>1k	<input type="text"/>	
				Spoerle	>1k	<input type="text"/>	

SN74HCT574NE4 As of 9:11 AM GMT, 29 Nov 2005 As of 9:11 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	8889*	1111 28 Dec	10 Weeks	None Reported View Distributors			
				1000 5 Jan			
				>10k 30 Jan			

SN74HCT574NSR As of 9:11 AM GMT, 29 Nov 2005 As of 9:11 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Feb	10 Weeks	None Reported View Distributors			

SN74HCT574NSRE4	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Feb	10 Weeks	None Reported View Distributors			
SN74HCT574PW	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1 28 Mar	16 Weeks	None Reported View Distributors			
		>10k 31 Mar					
SN74HCT574PWE4	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1 28 Mar	16 Weeks	None Reported View Distributors			
		>10k 31 Mar					
SN74HCT574PWR	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	Americas	Arrow	>1k	<input type="text"/>
					DigiKey	>1k	<input type="text"/>
SN74HCT574PWRE4	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74HCT574PWT	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74HCT574PWTE4	As of 9:11 AM GMT, 29 Nov 2005			As of 9:11 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your [TI Authorized Distributor](#), including those [listed above](#), for real time stock information.

** Lead time information is not available at this time. However, our information is updated daily so please check back with us soon. Please contact your preferred [TI Authorized Distributor](#) for additional information.

Quality & Lead (Pb)-Free Data

Device	Product Content			MTBF/FIT Rate	
	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
SN74HCT574DBR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574DBRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574DW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574DWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574DWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574N <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74HCT574NE4 <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
SN74HCT574NSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574NSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574PW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574PWE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574PWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574PWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574PWT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74HCT574PWTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents

Datasheets	Keep track of what's new
SN54HCT574, SN74HCT574 (Rev. E) (sn74hct574.pdf, 387 KB) 19 Aug 2003 Download	
Application Notes	
Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB) 08 Jul 2004 Abstract	
Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB) 24 May 2004 Abstract	
Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB) 28 May 2003 Abstract	
TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB) 29 Aug 2002 Abstract	
Implications of Slow or Floating CMOS Inputs (Rev. C) (scba004c.htm, 9 KB) 01 Feb 1998 Abstract	
CMOS Power Consumption and CPD Calculation (Rev. B) (scaa035b.htm, 9 KB) 01 Jun 1997 Abstract	
Designing With Logic (Rev. C) (sdya009c.htm, 9 KB) 01 Jun 1997 Abstract	
SN54/74HCT CMOS Logic Family Applications and Restrictions (scla011.htm, 9 KB) 01 May 1996 Abstract	
Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (scla008.htm, 9 KB) 01 Apr 1996 Abstract View Application Notes for D-TYPE (3-STATE) FLIP-FLOPS	
User Guides	
Signal Switch Data Book (Rev. A) (scdd003a.pdf, 19732 KB) 14 Nov 2003 Download	
LOGIC Pocket Data Book (scyd013.pdf, 4835 KB) 05 Dec 2002 Download	
More Literature	

Logic Selection Guide 2005 (Rev. X) (sdyu001x.pdf, 6909 KB)

15 Mar 2005 [Download](#)

Military Semiconductors Selection Guide 2004-2005 (Rev. D) (sgyc003d.pdf, 964 KB)

10 Aug 2004 [Download](#)

Logic Cross-Reference (Rev. A) (scyb017a.pdf, 2938 KB)

07 Oct 2003 [Download](#)

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