

## Introduction

The MAX® II family of instant-on, non-volatile CPLDs is based on a 0.18- $\mu\text{m}$ , 6-layer-metal-flash process, with densities from 240 to 2,210 logic elements (LEs) (128 to 2,210 equivalent macrocells) and non-volatile storage of 8 Kbits. MAX II devices offer high I/O counts, fast performance, and reliable fitting versus other CPLD architectures. Featuring MultiVolt core, a user flash memory (UFM) block, and enhanced in-system programmability (ISP), MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.

## Features

The MAX II CPLD has the following features:

- Low-cost, low-power CPLD
- Instant-on, non-volatile architecture
- Standby current as low as 25  $\mu\text{A}$
- Provides fast propagation delay and clock-to-output times
- Provides four global clocks with two clocks available per logic array block (LAB)
- UFM block up to 8 Kbits for non-volatile storage
- MultiVolt core enabling external supply voltages to the device of either 3.3 V/2.5 V or 1.8 V
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
- I/Os are fully compliant with the Peripheral Component Interconnect Special Interest Group (PCI SIG) PCI Local Bus Specification, Revision 2.2 for 3.3-V operation at 66 MHz
- Supports hot-socketing
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- ISP circuitry compliant with IEEE Std. 1532

Table 1-1 shows the MAX II family features.

**Table 1-1.** MAX II Family Features

| Feature                       | EPM240<br>EPM240G | EPM570<br>EPM570G | EPM1270<br>EPM1270G | EPM2210<br>EPM2210G | EPM240Z    | EPM570Z    |
|-------------------------------|-------------------|-------------------|---------------------|---------------------|------------|------------|
| LEs                           | 240               | 570               | 1,270               | 2,210               | 240        | 570        |
| Typical Equivalent Macrocells | 192               | 440               | 980                 | 1,700               | 192        | 440        |
| Equivalent Macrocell Range    | 128 to 240        | 240 to 570        | 570 to 1,270        | 1,270 to 2,210      | 128 to 240 | 240 to 570 |
| UFM Size (bits)               | 8,192             | 8,192             | 8,192               | 8,192               | 8,192      | 8,192      |
| Maximum User I/O pins         | 80                | 160               | 212                 | 272                 | 80         | 160        |
| $t_{PD1}$ (ns) (1)            | 4.7               | 5.4               | 6.2                 | 7.0                 | 7.5        | 9.0        |
| $f_{CNT}$ (MHz) (2)           | 304               | 304               | 304                 | 304                 | 152        | 152        |
| $t_{SU}$ (ns)                 | 1.7               | 1.2               | 1.2                 | 1.2                 | 2.3        | 2.2        |
| $t_{CO}$ (ns)                 | 4.3               | 4.5               | 4.6                 | 4.6                 | 6.5        | 6.7        |

**Notes to Table 1-1:**

- (1)  $t_{PD1}$  represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.
- (2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.



For more information about equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

MAX II and MAX IIG devices are available in three speed grades: -3, -4, and -5, with -3 being the fastest. Similarly, MAX IIZ devices are available in three speed grades: -6, -7, and -8, with -6 being the fastest. These speed grades represent the overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 1-2 shows MAX II device speed-grade offerings.

**Table 1-2.** MAX II Speed Grades

| Device              | Speed Grade |    |    |    |    |    |
|---------------------|-------------|----|----|----|----|----|
|                     | -3          | -4 | -5 | -6 | -7 | -8 |
| EPM240<br>EPM240G   | ✓           | ✓  | ✓  | —  | —  | —  |
| EPM570<br>EPM570G   | ✓           | ✓  | ✓  | —  | —  | —  |
| EPM1270<br>EPM1270G | ✓           | ✓  | ✓  | —  | —  | —  |
| EPM2210<br>EPM2210G | ✓           | ✓  | ✓  | —  | —  | —  |
| EPM240Z             | —           | —  | —  | ✓  | ✓  | ✓  |
| EPM570Z             | —           | —  | —  | ✓  | ✓  | ✓  |

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to [Table 1-3](#) and [Table 1-4](#)). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

**Table 1-3.** MAX II Packages and User I/O Pins

| Device              | 68-Pin<br>Micro<br>FineLine<br>BGA (1) | 100-Pin<br>Micro<br>FineLine<br>BGA (1) | 100-Pin<br>FineLine<br>BGA | 100-Pin<br>TQFP | 144-Pin<br>TQFP | 144-Pin<br>Micro<br>FineLine<br>BGA (1) | 256-Pin<br>Micro<br>FineLine<br>BGA (1) | 256-Pin<br>FineLine<br>BGA | 324-Pin<br>FineLine<br>BGA |
|---------------------|--|---|----------------------------|-----------------|-----------------|---|---|----------------------------|----------------------------|
| EPM240<br>EPM240G   | —                                      | 80                                      | 80                         | 80              | —               | —                                       | —                                       | —                          | —                          |
| EPM570<br>EPM570G   | —                                      | 76                                      | 76                         | 76              | 116             | —                                       | 160                                     | 160                        | —                          |
| EPM1270<br>EPM1270G | —                                      | —                                       | —                          | —               | 116             | —                                       | 212                                     | 212                        | —                          |
| EPM2210<br>EPM2210G | —                                      | —                                       | —                          | —               | —               | —                                       | —                                       | 204                        | 272                        |
| EPM240Z             | 54                                     | 80                                      | —                          | —               | —               | —                                       | —                                       | —                          | —                          |
| EPM570Z             | —                                      | 76                                      | —                          | —               | —               | 116                                     | 160                                     | —                          | —                          |

**Note to Table 1-3:**

(1) Packages available in lead-free versions only.

**Table 1-4.** MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

| Package                     | 68-Pin<br>Micro<br>FineLine<br>BGA | 100-Pin<br>Micro<br>FineLine<br>BGA | 100-Pin<br>FineLine<br>BGA | 100-Pin<br>TQFP | 144-Pin<br>TQFP | 144-Pin<br>Micro<br>FineLine<br>BGA | 256-Pin<br>Micro<br>FineLine<br>BGA | 256-Pin<br>FineLine<br>BGA | 324-Pin<br>FineLine<br>BGA |
|-----------------------------|------------------------------------|-------------------------------------|----------------------------|-----------------|-----------------|-------------------------------------|-------------------------------------|----------------------------|----------------------------|
| Pitch (mm)                  | 0.5                                | 0.5                                 | 1                          | 0.5             | 0.5             | 0.5                                 | 0.5                                 | 1                          | 1                          |
| Area (mm <sup>2</sup> )     | 25                                 | 36                                  | 121                        | 256             | 484             | 49                                  | 121                                 | 289                        | 361                        |
| Length × width<br>(mm × mm) | 5 × 5                              | 6 × 6                               | 11 × 11                    | 16 × 16         | 22 × 22         | 7 × 7                               | 11 × 11                             | 17 × 17                    | 19 × 19                    |

MAX II devices have an internal linear voltage regulator which supports external supply voltages of 3.3 V or 2.5 V, regulating the supply down to the internal operating voltage of 1.8 V. MAX IIG and MAX IIZ devices only accept 1.8 V as the external supply voltage. MAX IIZ devices are pin-compatible with MAX IIG devices in the 100-pin Micro FineLine BGA and 256-pin Micro FineLine BGA packages. Except for external supply voltage requirements, MAX II and MAX II G devices have identical pin-outs and timing specifications. Table 1-5 shows the external supply voltages supported by the MAX II family.

**Table 1-5.** MAX II External Supply Voltages

| Devices  | EPM240<br>EPM570<br>EPM1270<br>EPM2210 | EPM240G<br>EPM570G<br>EPM1270G<br>EPM2210G<br>EPM240Z<br>EPM570Z (1) |
|--|--|--|
| MultiVolt core external supply voltage ( $V_{CCINT}$ ) (2) | 3.3 V, 2.5 V                           | 1.8 V  |
| MultiVolt I/O interface voltage levels ( $V_{CCIO}$ )      | 1.5 V, 1.8 V, 2.5 V, 3.3 V             | 1.5 V, 1.8 V, 2.5 V, 3.3 V   |

**Notes to Table 1-5:**

- (1) MAX IIG and MAX IIZ devices only accept 1.8 V on their  $V_{CCINT}$  pins. The 1.8-V  $V_{CCINT}$  external supply powers the device core directly.
- (2) MAX II devices operate internally at 1.8 V.

## Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *MAX II Logic Element to Macrocell Conversion Methodology* white paper

## Document Revision History

Table 1-6 shows the revision history for this chapter.

**Table 1-6.** Document Revision History

| Date and Revision          | Changes Made  | Summary of Changes                         |
|----------------------------|---|--|
| August 2009, version 1.9   | ■ Updated Table 1-2.  | Added information for speed grade -8       |
| October 2008, version 1.8  | ■ Updated "Introduction" section.<br>■ Updated new Document Format.               | —  |
| December 2007, version 1.7 | ■ Updated Table 1-1 through Table 1-5.<br>■ Added "Referenced Documents" section. | Updated document with MAX IIZ information. |
| December 2006, version 1.6 | ■ Added document revision history.  | —  |
| August 2006, version 1.5   | ■ Minor update to features list.  | —  |
| July 2006, version 1.4     | ■ Minor updates to tables.  | —  |

**Table 1-6.** Document Revision History

| <b>Date and Revision</b>      | <b>Changes Made</b>                    | <b>Summary of Changes</b> |
|-------------------------------|--|---------------------------|
| June 2005,<br>version 1.3     | ■ Updated timing numbers in Table 1-1. | —                         |
| December 2004,<br>version 1.2 | ■ Updated timing numbers in Table 1-1. | —                         |
| June 2004,<br>version 1.1     | ■ Updated timing numbers in Table 1-1. | —                         |

