# AAT2820
## Triple-Output Charge Pump Regulator

ChargePump™

## General Description

The AAT2820 is a member of AnalogicTech's Total Power Management IC™ (TPMIC™) product family. It is a triple output charge pump targeted for active matrix thin-film transistor (TFT), liquid crystal displays (LCDs), and CCD camera bias for systems operating with lithium-ion/polymer batteries. The device generates three regulated output voltages for turn-on gate drive bias ($V_{POS}$), turn-off gate voltage bias ($V_{NEG}$), and logic voltage.

The $V_{POS}$ and $V_{NEG}$ output voltages are independently regulated. Both outputs use external diode and capacitor multiplier stages (as many stages as required) to regulate output voltages up to +25V and -25V. An additional regulated output voltage is provided for biasing the display module. Built-in soft-start circuitry prevents excessive inrush current during start-up. A high switching frequency enables the use of very small external capacitors. A low shutdown feature disconnects the load from $V_{IN}$ and reduces quiescent current to less than 0.1μA.

The AAT2820 is available in a Pb-free TDFN44-16 package and is specified over the -40°C to +85°C operating temperature range.

## Features

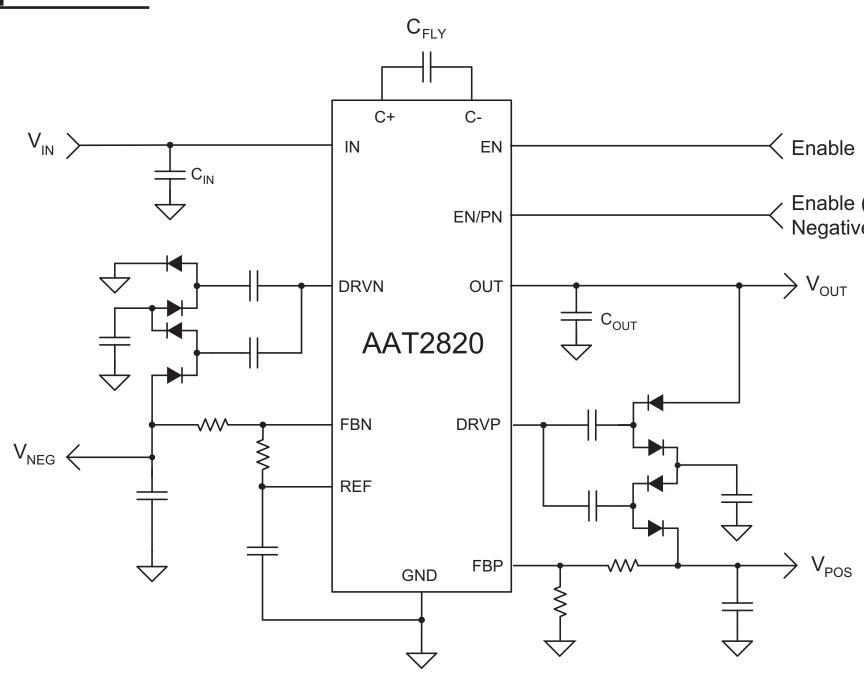
- $V_{IN}$ Range: 2.7V to 5.5V
- 5V Regulated Output Voltage
- Two Adjustable Regulated Output Voltages: $V_{POS}$ and $V_{NEG}$
  - — Positive Charge Pump Up to +25V
  - — Negative Charge Pump Down to -25V
  - — Optional Power-Up Sequence with AAT2820-1
- Internal Power MOSFETs
- <1μA of Shutdown Current
- Internally Controlled Soft Start
- Fast Transient Response
- Ultra-Thin Solution (No Inductors)
- 16-Pin TDFN44 Package
- Temperature Range: -40°C to +85°C

## Applications

- CCD Cameras
- Hand-Held Instruments
- Passive-Matrix Displays
- Personal Digital Assistants (PDAs)
- TFT Active-Matrix LCDs



## Typical Application

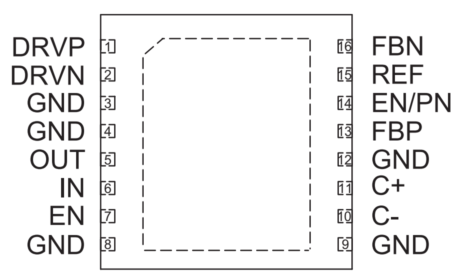


## Pin Description

| Pin # | Symbol | Function |
|---|---|---|
| 1 | DVRP | Positive charge pump driver output. Output high level is $V_{SUPP}$ and low level is PGND. |
| 2 | DRVN | Negative charge pump driver output. Output high level is $V_{SUPN}$ and low level is PGND. |
| 3, 4, 8, 9, 12 | GND | Ground connection. |
| 5 | OUT | Regulated 5V output. Requires a 4.7µF bypass capacitor to ground. |
| 6 | IN | Input power supply. A 1µA capacitor should be connected between this pin and ground. |
| 7 | EN | Enable input control pin. When low, the device is powered down and consumes less than 0.1µA. This pin should not be left floating. |
| 10 | C- | Flying capacitor negative terminal. |
| 11 | C+ | Flying capacitor positive terminal. Connect a 1µF capacitor between C+ and C-. |
| 13 | FBP | Positive charge pump feedback input. Regulates to 1.2V nominal. Connect feedback resistive divider to analog ground (GND). |
| 14 | EN/PN | Enable input. When EN/PN is pulled low, $V_{POS}$ and $V_{NEG}$ are turned off. |
| 15 | REF | Internal reference bypass terminal. Connect a 0.1µF capacitor from this terminal to analog ground (GND). External load capability to 50uA. REF is disabled in shutdown. |
| 16 | FBN | Negative charge pump regulator feedback input. Regulates to 0V nominal. Connect feedback resistive divider to the reference (REF). |
| EP | | Exposed paddle (bottom); connect to GND directly beneath package. |

## Pin Configuration

**TDFN44-16**
**(Top View)**



## Absolute Maximum Ratings[1]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{IN}$ | Input Voltage | -0.3 to 6.0 | V |
| $V_{OUT}$ | Charge Pump Output | -0.3 to 6.0 | V |
| $V_{EN}$ | EN or EN/PN to GND | -0.3 to 6.0 | V |
| $V_{N\_CH}$ | DRVN to GND | -0.3V to ($V_{IN}$ + 0.3V) | V |
| $V_{P\_CH}$ | DRVP to GND | -0.3V to ($V_{IN}$ + 0.3V) | V |
| Other Inputs | REF, FBN, FBP to GND | -0.3V to ($V_{IN}$ + 0.3V) | V |
| $I_{MAX}$ | Continuous Current into DRVN, DRVP, OUT | ±200 | mA |
| | All Other Pins | ±10 | |
| $T_{LEAD}$ | Maximum Soldering Temperature (at leads, 10 sec) | 300 | °C |

## Thermal Information[2]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $\theta_{JA}$ | Maximum Thermal Resistance | 50 | °C/W |
| $P_D$ | Power Dissipation[3] | 2.0 | W |

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.
3. Derate 6.25mW/°C above 25°C.

## Electrical Characteristics[1]

$V_{IN}$ = 3.3V; $C_{IN}$ = $C_{OUT}$ = $C_{FLY}$ = 1.0µF, $T_A$ = 0°C to +85°C, unless otherwise noted. Typical values are $T_A$ = 25°C.

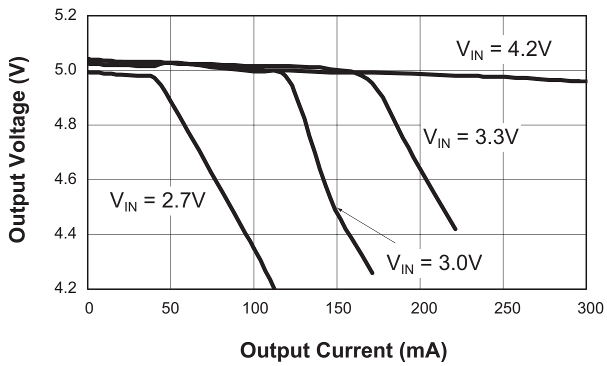
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Supply Range | | 2.7 | | 5.5 | V |
| UVLO | Input Under-Voltage Lockout Threshold | $V_{IN}$ Rising | | 1.8 | | V |
| | | $V_{IN}$ Falling | | 1.6 | | |
| $I_{CC}$ | Operating Current | $V_{FBP}$ = 1.5V, $V_{FBN}$ = -0.2V, No Load on DRVN and DRVP; EN = EN/PN = $V_{IN}$ | | 5.0 | | mA |
| $I_{SD}$ | Shutdown Supply Current | $V_{EN}$ = $V_{EN/PN}$ = 0V | | 0.1 | 1.0 | µA |
| $T_{SS}$ | Soft-Start Time | | | 200 | | µs |
| $F_{OSC}$ | Operating Frequency | | | 1.0 | | MHz |
| **Negative Low-Power Charge Pump** | | | | | | |
| $V_{FBN}$ | FBN Regulation Voltage | | -100 | 0 | +100 | mV |
| $I_{FBN}$ | FBN Input Bias Current | $V_{FBN}$ = -50mV | -100 | | +100 | nA |
| $I_{NEG}$ | Maximum Negative Output Current[2] | 3.3 ≤ $V_{IN}$ ≤ 5.5; No Load at $V_{POS}$ and $V_{OUT}$ | | | 25 | mA |
| $R_{DS\_NCH}$ | DRVN NCH On-Resistance | | | 1.5 | 5.0 | Ω |
| $R_{DS\_PCH}$ | MIN DRVN PCH On-Resistance | $V_{FBN}$ = 100mV, $V_{IN}$ = 4V | | 1.0 | 5.0 | Ω |
| | MAX DRVN PCH On-Resistance | $V_{FBN}$ = -100mV, $V_{IN}$ = 4V | | 20 | | kΩ |
| **Positive Low-Power Charge Pump** | | | | | | |
| $V_{FBP}$ | FBP Regulation Voltage | | 1.15 | 1.2 | 1.25 | V |
| $I_{FBP}$ | FBP Input Bias Current | $V_{FBP}$ = 1.5V | -60 | | +100 | nA |
| $I_{POS}$ | Maximum Positive Output Current[2] | 3.3 ≤ $V_{IN}$ ≤ 5.5; No Load at $V_{NEG}$ and $V_{OUT}$ | | | 25 | mA |
| $R_{DS\_PCH}$ | DRVP PCH On-Resistance | | | 1.0 | 5.0 | Ω |
| $R_{DS\_NCH}$ | MIN DRVP NCH On-Resistance | $V_{FBP}$ = 1.15V, $V_{IN}$ = 4V | | 3 | 15 | Ω |
| | MAX DRVP NCH On-Resistance | $V_{FBP}$ = 1.25V, $V_{IN}$ = 4V | | 20 | | kΩ |
| **Reference** | | | | | | |
| $V_{REF}$ | Reference Voltage | -2.0µA < $I_{REF}$ < 50µA | 1.18 | 1.2 | 1.22 | V |
| | Reference Under-Voltage Lockout Threshold | $V_{REF}$ Rising | | 0.8 | | |
| $V_{EN(L)}$ | EN and EN/PN Threshold Low | | | | 0.5 | V |
| $V_{EN(H)}$ | EN and EN/PN Threshold High | | 1.5 | | | V |
| $I_I$ | Enable Input Current | | -1.0 | | 1.0 | µA |
| $T_{SD}$ | Over-Temperature Shutdown Threshold | | | 140 | | °C |
| $T_{HYS}$ | Over-Temperature Shutdown Hysteresis | | | 15 | | °C |
| **Regulated 5V Charge Pump** | | | | | | |
| $V_{OUT}$ | Output Voltage Tolerance | 2.7V < $V_{IN}$ < 5V, $I_{OUT}$ = 50mA | | ±4.0 | | % |
| | Output Voltage | 3.0V < $V_{IN}$ < 5V, $I_{OUT}$ = 100mA | 4.8 | 5.0 | 5.2 | V |
| $I_{OUT}$ | Maximum Output Current[2] | 3.3 ≤ $V_{IN}$ ≤ 5.5; No Load at $V_{POS}$ and $V_{NEG}$ | | | 150 | mA |

1. The AAT2820 is guaranteed to meet performance specifications from 0°C to 70°C. Specification over the -40°C to +85°C operating temperature range is assured by design, characterization, and correlation with statistical process controls.
2. Loads greater than those listed in maximum output load conditions may cause permanent damage to the device.

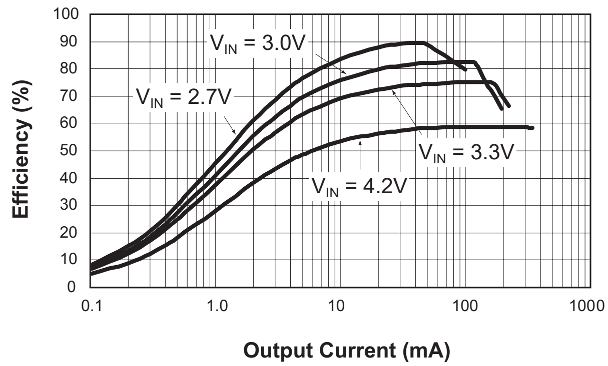
## Typical Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 5V, $V_{POS}$ = 12.5V, $V_{NEG}$ = -7.8V, $C_{IN}$ = $C_{FLY}$ = 1µF, $C_{OUT}$ = 4.7µF; $T_A$ = 25°C, unless otherwise noted.

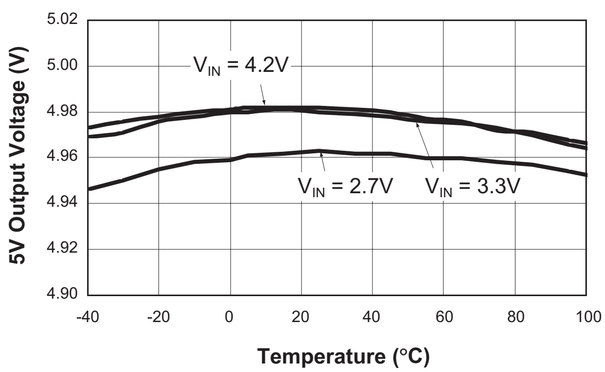
**5V Output vs. Output Current**



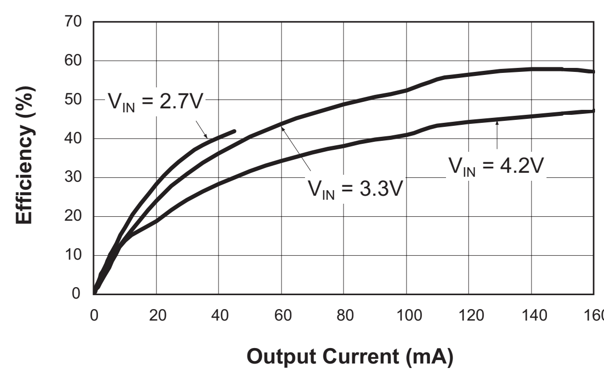

**5V Output Efficiency vs. Output Current**
**(No-Load at $V_{POS}$ and $V_{NEG}$)**



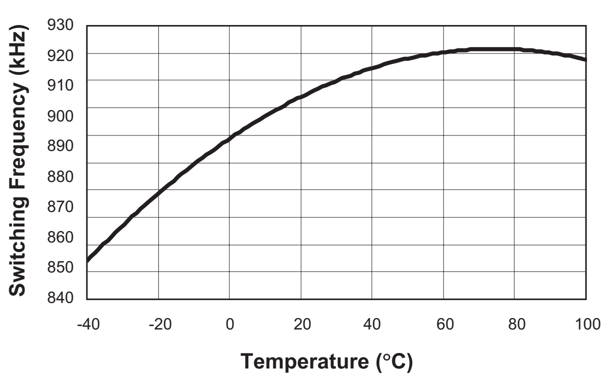

**5V Output Voltage vs. Temperature**
**(No-Load at $V_{POS}$ and $V_{NEG}$)**



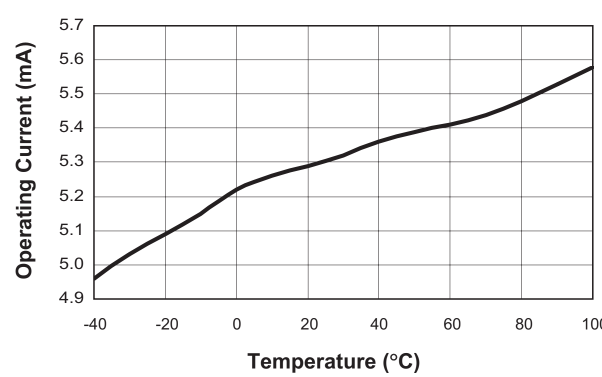

**5V Output Efficiency vs. Output Current**
**($V_{OUT}$ = 5V; $V_{POS}$ = 12.5V @ 10mA; $V_{NEG}$ = -7.8V @ 5mA)**




**Switching Frequency vs. Temperature**



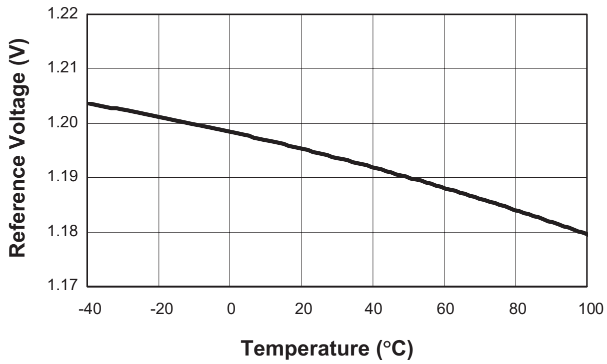

**Operating Current vs. Temperature**



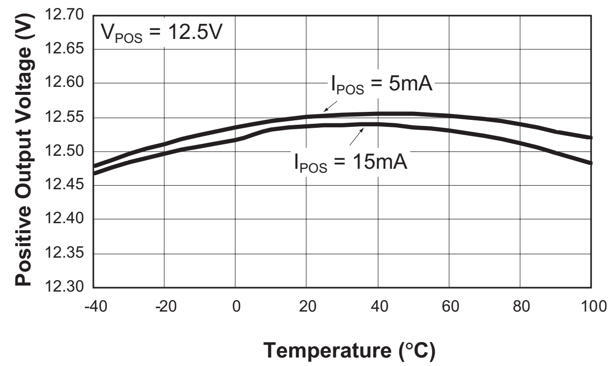
## Typical Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 5V, $V_{POS}$ = 12.5V, $V_{NEG}$ = -7.8V, $C_{IN}$ = $C_{FLY}$ = 1µF, $C_{OUT}$ = 4.7µF; $T_A$ = 25°C, unless otherwise noted.

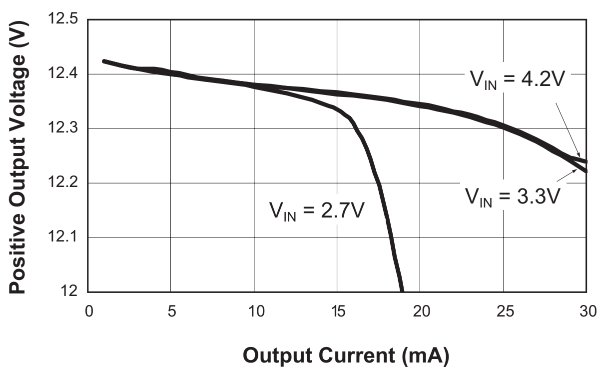
**Reference Voltage vs. Temperature**



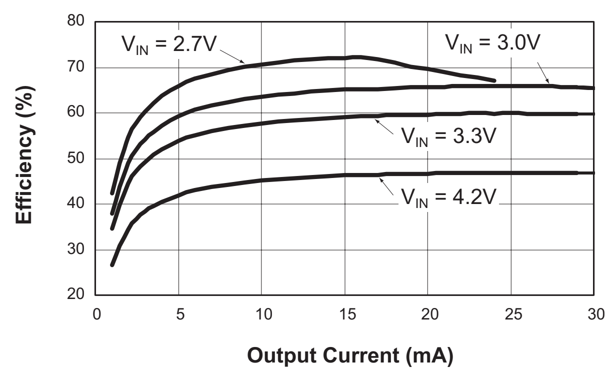

**Positive Charge Pump Output Voltage vs. Temperature**
**(No Load at $V_{NEG}$ and $V_{OUT}$)**



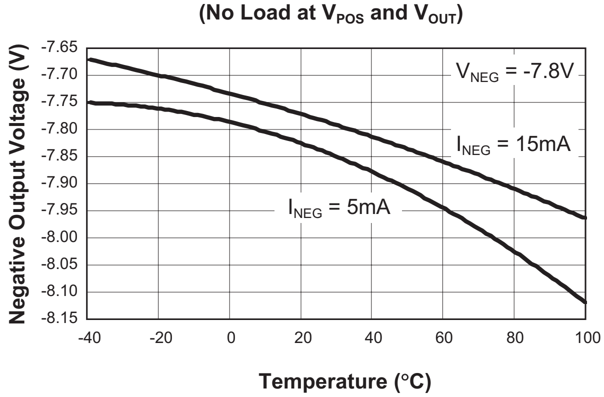

**Positive Charge Pump Output Voltage vs. Output Current**
**(No Load at $V_{NEG}$ and $V_{OUT}$)**



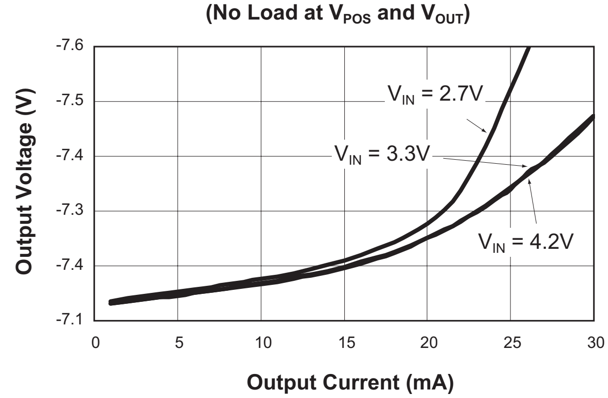

**Positive Charge Pump Efficiency vs. Output Current**
**(No Load at $V_{NEG}$ and $V_{OUT}$)**




**Negative Charge Pump Output Voltage vs. Temperature**
**(No Load at $V_{POS}$ and $V_{OUT}$)**



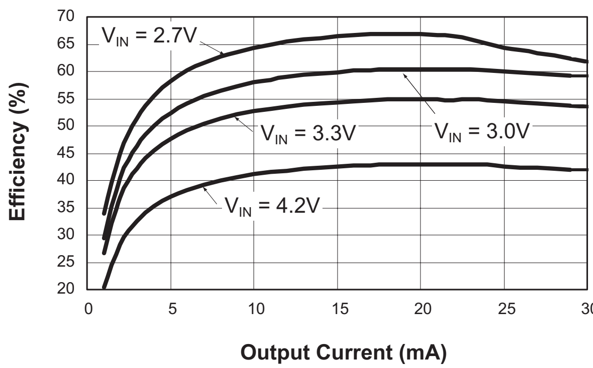

**Negative Charge Pump Output vs. Output Current**
**(No Load at $V_{POS}$ and $V_{OUT}$)**



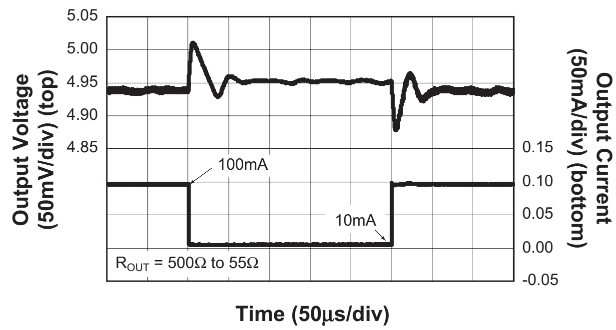
## Typical Characteristics

$V_{IN}$ = 3.3V, $V_{OUT}$ = 5V, $V_{POS}$ = 12.5V, $V_{NEG}$ = -7.8V, $C_{IN}$ = $C_{FLY}$ = 1µF, $C_{OUT}$ = 4.7µF; $T_A$ = 25°C, unless otherwise noted.

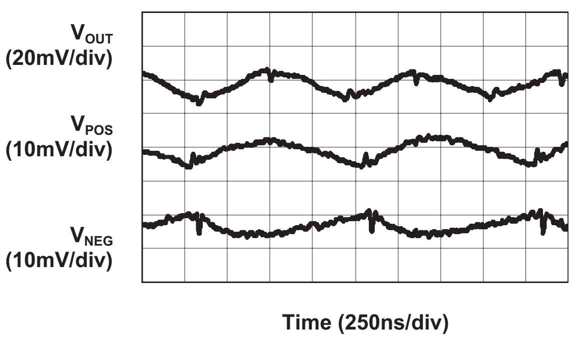
**Negative Charge Pump Efficiency vs. Output Current**
**(No Load at $V_{POS}$ and $V_{OUT}$)**



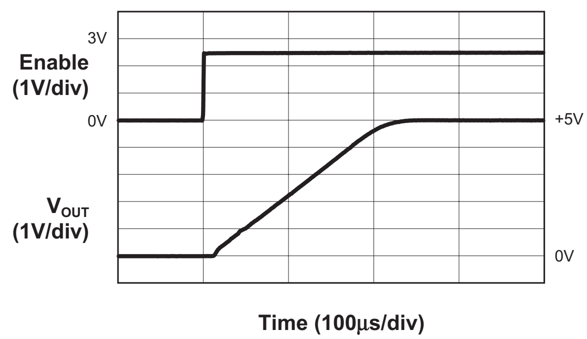

**Load Transient Response**
**(10mA - 100mA; $V_{IN}$ = 3.3V)**



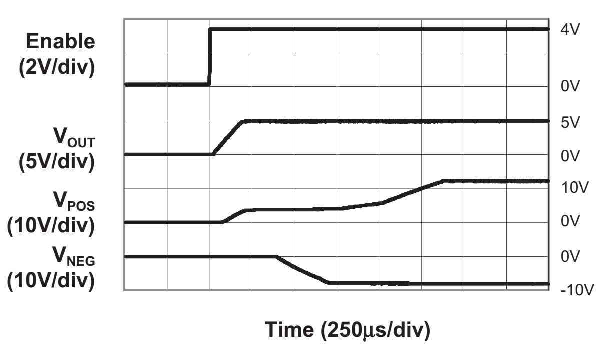

**Output Ripple Waveform**
**($V_{OUT}$ = 5V @ 100mA; $V_{POS}$ = 12.5V @ 10mA; $V_{NEG}$ = -7.8V @ 10mA)**



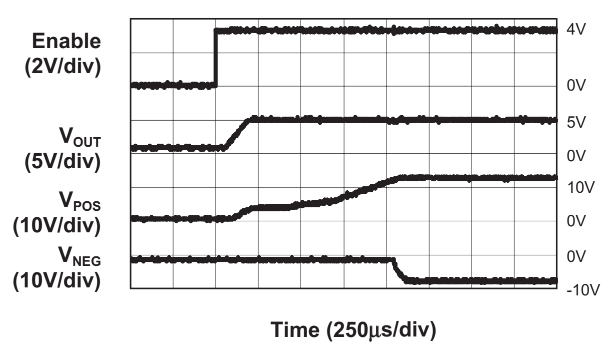

**5V Output Startup Time with 100mA Load**




**AAT2820 Power-Up Sequence**




**AAT2820-1 Power-Up Sequence**
**($V_{IN}$ = 4.2V)**



## Typical Characteristics

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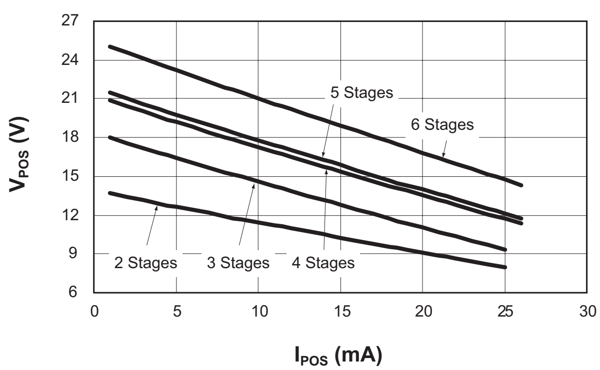
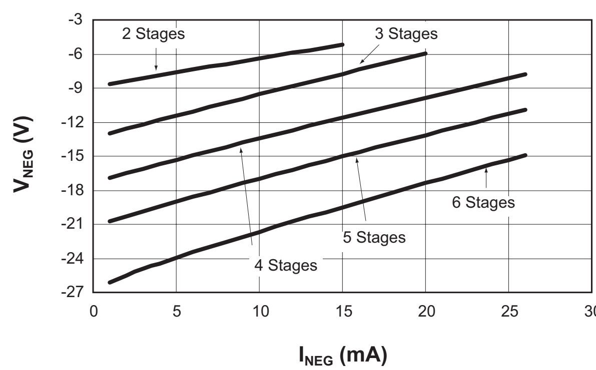
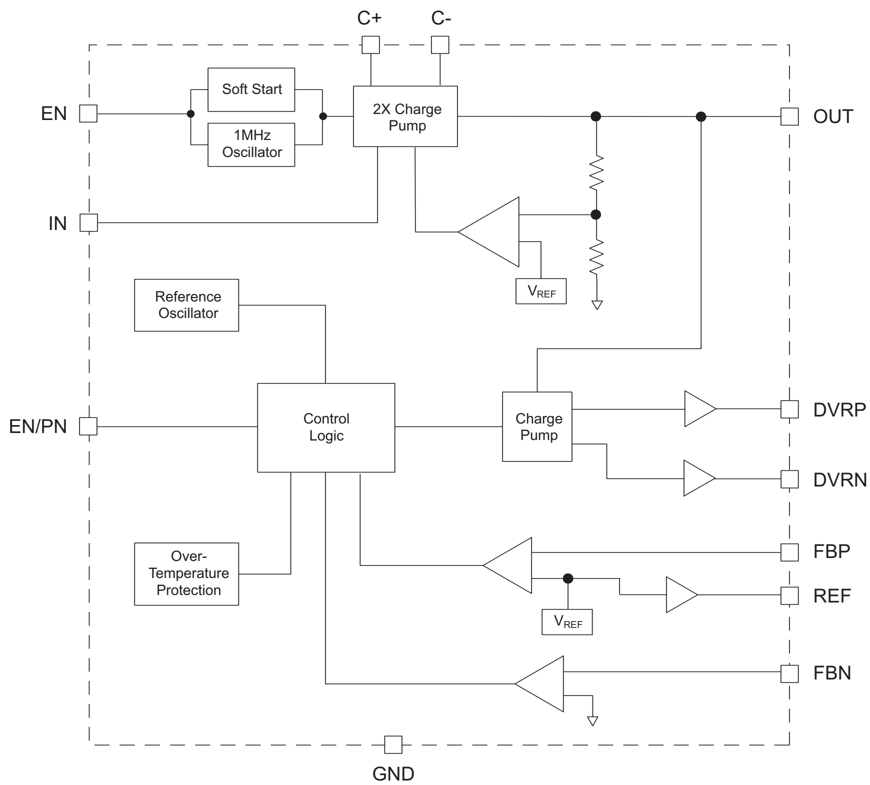
**Maximum Line Load**
**(Positive Charge Pump)**




**Maximum Line Load**
**(Negative Charge Pump)**



## Functional Block Diagram




## Functional Description

### 5V Regulated Output

The main power supply is a charge pump doubler architecture used to support the high-current demand required by the application. Charge pump regulation is achieved by sensing the output voltage through an internal resistor divider network. A switch doubling circuit is enabled when the divided output drops below a preset trip point controlled by an internal comparator. The free-running charge pump switching frequency is approximately 1MHz. The charge pump is designed to deliver 150mA of continuous current (loads greater than the maximum load condition may cause permanent damage to the device).

### Dual Charge Pump Regulators

The dual charge pump provides low-power regulated output voltages from two individual charge pumps. Using a single stage, the first charge pump inverts the supply voltage ($V_{IN}$) and provides a regulated negative output voltage. The second charge pump doubles $V_{IN}$ and provides a regulated positive output voltage. These outputs use external Schottky diodes and capacitor multiplier stages (as many as required) to regulate up to ±25V. A constant switching frequency of 1MHz minimizes the output ripple and capacitor size.

### Negative Charge Pump Regulator

During the first half-cycle, the P-channel MOSFET turns on and the flying capacitor C11 charges to $V_{IN}$ minus a diode drop (Figure 1). During the second half-cycle, the P-channel MOSFET turns off and the N-channel MOSFET turns on, level shifting C11. This connects C11 in parallel with the output reservoir capacitor C23. If the voltage across C23 minus a diode drop is less than the voltage across C11, current flows from C11 to C23 until the diode turns off.

## Positive Charge Pump Regulator

During the first half-cycle, the N-channel MOSFET turns on and charges the flying capacitor C12 (Figure 2). During the second half-cycle, the N-channel MOSFET turns off and the P-channel MOSFET turns on, level shifting C12 the input voltage. This connects C12 in parallel with the reservoir capacitor C24. If the voltage across C24 plus a diode drop is less than the level shifted by the flying capacitor (C12 + $V_{IN}$), charge is transferred from C12 to C24 until the diode turns off. If the positive charge pump output is connected to ground, output may not recover until power is recycled. Loads greater than the maximum load condition may cause permanent damage to the device; please review the Maximum Line Load Curves and the Electrical Characteristics table.

## Voltage Reference

The voltage reference is a simple band gap with an output voltage equal to $V_{BE}$ + K*$V_T$. The band gap reference amplifier has an additional compensation capacitor from the negative input to the output. This capacitor serves to slow down the circuit during startup and soft starts the voltage reference and the regulator output from overshoot. The reference circuit amplifier also increases the overall PSRR of the device. An 80kΩ resistor serves to isolate and buffer the amplifier from a small internal filter capacitor and an optional large external filter capacitor.

## Enable

In the normal operating state, the AAT2820 typically consumes 5mA of quiescent operating current. By pulling the enable pin (EN) low, the AAT2820 disables all three outputs. Once the device is shut down, the supply current drops to less than 1µA to maximize battery life.

The AAT2820 gives the application an option to independently turn on/off the positive and negative charge pump outputs. These two outputs can be disabled by pulling the EN/PN pin low. The threshold levels lie between 0.5V and 1.5V. Depending on the application, the supplies must be sequenced properly to avoid damage or latch-up.

## Soft-Start and Start-up Sequence

The AAT2820 has an internal soft-start circuit to guarantee a smooth transition to 5V for the main output when the device is enabled (typical 200µs). This device has two versions for the start-up sequence. The AAT2820 ramps up the positive charge pump after the negative charge pump is present; the AAT2820-1 ramps up the positive charge pump before the negative charge pump.

## Over-Temperature Protection

To protect the AAT2820, as well as the system application, this device has a thermal protection circuit that will shut down all the charge pumps if the die temperature rises above the preset internal thermal limit. This protects the device if the ambient temperature exceeds the operating limit for the device.

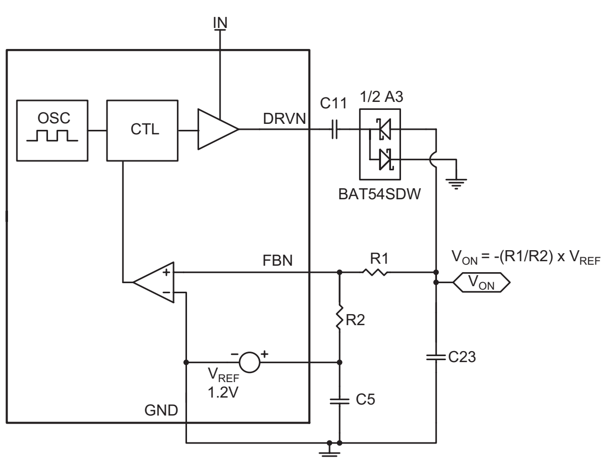



**Figure 1: Negative Charge Pump Block Diagram.**

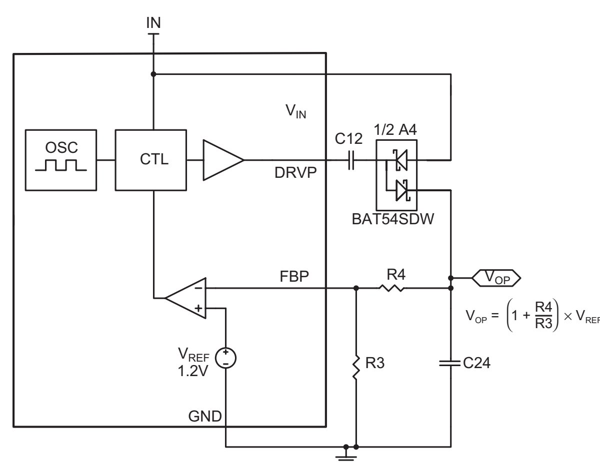



**Figure 2: Postive Charge Pump Block Diagram.**

# Design Procedure and Component Selection

## Number of Stages for Dual Charge Pump Regulators

The number of stages required can be determined by:

$$N_{POS} = \frac{V_{POS} - 5}{5 - 2V_{FWD}}$$

for the positive output, and

$$N_{NEG} = \frac{V_{NEG}}{2V_{FWD} - 5}$$

for the negative output.

Where,

$V_{NEG}$ = Negative output voltage

$V_{POS}$ = Positive output voltage

$V_{FWD}$ = Forward voltage drop of the Schottky diode (0.31V, based on BAT54SDW diode when $I_F$ = 4mA)

After solving for the number of stages ($N_{POS}$ and $N_{NEG}$), round up the solutions to the next highest integers for the number of stages required.

Tables 1 and 2 show the number of stages required for positive and negative charge pumps, respectively.

| $V_{POS}$ (V) | # of Stages (n) |
|---|---|
| 7 | 1 |
| 8 | 1 |
| 9 | 1 |
| 10 | 2 |
| 11 | 2 |
| 12 | 2 |
| 13 | 2 |
| 14 | 3 |
| 15 | 3 |
| 16 | 3 |
| 17 | 3 |
| 18 | 3 |
| 19 | 4 |
| 20 | 4 |
| 21 | 4 |
| 22 | 4 |
| 23 | 5 |
| 24 | 5 |
| 25 | 5 |

**Table 1: Number of Stages Required for Positive Charge Pump.**

| $V_{NEG}$ (V) | # of Stages (n) |
|---|---|
| -7 | 2 |
| -8 | 2 |
| -9 | 3 |
| -10 | 3 |
| -11 | 3 |
| -12 | 3 |
| -13 | 3 |
| -14 | 4 |
| -15 | 4 |
| -16 | 4 |
| -17 | 4 |
| -18 | 5 |
| -19 | 5 |
| -20 | 5 |
| -21 | 5 |
| -22 | 6 |
| -23 | 6 |
| -24 | 6 |
| -25 | 6 |

**Table 2: Number of Stages Required for Negative Charge Pump.**

### $V_{NEG}$

The negative output voltage is adjusted by a resistive divider from the output ($V_{NEG}$) to the FBN and REF pin. The maximum reference voltage current is 50µA; therefore, the minimum allowable value for R2 of Figure 1 is 24kΩ. It is best to select the smallest value possible for R2 as this will keep R1 to a minimum. This limits errors due to the FBN input bias current. The FBN input has a maximum input bias current of 100nA. Using the full 50µA reference current for programming $V_{NEG}$:

$$I_{PGM} = \frac{V_{REF}}{R2} = \frac{1.2V}{24k\Omega} = 50\mu A$$

will limit the error due to the input bias current at FBN to less than 0.2%.

$$\frac{I_{FBN}}{I_{PGM}} = \frac{0.1\mu A}{50\mu A} = 0.2\%$$

With R2 selected, R1 can be determined by:

$$R1 = \frac{V_{NEG} \cdot R2}{-V_{REF}}$$

See the example in Table 3.

| $V_{NEG}$ (V) | R1, Closest Value (kΩ) |
|---|---|
| -7 | 143 |
| -8 | 162 |
| -9 | 182 |
| -10 | 205 |
| -11 | 226 |
| -12 | 243 |
| -13 | 267 |
| -14 | 287 |
| -15 | 309 |
| -16 | 324 |
| -17 | 348 |
| -18 | 360 |
| -19 | 390 |
| -20 | 412 |
| -21 | 430 |
| -22 | 453 |
| -23 | 470 |
| -24 | 487 |
| -25 | 510 |

**Table 3: Closest Value for R1 if Using 24.3kΩ as R2.**

### $V_{POS}$

The positive output voltage is set by way of a resistive divider from the output ($V_{POS}$) to the FBP and ground pin. Limiting the size of R3 reduces the effect of the FBP bias current. For less than 0.1% error, limit R3 to less than 12kΩ.

$$I_{PGM} = \frac{V_{REF}}{R3} = \frac{1.2V}{12k\Omega} = 100\mu A$$

$$\frac{I_{FBN}}{I_{PGM}} = \frac{0.1\mu A}{100\mu A} = 0.1\%$$

Once R3 has been determined, then solve for R4 (see example in Table 4).

$$R4 = R3 \cdot \left(\frac{V_{POS}}{V_{REF}} - 1\right)$$

| $V_{POS}$ (V) | R4, Closest Value (kΩ) |
|---|---|
| 7 | 59.0 |
| 8 | 69.8 |
| 9 | 78.7 |
| 10 | 88.7 |
| 11 | 100.0 |
| 12 | 110.0 |
| 13 | 120.0 |
| 14 | 130.0 |
| 15 | 140.0 |
| 16 | 150.0 |
| 17 | 160.0 |
| 18 | 169.0 |
| 19 | 180.0 |
| 20 | 191.0 |
| 21 | 200.0 |
| 22 | 210.0 |
| 23 | 220.0 |
| 24 | 232.0 |
| 25 | 240.0 |

**Table 4: Closest Value for R4 if Using 12.1kΩ as R3.**

### Capacitor Selection

Careful selection of the three external capacitors $C_{IN}$, $C_{FLY}$, and $C_{OUT}$ is important because they will affect turn-on time, output ripple, efficiency, and load transient response. Optimum performance will be obtained when low equivalent series resistance (ESR) ceramic capacitors are used. In general, low ESR may be defined as less than 100mΩ. A value of 1μF for input and flying capacitors is a good starting point when designing with the AAT2820. This not only provides for a very small printed circuit board area, but cost is further reduced by the minimized bill of materials.

### Input Capacitor

A 1μF multilayer ceramic chip capacitor is suggested for the input. This capacitor should be connected between the IN pin and ground; 1μF should be suitable for most applications. Even though the AAT2820 switching ripple and noise are very low, back-injected line noise may be further reduced by increasing the value of $C_{IN}$. A low equivalent series inductance (ESL) ceramic capacitor is ideal for this function. The size required will vary depending on the load, output voltage, and input voltage characteristics. Other types of capacitors may be used for $C_{IN}$ at the cost of compromised circuit performance.

### Output Capacitor

The output capacitor ($C_{OUT}$) should be connected between the OUT pin and ground. Switching noise and ripple seen on the charge pump output increases with load current. Typically, the output capacitor should be 5 to 10 times greater than the flying capacitor. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing radiated and conducted EMI.

A 1μF ceramic capacitor is recommended for most applications for optimum transient response. However, if the application has a larger load from the main and multiplier stage charge pump outputs, a 4.7μF ceramic capacitor is suggested to reduce the feedback injection noise from the multiplier stage and lower switching ripple. Capacitor types other than ceramic capacitors can be used for $C_{OUT}$. However, capacitors composed of non-ceramic material will typically have a greater value of ESR, resulting in increased output switching ripple.

### Charge Pump Capacitor ($C_{FLY}$)

Due to the switching operation of the voltage doubling circuit topology, current flow through the flying capacitor is bi-directional. The flying capacitor selected must be a non-polarized type. A 1μF low ESR ceramic capacitor is ideal for most applications.

### Capacitor Characteristics

Ceramic composition capacitors are highly recommended over all other types of capacitors for use with the AAT2820. Ceramic capacitors offer many advantages over their tantalum and aluminum electrolytic counterparts. A ceramic capacitor typically has very low ESR, is lowest cost, has a smaller

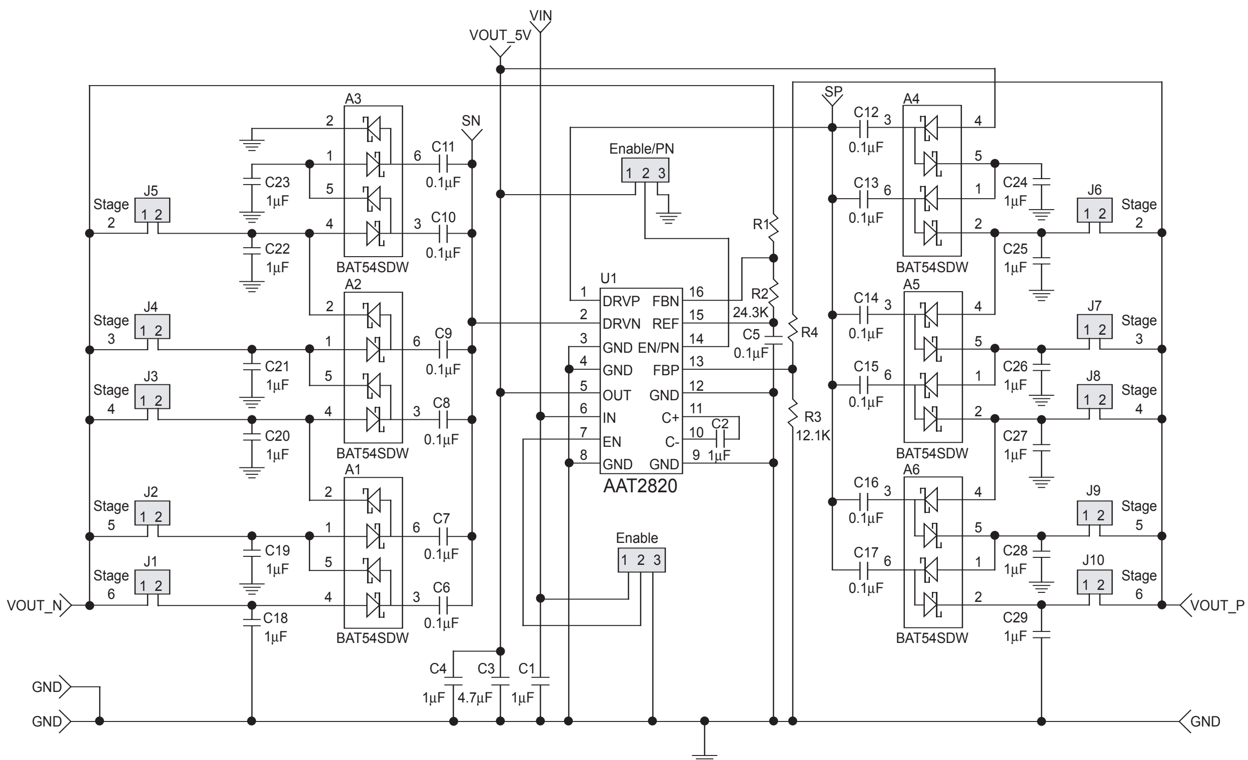
PCB footprint, and is non-polarized. Low ESR ceramic capacitors help maximize charge pump transient response. Since ceramic capacitors are non-polarized, they are not prone to incorrect connection damage.

## Rectifier Diodes

For the rectifiers, use Schottky diodes with a voltage rating of 1.5X the input voltage. The maximum steady-state voltage seen by the rectifier diodes for both the positive and negative charge pumps (regardless of the number of stages) is:

$$V_{RESERVE} = V_{IN} - V_F$$

The BAT54SDW quad Schottky in an SOT363 (2x2mm) package is a good choice for multiple-stage charge pump configuration (see evaluation board schematic in Figure 3).




C1 Taiyo Yuden LMK212 BJ105KD 1µF 10V X7R 0805
C2 Taiyo Yuden LMK107 BJ105KA 1µF 10V X7R 0603
C3 Taiyo Yuden LMK212 BJ475KD 4.7µF 10V X5R 0805
C5, C9-C14 Taiyo Yuden EMK107 BJ104MA 0.1µF 16V X7R 0603
C6-C8, C15-C17 Taiyo Yuden TMK107 BJ104KA 0.1µF 25V X5R 0603
C20-C27 Taiyo Yuden EMK212 BJ105KG 1µF 16V X7R 0805
C18, C19, C28, C29 Taiyo Yuden TMK212 BJ105KG 1µF 25V X5R 0805
[Optional] C4 Taiyo Yuden LMK212 BJ105KD 1µF 10V X7R 0805

**Figure 3: AAT2820 Evaluation Board Schematic (Shown With Six Stages).**

## Flying and Output Capacitor Multiplier Stages

A 0.1µF X7R or X5R ceramic capacitor is typically used. The voltage rating of the flying and reservoir output capacitors will vary with the number of charge pump stages. The reservoir output capacitor should be roughly 10X the flying capacitor. Use larger capacitors for reduced output ripple. A 1µF X7R or X5R type ceramic is typically used.

## Positive Charge Pump Capacitor Voltage Ratings

The absolute steady-state maximum output voltage (neglecting the internal $R_{DS(ON)}$ drop of the internal MOSFETs) for the nth stage is:

$$V_{BULK(n)} = (n + 1) \cdot V_{IN} - 2 \cdot n \cdot V_{FWD}$$

where $V_{FWD}$ is the estimated forward drop of the Schottky diode. This is also the voltage rating required for the nth bulk capacitor in the positive output charge pump.

The voltage rating for the nth flying capacitor in the positive stage is:

$$V_{FLY(n)} = V_{BULK(n+1)} - V_{FWD}$$

where $V_{BULK(0)}$ is the input voltage (see Table 5).

| # of Stages (n) | $V_{BULK(n)}$ | $V_{FLY(n)}$ |
|---|---|---|
| 1 | 9.4V | 4.7V |
| 2 | 13.8V | 9.1V |
| 3 | 18.2V | 13.5V |
| 4 | 22.6V | 17.9V |
| 5 | 27.0V | 22.3V |
| 6 | 31.4V | 26.7V |

**Table 5: Positive Charge Pump Capacitor Voltages ($V_{FWD}$ = 0.31V).**

## Negative Charge Pump Capacitor Voltage Ratings

The absolute steady-state maximum output voltage (neglecting the internal $R_{DS(ON)}$ drop of the internal MOSFETs) for the nth stage is:

$$V_{BULK(n)} = -n \cdot V_{IN} + 2 \cdot n \cdot V_{FWD}$$

This is also the voltage rating required for the nth bulk capacitor in the negative output charge pump.

The voltage rating for the nth flying capacitor in the negative stage (see Table 6) is:

$$V_{FLY(n)} = V_{FWD} - V_{BULK(n)}$$

| # of Stages (n) | $V_{BULK(n)}$ | $V_{FLY(n)}$ |
|---|---|---|
| 1 | -4.4V | 4.7V |
| 2 | -8.8V | 9.1V |
| 3 | -13.2V | 13.5V |
| 4 | -17.6V | 17.9V |
| 5 | -22.0V | 22.3V |
| 6 | -26.4V | 26.7V |

**Table 6: Negative Charge Pump Capacitor Voltages ($V_{FWD}$ = 0.31V).**

## PC Board Layout

The input and reference capacitor should be placed as closely to the IC as possible. Place the programming resistors (R1-R4) close to the IC, minimizing trace length to FBN and FBP. Place the main charge pump flying capacitor close to the C+ and C- pins, with wide traces and no vias. Place all multiplier stage (charge pump) circuitry to the IC as closely as possible using wide traces, and avoid using vias when possible.

Figures 4 and 5 show the recommended evaluation board layout with the TDFN44-16 package.

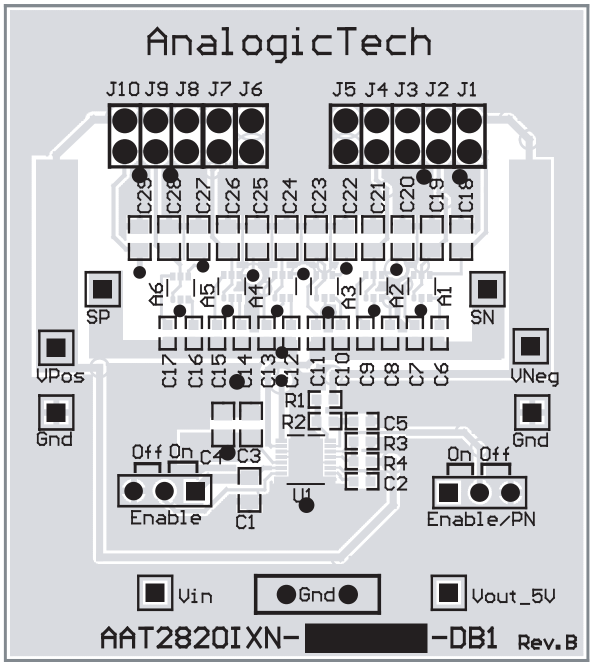



**Figure 4: AAT2820 Evaluation Board Top Side Layout.**

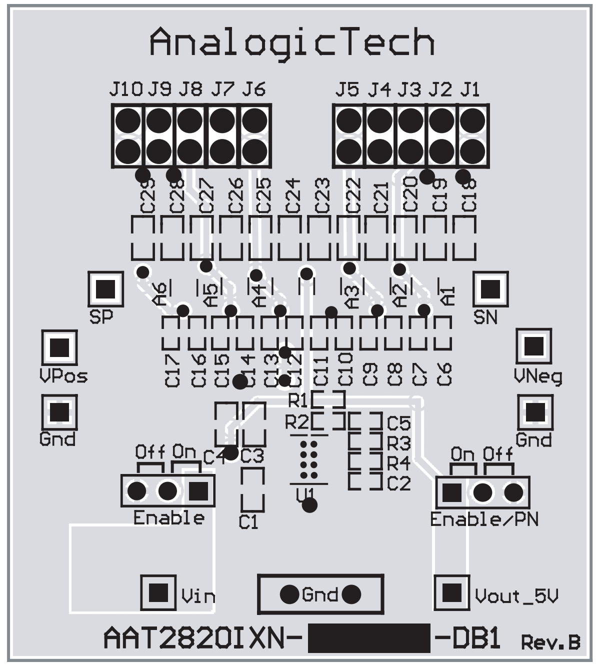



**Figure 5: AAT2820 Evaluation Board Bottom Side Layout.**

## Ordering Information

| Package | Power-Up Sequence | Marking[1] | Part Number (Tape and Reel)[2] |
|---|---|---|---|
| TDFN44-16 | -, + | OCXYY | **AAT2820IXN-5.0-T1** |
| TDFN44-16 | +, - | ODXYY | **AAT2820IXN-5.0-1-T1** |

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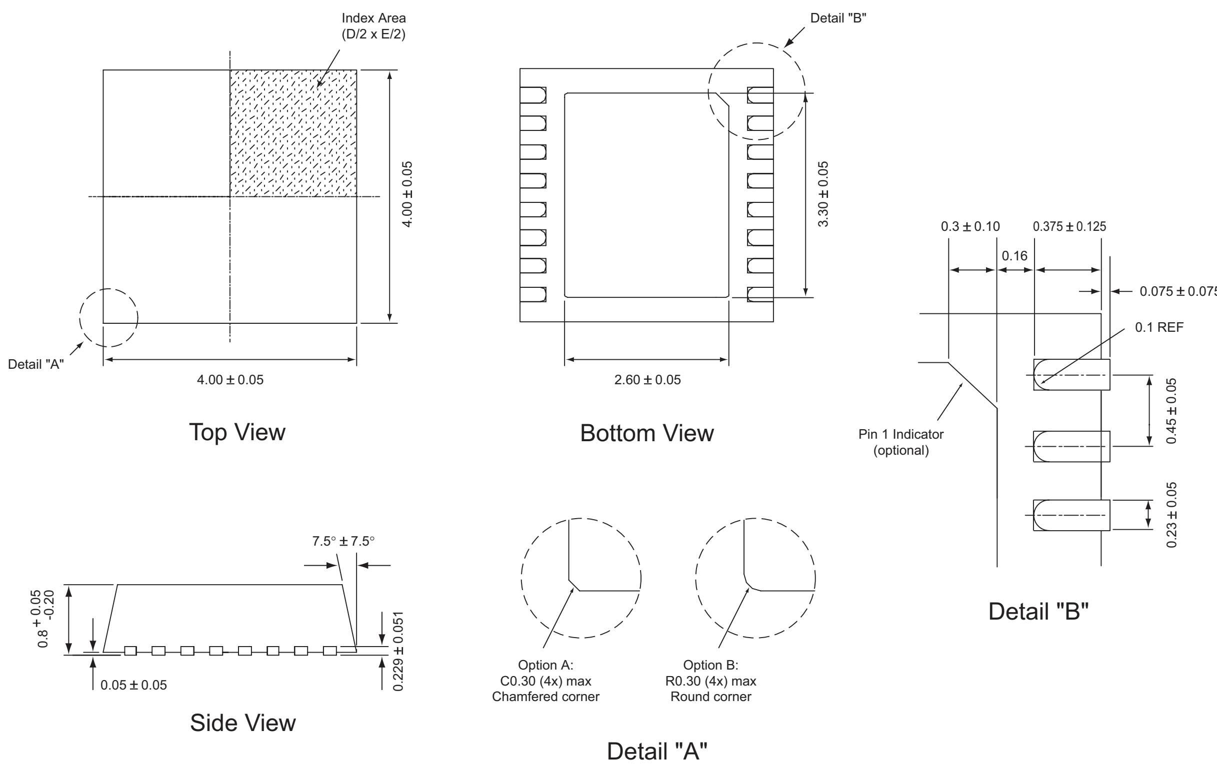
## Package Information




All dimensions in millimeters

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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