Remote 8-bit I/O expander for I²C-bus — PCF8574/PCF8574A

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C). It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only). The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage — 2.5 V to 6 V
- Low stand-by current consumption — max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

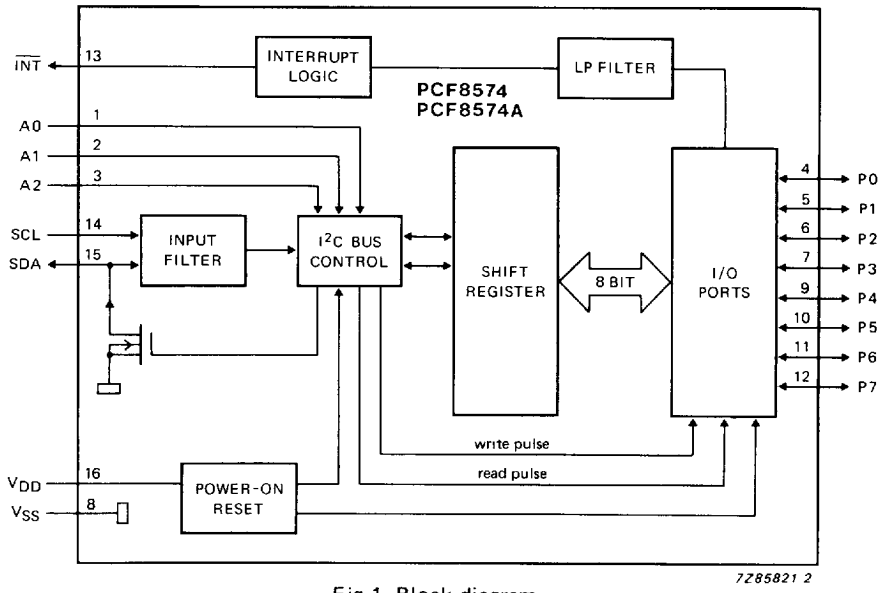


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

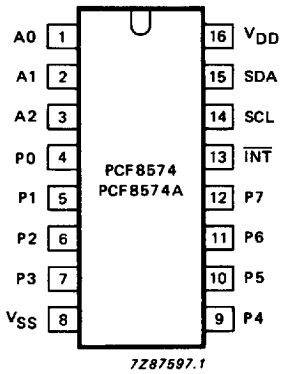


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

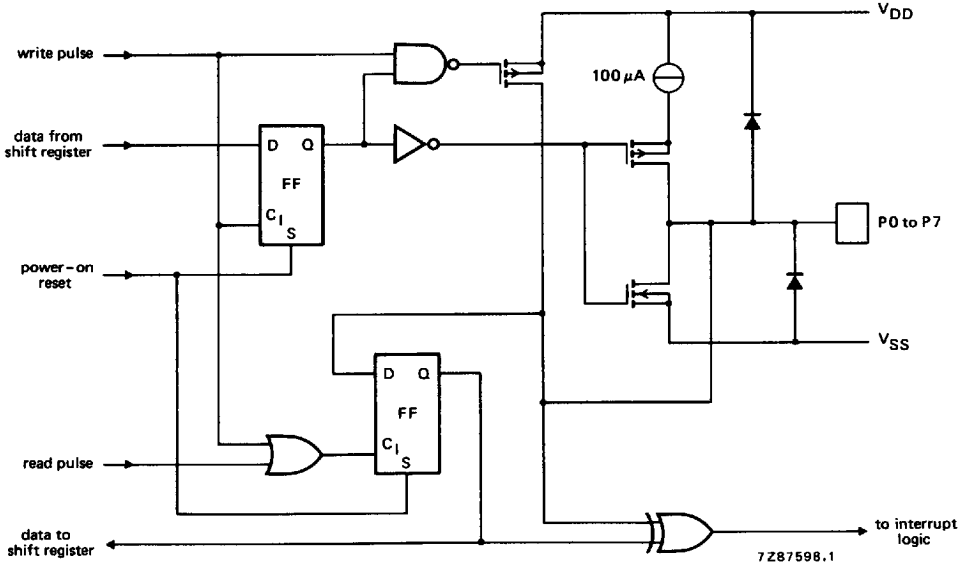


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

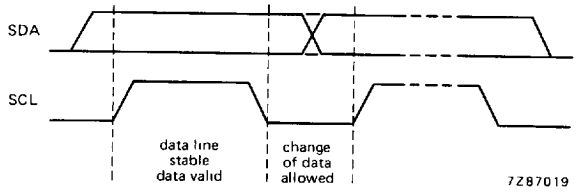


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

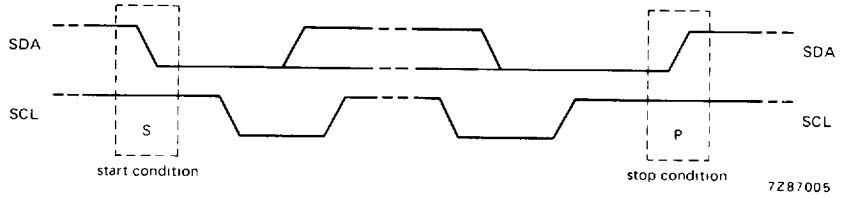


Fig.5 Definition of start and stop conditions.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

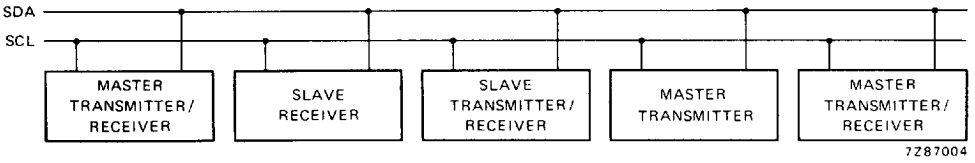


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

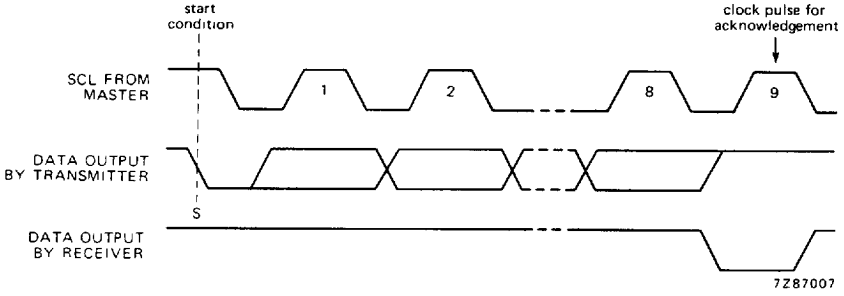


Fig.7 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

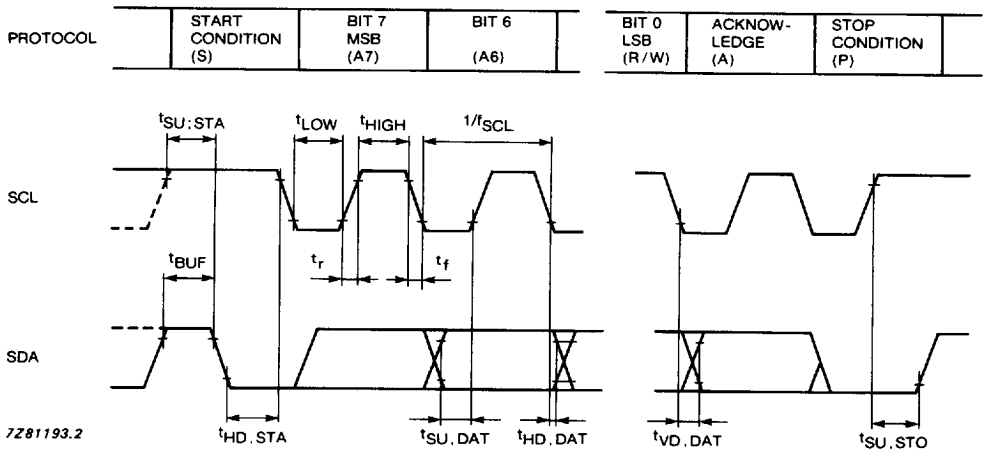
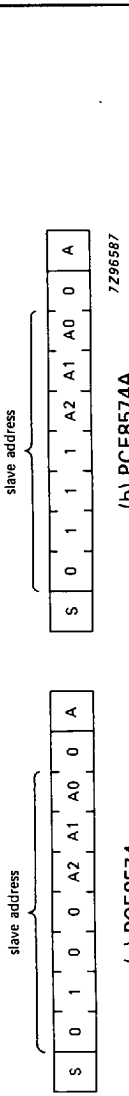


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)



(a) PCF8574.

(b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

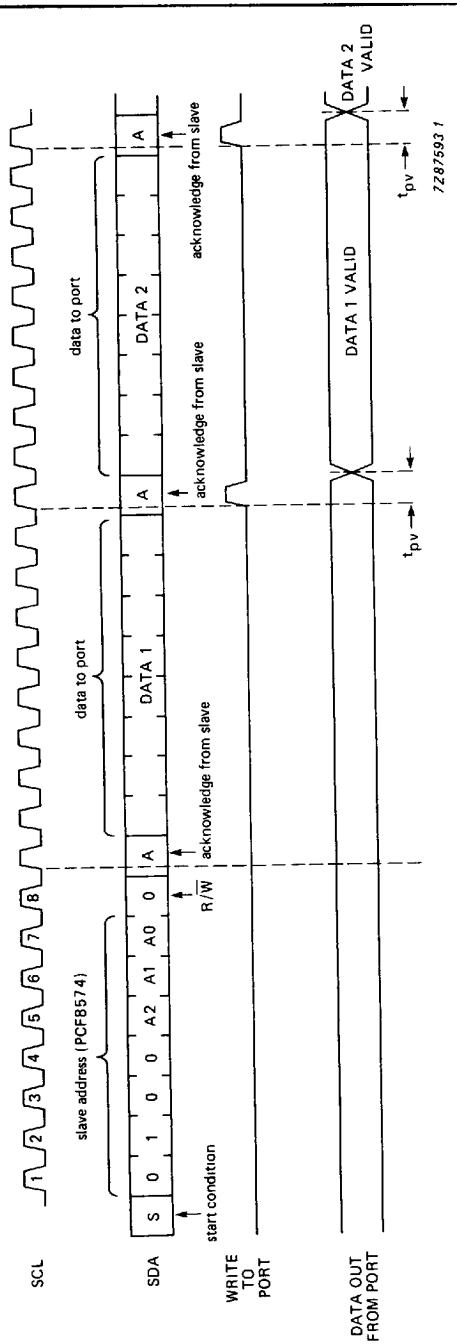


Fig.10 WRITE mode (output port).

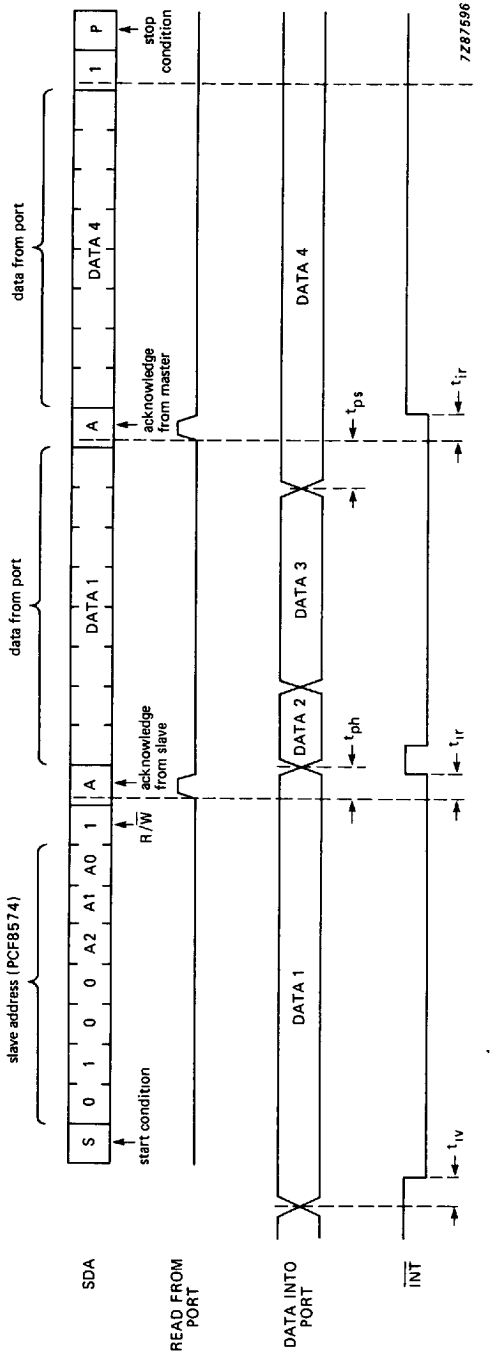


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

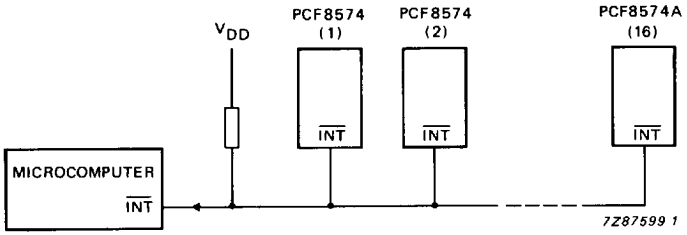


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

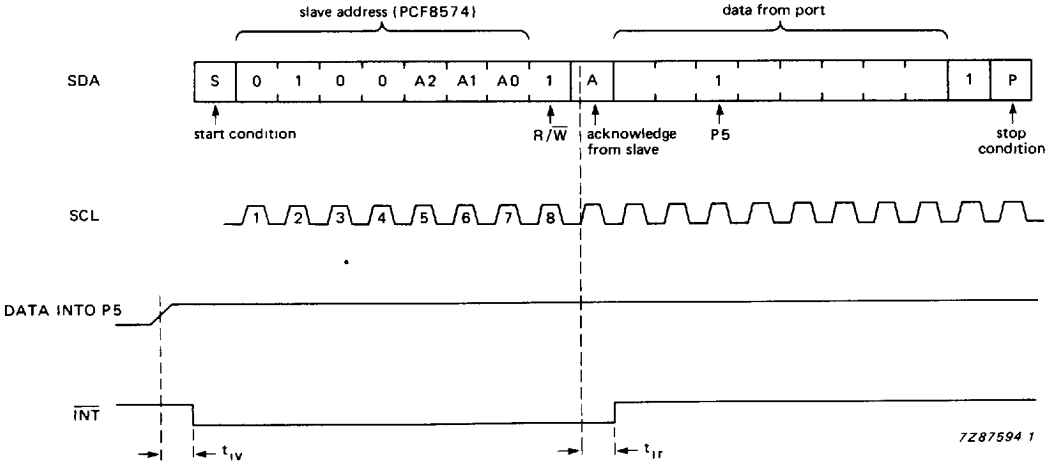


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

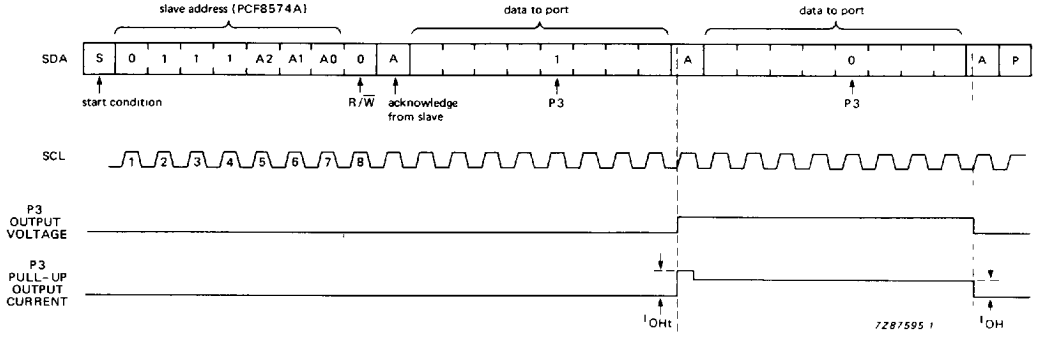


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	–	20	mA
DC output current	$\pm I_O$	–	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	100	mA
Total power dissipation	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	C_L = ⩽ 100 pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L = \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Input leakage current	pin at V_{DD} or V_{SS}	$\|I_L\|$	–	–	250	nA

Note to the characteristics

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).