

November 1997 - Revised July 2004

Features

- Wide Analog Input Voltage Range $\pm 5V$ Max
- Low "On" Resistance
 - 70 Ω Typical ($V_{CC} - V_{EE} = 4.5V$)
 - 40 Ω Typical ($V_{CC} - V_{EE} = 9V$)
- Low Crosstalk between Switches
- Fast Switching and Propagation Speeds
- "Break-Before-Make" Switching
- Wide Operating Temperature Range . . -55 $^{\circ}C$ to 125 $^{\circ}C$
- CD54HC/CD74HC Types
 - Operation Control Voltage 2V to 6V
 - Switch Voltage 0V to 10V
 - High Noise Immunity . . . $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , $V_{CC} = 5V$
- CD54HCT/CD74HCT Types
 - Operation Control Voltage 4.5V to 5.5V
 - Switch Voltage 0V to 10V
 - Direct LSTTL Input Logic Compatibility . . . $V_{IL} = 0.8V$ Max, $V_{IH} = 2V$ Min
 - CMOS Input Compatibility $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

These devices are digitally controlled analog switches which utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e. V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low "on" resistance and low "off" leakages. In addition, all three devices have an enable control which, when high, disables all switches to their "off" state.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4051F3A	-55 to 125	16 Ld CERDIP
CD54HC4052F3A	-55 to 125	16 Ld CERDIP
CD54HC4053F3A	-55 to 125	16 Ld CERDIP
CD54HCT4051F3A	-55 to 125	16 Ld CERDIP

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4051E	-55 to 125	16 Ld PDIP
CD74HC4051M	-55 to 125	16 Ld SOIC
CD74HC4051MT	-55 to 125	16 Ld SOIC
CD74HC4051M96	-55 to 125	16 Ld SOIC
CD74HC4051NSR	-55 to 125	16 Ld SOP
CD74HC4051PWR	-55 to 125	16 Ld TSSOP
CD74HC4051PWT	-55 to 125	16 Ld TSSOP
CD74HC4052E	-55 to 125	16 Ld PDIP
CD74HC4052M	-55 to 125	16 Ld SOIC
CD74HC4052MT	-55 to 125	16 Ld SOIC
CD74HC4052M96	-55 to 125	16 Ld SOIC
CD74HC4052NSR	-55 to 125	16 Ld SOP
CD74HC4052PW	-55 to 125	16 Ld TSSOP
CD74HC4052PWR	-55 to 125	16 Ld TSSOP
CD74HC4052PWT	-55 to 125	16 Ld TSSOP
CD74HC4053E	-55 to 125	16 Ld PDIP
CD74HC4053M	-55 to 125	16 Ld SOIC
CD74HC4053MT	-55 to 125	16 Ld SOIC
CD74HC4053M96	-55 to 125	16 Ld SOIC
CD74HC4053NSR	-55 to 125	16 Ld SOP
CD74HC4053PW	-55 to 125	16 Ld TSSOP
CD74HC4053PWR	-55 to 125	16 Ld TSSOP
CD74HC4053PWT	-55 to 125	16 Ld TSSOP
CD74HCT4051E	-55 to 125	16 Ld PDIP
CD74HCT4051M	-55 to 125	16 Ld SOIC
CD74HCT4051MT	-55 to 125	16 Ld SOIC
CD74HCT4051M96	-55 to 125	16 Ld SOIC
CD74HCT4052E	-55 to 125	16 Ld PDIP
CD74HCT4052M	-55 to 125	16 Ld SOIC
CD74HCT4052MT	-55 to 125	16 Ld SOIC
CD74HCT4052M96	-55 to 125	16 Ld SOIC
CD74HCT4053E	-55 to 125	16 Ld PDIP
CD74HCT4053M	-55 to 125	16 Ld SOIC
CD74HCT4053MT	-55 to 125	16 Ld SOIC
CD74HCT4053M96	-55 to 125	16 Ld SOIC
CD74HCT4053PWR	-55 to 125	16 Ld TSSOP
CD74HCT4053PWT	-55 to 125	16 Ld TSSOP

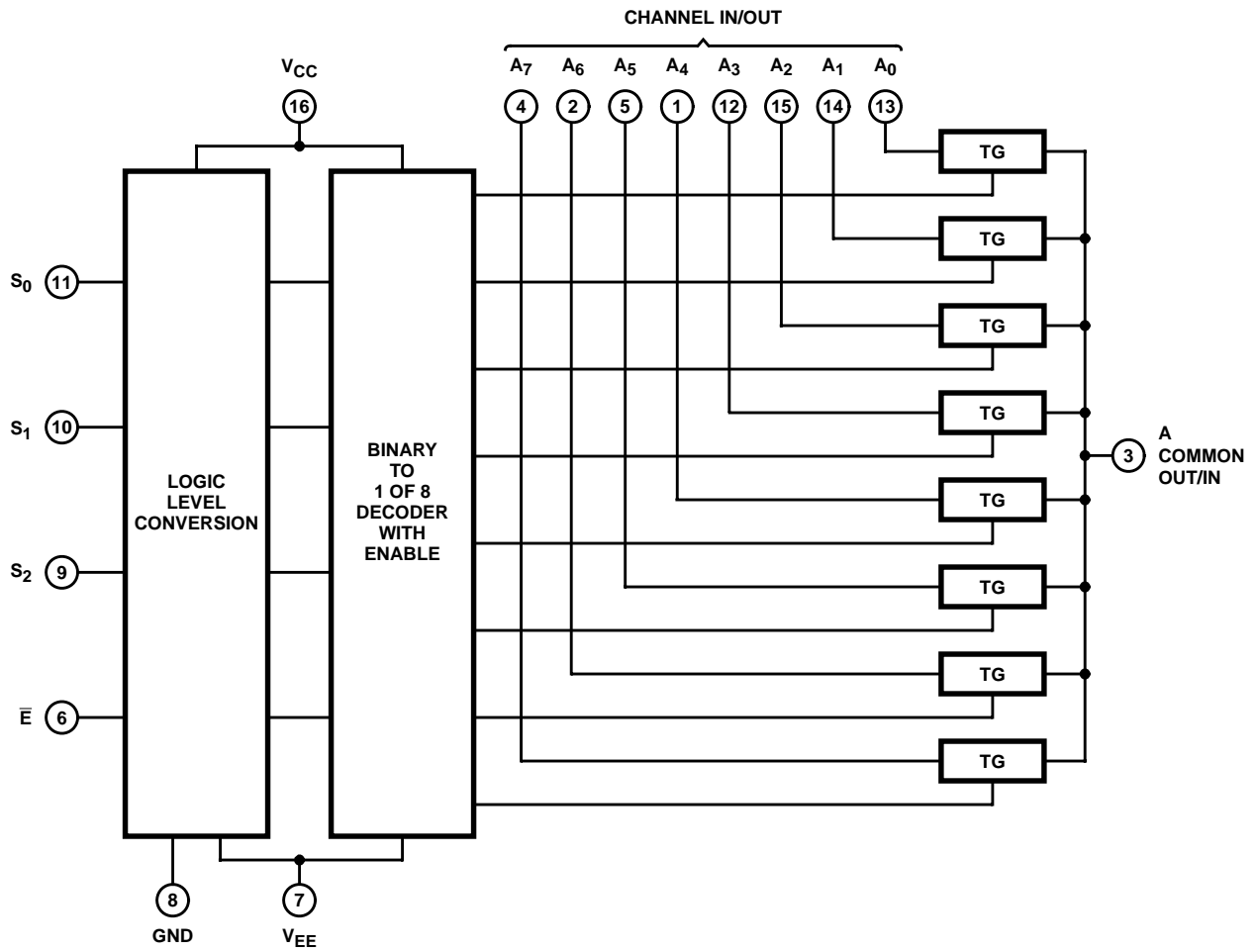
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

Pinouts



Functional Diagram of HC/HCT4051

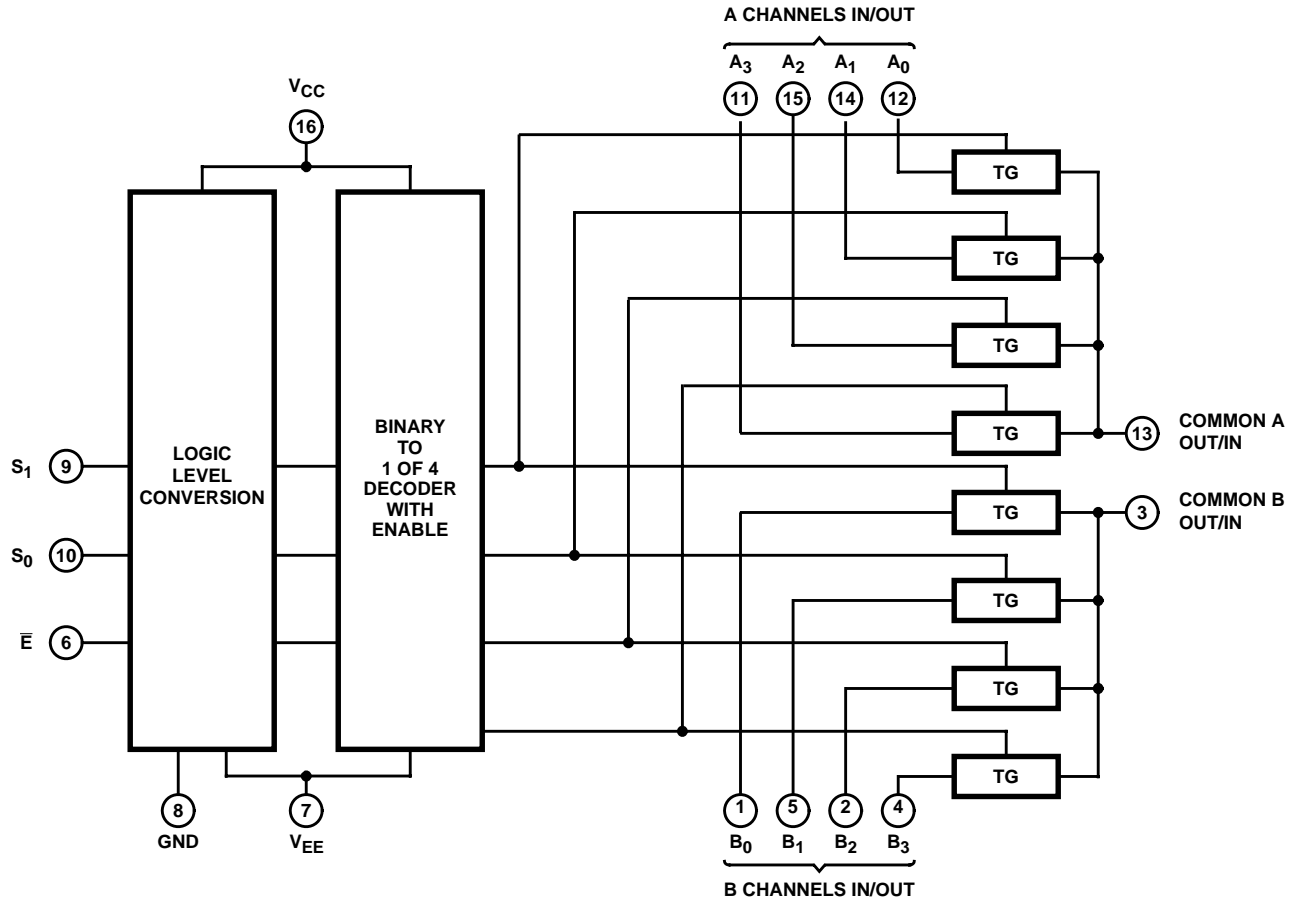


**TRUTH TABLE
HC/HCT4051**

INPUT STATES				"ON" CHANNELS
ENABLE	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

Functional Diagram of 'HC4052, CD74HCT4052



TRUTH TABLE
'HC4052, CD74HCT4052

INPUT STATES			"ON" CHANNELS
ENABLE	S ₁	S ₀	
L	L	L	A0, B0
L	L	H	A1, B1
L	H	L	A2, B2
L	H	H	A3, B3
H	X	X	None

X = Don't care

Functional Diagram of 'HC4053, CD74HCT4053



TRUTH TABLE
'HC4053, CD74HCT4053

INPUT STATES				"ON" CHANNELS
ENABLE	S ₀	S ₁	S ₂	
L	L	L	L	C0, B0, A0
L	H	L	L	C0, B0, A1
L	L	H	L	C0, B1, A0
L	H	H	L	C0, B1, A1
L	L	L	H	C1, B0, A0
L	H	L	H	C1, B0, A1
L	L	H	H	C1, B1, A0
L	H	H	H	C1, B1, A1
H	X	X	X	None

X = Don't care

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

Absolute Maximum Ratings (Note 2)

DC Supply Voltage, $V_{CC} - V_{EE}$	-0.5V to 10.5V
DC Supply Voltage, V_{CC}	-0.5V to +7V
DC Supply Voltage, V_{EE}	+0.5V to -7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Switch Diode Current, I_{OK}	
For $V_I < V_{EE} - 0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Switch Current, (Note 2)	
For $V_I > V_{EE} - 0.5V$ or $V_I < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$
DC V_{EE} Current, I_{EE}	-20mA

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):	
E (PDIP) Package	67°C/W
M (SOIC) Package	73°C/W
NS (SOP) Package	64°C/W
PW (TSSOP) Package	108°C/W
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

PARAMETER	MIN	MAX	UNITS
Supply Voltage Range (For T_A = Full Package Temperature Range), V_{CC} (Note 2)			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
Supply Voltage Range (For T_A = Full Package Temperature Range), $V_{CC} - V_{EE}$			
CD54/74HC Types, CD54/74HCT Types (See Figure 1)	2	10	V
Supply Voltage Range (For T_A = Full Package Temperature Range), V_{EE} (Note 3)			
CD54/74HC Types, CD54/74HCT Types (See Figure 2)	0	-6	V
DC Input Control Voltage, V_I	GND	V_{CC}	V
Analog Switch I/O Voltage, V_{IS}	V_{EE}	V_{CC}	V
Operating Temperature, T_A	-55	125	°C
Input Rise and Fall Times, t_r, t_f			
2V	0	1000	ns
4.5V	0	500	ns
6V	0	400	ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- All voltages referenced to GND unless otherwise specified.
- In certain applications, the external load resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{ON} values shown in Electrical Specifications table). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC/HCT4051; terminals 3 and 13 on the HC/HCT4052; terminals 4, 14 and 15 on the HC/HCT4053.

Recommended Operating Area as a Function of Supply Voltages

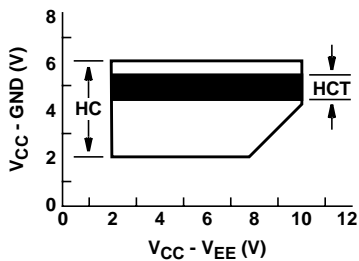


FIGURE 1.

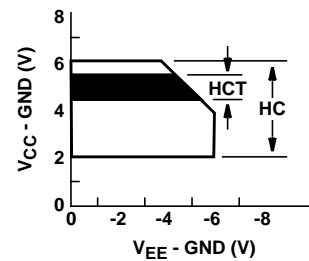


FIGURE 2.

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

DC Electrical Specifications

PARAMETER	TEST CONDITIONS				AMBIENT TEMPERATURE, T _A						UNITS		
	V _{IS} (V)	V _I (V)	V _{EE} (V)	V _{CC} (V)	25°C			-40°C - 85°C		-55°C - 125°C			
					MIN	TYP	MAX	MIN	MAX	MIN		MAX	
HC TYPES													
High Level Input Voltage, V _{IH}				2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	0	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage, V _{IL}				2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
On Resistance, r _{ON} I _O = 1mA, (Figure 11)	V _{CC} or V _{EE}	V _{IL} or V _{IH}	0	4.5	-	70	160	-	200	-	240	Ω	
			0	6	-	60	140	-	175	-	210	Ω	
			-4.5	4.5	-	40	120	-	150	-	180	Ω	
	V _{CC} to V _{EE}		0	4.5	-	90	180	-	225	-	270	Ω	
			0	6	-	80	160	-	200	-	240	Ω	
			-4.5	4.5	-	45	130	-	162	-	195	Ω	
Maximum On Resistance Between any Two Channels, Δr _{ON}			0	4.5	-	10	-	-	-	-	Ω		
			0	6	-	8.5	-	-	-	-	Ω		
			-4.5	4.5	-	5	-	-	-	-	Ω		
Switch On/Off Leakage Current, I _{IZ}	For Switch Off: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For Switch On: All Applicable Combinations of V _{IS} and V _{OS} Voltage Levels	V _{IL} or V _{IH}											
			1 and 2 Channels	0	6	-	-	±0.1	-	±1	-	±1	μA
			4053	-5	5	-	-	±0.1	-	±1	-	±1	μA
			4 Channels	0	6	-	-	±0.1	-	±1	-	±1	μA
			4052	-5	5	-	-	±0.2	-	±2	-	±2	μA
			8 Channels	0	6	-	-	±0.2	-	±2	-	±2	μA
			4051	-5	5	-	-	±0.4	-	±4	-	±4	μA
Control Input Leakage Current, I _{IL}		V _{CC} or GND	0	6	-	-	±0.1	-	±1	-	±1	μA	
Quiescent Device Current, I _{CC} I _O = 0	When V _{IS} = V _{EE} , V _{OS} = V _{CC}	V _{CC} or GND	0	6	-	-	8	-	80	-	160	μA	
	When V _{IS} = V _{CC} , V _{OS} = V _{EE}		-5	5	-	-	16	-	160	-	320	μA	

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS				AMBIENT TEMPERATURE, T _A						UNITS		
	V _{IS} (V)	V _I (V)	V _{EE} (V)	V _{CC} (V)	25°C			-40°C - 85°C		-55°C - 125°C			
					MIN	TYP	MAX	MIN	MAX	MIN		MAX	
HCT TYPES													
High Level Input Voltage, V _{IH}				4.5 to 5.5	2	-	-	2	-	2	-	V	
Low Level Input Voltage, V _{IL}				4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V	
On Resistance, r _{ON} I _O = 1mA, (Figure 15)	V _{CC} or V _{EE}	V _{IL} or V _{IH}	0	4.5	-	70	160	-	200	-	240	Ω	
			-	-	-	-	-	-	-	-	-	Ω	
			-4.5	4.5	-	40	120	-	150	-	180	Ω	
	V _{CC} to V _{EE}		0	4.5	-	90	180	-	225	-	270	Ω	
			-	-	-	-	-	-	-	-	-	-	Ω
			-4.5	4.5	-	45	130	-	162	-	195	Ω	
Maximum On Resistance Between any Two Channels, Δr _{ON}			0	4.5	-	10	-	-	-	-	-	Ω	
			-	-	-	-	-	-	-	-	-	Ω	
			-4.5	4.5	-	5	-	-	-	-	-	Ω	
Switch On/Off Leakage Current, I _{Iz}	For Switch Off: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For Switch On: All Applicable Combinations of V _{IS} and V _{OS} Voltage Levels	V _{IL} or V _{IH}											
1 and 2 Channels			0	6	-	-	±0.1	-	±1	-	±1	μA	
4053			-5	5	-	-	±0.1	-	±1	-	±1	μA	
4 Channels			0	6	-	-	±0.1	-	±1	-	±1	μA	
4052			-5	5	-	-	±0.2	-	±2	-	±2	μA	
8 Channels			0	6	-	-	±0.2	-	±2	-	±2	μA	
4051	-5	5	-	-	±0.4	-	±4	-	±4	μA			
Control Input Leakage Current, I _{IL}	-	(Note 4)	-	5.5	-	-	±0.1	-	±1	-	±1	μA	
Quiescent Device Current, I _{CC} I _O = 0	When V _{IS} = V _{EE} , V _{OS} = V _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA	
	When V _{IS} = V _{CC} , V _{OS} = V _{EE}		-4.5	5.5	-	-	16	-	160	-	320	μA	
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 5)	V _{CC} - 2.1	4.5 to 5.5	-	100	360	-	450	-	490	μA		

NOTES:

- Any voltage between V_{CC} and GND.
- For dual supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

TYPE	INPUT	UNIT LOADS (NOTE)
4051, 4053	All	0.5
4052	All	0.4

NOTE: Unit load is ΔI_{CC} limit specified in DC Specifications table, e.g., 360mA max. at 25°C.

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

Switching Specifications $V_{CC} = 5V$, $T_A = 25^{\circ}C$, Input t_r , $t_f = 6ns$

PARAMETER	C_L (pF)	TYPICAL						UNITS
		4051		4052		4053		
		HC	HCT	HC	HCT	HC	HCT	
Propagation Delay Switch IN to OUT, t_{PHL} , t_{PLH}	15	4	4	4	4	4	4	ns
Switch Turn-Off (S or \bar{E}), t_{PHZ} , t_{PLZ}	15	19	19	21	21	18	18	ns
Switch Turn-On (S or \bar{E}), t_{PZH} , t_{PZL}	15	19	23	27	29	18	20	ns
Power Dissipation Capacitance, C_{PD} (Note 6)	-	50	52	74	76	38	42	pF

NOTE:

6. C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_I + \sum (C_L + C_S) V_{CC}^2 f_O$$

f_O = output frequency

f_I = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

Switching Specifications $C_L = 50pF$, Input t_r , $t_f = 6ns$

PARAMETER	V_{EE} (V)	V_{CC} (V)	AMBIENT TEMPERATURE, T_A												UNITS	
			25°C				-40°C - 85°C				-55°C - 125°C					
			HC		HCT		HC		HCT		HC		HCT			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Propagation Delay, Switch In to Out, t_{PLH} , t_{PHL}	0	2	-	60	-	-	-	75	-	-	-	90	-	-	ns	
	0	4.5	-	12	-	12	-	15	-	15	-	18	-	18	ns	
	0	6	-	10	-	-	-	13	-	-	-	15	-	-	ns	
	-4.5	4.5	-	8	-	8	-	10	-	10	-	12	-	12	ns	
Maximum Switch Turn "Off" Delay from S or \bar{E} to Switch Output t_{PHZ} , t_{PLZ}	4051	0	2	-	225	-	-	-	280	-	-	-	340	-	-	ns
		0	4.5	-	45	-	45	-	56	-	56	-	68	-	68	ns
		0	6	-	38	-	-	-	48	-	-	-	57	-	-	ns
		-4.5	4.5	-	32	-	32	-	40	-	40	-	48	-	48	ns
	4052	0	2	-	250	-	-	-	315	-	-	-	375	-	-	ns
		0	4.5	-	50	-	50	-	63	-	63	-	75	-	75	ns
		0	6	-	43	-	-	-	54	-	-	-	65	-	-	ns
		-4.5	4.5	-	38	-	38	-	48	-	48	-	57	-	57	ns
	4053	0	2	-	210	-	-	-	265	-	-	-	315	-	-	ns
		0	4.5	-	42	-	44	-	53	-	55	-	63	-	66	ns
		0	6	-	36	-	-	-	45	-	-	-	54	-	-	ns
		-4.5	4.5	-	29	-	31	-	36	-	39	-	44	-	47	ns

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

Switching Specifications $C_L = 50\text{pF}$, Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER		V_{EE} (V)	V_{CC} (V)	AMBIENT TEMPERATURE, T_A												UNITS
				25°C				-40°C - 85°C				-55°C - 125°C				
				HC		HCT		HC		HCT		HC		HCT		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Maximum Switch Turn "On" Delay from S or E to Switch Output t_{PZL}, t_{PZH}	4051	0	2	-	225	-	-	-	280	-	-	-	340	-	-	ns
		0	4.5	-	45	-	55	-	56	-	69	-	68	-	83	ns
		0	6	-	38	-	-	-	48	-	-	-	57	-	-	ns
		-4.5	4.5	-	32	-	39	-	40	-	49	-	48	-	59	ns
	4052	0	2	-	325	-	-	-	405	-	-	-	490	-	-	ns
		0	4.5	-	65	-	70	-	81	-	68	-	98	-	105	ns
		0	6	-	55	-	-	-	69	-	-	-	83	-	-	ns
		-4.5	4.5	-	46	-	48	-	58	-	60	-	69	-	72	ns
	4053	0	2	-	220	-	-	-	275	-	-	-	330	-	-	ns
		0	4.5	-	44	-	48	-	55	-	60	-	66	-	72	ns
		0	6	-	37	-	-	-	47	-	-	-	56	-	-	ns
		-4.5	4.5	-	31	-	34	-	39	-	43	-	47	-	51	ns
Input (Control) Capacitance, C_I	-	-	-	10	-	10	-	10	-	10	-	10	-	10	pF	

Analog Channel Specifications Typical Values at $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	HC/HCT TYPES	V_{EE} (V)	V_{CC} (V)	HC/HCT	UNITS
Switch Input Capacitance, C_I		All	-	-	5	pF
Common Output Capacitance, C_{COM}		4051	-	-	25	pF
		4052	-	-	12	pF
		4053	-	-	8	pF
Minimum Switch Frequency Response at -3dB, f_{MAX} (Figures 12, 14, 16)	See Figure 3 (Notes 7, 8)	4051	-2.25	2.25	145	MHz
		4052			165	MHz
		4053			200	MHz
		4051	-4.5	4.5	180	MHz
		4052			185	MHz
		4053			200	MHz

'HC4051, 'HCT4051, 'HC4052, CD74HCT4052, 'HC4053, CD74HCT4053

Analog Channel Specifications Typical Values at $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	HC/HCT TYPES	V_{EE} (V)	V_{CC} (V)	HC/HCT	UNITS
Crosstalk Between any Two Switches (Note 10)	See Figure 4 (Notes 8, 9)	4051	-2.25	2.25	N/A	dB
		4052			(TBE)	dB
		4053			(TBE)	dB
		4051	-4.5	4.5	N/A	dB
		4052			(TBE)	dB
		4053			(TBE)	dB
Sinewave Distortion	See Figure 5	All	-2.25	2.25	0.035	%
		All	-4.5	4.5	0.018	%
\bar{E} or S to Switch Feedthrough Noise	See Figure 6 (Notes 8, 9)	4051	-2.25	2.25	(TBE)	mV
		4052				mV
		4053				mV
		4051	-4.5	4.5	(TBE)	mV
		4052				mV
		4053				mV
Switch "OFF" Signal Feedthrough (Figures 13, 15, 17)	See Figure 7 (Notes 8, 9)	4051	-2.25	2.25	-73	dB
		4052			-65	dB
		4053			-64	dB
		4051	-4.5	4.5	-75	dB
		4052			-67	dB
		4053			-66	dB

NOTES:

7. Adjust input voltage to obtain 0dBm at V_{OS} for $f_{IN} = 1\text{MHz}$.
8. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
9. Adjust input for 0dBm.
10. Not applicable for HC/HCT4051.

Test Circuits and Waveforms



FIGURE 3. FREQUENCY RESPONSE TEST CIRCUIT



FIGURE 4. CROSSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

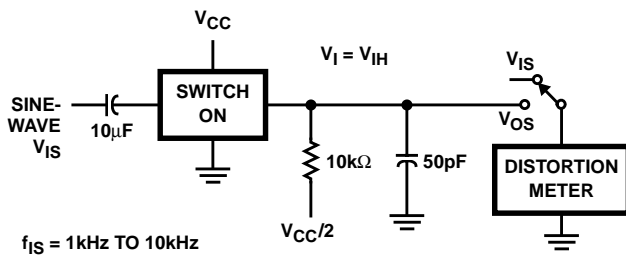


FIGURE 5. SINEWAVE DISTORTION TEST CIRCUIT

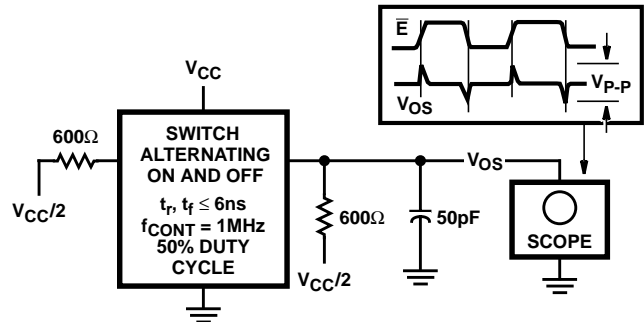


FIGURE 6. CONTROL TO SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

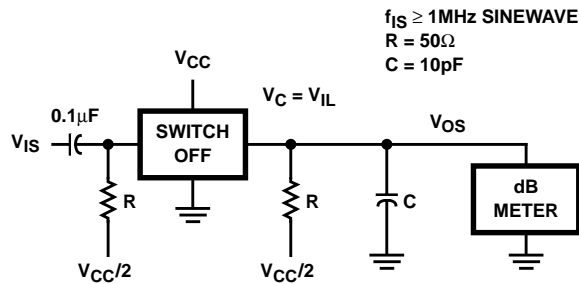


FIGURE 7. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms (Continued)

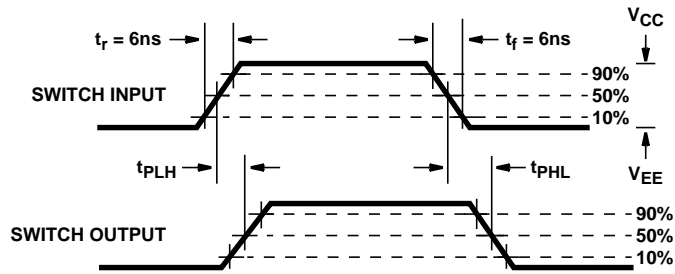


FIGURE 8A.

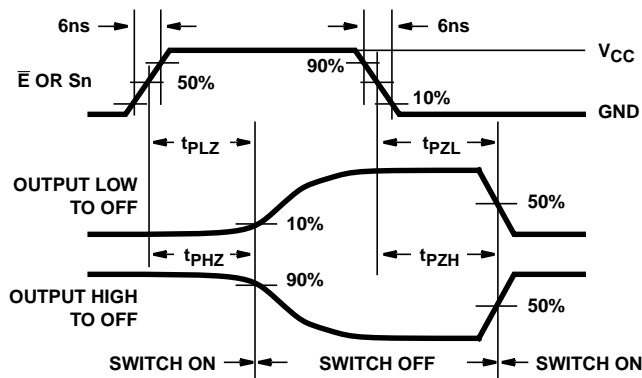


FIGURE 8B. HC TYPES

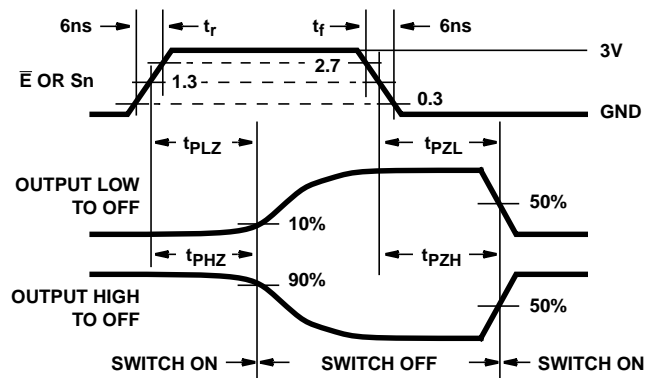


FIGURE 8C. HCT TYPES

FIGURE 8. SWITCH PROPAGATION DELAY, TURN-ON, TURN-OFF TIMES



FIGURE 9. SWITCH ON/OFF PROPAGATION DELAY TEST CIRCUIT

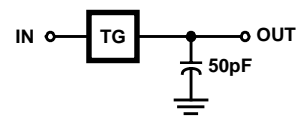


FIGURE 10. SWITCH IN TO SWITCH OUT PROPAGATION DELAY TEST CIRCUIT

Typical Performance Curves



FIGURE 11. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE



FIGURE 12. CHANNEL ON BANDWIDTH (HC/HCT4051)

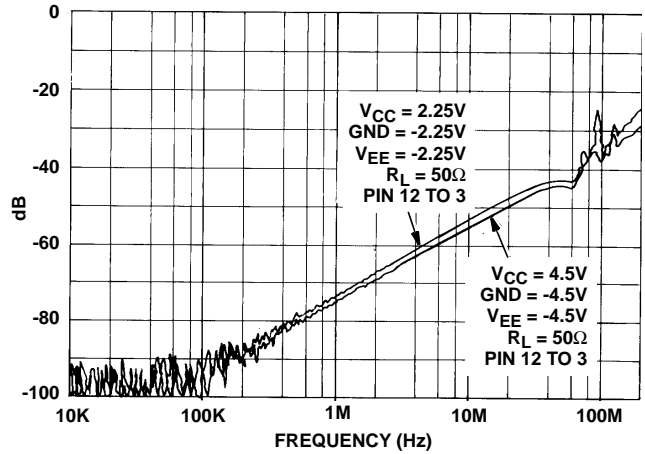


FIGURE 13. CHANNEL OFF FEEDTHROUGH (HC/HCT4051)



FIGURE 14. CHANNEL ON BANDWIDTH (HC/HCT4052)



FIGURE 15. CHANNEL OFF FEEDTHROUGH (HC/HCT4052)

Typical Performance Curves (Continued)

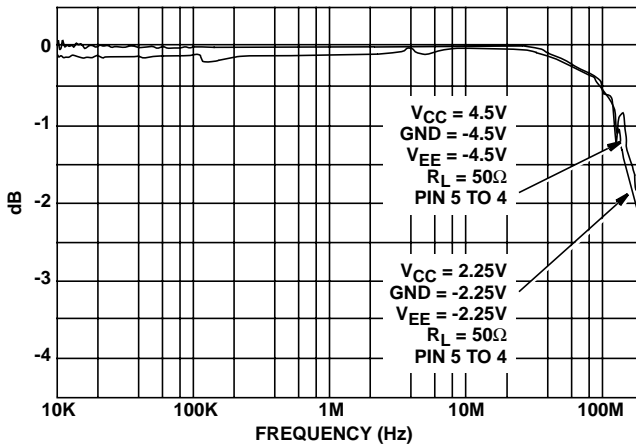


FIGURE 16. CHANNEL ON BANDWIDTH (HC/HCT4053)

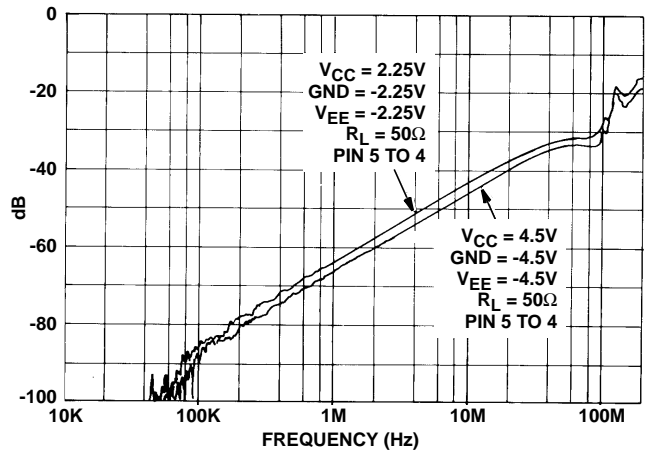


FIGURE 17. CHANNEL OFF FEEDTHROUGH (HC/HCT4053)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8775401EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-8855601EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9065401MEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4051F	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4051F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4052F	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4052F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4053F	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HC4053F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD54HCT4051F3A	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
CD74HC4051E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4051EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4051PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4052EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HC4052ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4052SM	OBSOLETE	SSOP	DB	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4053EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HC4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HC4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HC4053PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4051EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4051M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4051MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4052EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4052M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4052MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4053EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD74HCT4053M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HCT4053ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053MTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74HCT4053PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

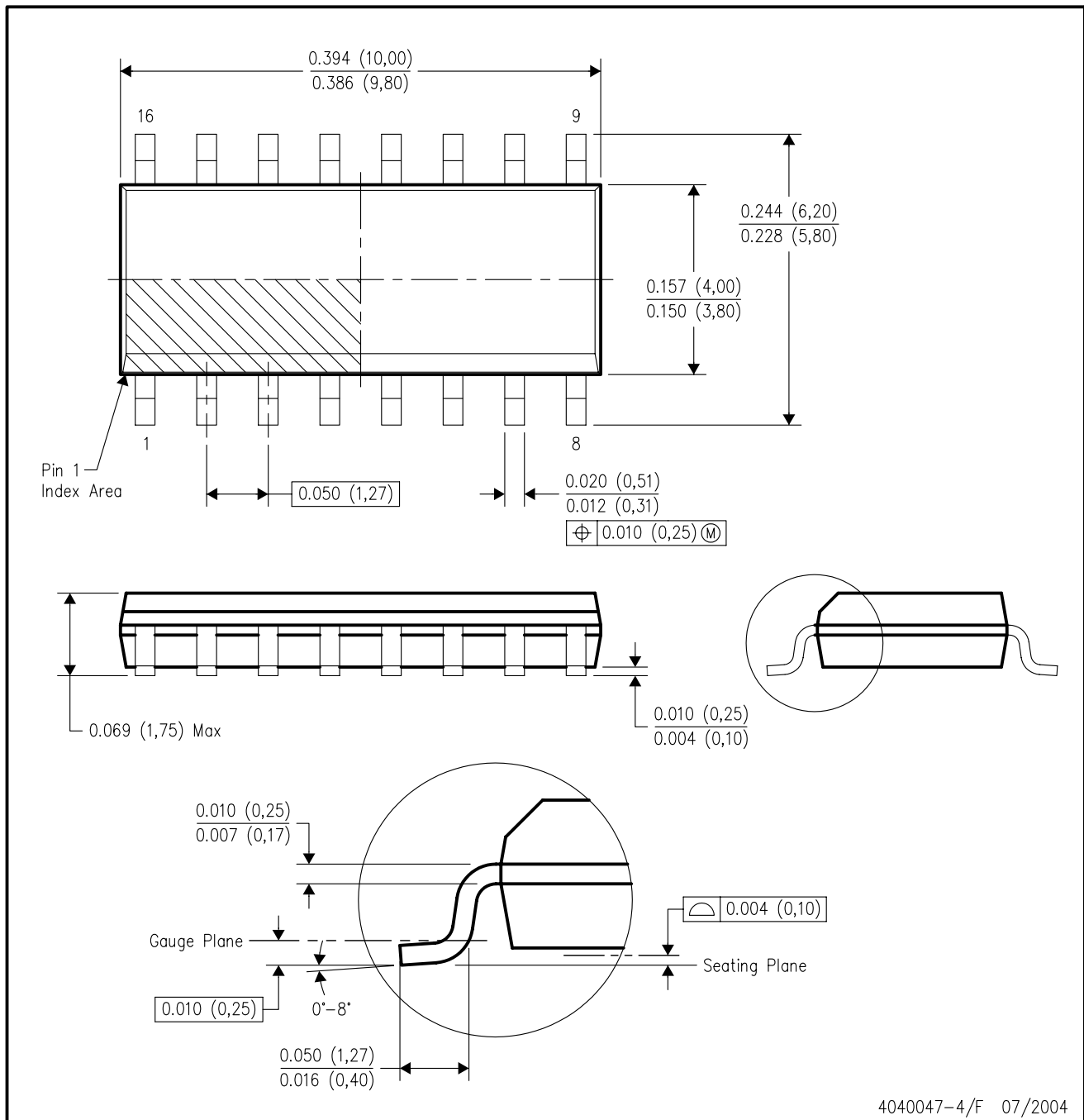
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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View ROHS Compliant Devices

clear gif

CD74HC4051, Status: ACTIVE

View RoHS Compliant Devices

High Speed CMOS 8-Channel Analog Multiplexer/Demultiplexer



clear gif

<input type="checkbox"/> Features	<input type="checkbox"/> Samples	<input type="checkbox"/> Technical Documents
<input type="checkbox"/> Quality & Pb-Free Data	<input type="checkbox"/> Pricing/Packaging	<input type="checkbox"/> Applications Notes
<input type="checkbox"/> Related Products	<input type="checkbox"/> Inventory	<input type="checkbox"/> Simulation Models
<input type="checkbox"/> Tools & Software	<input type="checkbox"/> Symbols/Footprints	<input type="checkbox"/> Reference Designs



Refine Your Selection

- Logic: Analog Switches Multiplexers

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet



Download Datasheet

CD54/74HC4051, CD54/74HCT4051, CD54/74HC4052, CD74HCT4052, CD54/74HC4053 (Rev. I) (cd74hc4051.pdf, 465 KB)
15 Jul 2004 Download

	CD54HC4051	CD74HC4051	CD74HC4051-EP
Number of Channels		8	8
Pd(Typ)(mW)		-	-
Configuration		1 X 1:8 MUX	1 X 1:8 MUX
ron(max)(ohms)		130	180
tpd max(ns)		60	60
Dual Supply (+/- V)(Min)(V)		1	
Dual Supply (+/- V)(Max)(V)		5	
Voltage Nodes(V)	6, 5, 2	2, 4.5, 6	2, 4.5, 6
IL OFF(Max)(nA)		+/-1000	
RON Mis-match(Max)(Ohms)		5	
ON Time(Max)(ns)		40	
OFF Time(Max)(ns)		40	
	Samples	Samples	Samples
	Inventory	Inventory	Inventory

Product Information

Features

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- Wide Analog Input Voltage Range ©5V Max
- Low "On" Resistance
 - 70 Typical ($V_{CC} - V_{EE} = 4.5V$)
 - 40 Typical ($V_{CC} - V_{EE} = 9V$)
- Low Crosstalk between Switches
- Fast Switching and Propagation Speeds
- "Break-Before-Make" Switching
- Wide Operating Temperature Range . . -55°C to 125°C
- CD54HC/CD74HC Types
 - Operation Control Voltage 2V to 6V
 - Switch Voltage 0V to 10V
 - High Noise Immunity . . . $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , $V_{CC} = 5V$
- CD54HCT/CD74HCT Types
 - Operation Control Voltage 4.5V to 5.5V
 - Switch Voltage 0V to 10V
 - Direct LSTTL Input Logic Compatibility . . . $V_{IL} = 0.8V$ Max, $V_{IH} = 2V$ Min
 - CMOS Input Compatibility. $I_I = 1\mu A$ at V_{OL} , V_{OH}

Data sheet acquired from Harris Semiconductor

Description

These devices are digitally controlled analog switches which utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range (i.e. V_{CC} to V_{EE}). They are bidirectional switches thus allowing any analog input to be used as an output and visa-versa. The switches have low "on" resistance and low "off" leakages. In addition, all three devices have an enable control which, when high, disables all switches to their "off" state.

Pricing/Packaging/CAD Design Tools/Samples								
Device	Status	Temp (°C)	Price Budget Price (\$US) QTY	Packaging Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	CAD Design Tools Footprints	Samples
CD74HC4051E	ACTIVE	-55 to 125	0.27 1KU	PDIP (N) 16	View	25	<input type="checkbox"/>	Contact TI Distributor or Sales Office
CD74HC4051EE4	ACTIVE	-55 to 125	0.27 1KU	PDIP (N) 16	View	25	<input type="checkbox"/>	Request Free Samples
CD74HC4051M	ACTIVE	-55 to 125	0.24 1KU	SOIC (D) 16	View	40	<input type="checkbox"/>	Purchase Samples
CD74HC4051M96	ACTIVE	-55 to 125	0.24 1KU	SOIC (D) 16	View	2500	<input type="checkbox"/>	Contact TI Distributor or Sales Office
CD74HC4051M96E4	ACTIVE	-55 to 125	0.24 1KU	SOIC (D) 16	View	2500	<input type="checkbox"/>	Request Free Samples
CD74HC4051ME4	ACTIVE	-55 to 125	0.24 1KU	SOIC (D) 16	View	40	<input type="checkbox"/>	Purchase Samples
CD74HC4051MT	ACTIVE	-55 to 125	0.34 1KU	SOIC (D) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC4051MTE4	ACTIVE	-55 to 125	0.34 1KU	SOIC (D) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC4051NSR	ACTIVE	-55 to 125	0.24 1KU	SO (NS) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4051NSRE4	ACTIVE	-55 to 125	0.24 1KU	SO (NS) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4051PWR	ACTIVE	-55 to 125	0.24 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
CD74HC4051PWRG4	ACTIVE	-55 to 125	0.29 1KU	TSSOP (PW) 16	View	2000	<input type="checkbox"/>	Purchase Samples
CD74HC4051PWT	ACTIVE	-55 to 125	0.34 1KU	TSSOP (PW) 16	View	250	<input type="checkbox"/>	Purchase Samples
CD74HC4051PWTE4	ACTIVE	-55 to 125	0.34 1KU	TSSOP (PW) 16	View	250	<input type="checkbox"/>	Purchase Samples

Inventory							
CD74HC4051E	TI Inventory Status			Reported Distributor Inventory			
	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 23 Jan	10 Weeks	Americas	DigiKey	498	<input type="text"/>
					Newark InOne	912	<input type="text"/>
				Asia	P&S	35	<input type="text"/>
				Europe	Abacus Polar	>1k	<input type="text"/>
					Arrow Southern Europe	>1k	<input type="text"/>
					Avnet-SILICA	>1k	<input type="text"/>
					Spoerle	728	<input type="text"/>
CD74HC4051EE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			

[View all Distributors](#)



	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 23 Jan	10 Weeks	None Reported	View Distributors		
CD74HC4051M	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	3000 16 Jan	10 Weeks	Americas	Newark InOne	>1k	<input type="text"/>
		>10k 26 Jan		Europe	Abacus Polar	>1k	<input type="text"/>
					Arrow Northern Europe	>1k	<input type="text"/>
					Avnet-SILICA	>1k	<input type="text"/>
					EBV Elektronik	>1k	<input type="text"/>
					Farnell InOne	>1k	<input type="text"/>
CD74HC4051M96	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 26 Jan	18 Weeks	Americas	Avnet	>1k	<input type="text"/>
				Europe	Abacus Polar	>1k	<input type="text"/>
					Arrow Northern Europe	>1k	<input type="text"/>
					Arrow Southern Europe	>1k	<input type="text"/>
CD74HC4051M96E4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 26 Jan	18 Weeks	None Reported	View Distributors		
CD74HC4051ME4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	3000 16 Jan	10 Weeks	None Reported View Distributors			
		>10k 26 Jan					
CD74HC4051MT	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 24 Jan	10 Weeks	None Reported	View Distributors		
CD74HC4051MTE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 24 Jan	10 Weeks	None Reported	View Distributors		
CD74HC4051NSR	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	684 20 Jan	10 Weeks	Americas	Rochester Electronics	>1k	<input type="text"/>
		>10k 23 Jan					
CD74HC4051NSRE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

	0*	684 20 Jan	10 Weeks	None Reported View Distributors			
		>10k 23 Jan					
CD74HC4051PWR	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 27 Feb	13 Weeks	Europe	Arrow Northern Europe	>1k	<input type="text"/>
CD74HC4051PWRG4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
CD74HC4051PWT	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	>10k*		12 Weeks	None Reported View Distributors			
CD74HC4051PWTE4	As of 9:50 AM GMT, 29 Nov 2005			As of 9:50 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	>10k*		12 Weeks	None Reported View Distributors			

* Our information is updated daily, so please check back with us soon if this does not meet your needs. You may also contact your [TI Authorized Distributor](#), including those [listed above](#), for real time stock information.

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Quality & Lead (Pb)-Free Data

	Product Content			MTBF/FIT Rate	
Device	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
CD74HC4051E <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
CD74HC4051EE4 <input type="checkbox"/>	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC	View	View
CD74HC4051M <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051M96 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051M96E4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051ME4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051MT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051MTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051NSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051NSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051PWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051PWRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051PWT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
CD74HC4051PWTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents

<input type="checkbox"/> Datasheets	Keep track of what's new
CD54/74HC4051, CD54/74HCT4051, CD54/74HC4052, CD74HCT4052, CD54/74HC4053 (Rev. I) (cd74hc4051.pdf, 465 KB)	
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<input type="checkbox"/> Application Notes	

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)

29 Aug 2002 [Abstract](#)

Selecting the Right Texas Instruments Signal Switch (szza030.htm, 9 KB)

07 Sep 2001 [Abstract](#)

Implications of Slow or Floating CMOS Inputs (Rev. C) (scba004c.htm, 9 KB)

01 Feb 1998 [Abstract](#)

CMOS Power Consumption and CPD Calculation (Rev. B) (scaa035b.htm, 9 KB)

01 Jun 1997 [Abstract](#)

Designing With Logic (Rev. C) (sdya009c.htm, 9 KB)

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Live Insertion (sdya012.htm, 9 KB)

01 Oct 1996 [Abstract](#)

Input and Output Characteristics of Digital Integrated Circuits (sdya010.htm, 9 KB)

01 Oct 1996 [Abstract](#)

SN54/74HCT CMOS Logic Family Applications and Restrictions (scla011.htm, 9 KB)

01 May 1996 [Abstract](#)

Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (scla008.htm, 9 KB)

01 Apr 1996 [Abstract](#)

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LOGIC Pocket Data Book (scyd013.pdf, 4835 KB)

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