

## PUSH-PULL FOUR CHANNEL/DUAL H-BRIDGE DRIVER

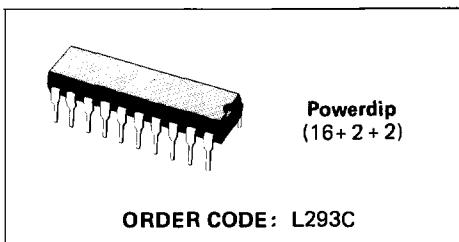
PRELIMINARY DATA

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (NON REPETITIVE) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5V (HIGH NOISE IMMUNITY)
- SEPARATE HIGH VOLTAGE POWER SUPPLY (UP TO 44V)

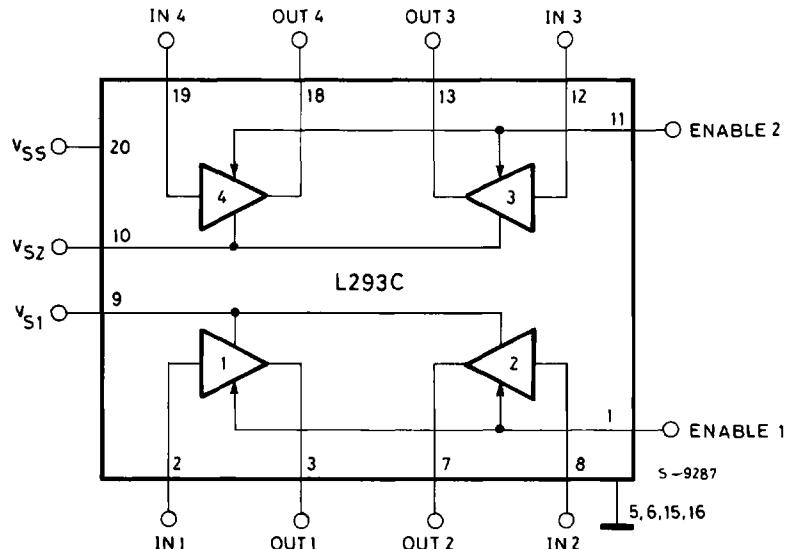
The L293C is a monolithic high voltage, high current integrated circuit four channel driver in a 20 pin DIP. It is designed to accept standard TTL or DTL input logic levels and drive inductive loads (such as relays, solenoids, DC and stepping motors) and switching power transistors.

The device may easily be used as a dual H-bridge driver: separate chip enable and high voltage power supply pins are provided for each H-bridge. In addition, a separate power supply is provided for the logic section of the device. This device is suitable for use in switching applications at frequencies up to 5 kHz.

The L293C is assembled in a 20 lead plastic package which has 4 center pins connected together and used for heatsinking.

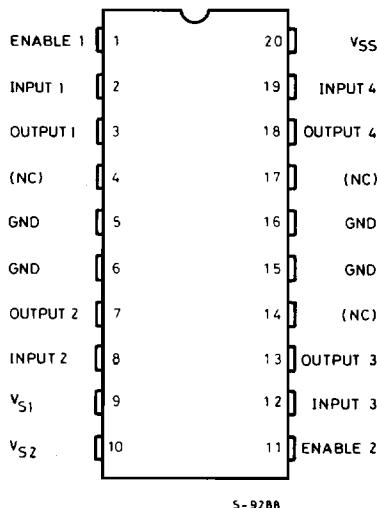


### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

$V_s$	Supply voltage	50	V
$V_{ss}$	Logic supply voltage	7	V
$V_i$	Input voltage	7	V
$V_{EN}$	Enable voltage	7	V
$I_{out}$	Peak output current (non-repetitive $t = 5\text{ms}$ )	1.2	A
$P_{tot}$	Total power dissipation at $T_{\text{ground-plns}} = 80^\circ\text{C}$	5	W
$T_{stg}, T_j$	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

CONNECTION DIAGRAM  
(Top view)

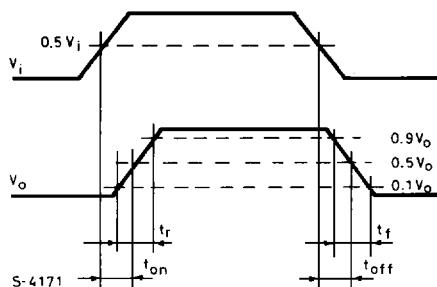
## TRUTH TABLE

INPUT	ENABLE	OUTPUT
H	H	H
L	H	L
X	L	Z

Z = High output impedance

X = Don't care

## SWITCHING TIMES



## THERMAL DATA

$R_{th\ j\text{-case}}$	Thermal resistance junction-case	max	14	$^\circ\text{C/W}$
$R_{th\ j\text{-amb}}$	Thermal resistance junction-ambient	max	80	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS** (For each channel,  $V_S = 24V$ ,  $V_{SS} = 5V$ ,  $T_{amb} = 25^\circ C$ , unless otherwise specified)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_S$ Supply voltage (pin 9, 10)		$V_{SS}$		44	V
$V_{SS}$ Logic supply voltage (pin 20)		4.5		7	V
$I_S$ Total quiescent supply current (pin 9, 10)	$V_I = L; I_o = 0; V_{EN} = H$		2	6	mA
	$V_I = H; I_o = 0; V_{EN} = H$		16	24	
	$V_{EN} = L$			4	
$I_{SS}$ Total quiescent logic supply current (pin 20)	$V_I = L; I_o = 0; V_{EN} = H$		44	60	mA
	$V_I = H; I_o = 0; V_{EN} = H$		16	22	
	$V_{EN} = L$		16	24	
$V_{IL}$ Input low voltage (pin 2, 8, 12, 19)		-0.3		1.5	V
$V_{IH}$ Input high voltage (pin 2, 8, 12, 19)		2.3		$V_{SS}$	V
$I_{IL}$ Low voltage input current (pin 2, 8, 12, 19)	$V_I = 1.5V$			-10	$\mu A$
$I_{IH}$ High voltage input current (pin 2, 8, 12, 19)	$2.3V \leq V_I \leq V_{SS} - 0.6V$		30	100	$\mu A$
$V_{ENL}$ Enable low voltage (pin 1, 11)		-0.3		1.5	V
$V_{ENH}$ Enable high voltage (pin 1, 11)		2.3		$V_{SS}$	V
$I_{ENL}$ Low voltage enable current (pin 1, 11)	$V_{ENL} = 1.5V$		-30	-100	$\mu A$
$I_{ENH}$ High voltage enable current (pin 1, 11)	$2.3V \leq V_{ENH} \leq V_{SS} - 0.6$			$\pm 10$	$\mu A$
$V_{CE(sat)H}$ Source output saturation voltage (pins 3, 7, 13, 18)	$I_o = -0.6A$		1.4	1.8	V
$V_{CE(sat)L}$ Sink output saturation voltage (pins 3, 7, 13, 18)	$I_o = +0.6A$		1.2	1.8	V
$t_r$ Rise time (*)	0.1 to 0.9 $V_o$		250		ns
$t_f$ Fall time (*)	0.9 to 0.1 $V_o$		250		ns
$t_{on}$ Turn-on delay (*)	0.5 $V_I$ to 0.5 $V_o$		750		ns
$t_{off}$ Turn-off delay (*)	0.5 $V_I$ to 0.5 $V_o$		200		ns

(\*) See switching times diagram