

CD4001B, CD4002B, CD4025B Types

CMOS NOR Gates

High-Voltage Types (20-Volt Rating)

Quad 2 Input – CD4001B

Dual 4 Input – CD4002B

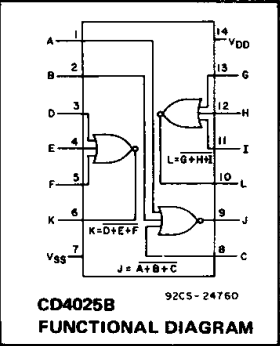
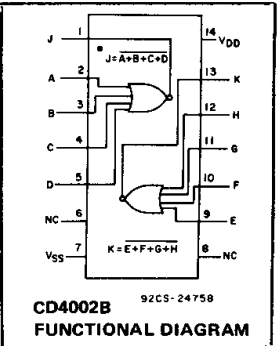
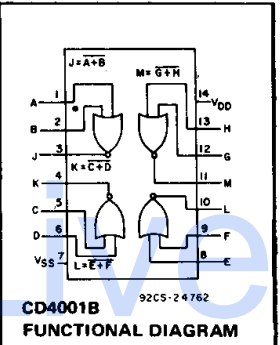
Triple 3 Input – CD4025B

■ CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

The CD4001B, CD4002B, and CD4025B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).

Features:

- Propagation delay time = 60 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Buffered inputs and outputs
- Standardized symmetrical output characteristics
- 100% tested for maximum quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"



STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	0,25	0,25	7,5	7,5	-	0,01	0,25	μ A
	-	0,10	10	0,5	0,5	15	15	-	0,01	0,5	
	-	0,15	15	1	1	30	30	-	0,01	1	
	-	0,20	20	5	5	150	150	-	0,02	5	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage, V _{IL} Max.	0,5,4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5,13,5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0,5	-	5	3,5				3,5	-	-	V
	1	-	10	7				7	-	-	
	1,5	-	15	11				11	-	-	
Input Current I _{IN} Max.		0,18	18	$\pm 0,1$	$\pm 0,1$	± 1	± 1	-	$\pm 10^{-5}$	$\pm 0,1$	μ A

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4001B, CD4002B, CD4025B Types

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to V_{DD} + 0.5V

DC INPUT CURRENT, ANY ONE INPUT

..... ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A)

..... -55°C to $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg})

..... -65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max $+265^\circ\text{C}$

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200k\Omega$

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS	
		V_{DD} VOLTS	TYP.		MAX.
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{iN}	Any Input	5	7.5	pF	

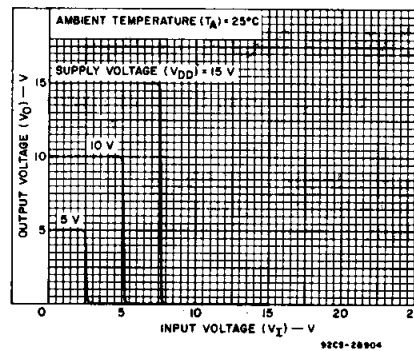


Fig. 1 - Typical voltage transfer characteristics.

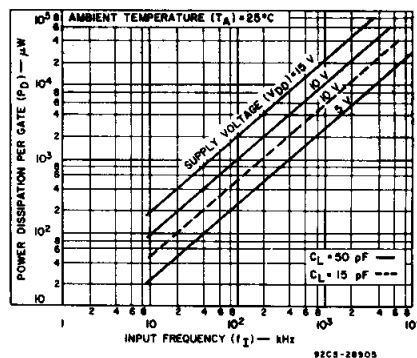


Fig. 2 - Typical power dissipation vs. frequency.

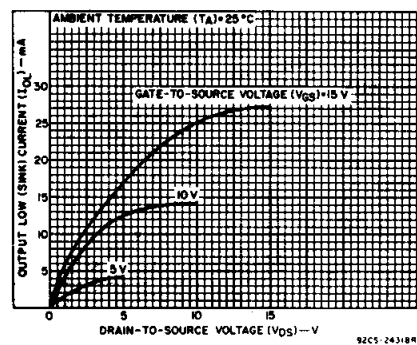


Fig. 3 - Typical output low (sink) current characteristics.

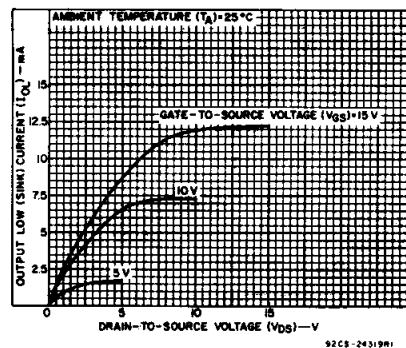


Fig. 4 - Minimum output low (sink) current characteristics.

CD4001B, CD4002B, CD4025B Types

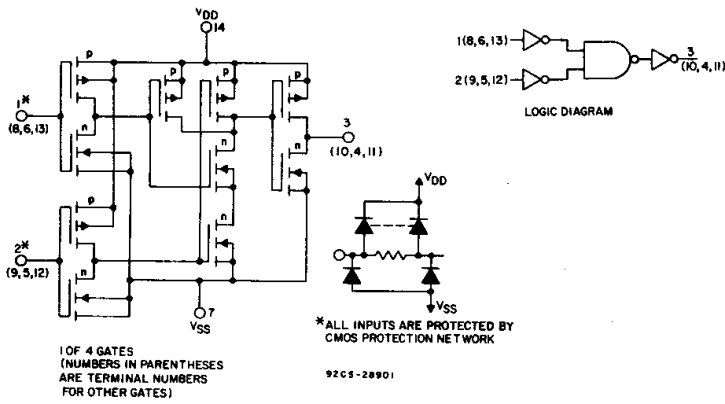


Fig.5 - Schematic and logic diagrams for CD4001B.

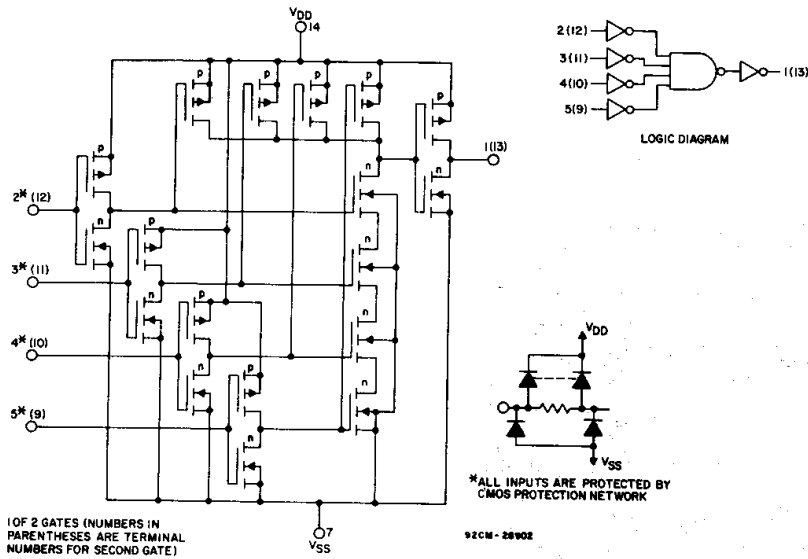


Fig.6 - Schematic and logic diagrams for CD4002B.

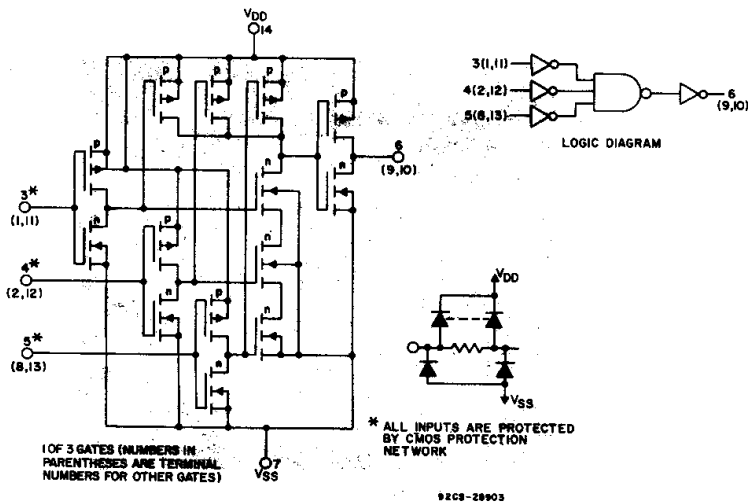


Fig.7 - Schematic and logic diagrams for CD4025B.

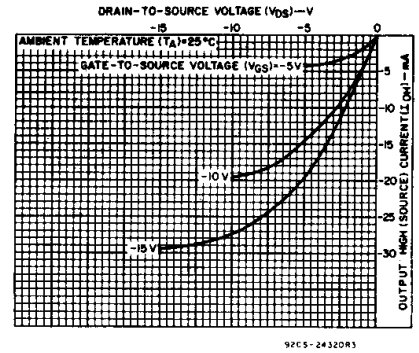


Fig.8 - Typical output high (source) current characteristics.

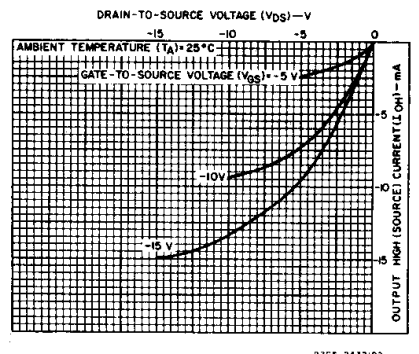


Fig.9 - Minimum output high (source) current characteristics.

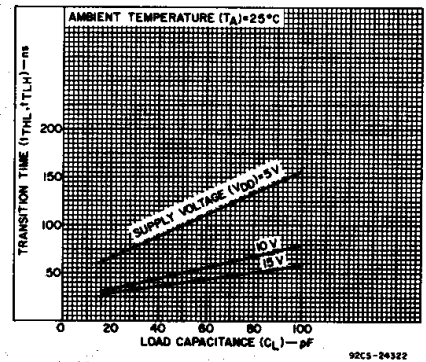


Fig.10 - Typical transition time vs. load capacitance.

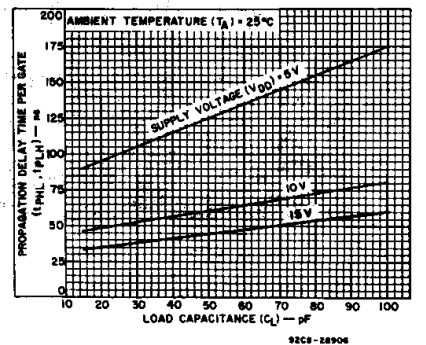


Fig.11 - Typical propagation delay time vs. load capacitance.

COMMERCIAL CMOS HIGH VOLTAGE ICs

CD4001B, CD4002B, CD4025B Types

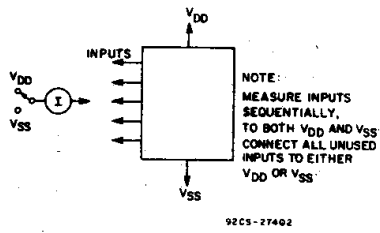


Fig. 13 - Input leakage current test circuit.

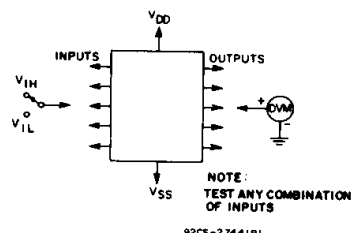


Fig. 14 - Input-voltage test circuit.

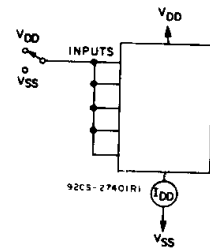
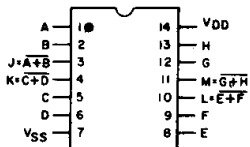
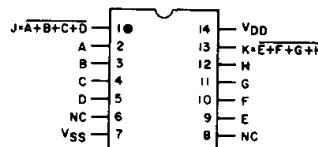


Fig. 15 - Quiescent-device current test circuit.

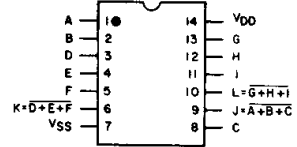
TERMINAL ASSIGNMENTS (TOP VIEW)



NC = NO CONNECTION
CD4001B

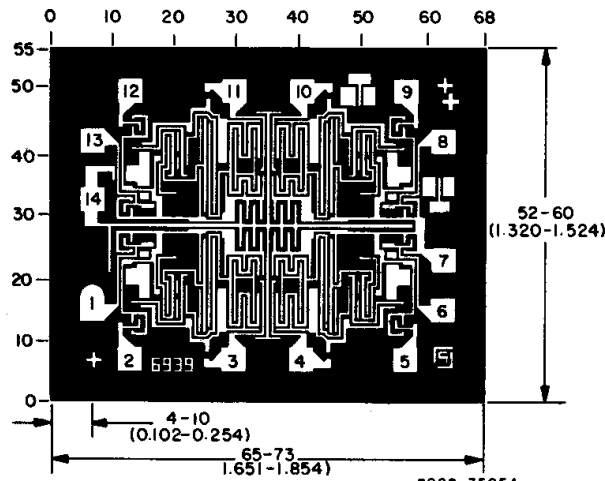


NC = NO CONNECTION
CD4002B

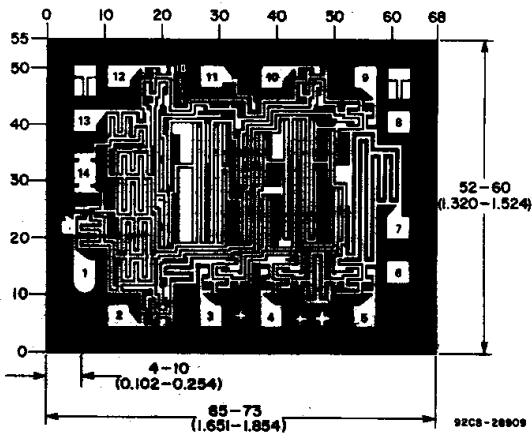


NC = NO CONNECTION
CD4025B

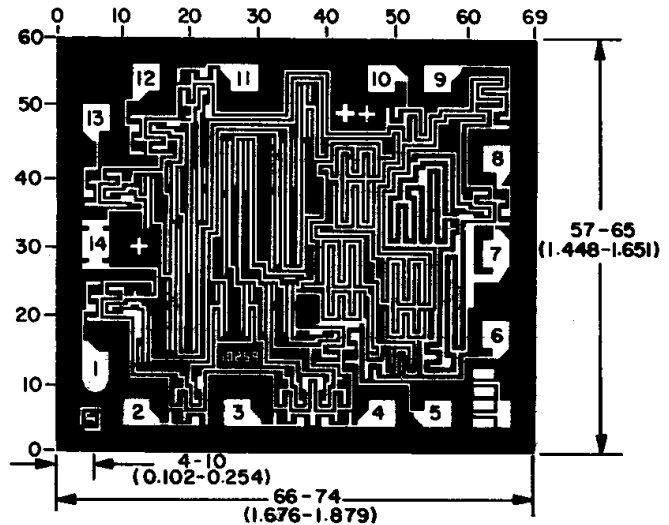
Chip Dimensions and Pad Layouts



CD4001B



CD4002B



CD4025B

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[APPLICATION NOTES](#) | [USER GUIDES](#) | [MORE LITERATURE](#)

PRODUCT SUPPORT: [TRAINING](#)

CD4002B, CMOS Dual 4-Input NOR Gate

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD4002B
Voltage Nodes (V)	5, 10, 15

FEATURES

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- Propagation delay time = 60 ns (typ.) at $C_L = 50$ pF, $V_{DD} = 10$ V
- Buffered inputs and outputs
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

DESCRIPTION

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CD4001B, CD4002B, and CD4025B NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of CMOS gates. All inputs and outputs are buffered.

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TECHNICAL DOCUMENTS

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To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: [cd4002b.pdf](#) (202 KB, Rev.A) (Updated: 03/14/2002)

APPLICATION NOTES

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View Application Notes for [Digital Logic](#)

- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Understanding Buffered and Unbuffered CD4xxxB Series Device Characteristics](#) (SCHA004 - Updated: 12/03/2001)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)

- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)
- [Signal Switch Data Book](#) (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	DSCC NUMBER	PRODUCT CONTENT	SAMPLES
CD4002BE	PDIP (N)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4002BNSR	SOP (NS)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples
CD4002BPWR	TSSOP (PW)	14	-55 TO 125	ACTIVE		View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY
7704403CA	ACTIVE	CDIP (J) 14	-55 TO 125		View Contents	1KU 2.70	1
CD4002BE	ACTIVE	PDIP (N) 14	-55 TO 125		View Contents	1KU 0.11	25
CD4002BF	ACTIVE	CDIP (J) 14	-55 TO 125		View Contents	1KU 2.30	1
CD4002BF3A	ACTIVE	CDIP (J) 14	-55 TO 125	7704403CA	View Contents	1KU 2.70	1
CD4002BM	ACTIVE	SOIC (D) 14	-55 TO 125		View Contents	1KU 0.11	50
CD4002BM96	ACTIVE	SOIC (D) 14	-55 TO 125		View Contents	1KU 0.11	2500

TI INVENTORY STATUS

As Of 08:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY DATE	LEAD TIME
345*	> 10k 20 May	8 WKS
0*	1000 21 Apr	4 WKS
	> 10k 13 May	
1933*	> 10k 20 May	8 WKS
0*	38 16 Apr	8 WKS
	> 10k 20 May	
0*	> 10k 12 May	4 WKS
0*	> 10k 12 May	4 WKS

REPORTED DISTRIBUTOR INVENTORY

As Of 08:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
Avnet Americas	66	BUY NOW
EBV Elektronik Europe	25	BUY NOW
Avnet Americas	> 1k	BUY NOW
EBV Elektronik Europe	> 1k	BUY NOW
DigiKey Americas	> 1k	BUY NOW
Newark Electronics Americas	> 1k	BUY NOW
Insight Americas	884	BUY NOW
None Reported View Distributors		
None Reported View Distributors		
None Reported View Distributors		

CD4002BNSR	ACTIVE	SOP (NS) 14	-55 TO 125		View Contents	1KU 0.21	2000	<u>0</u> *	> 10k 12 May	4 WKS	None Reported View Distributors		
CD4002BPW	ACTIVE	TSSOP (PW) 14	-55 TO 125		View Contents	1KU 0.17	90	<u>0</u> *	> 10k 08 May	4 WKS	DigiKey Americas	> 1k	BUY NOW
CD4002BPWR	ACTIVE	TSSOP (PW) 14	-55 TO 125		View Contents	1KU 0.07	2000	<u>0</u> *	4000 16 Apr	4 WKS	Avnet Americas	450	BUY NOW
									1537 21 Apr		DigiKey Americas	> 1k	BUY NOW
									> 10k 08 May				

Table Data Updated on: 4/17/2003