# 11.3 Gbps Active Back-Termination, Differential Laser Diode Driver

Data Sheet

# ADN2526

## FEATURES

**3.3 V operation**
**Up to 11.3 Gbps operation**
**Typical 24 ps rise/fall times**
**Full back-termination of output transmission lines**
**Drives TOSAs with resistances ranging from 5 Ω to 50 Ω**
**Bias current range: 10 mA to 100 mA**
**Differential modulation current range: 10 mA to 80 mA**
**Voltage input control for bias and modulation currents**
**Data inputs sensitivity: 150 mV p-p diff**
**Automatic laser shutdown (ALS)**
**Cross point adjustment (CPA)**
**XFP-compliant bias current monitor**
**SFP+ MSA compliant**
**Optical evaluation board available**
**Compact 3 mm × 3 mm LFCSP**

## APPLICATIONS

**SONET OC-192 and SDH STM-64 optical transceivers**
**10 Gb Fibre Channel transceivers**
**10 Gb Ethernet optical transceivers**
**SFP+/XFP/X2/XENPAK/XPAK/MSA 300 optical modules**

## GENERAL DESCRIPTION

The ADN2526 laser diode driver is designed for direct modulation of packaged laser diodes that have a differential resistance ranging from 5 Ω to 50 Ω. The active back-termination in the ADN2526 absorbs signal reflections from the TOSA end of the output transmission lines, enabling excellent optical eye quality to be achieved even when the TOSA end of the output transmission lines is significantly misterminated. ADN2526 is an SFP+ MSA-compliant device, and its small package and enhanced ESD protection provide the optimum solution for compact modules where laser diodes are packaged in low pin-count optical subassemblies.

The modulation and bias currents are programmable via the MSET and BSET control pins. By driving these pins with control voltages, the user has the flexibility to implement various average optical power and extinction ratio control schemes, including closed-loop or look-up table control. The automatic laser shutdown (ALS) feature allows the user to turn on/off the bias and modulation currents by driving the ALS pin with a LVTTL logic source.

The product is available in a space-saving 3 mm × 3 mm LFCSP specified from −40°C to +85°C.



## FUNCTIONAL BLOCK DIAGRAM

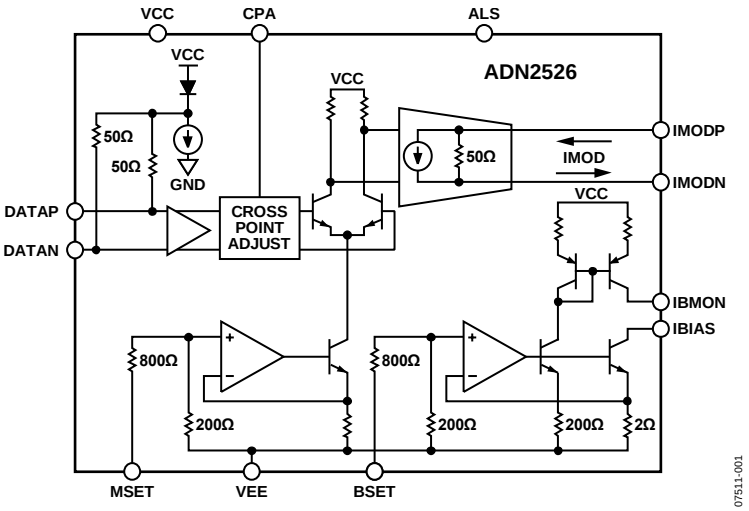


*Figure 1.*


Document Feedback


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# TABLE OF CONTENTS



## REVISION HISTORY

**10/13—Rev. A to Rev. B**

Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

**8/09—Rev. 0 to Rev. A**

Changes to $\theta_{J\text{-}PAD}$ Maximum Value (Table 2) ... 4
Changes to Figure 5 and Figure 6 ... 8

**1/09—Revision 0: Initial Version**

# SPECIFICATIONS

VCC = $VCC_{MIN}$ to $VCC_{MAX}$, $T_A$ = −40°C to +85°C, 50 Ω differential load resistance, unless otherwise noted. Typical values are specified at $T_A$ = 25°C, IMOD[1] = 40 mA, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| BIAS CURRENT (IBIAS) | | | | | |
| Bias Current Range | 10 | | 100 | mA | |
| Bias Current While ALS Asserted | | | 300 | µA | ALS = high |
| Compliance Voltage[2] | 0.6 | | VCC | V | IBIAS = 100 mA |
| | 0.6 | | VCC | V | IBIAS = 10 mA |
| MODULATION CURRENT (IMODP, IMODN) | | | | | |
| Modulation Current Range | 10 | | 80 | mA diff | $R_{LOAD}$ = 5 Ω to 50 Ω differential |
| Modulation Current While ALS Asserted | | | 0.5 | mA diff | ALS = high |
| Rise Time (20% to 80%)[3, 4] | | 24 | 32.5 | ps | |
| Fall Time (20% to 80%)[3, 4] | | 24 | 32.5 | ps | |
| Random Jitter[3, 4] | | 0.4 | 0.9 | ps rms | |
| Deterministic Jitter[3, 5] | | 7.2 | 12 | ps p-p | Includes pulse width distortion |
| Pulse Width Distortion[3, 4] | | 2 | 5 | ps | PWD = ($\lvert T_{HIGH} - T_{LOW} \rvert$)/2 |
| Differential \|S22\| | | −10 | | dB | 5 GHz < f < 10 GHz, $Z_0$ = 50 Ω differential |
| | | −14 | | dB | f < 5 GHz, $Z_0$ = 50 Ω differential |
| Compliance Voltage[2] | VCC − 1.1 | | VCC + 1.1 | V | |
| DATA INPUTS (DATAP, DATAN) | | | | | |
| Input Data Rate | | | 11.3 | Gbps | NRZ |
| Differential Input Swing | 0.15 | | 1.6 | V p-p diff | Differential, ac-coupled |
| Differential \|S11\| | | −16.8 | | dB | f < 10 GHz, $Z_0$ = 100 Ω differential |
| Input Termination Resistance | | 100 | | Ω | Differential |
| BIAS CONTROL INPUT (BSET) | | | | | |
| BSET Voltage to IBIAS Gain | | 90 | | mA/V | |
| BSET Input Resistance | | 1000 | | Ω | |
| MODULATION CONTROL INPUT (MSET) | | | | | |
| MSET Voltage to IMOD Gain | 50 | 78 | 100 | mA/V | See Figure 29 |
| MSET Input Resistance | | 1000 | | Ω | |
| BIAS MONITOR (IBMON) | | | | | |
| IBMON to IBIAS Ratio | | 10 | | µA/mA | |
| Accuracy of IBIAS to IBMON Ratio | −5.0 | | +5.0 | % | 10 mA ≤ IBIAS < 20 mA, $R_{IBMON}$ = 1 kΩ |
| | −4.0 | | +4.0 | % | 20 mA ≤ IBIAS < 40 mA, $R_{IBMON}$ = 1 kΩ |
| | −2.5 | | +2.5 | % | 40 mA ≤ IBIAS < 70 mA, $R_{IBMON}$ = 1 kΩ |
| | −2 | | +2 | % | 70 mA ≤ IBIAS < 100 mA, $R_{IBMON}$ = 1 kΩ |
| AUTOMATIC LASER SHUTDOWN (ALS) | | | | | |
| $V_{IH}$ | 2.0 | | | V | |
| $V_{IL}$ | | | 0.8 | V | |
| $I_{IL}$ | −30 | | +30 | µA | |
| $I_{IH}$ | 0 | | 200 | µA | |
| ALS Assert Time | | | 2 | µs | Rising edge of ALS to falling edge of IBIAS and IMOD below 10% of nominal, see Figure 2 |
| ALS Negate Time | | | 10 | µs | Falling edge of ALS to rise of IBIAS and IMOD above 90% of nominal, see Figure 2 |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER SUPPLY | | | | | |
| $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | |
| $I_{CC}$[6] | | 46 | 55 | mA | $V_{BSET} = V_{MSET} = 0$ V |
| $I_{SUPPLY}$[7] | | 74 | 95 | mA | $V_{BSET} = V_{MSET} = 0$ V; $I_{SUPPLY} = I_{CC}$ + IMODP + IMODN |
| CPA | | 1.88 | | V | In NC mode (refer to Table 4) |
| Cross Point | | 50 | | % | From an optical eye in NC mode |

[1] IMOD is the total modulation current sink capability for a differential driver. IMOD = $I_{MODP}$ + $I_{MODN}$, the dynamic current sank by the IMODP and IMODN pins.
[2] Refers to the voltage between the pin for which the compliance voltage is specified and VEE.
[3] The pattern used is a repetitive sequence of eight 1s followed by eight 0s at 11.3 Gbps.
[4] Measured using the high speed characterization circuit shown in Figure 3.
[5] The pattern used is K28.5 (00111110101100000101) at a 11.3 Gbps rate.
[6] Only includes current in the VCC pins.
[7] Without laser diode loaded.

## THERMAL SPECIFICATIONS

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Conditions/Comments |
|---|---|---|---|---|---|
| $\theta_{J\text{-}PAD}$ | 2.6 | 5.8 | 10.7 | °C/W | Thermal resistance from junction to bottom of exposed pad |
| $\theta_{J\text{-}TOP}$ | 65 | 72.2 | 79.4 | °C/W | Thermal resistance from junction to top of package |
| IC Junction Temperature | | | 125 | °C | |

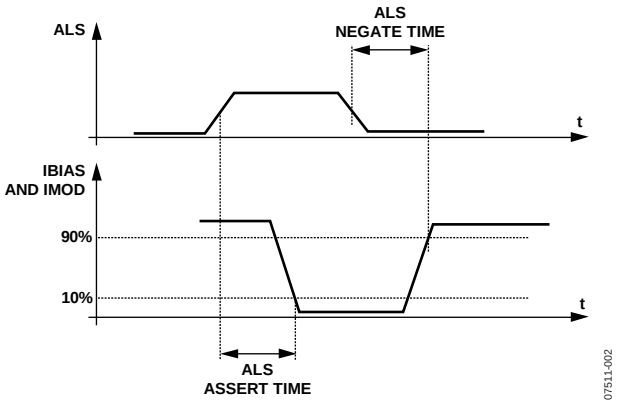


*Figure 2. ALS Timing Diagram*

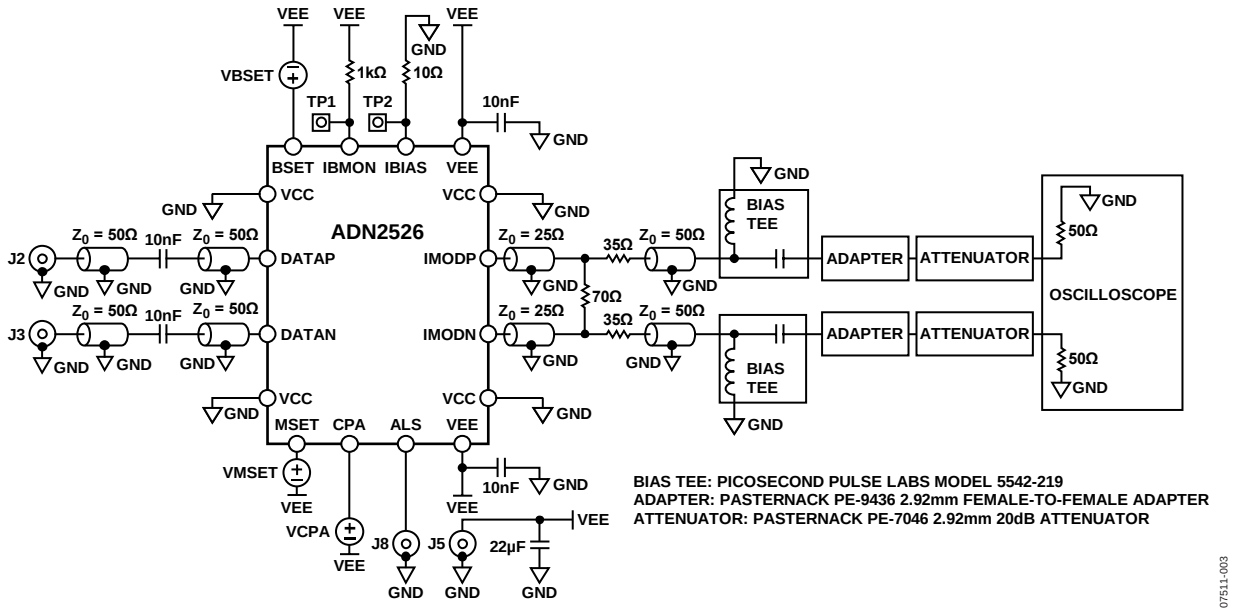


*Figure 3. High Speed Characterization Circuit*

# ABSOLUTE MAXIMUM RATINGS

VEE connected to supply ground.

**Table 3.**

| Parameter | Rating |
|---|---|
| Supply Voltage, VCC to VEE | −0.3 V to +4.2 V |
| IMODP, IMODN to VEE | 1.1 V to 4.75 V |
| DATAP, DATAN to VEE | VCC − 1.8 V to VCC − 0.4 V |
| All Other Pins | −0.3 V to VCC + 0.3 V |
| HBM ESD on IMODP, IMODN | 200 V |
| HBM ESD on All Other Pins | 1 kV |
| Junction Temperature | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Temperature (Less Than 10 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

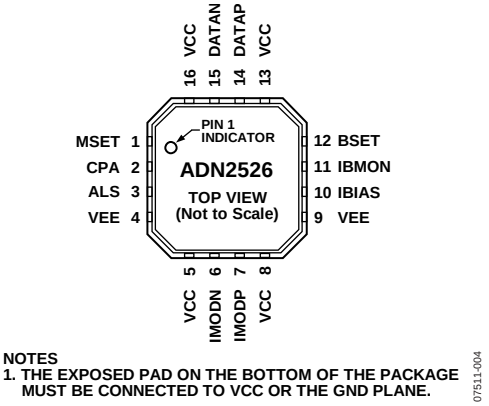


*Figure 4. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | I/O[1] | Description |
|---|---|---|---|
| 1 | MSET | AI | Modulation Current Control Input. |
| 2 | CPA | AI | Adjustable Cross Point. Defaults to not connected (NC) mode (floating). |
| 3 | ALS | DI | Automatic Laser Shutdown. |
| 4 | VEE | P | Negative Power Supply. Normally connected to system ground. |
| 5 | VCC | P | Positive Power Supply. |
| 6 | IMODN | AI | Modulation Current Sink, Negative. |
| 7 | IMODP | AI | Modulation Current Sink, Positive. |
| 8 | VCC | P | Positive Power Supply. |
| 9 | VEE | P | Negative Power Supply. Normally connected to system ground. |
| 10 | IBIAS | AI | Bias Current Sink. |
| 11 | IBMON | AO | Bias Current Monitoring Output. |
| 12 | BSET | AI | Bias Current Control Input. |
| 13 | VCC | P | Positive Power Supply. |
| 14 | DATAP | AI | Data Signal Positive Input. |
| 15 | DATAN | AI | Data Signal Negative Input. |
| 16 | VCC | P | Positive Power Supply. |
| 17 (EPAD) | Exposed Pad (EPAD) | P | The exposed pad on the bottom of the package must be connected to VCC or the GND plane. |

[1] AI = analog input, DI = digital input, P = power, AO = analog output.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, VCC = 3.3 V, unless otherwise noted.

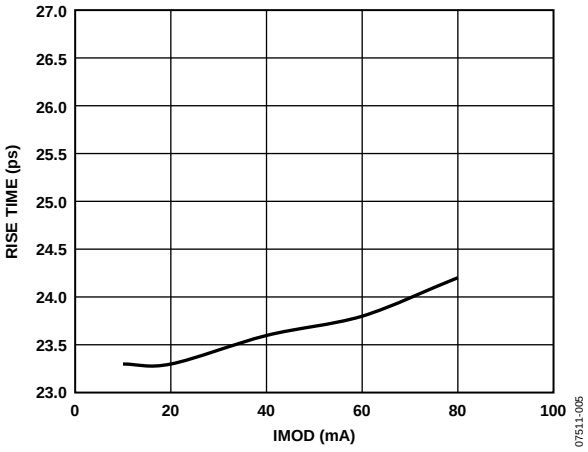


Figure 5. Rise Time vs. IMOD

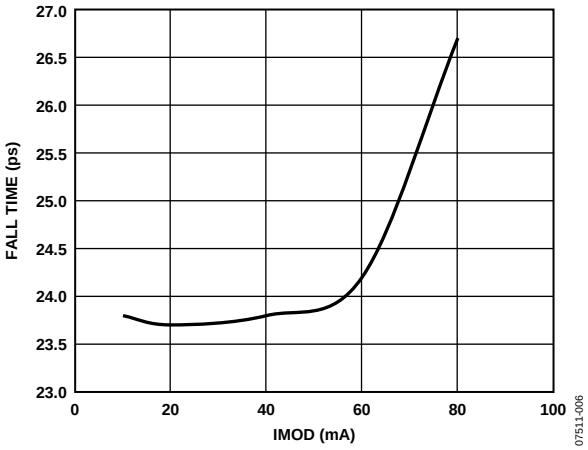


Figure 6. Fall Time vs. IMOD

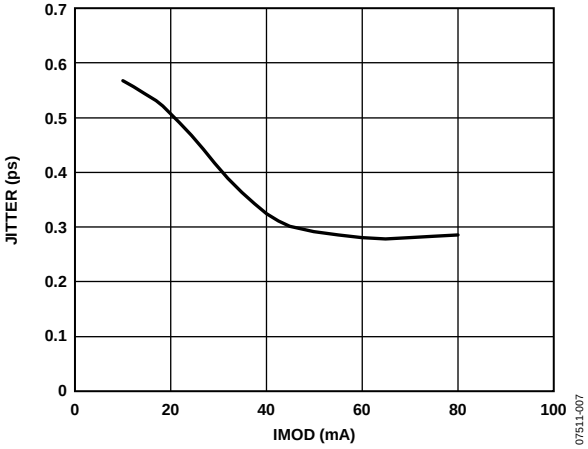


Figure 7. Random Jitter vs. IMOD

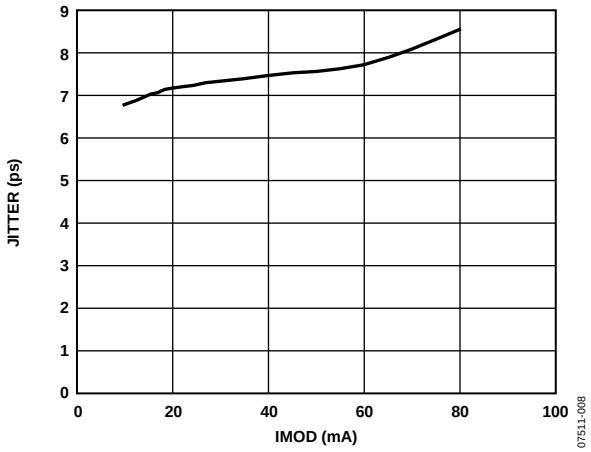


Figure 8. Deterministic Jitter vs. IMOD

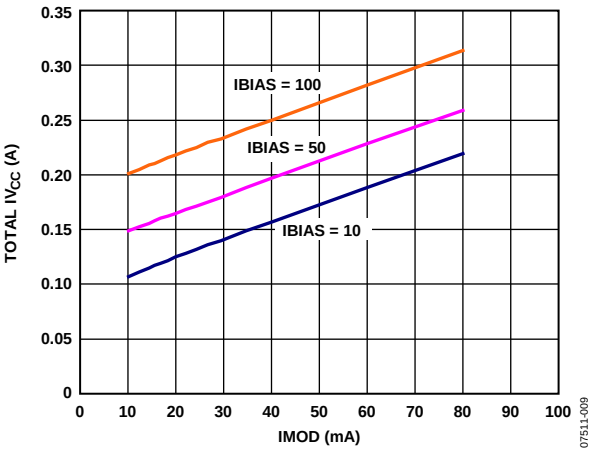


Figure 9. Total Supply Current vs. IMOD

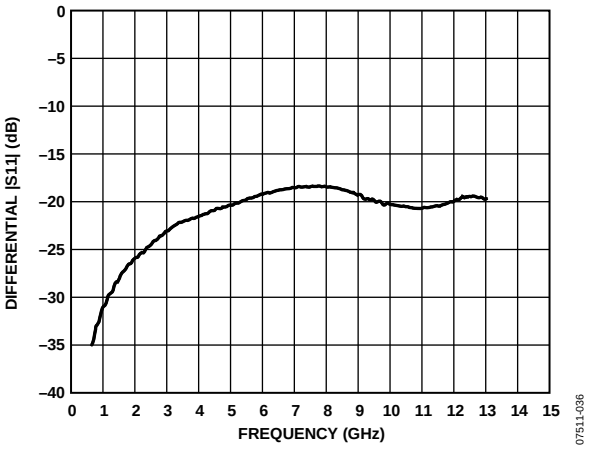


Figure 10. Differential |S11|

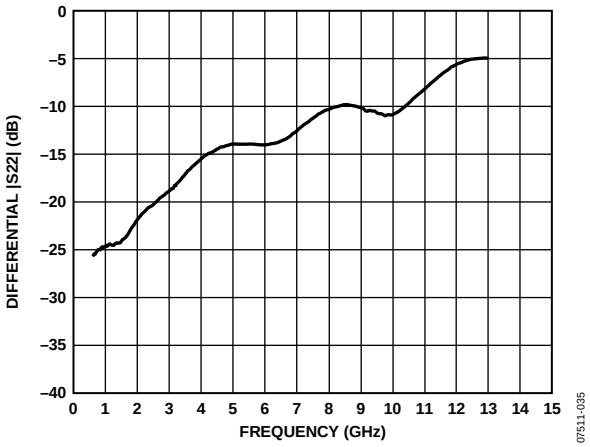


*Figure 11. Differential |S22|*

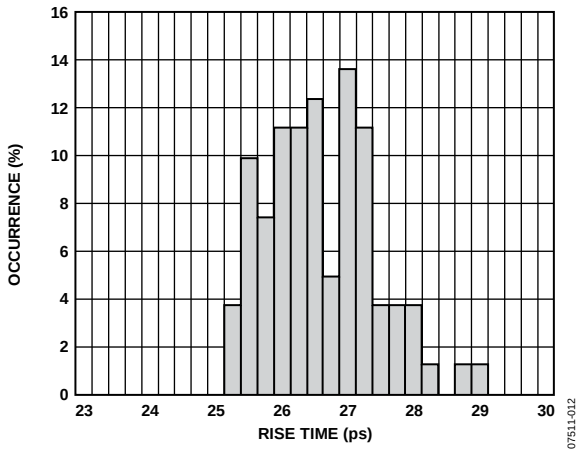


*Figure 12. Worst-Case Rise Time Distribution (VCC = 3.07 V, IBIAS = 100 mA, IMOD = 80 mA, $T_A$ = 85°C)*

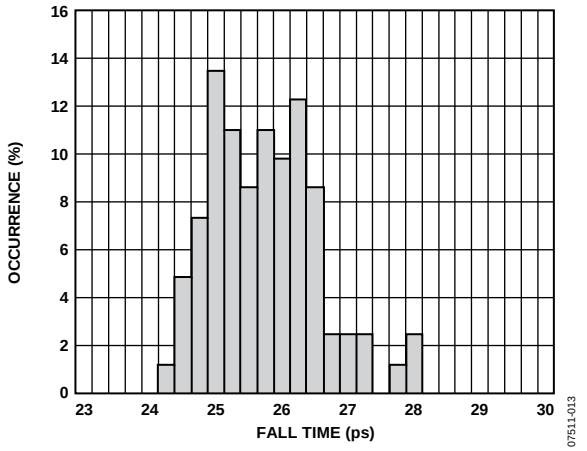


*Figure 13. Worst-Case Fall Time Distribution (VCC = 3.07 V, IBIAS = 100 mA, IMOD = 80 mA, $T_A$ = 85°C)*

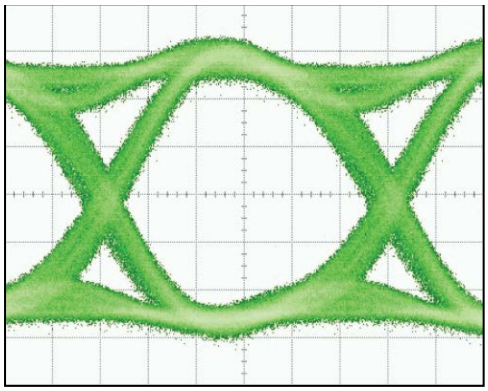


*Figure 14. Electrical Eye Diagram (11.3 Gbps, PRBS31, IMOD = 80 mA)*

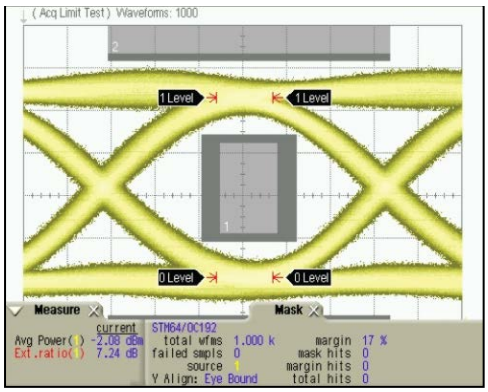


*Figure 15. Filtered SONET OC192 Optical Eye Diagram (for Reference)*

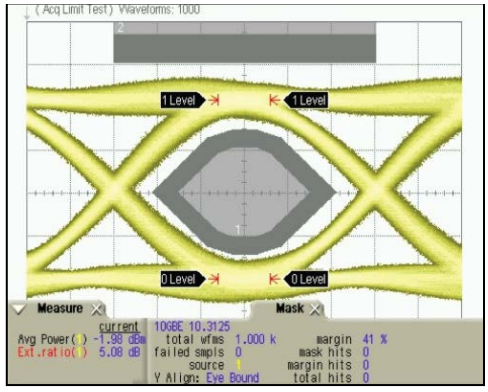


*Figure 16. Filtered 10 Gb Ethernet Optical Eye*

# THEORY OF OPERATION

As shown in Figure 1, the ADN2526 consists of an input stage and two voltage-controlled current sources for bias and modulation. The bias current, which is available at the IBIAS pin, is controlled by the voltage applied at the BSET pin and can be monitored at the IBMON pin. The differential modulation current, which is available at the IMODP and IMODN pins, is controlled by the voltage applied to the MSET pin. The output stage implements the active back-match circuitry for proper transmission line matching and power consumption reduction. The ADN2526 can drive a load having differential resistance ranging from 5 Ω to 50 Ω. The excellent back-termination in the ADN2526 absorbs the signal reflections from the TOSA end, enabling excellent optical eye quality, even though the TOSA is significantly misterminated.

## INPUT STAGE

The input stage of the ADN2526 converts the data signal applied to the DATAP and DATAN pins to a level that ensures proper operation of the high speed switch. The equivalent circuit of the input stage is shown in Figure 17.

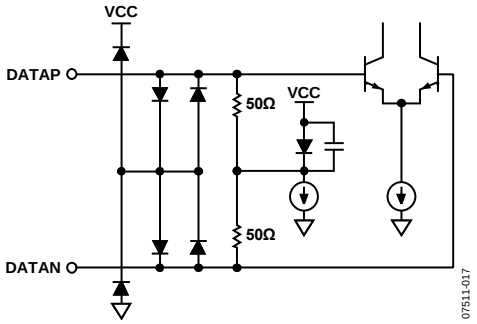


*Figure 17. Equivalent Circuit of the Input Stage*

The DATAP and DATAN pins are terminated internally with a 100 Ω differential termination resistor. This minimizes signal reflections at the input, which can otherwise lead to degradation in the output eye diagram. It is not recommended to drive the ADN2526 with single-ended data signal sources.

The ADN2526 input stage must be ac-coupled to the signal source to eliminate the need for matching between the common-mode voltages of the data signal source and the input stage of the driver (see Figure 18). The ac-coupling capacitors should have an impedance much less than 50 Ω over the required frequency range. Generally, this is achieved using 10 nF to 100 nF capacitors.

In SFP+ MSA applications, the DATAP and DATAN pins need to be connected to the SFP+ connector directly. This connection requires enhanced ESD protection to support the SFP+ module hot plug-in application.

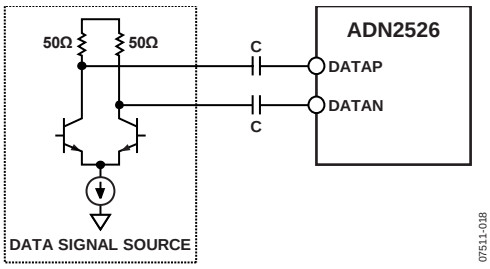


*Figure 18. AC-Coupling the Data Source to the ADN2526 Data Inputs*

## BIAS CURRENT

The bias current is generated internally using a voltage-to-current converter consisting of an internal operational amplifier and a transistor, as shown in Figure 19.

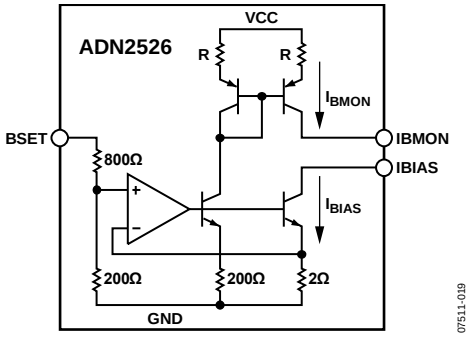


*Figure 19. Voltage-to-Current Converter Used to Generate IBIAS*

The voltage-to-current conversion factor is set at 100 mA/V by the internal resistors, and the bias current is monitored using a current mirror with a gain equal to 1/100. By connecting a 1 kΩ resistor between IBMON and VEE, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor must be used for the IBMON resistor ($R_{IBMON}$). Any error in the value of $R_{IBMON}$ that is due to tolerances or to drift in its value over temperature contributes to the overall error budget for the IBIAS monitor voltage. If the IBMON voltage is connected to an ADC for analog-to-digital conversion, $R_{IBMON}$ should be placed close to the ADC to minimize errors due to voltage drops on the ground plane.

The equivalent circuits of the BSET, IBIAS, and IBMON pins are shown in Figure 20, Figure 21, and Figure 22.

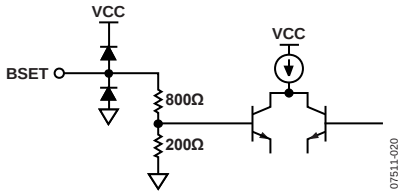


*Figure 20. Equivalent Circuit of the BSET Pin*

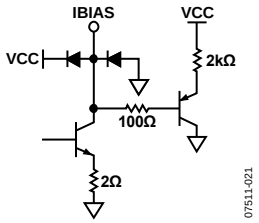


*Figure 21. Equivalent Circuit of the IBIAS Pin*

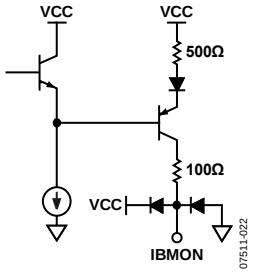


*Figure 22. Equivalent Circuit of the IBMON Pin*

The recommended configuration for BSET, IBIAS, and IBMON is shown in Figure 23.

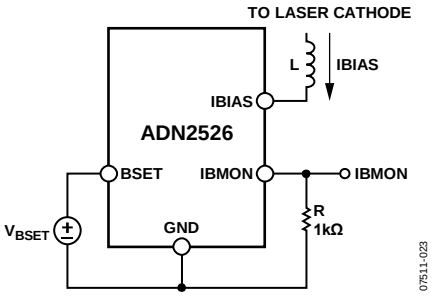


*Figure 23. Recommended Configuration for the BSET, IBIAS, and IBMON Pins*

The circuit used to drive the BSET voltage must be able to drive the 1 kΩ input resistance of the BSET pin. For proper operation of the bias current source, the voltage at the IBIAS pin must be between the compliance voltage specifications for this pin over supply, temperature, and bias current range (see Table 1). The maximum compliance voltage is specified for only two bias current levels (10 mA and 100 mA), but it can be calculated for any bias current by

$$V_{COMPLIANCE\_MAX}\,(\text{V}) = VCC\,(\text{V}) - 0.75 - 4.4 \times IBIAS \qquad (1)$$

See the Applications Information section for examples of headroom calculations.

The function of the inductor, L, is to isolate the capacitance of the IBIAS output from the high frequency signal path. For recommended components, see Table 7.

## AUTOMATIC LASER SHUTDOWN (ALS)

The ALS pin is a digital input that enables/disables both the bias and modulation currents, depending on the logic state applied, as shown in Table 5.

**Table 5. ALS Functions**

| ALS Logic State | IBIAS and IMOD |
|---|---|
| High | Disabled |
| Low | Enabled |
| Floating | Enabled |

The ALS pin is compatible with 3.3 V CMOS and LVTTL logic levels. Its equivalent circuit is shown in Figure 24.

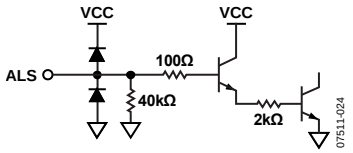


*Figure 24. Equivalent Circuit of the ALS Pin*

## MODULATION CURRENT

The modulation current can be controlled by applying a dc voltage to the MSET pin. This voltage is converted into a dc current by using a voltage-to-current converter using an operational amplifier and a bipolar transistor, as shown in Figure 25.

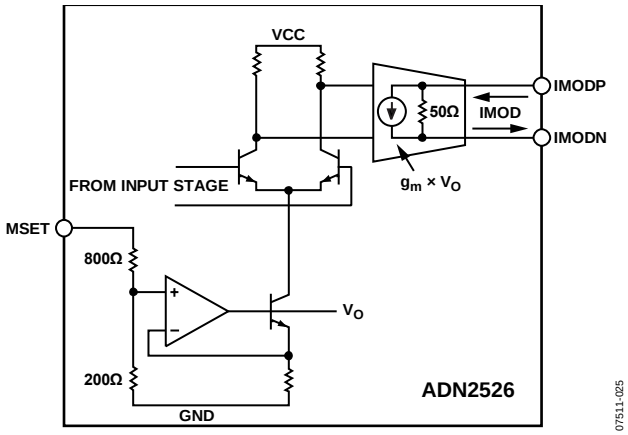


*Figure 25. Generation of Modulation Current on the ADN2526*

This dc current is switched by the data signal applied to the input stage (DATAP and DATAN pins) and amplified by the output stage to generate the differential modulation current at the IMODP and IMODN pins.

The output stage also generates the active back-termination, which provides proper transmission line termination. Active back-termination uses feedback around an active circuit to synthesize a broadband termination resistance. This provides excellent transmission line termination, while dissipating less power than a traditional resistor passive back-termination. A small portion of the modulation current flows in the virtual 50 Ω active back-termination resistor. All of the preset IMOD modulation current, the range specified in Table 1, flows into the external load. The equivalent circuits for MSET, IMODP, and IMODN are shown in Figure 26 and Figure 27. The two 25 Ω resistors in Figure 27 are not actual resistors. They represent the active back-termination resistance.

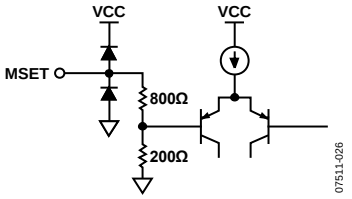


*Figure 26. Equivalent Circuit of the MSET Pin*

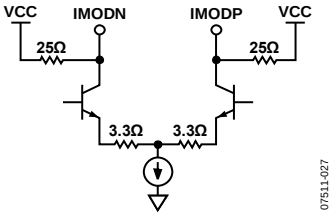


*Figure 27. Equivalent IMODP and IMODN Pins, As Seen From Laser Side*

The recommended configuration of the MSET, IMODP, and IMODN pins is shown in Figure 28. See Table 7 for the recommended components.

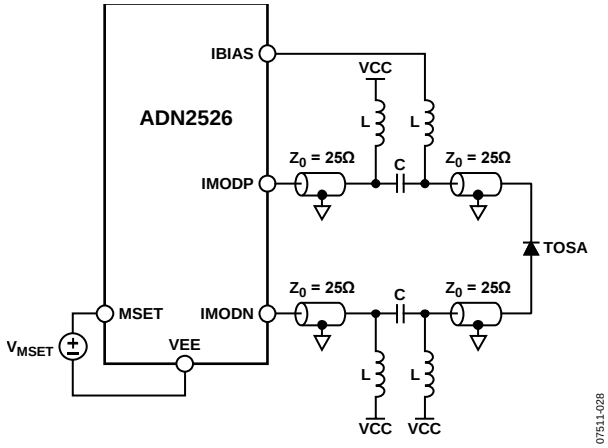


*Figure 28. Recommended Configuration for the MSET, IMODP, and IMODN Pins*

The ratio between the voltage applied to the MSET pin and the differential modulation current available at the IMODP and IMODN pins is a function of the load resistance value, as shown in Figure 29.

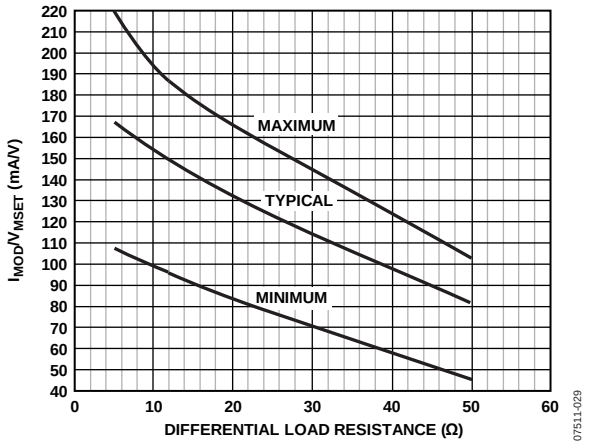


*Figure 29. MSET Voltage-to-Modulation Current Ratio vs. Differential Load Resistance*

Using the resistance of the TOSA, the user can calculate the voltage range that should be applied to the MSET pin to generate the required modulation current range (see the example in the Applications Information section).

The circuit used to drive the MSET voltage must be able to drive the 1 kΩ resistance of the MSET pin. To be able to drive 80 mA modulation currents through the differential load, the output stage of the ADN2526 (the IMODP and IMODN pins) must be ac-coupled to the load. The voltages at these pins have a dc component equal to VCC and an ac component with single-ended, peak-to-peak amplitude of IMOD × 25 Ω. This is the case even if the load impedance is less than 50 Ω differential, because the transmission line characteristic impedance sets the peak-to-peak amplitude. For proper operation of the output stage, the voltages at the IMODP and IMODN pins must be between the compliance voltage specifications for these pins over supply, temperature, and modulation current range, as shown in Figure 30. See the Applications Information section for examples of headroom calculations.

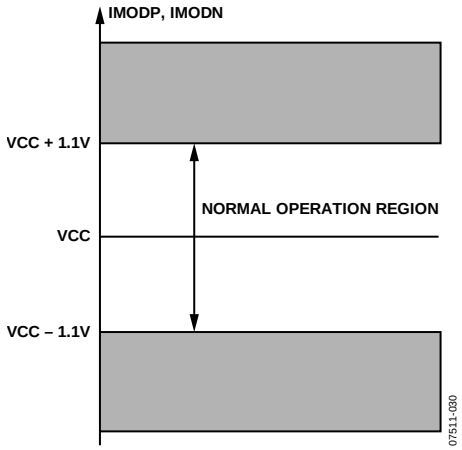


*Figure 30. Allowable Range for the Voltage at IMODP and IMODN*

## LOAD MISTERMINATION

Due to its excellent S22 performance, the ADN2526 can drive differential loads that range from 5 Ω to 50 Ω. In practice, many TOSAs have differential resistance less than 50 Ω. In this case, with 50 Ω differential transmission lines connecting the ADN2526 to the load, the load end of the transmission lines are misterminated. This mistermination leads to signal reflections back to the driver. The excellent back-termination in the ADN2526 absorbs these reflections, preventing their reflection back to the load. This enables excellent optical eye quality to be achieved, even when the load end of the transmission lines is significantly misterminated. The connection between the load and the ADN2526 must be made with 50 Ω differential (25 Ω single-ended) transmission lines so that the driver end of the transmission lines is properly terminated.

## CROSSPOINT ADJUSTMENT

The optical eye cross point is adjustable between 35% and 65% using the cross point adjust (CPA) control input. The equivalent circuit for the CPA pin is shown in Figure 31. In a default CPA setting, leave CPA unconnected (maintain pin-to-pin compatibility with the ADN2525). The internal bias circuit presents about 1.9 V at the CPA pin and the eye cross point is set to 50%. To set the cross point at various points, apply an external voltage to the CPA pin.

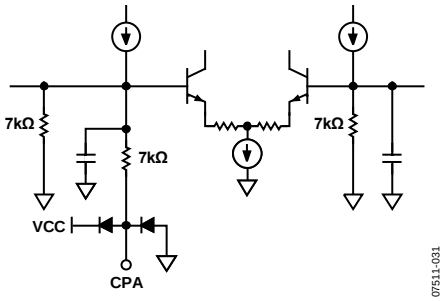


*Figure 31. Equivalent Circuit for CPA Pin*

## POWER SEQUENCE

To ensure reliable operation, the recommended power-up sequence is: the supply rail to ADN2526 first, then the BSET pin, followed by the MSET pin, and, finally, the CPA pin.

To turn off the ADN2526, the operation is reversed: shut down CPA first, then MSET, followed by BSET, and, last, the supply rail.

## POWER CONSUMPTION

The power dissipated by the ADN2526 is given by

$$P = VCC \times \left( \frac{V_{MSET}}{13.5} + I_{SUPPLY} \right) + V_{IBIAS} \times IBIAS$$

where:
*VCC* is the power supply voltage.
$V_{MSET}$ is the voltage applied to the MSET pin.
$I_{SUPPLY}$ is the sum of the currents that flow into VCC, IMODP, and IMODN, which are sank by the ADN2526 when $V_{BSET} = V_{MSET} = 0$ V, expressed in amps (see Table 1).
$V_{IBIAS}$ is the average voltage presented on the IBIAS pin.
*IBIAS* is the bias current sank by the ADN2526.

Considering $V_{BSET}$/IBIAS = 10 mV/mA as the conversion factor from $V_{BSET}$ to IBIAS, the dissipated power becomes

$$P = VCC \times \left( \frac{V_{MSET}}{13.5} + I_{SUPPLY} \right) + \frac{V_{BSET}}{10} \times V_{IBIAS}$$

To ensure long-term reliable operation, the junction temperature of the ADN2526 must not exceed 125°C, as specified in Table 2. For improved heat dissipation, the SFP+ module case can work as a heat sink, as shown in Figure 32. A compact optical module is a complex thermal environment, and calculations of device junction temperature using the package junction-to-ambient thermal resistance ($\theta_{JA}$) do not yield accurate results.

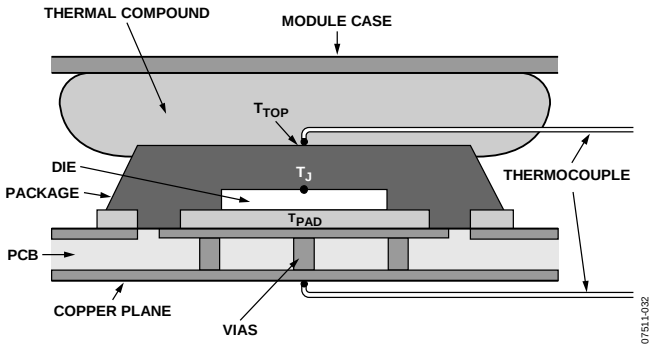


*Figure 32. Typical Optical Module Structure*

The parameters in Table 6 can be used to estimate the IC junction temperature.

**Table 6. Definitions**

| Parameter | Description | Unit |
|---|---|---|
| $T_{TOP}$ | Temperature at the top of the package | °C |
| $T_{PAD}$ | Temperature at the package exposed paddle | °C |
| $T_J$ | IC junction temperature | °C |
| P | Power dissipation | W |
| $\theta_{J-TOP}$ | Thermal resistance from the IC junction to the package top | °C/W |
| $\theta_{J-PAD}$ | Thermal resistance from the IC junction to the package exposed paddle | °C/W |

$T_{TOP}$ and $T_{PAD}$ can be determined by measuring the temperature at points inside the module, as shown in Figure 32. The thermocouples should be positioned to obtain an accurate measurement of the package top and paddle temperatures. Using the model shown in Figure 33, the junction temperature can be calculated by

$$T_J = \frac{P \times (\theta_{J-PAD} \times \theta_{J-TOP}) + T_{TOP} \times \theta_{J-PAD} + T_{PAD} \times \theta_{J-TOP}}{\theta_{J-PAD} + \theta_{J-TOP}}$$

where:
$\theta_{J-TOP}$ and $\theta_{J-PAD}$ are given in Table 2.
*P* is the power dissipated by the ADN2526.

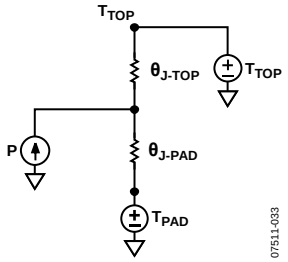


*Figure 33. Electrical Model for Thermal Calculations*

# APPLICATIONS INFORMATION

## TYPICAL APPLICATION CIRCUIT

Figure 34 shows the typical application circuit for the ADN2526. The dc voltages applied to the BSET and MSET pins control the bias and modulation currents. The bias current can be monitored as a voltage drop across the 1 kΩ resistor connected between the IBMON pin and GND. The ALS pin allows the user to turn on or turn off the bias and modulation currents, depending on the logic level applied to the pin. The data signal source must be connected to the DATAP and DATAN pins of the ADN2526 using 50 Ω transmission lines. The modulation current outputs, IMODP and IMODN, must be connected to the load (TOSA) using 50 Ω differential (25 Ω single-ended) transmission lines. It is recommended that the components shown in Table 7 be used between the ADN2526 and the TOSA for an example ac coupling circuit. For up-to-date component recommendations, contact your local Analog Devices, Inc., sales representative.

Working with a TOSA laser sample, the circuit in Figure 34 delivers optical performance shown in Figure 15 and Figure 16. For additional applications information and optical eye performance of other laser samples, contact your local Analog Devices sales representative.

## LAYOUT GUIDELINES

Due to the high frequencies at which the ADN2526 operates, care should be taken when designing the PCB layout to obtain optimum performance. Well controlled transmission line impedance must be used for the high speed signal paths. The length of the transmission lines must be kept to a minimum to reduce losses and pattern-dependent jitter. The PCB layout must be symmetrical, on both the DATAP and DATAN inputs and the IMODP and IMODN outputs, to ensure a balance between the differential signals. All VCC and VEE pins must be connected to solid copper planes by using low inductance connections. When the connections are made through vias, multiple vias should be used in parallel to reduce the parasitic inductance. Each VEE pin must be locally decoupled with high quality capacitors. If proper decoupling cannot be achieved using a single capacitor, the user can use multiple capacitors in parallel for each VEE pin. A 20 µF tantalum capacitor must be used as a general decoupling capacitor for the entire module. For guidelines on the surface-mount assembly of the ADN2526, see the Amkor Technology® Application Notes for Surface Mount Assembly of Amkor's *Micro*LeadFrame® (MLF®) Packages.

**Table 7. Recommended Components for AC-Coupling**

| Component | Value | Description |
|---|---|---|
| R1, R2 | 36 Ω | 0603 size resistor |
| R3, R4 | 200 Ω | 0603 size resistor |
| C3, C4 | 100 nF | 0603 size capacitor, Phycomp 223878615649 |
| L2, L3 | 20 nH | 0402 size inductor, Murata LQW15AN20NJ0 |
| L6, L7 | 0402 size ferrite | Murata BLM15HG102SN1 |
| L1, L4, L5, L8 | 10 µH | 0603 size inductor, Murata LQM21FN100M70L |

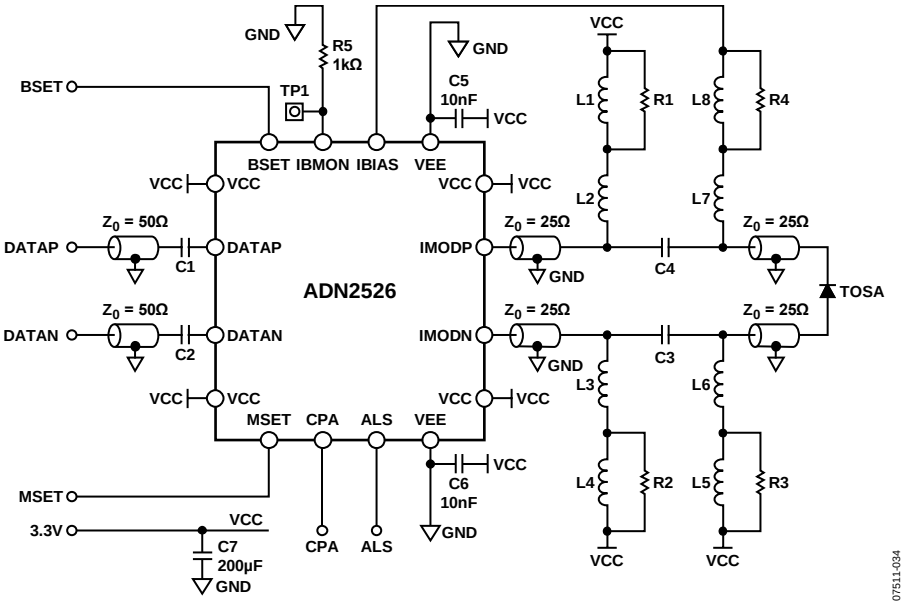


*Figure 34. Typical Application Circuit*

## DESIGN EXAMPLE

This design example covers:

- Headroom calculations for the IBIAS, IMODP, and IMODN pins.
- Calculation of the typical voltage required at the BSET and MSET pins to produce the desired bias and modulation currents.

This design example assumes that the resistance of the TOSA is 25 Ω, the forward voltage of the laser at low current is $V_F$ = 1 V, IBIAS = 40 mA, IMOD = 60 mA, and VCC = 3.3 V.

### *Headroom Calculations*

To ensure proper device operation, the voltages on the IBIAS, IMODP, and IMODN pins must meet the compliance voltage specifications in Table 1.

Considering the typical application circuit shown in Figure 34, the voltage at the IBIAS pin can be written as

$$V_{IBIAS} = VCC - V_F - (IBIAS \times R_{TOSA}) - V_{LA}$$

where:
$VCC$ is the supply voltage.
$V_F$ is the forward voltage across the laser at low current.
$R_{TOSA}$ is the resistance of the TOSA.
$V_{LA}$ is the dc voltage drop across L5, L6, L7, and L8.

For proper operation, the minimum voltage at the IBIAS pin should be greater than 0.6 V, as specified by the minimum IBIAS compliance specification in Table 1.

Assuming that the voltage drop across the 25 Ω transmission lines is negligible and that $V_{LA}$ = 0 V, $V_F$ = 1 V, and IBIAS = 40 mA

$$V_{IBIAS} = 3.3 - 1 - (0.04 \times 25) = 1.3 \text{ V}$$

$V_{IBIAS}$ = 1.3 V > 0.6 V, which satisfies the requirement.

The maximum voltage at the IBIAS pin must be less than the maximum IBIAS compliance specification as described by

$$V_{COMPLIANCE\_MAX} = VCC - 0.75 - 4.4 \times IBIAS \quad (2)$$

For this example,

$$V_{COMPLIANCE\_MAX} = VCC - 0.75 - 4.4 \times 0.04 = 2.53 \text{ V}$$

$V_{IBIAS}$ = 1.3 V < 2.53 V, which satisfies the requirement.

To calculate the headroom at the modulation current pins (IMODP and IMODN), the voltage has a dc component equal to VCC, due to the ac-coupled configuration, and a swing equal to IMOD × 25 Ω. For proper operation of the ADN2526, the voltage at each modulation output pin should be within the normal operation region shown in Figure 30.

$V_{LB}$ is the dc voltage drop across L1, L2, L3, and L4. Assuming that $V_{LB}$ = 0 V and IMOD = 60 mA, the minimum voltage at the modulation output pins is equal to

$$VCC - (IMOD \times 25)/2 = VCC - 0.75$$

$VCC - 0.75 > VCC - 1.1$ V, which satisfies the requirement.

The maximum voltage at the modulation pins is equal to

$$VCC + (IMOD \times 25)/2 = VCC + 0.75$$

$VCC + 0.75 < VCC + 1.1$ V, which satisfies the requirement.

Headroom calculations must be repeated for the minimum and maximum values of the required IBIAS and IMOD ranges to ensure proper device operation over all operating conditions.

### *BSET and MSET Pin Voltage Calculation*

To set the desired bias and modulation currents, the BSET and MSET pins of the ADN2526 must be driven with the appropriate dc voltage. The voltage range required at the BSET pin to generate the required IBIAS range can be calculated using the BSET voltage to IBIAS gain specified in Table 1. Assuming that IBIAS = 40 mA and the typical IBIAS/$V_{BSET}$ ratio of 100 mA/V, the BSET voltage is given by

$$V_{BSET} = \frac{IBIAS\,(\text{mA})}{100 \text{ mA/V}} = \frac{40}{100} = 0.4 \text{ V}$$

The BSET voltage range can be calculated using the required IBIAS range and the minimum and maximum BSET voltage to IBIAS gain values specified in Table 1.

The voltage required at the MSET pin to produce the desired modulation current can be calculated using

$$V_{MSET} = \frac{IMOD}{K}$$

where $K$ is the MSET voltage to IMOD ratio.

The value of K depends on the actual resistance of the TOSA. It can be read using the plot shown in Figure 29. For a TOSA resistance of 25 Ω, the typical value of K is equal to 120 mA/V. Assuming that IMOD = 60 mA and using the preceding equation, the MSET voltage is given by

$$V_{MSET} = \frac{IMOD\,(\text{mA})}{120 \text{ mA/V}} = \frac{60}{120} = 0.5 \text{ V}$$

The MSET voltage range can be calculated using the required IMOD range and the minimum and maximum K values. These can be obtained from the minimum and maximum curves in Figure 29.

# OUTLINE DIMENSIONS

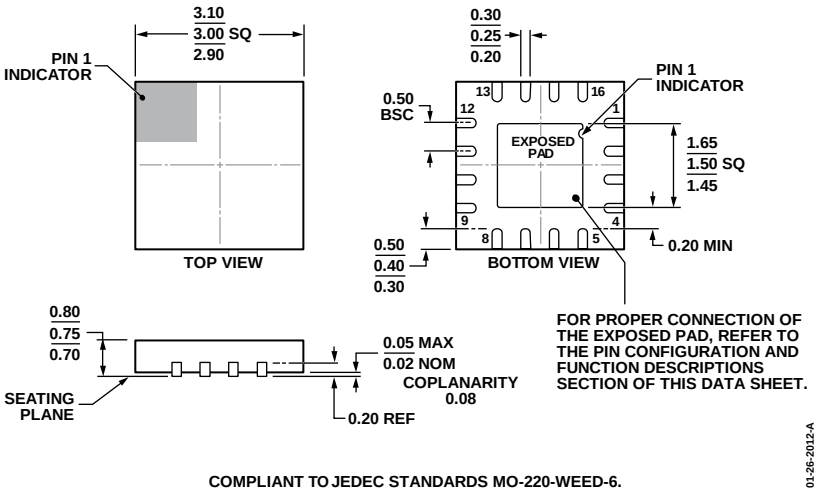


*Figure 35. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]*
*3 mm × 3 mm Body, Very Very Thin Quad*
*(CP-16-27)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADN2526ACPZ | −40°C to +85°C | 16-Lead LFCSP_WQ | CP-16-27 | F0C |
| ADN2526ACPZ-R2 | −40°C to +85°C | 16-Lead LFCSP_WQ, 7″ Tape & Reel, 250-Piece Reel | CP-16-27 | F0C |
| ADN2526ACPZ-R7 | −40°C to +85°C | 16-Lead LFCSP_WQ, 7″ Tape & Reel, 1,500-Piece Reel | CP-16-27 | F0C |

[1] Z = RoHS Compliant Part.


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