IR High Voltage IC

AUIRS1170S

Features

- Secondary side high speed SR controller
- Fly-back, Forward and Half-bridge topologies
- CCM operation with SYNC function
- 200V proprietary IC technology
- Max 500KHz switching frequency
- Anti-bounce logic and UVLO protection
- 6A peak turn off drive current
- Micropower start-up & ultra low quiescent current
- 10.7V gate drive clamp
- 60ns turn-off propagation delay
- Vcc range from 11V to 20V
- Enable function synchronized with MOSFET VDS transition
- Cycle by Cycle MOT Check Circuit prevents multiple false trigger GATE pulses
- Automotive Qualified
- Leadfree, RoHS compliant

Typical Applications

Synchronous rectification driver for:

- Automotive DC-DC converters
- Automotive SMPS
- High power industrial SMPS

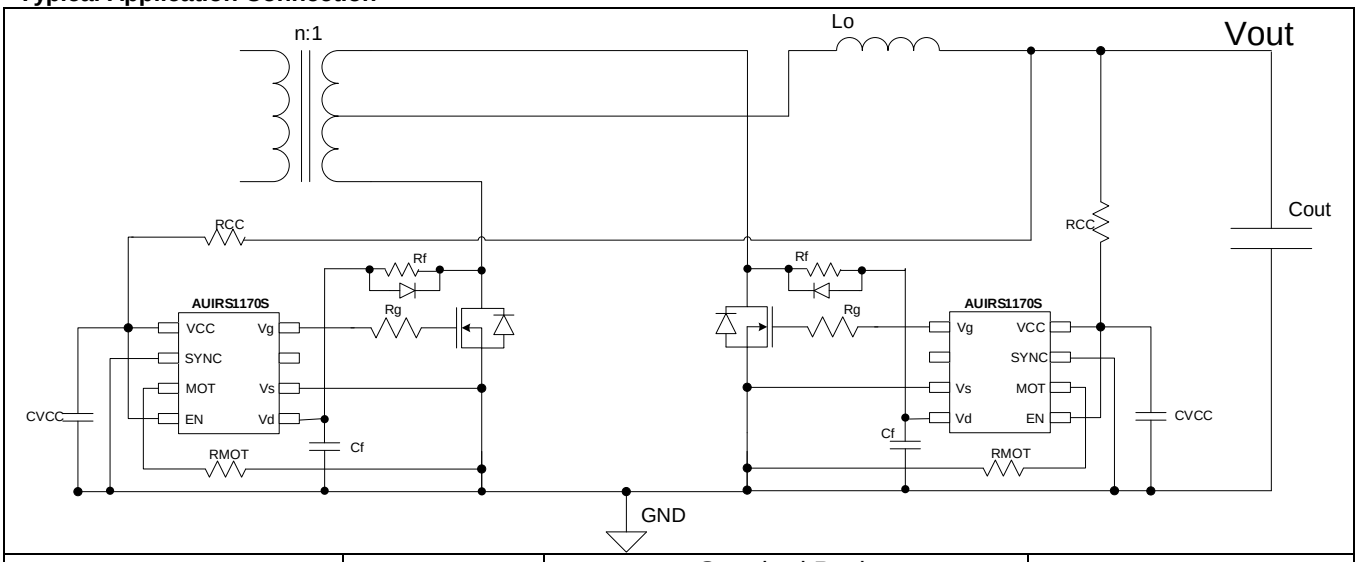
Product Summary

Topology	Flyback, Forward, Half Bridge
V_D	200V
V_{OUT}	10.7 V
I_{O+} & I_{O-} (typical)	+3/-6A
Turn on propagation Delay	90ns (typical)
Turn off propagation Delay	60ns (typical)

Package

PSOP8L

Typical Application Connection



		Standard Pack		
Base Part Number	Package Type	Form	Quantity	Orderable Part Number
AUIRS1170S	PSOP8L	T&R	2500	AUIRS1170STR

Description

AUIRS1170S is an automotive qualified smart secondary-side driver IC designed to drive N-Channel power MOSFETs used as synchronous rectifiers in isolated Resonant, Flyback and Forward converters. The IC can control one or more paralleled Nch-MOSFETs to emulate the behavior of Schottky diode rectifiers. The AUIRS1170S works in both DCM and CCM operation modes. The SYNC pin should be used in CCM mode to directly turn-off the MOSFET by a signal from secondary or primary controller. The IC is designed to use simple capacitor coupling interface with primary controller. In addition to the SYNC control, the drain to source voltage is sensed differentially to determine the polarity of the current and turn the power switch on and off in proximity of the zero current transition. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double-pulse suppression which allow reliable operation in all operating modes.

The AUIRS1170S is intended for automotive systems that must meet ASIL requirements. In safety critical applications power devices protection and their status monitoring is an important safety requirement which is currently addressed with discrete circuitry. The AUIRS1170S includes specific features that simplify and complement a proper system design, allowing users to achieve up to ASIL-D system rating.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to Vs lead. Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the “Recommended

Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is -40°C≤TA≤125°C, unless otherwise specified.

Symbol	Definition	Min.	Max.	Units	Remarks
V_{cc}	Supply voltage	-0.3	20	V	
V_{EN}	Enable voltage	-0.3	20		
V_{SYNC}	SYNC Voltage	-0.3	20		
V_{GATE}	Gate voltage	-0.3	20		Vcc=20V, Gate off
V_D	Continuous Drain Sense Voltage	-1	200		
V_D	Pulse Drain Sense Voltage	-5	200		
I_{SYNC}	SYNC Current	-10	10	mA	
Rth_{JC}	Thermal resistance, junction to case	—	4	°C/W	
P_D	Package power dissipation		970	mW	Ta=25C
f_{SW}	Switching frequency		500	kHz	
T_J	Operating Junction temperature	-40	150	°C	SOIC-8
T_S	Storage temperature	-55	150		SOIC-8, T_{AMB}=25C
T_L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltage referenced to Vs.

Symbol	Definition	Min.	Max.	Units
V_{cc}	Supply voltage	11	18	V
V_D	Drain Sense Voltage	-3	200	
T_J	Junction temperature	-25	125	°C
f_{SW}	Switching frequency	---	500	kHz
R_{MOT}	MOT pin resistor value	5	75	kΩ

Static Electrical Characteristics

VCC=15V and -40°C≤TA≤125°C unless otherwise specified. The output voltage and current (Vo and Io) parameters are referenced to Vs (pin6).

SUPPLY SECTION

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	Vcc Turn On Threshold	9.4	10.2	11.1	V	
V_{CCUV-}	Vcc Turn Off Threshold (UVLO)	8.2	9.3	10.1		
V_{CCHYST}	Vcc Turn On/Off Hysteresis		1.7			
I_{CC}	Operating Current		45	80	mA	C_{LOAD}=10nF,f_{SW}=400kHz
I_{QCC}	Quiescent Current		1.8	2.4		
$I_{CC\ START}$	Start-up Current		100	200	µA	V_{CC}=V_{CCUV+} -0.1V
I_{SLEEP}	Sleep Current		150	200		V_{EN}=0V,
V_{ENHI}	Enable Voltage High	2.15	2.70	3.4	V	
V_{ENLO}	Enable Voltage Low	1.2	1.6	2.2		
R_{EN}	Enable Pull-up Resistance		1.5		MΩ	

COMPARATOR SECTION

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{TH1}	Turn-off Threshold	-11	-5	0	mV	Vcc = 18V
V_{TH2}	Turn-on Threshold	-150	-100	-60		Vcc = 18V
V_{HYST}	Hysteresis		90			Vcc = 18V
I_{IBIAS1}	Input Bias Current		45	60	µA	V_D= - 20mV Vcc = 18V Ho = low

ONE SHOT SECTION

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{BLANK}	Blanking pulse duration	7.8	17	25	µs	
V_{TH3}	Reset Threshold		3.9		V	Vcc=15V
V_{HYST3}	Hysteresis *		20		mV	
T_B	V_{TH3} reset propagation delay**		400		ns	

* Guaranteed by design
** See MOT Protection Mode section

MINIMUM ON TIME SECTION

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
T_{ONmin}	Minimum On Time*	100	210	390	ns	R_{MOT} =5kΩ
		1.7	2.8	3.9	µs	R_{MOT} =75kΩ

*See Pin Description section for R_{MOT} calculation formula

Electrical Characteristics

VCC=15V and -40°C≤TA≤125°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to Vs (pin6).

SYNC and ENABLE SECTION

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{SYHI}	SYNC Voltage High (disable)	2	2.4	3	V	
V_{SYLO}	SYNC Voltage Low (enable)	0.6	0.7	1	V	
T_{SYon}	SYNC Turn-on Prop. Delay		90	130	ns	SYNC=high to low C_{LOAD}=1nF
T_{SYoff}	SYNC Turn-off Prop. Delay		80	120	ns	SYNC=low to high C_{LOAD}=1nF
T_{SYPWf}	Minimum SYNC Pulse Width(*)	50			ns	
I_{synch}	Synch pin input current		0.8		uA	
Td_{EN_on}	Delay from EN high to V_G high		20		us	EN_low >6us
Td_{EN_off}	Delay from EN low to V_G low (*)		300		ns	

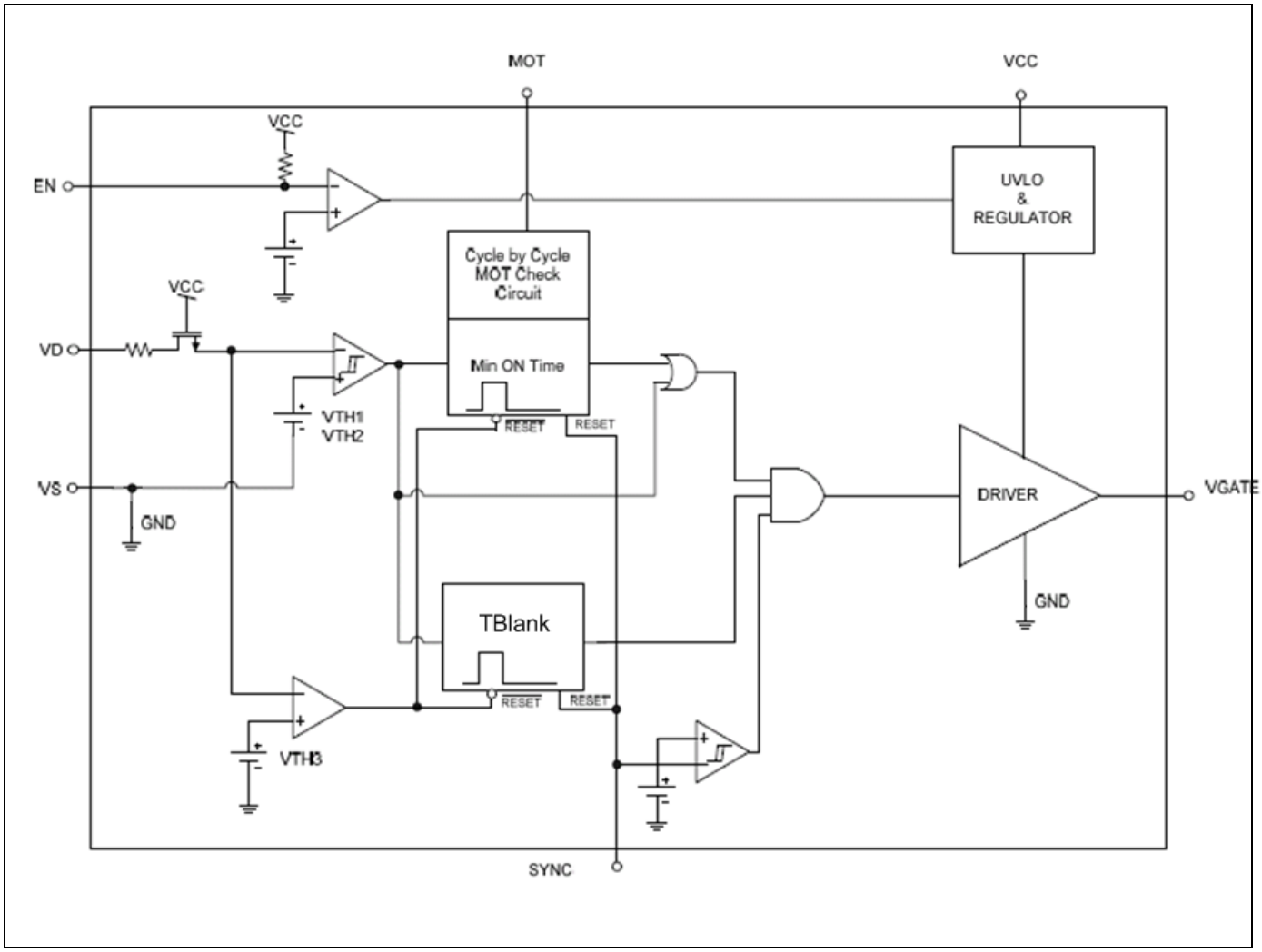
(*) guaranteed by design

GATE DRIVER SECTION

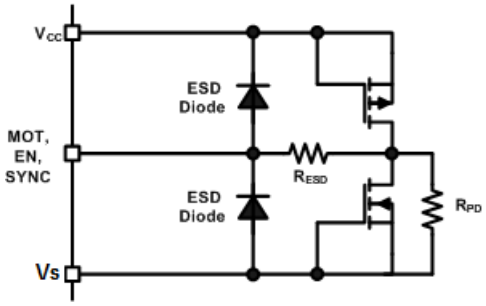
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{GLO}	Gate Low Voltage		0.19	0.29	V	I_{GATE}=200mA, Vcc = 12V
V_{GTH}	Gate High Voltage	9.4	10.7	11.9	V	V_{CC}=12V-18V (internally clamped) C_{LOAD}=1nF
t_{r1}	Rise Time		70		ns	C_{LOAD}=10nF, V_{CC}=15V
t_{f1}	Fall Time		35		ns	C_{LOAD}=10nF, V_{CC}=15V
T_{Don}	Turn on Propagation Delay		90	120	ns	C_{LOAD}=1nF, V_{CC}=15V
T_{Doff}	Turn off Propagation Delay		60	75	ns	C_{LOAD}=1nF, V_{CC}=15V
$I_{O\ source}$	Output Peak Current (source) (*)		3		A	C_{LOAD}=10nF
$I_{O\ sink}$	Output Peak Current (sink) (*)		6		A	C_{LOAD}=10nF

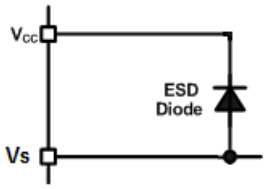
(*) guaranteed by design

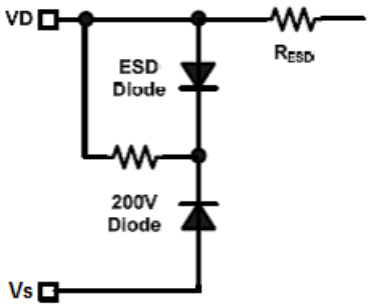
Functional Block Diagram

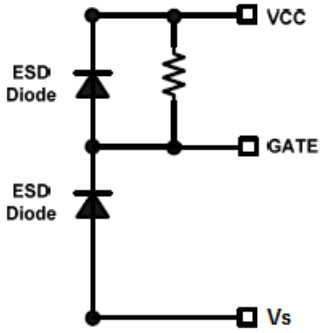


Input/Output/Enable Pin Equivalent Circuit Diagrams





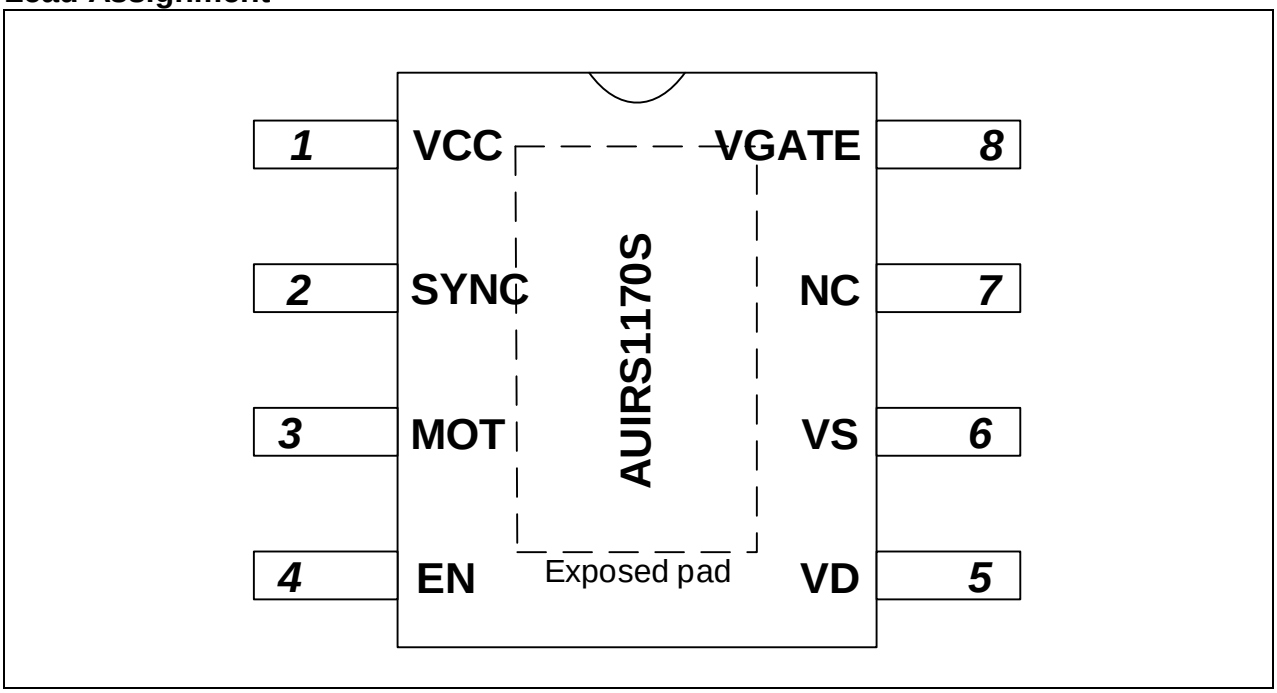




Lead Definitions

PIN #	Symbol	Description
1	VCC	Supply Voltage
2	SYNC	SYNC Input for direct turn off
3	MOT	Minimum On Time
4	EN	Enable
5	VD	FET Drain Sensing
6	VS	FET Source Sensing and GND connection
7	NC	Not connected
8	VGATE	Gate Driver Output
	ExpPad	at Vs potential, use only for thermal dissipation.

Lead Assignment



Detailed Pin Description

VCC: Power Supply
This is the supply voltage pin of the IC and it is monitored by the under voltage lockout circuit. It is possible to turn off the IC by pulling this pin below the minimum turn off threshold voltage, without damage to the IC.
To prevent noise problems, a bypass ceramic capacitor connected to Vcc and COM should be placed as close as possible to the AUIRS1170. This pin is internally clamped.

SYNC: Direct Turn-off and Reset
SYNC is used to directly turn-off the SR MOSFET by an external signal. The gate output of AUIRS1170 is low when SYNC voltage is higher than V_{SYHI} threshold. The propagation delay from SYNC goes high to gate turns off is 50ns maximum. The turn-off of SYNC is a direct control and it ignores the MOT time (override).
The SYNC pin will reset MOT and Blanking time when SYNC switches from low to high. It will reset MOT timer and Blanking timer only at the rising edge of signal. This function is useful for very low output voltage condition (such as overload or short circuit) where the VD voltage is too low to reach Vth3 threshold to reset the timers.
SYNC pin also can be used to control the turn-on time of SR MOSFET (adding additional delay time at turn-on for noise immunity). If not used, SYNC pin should be connected to COM.

MOT: Minimum On Time
The MOT programming pin controls the amount of minimum on time. Once V_{TH2} is crossed for the first time, the gate signal will become active and turn on the power FET. Spurious ringings and oscillations can trigger the input comparator off. The MOT blanks the input comparator keeping the FET on for a minimum time. The MOT is programmed between 200ns and 3us (typ.) by using a resistor referenced to COM and can be programmed using the following formula:

$$R_{MOT} = 2.5 * 10^{10}\, t_{MOT}$$

EN: Enable
This pin is used to activate the IC “sleep” mode by pulling the voltage level below 1.6V (typ). In sleep mode the IC will consume a minimum amount of current. All switching functions will be disabled and the gate will be inactive.

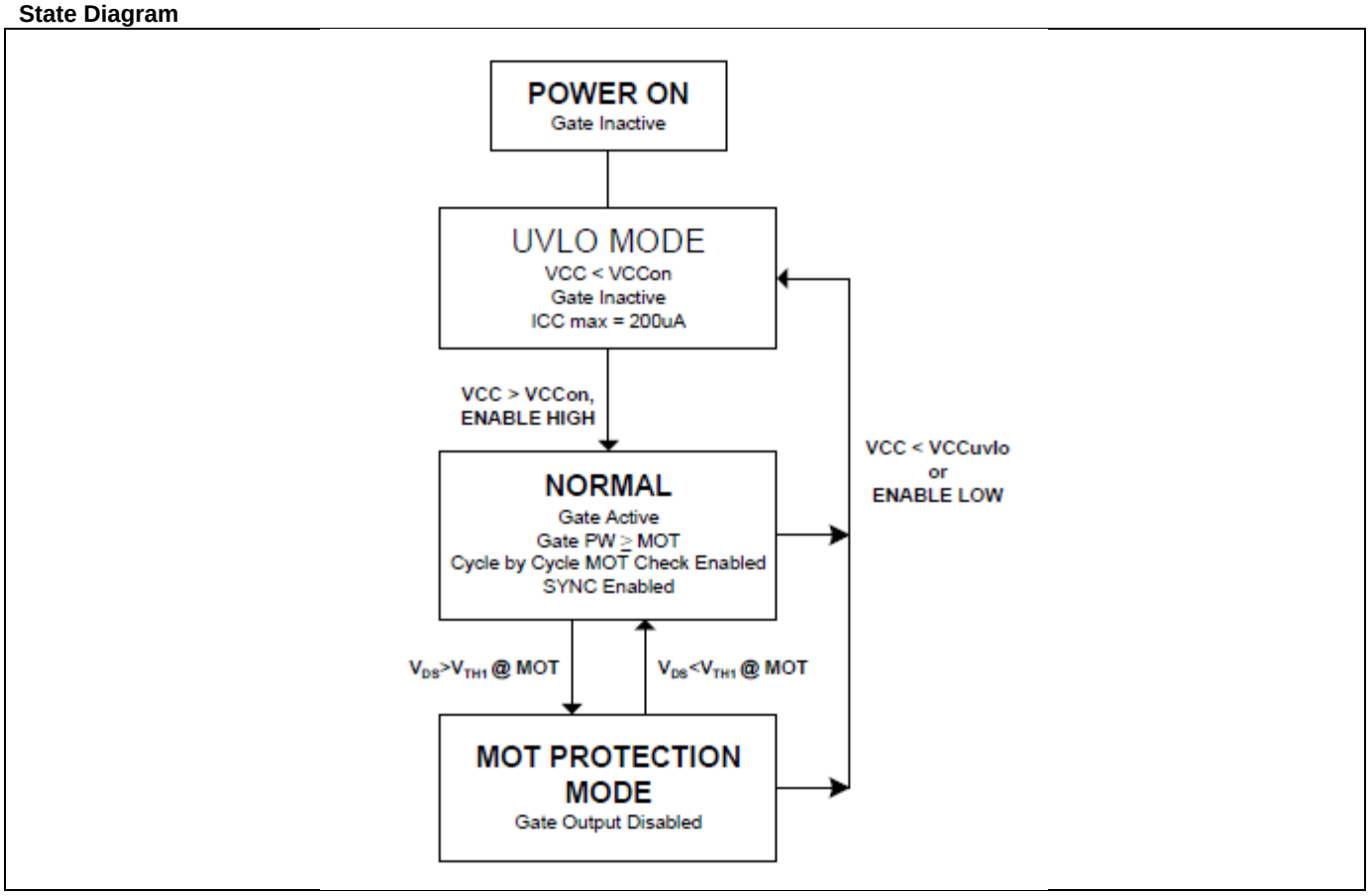
VD: Drain Voltage Sense
VD is the voltage sense pin for the power MOSFET Drain. This is a high voltage pin and particular care must be taken in properly routing the connection to the power MOSFET drain. Additional Filtering is recommended; see application section for details.

VS: Source Voltage Sense
VS is the differential sense pin for the power MOSFET Source and IC gnd connection. This pin must must be connected as close as possible to the power MOSFET source pin. Good electrical connection must be done to this pin since the internal devices and gate driver are referenced to this point.

VGATE: Gate Drive Output
This is the gate drive output of the IC. Drive voltage is internally limited and provides 2A peak source and 7A peak sink capability. Although this pin can be directly connected to the power MOSFET gate, the use of minimal gate resistor is recommended, especially when putting multiple FETs in parallel. Care must be taken in order to keep the gate loop as short and as small as possible in order to achieve optimal switching performance.

Functional Description

State Diagram



UVLO/Sleep Mode

The IC remains in the UVLO condition until the voltage on the VCC pin exceeds the VCC turn on threshold voltage, $V_{CC\ ON}$. During the time the IC remains in the UVLO state, the gate drive circuit is inactive and the IC draws a quiescent current of $I_{CC\ START}$. The UVLO mode is accessible from any other state of operation whenever the IC supply voltage condition of VCC < $V_{CC\ UVLO}$ occurs.

The sleep mode is initiated by pulling the EN pin below 1.6V (typ). In this mode the IC is essentially shut down and draws a very low quiescent supply current.

Normal Mode and Synchronized Enable Function

The IC enters in normal operating mode once the UVLO voltage has been exceeded and the EN voltage is above V_{ENHI} threshold. When the IC enters the Normal Mode from the UVLO Mode, the GATE output is disabled (stays low) until V_{DS} exceeds V_{TH3} to activate the gate. This ensures that the GATE output is not enabled in the middle of a switching cycle. This logic prevents any reverse currents across the device due to the minimum on time function in the IC. The gate will continuously drive the SR MOSFET after this one-time activation. The Cycle by Cycle MOT protection circuit is enabled in Normal Mode.

MOT Protection Mode

If the secondary current conduction time is shorter than the MOT (Minimum On Time) setting, the next driver output is disabled. This function can avoid reverse current that occurs when the system works at very low duty-cycles or at very light/no load conditions and reduce system standby power consumption by disabling GATE outputs. The Cycle by Cycle MOT Check circuit is always activated under Normal Mode and MOT Protection Mode, so that the IC can automatically resume normal operation once the load increases to a level and the secondary current conduction time is longer than MOT.

VG pulse can result shorter than MOT in case the sensed VDS voltage crosses both VTH1 and VTH3 before MOT time is expired. In particular, VG signal is VTH3 dominant and it is reset when VDS crosses VTH3. Despite the pulse length may result shorter, the MOT functionality is preserved and AUIRS1170S filters the following VDS pulse out by keeping VG low. Figure M1 shows the behavior of AUIRS1170S at VG pin in this specific case (continuous line) and in case VDS does not cross VTH3 before MOT is expired (dotted line).TP represents the VDS pulse length, TA defines the time at which VDS crosses VTH3, TB is the intrinsic delay of VTH3 reset circuit and TG is the VG pulse length. TB has been designed in order to filter out possible VDS noises due to switching of the driven switch and it is in the order of 400ns.

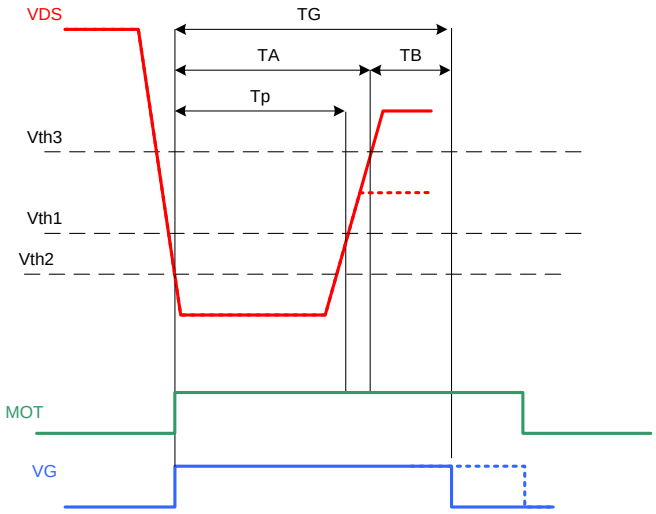


Figure M1: VG length as function of VDS in case it crosses VTH3 either before (continuous line) or after (dotted line) MOT expires.

Application Information

General Description

The AUIRS1170 Smart Rectifier IC can emulate the operation of diode rectifier by properly driving a Synchronous Rectifier (SR) MOSFET. The direction of the rectified current is sensed by the input comparator using the power MOSFET R_{DSon} as a shunt resistance and the GATE pin of the MOSFET is driven accordingly. Internal blanking logic is used to prevent spurious transitions. The Synchronous pin (SYNC) can directly take the signal sent from primary controller to turn off the gate of SR MOSFET prior to the turn-on of primary MOSFET therefore prevent negative current in SR circuit under CCM condition.

AUIRS1170 is suitable for Flyback, Forward and Resonant Half-Bridge topologies.

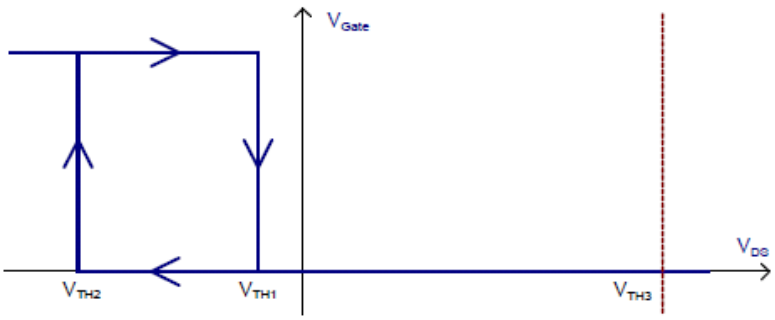


Figure 1: Input Comparator Threshold

Flyback Application

The modes of operation for a Flyback circuit differ mainly for the turn-off phase of the SR switch, while the turn-on phase of the secondary switch (which corresponds to the turn off of the primary side switch) is identical.

Turn-on phase

When the conduction phase of the SR FET is initiated, current will start flowing through its body diode, generating a negative V_{DS} voltage across it. The body diode has generally a much higher voltage drop than the one caused by the MOSFET on resistance and therefore will trigger the turn-on threshold V_{TH2}. At that point the AUIRS1170 will drive the gate of MOSFET on which will in turn cause the conduction voltage VDS to drop down. This drop is usually accompanied by some amount of ringing, that can trigger the input comparator to turn off; hence, a Minimum On Time (MOT) blanking period is used that will maintain the power MOSFET on for a minimum amount of time.
The programmed MOT will limit also the minimum duty cycle of the SR MOSFET and, as a consequence, the max duty cycle of the primary side switch.

DCM/CrCM Turn-off phase

Once the SR MOSFET has been turned on, it will remain on until the rectified current will decay to the level where V_{DS} will cross the turn-off threshold V_{TH1}. This will happen differently depending on the mode of operation. In DCM the current will cross the threshold with a relatively low dI/dt. Once the threshold is crossed, the current will start flowing again through the body diode, causing the V_{DS} voltage to jump negative. Depending on the amount of residual current, V_{DS} may trigger once again the turn on threshold: for this reason V_{TH2} is blanked for a certain amount of time (T_{BLANK}) after V_{TH1} has been triggered.
The blanking time is internally set. As soon as V_{DS} crosses the positive threshold V_{TH3} also the blanking time is terminated and the IC is ready for next conduction cycle.

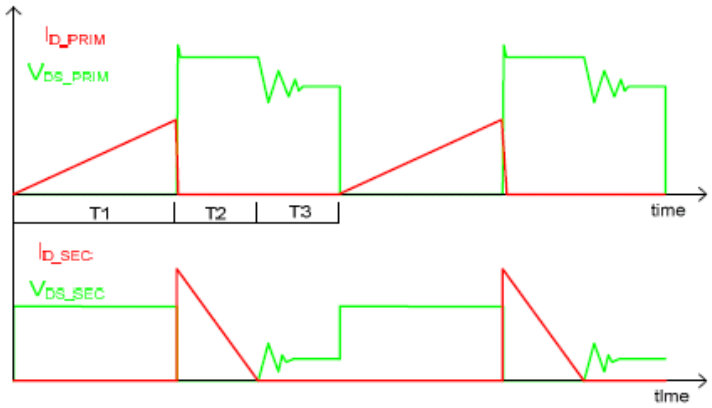


Figure 2: Flyback primary and secondary currents and voltages for DCM mode

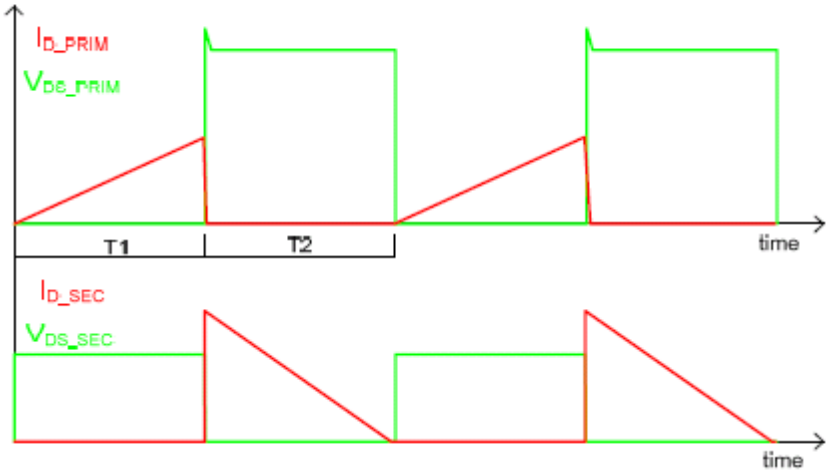


Figure 3: Flyback primary and secondary currents and voltages for CrCM mode

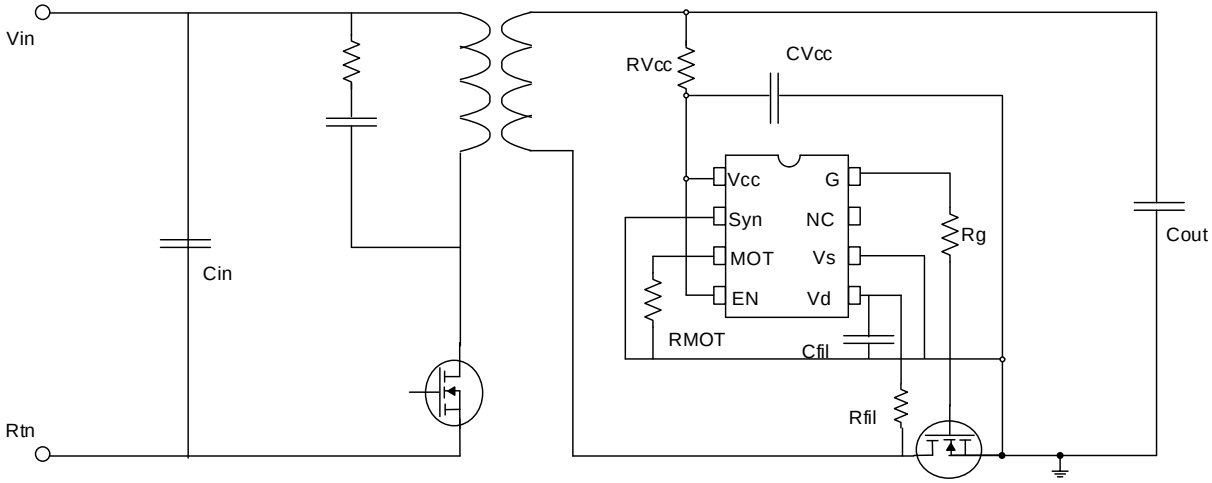


Figure 4: AUIRS1170 in DCM/CrCM mode Flyback

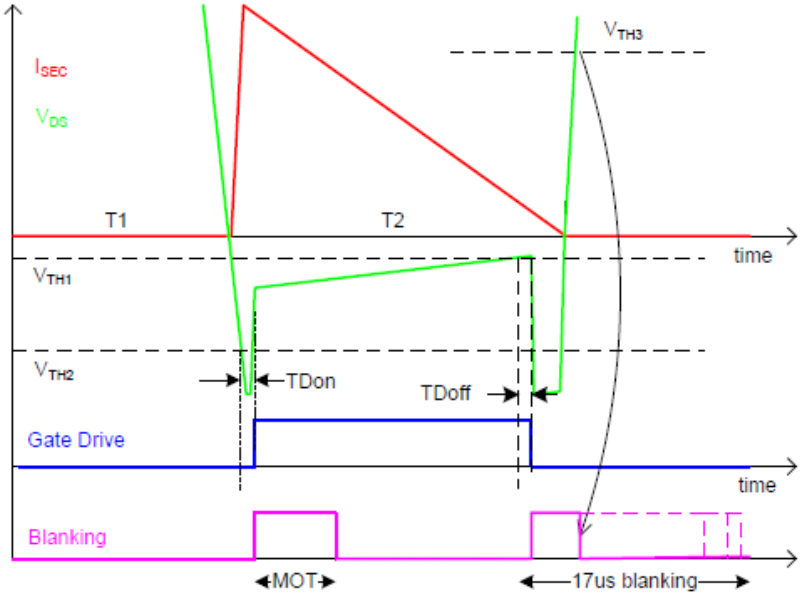


Figure 5: AUIRS1170 DCM/CrCM Sync Rect operation (with SYNC connected to COM)

CCM Turn-off phase

In CCM mode the turn on phase is identical to DCM or CrCM and therefore won't be repeated here. The turn off transition is much steeper and dI/dt involved is much higher (Figure 6). If the SR controller wait for the primary switch to turn back on and turn the gate off according to the FET current crossing V_{TH1}, it has high chance to get reverse current in the SR MOSFET. A predictable turn-off prior to the primary turn-on is necessary. A decoupling and isolation capacitor can be used to couple the primary gate signal to AUIRS1170 SYNC pin and turn-off the SR MOSFET prior to the current slope goes to negative. Some turn-on delay to the primary MOSFET can guarantee no shoot through between the primary and secondary.

In CCM application the connection of AUIRS1170 is recommended as shown in Figure 7.

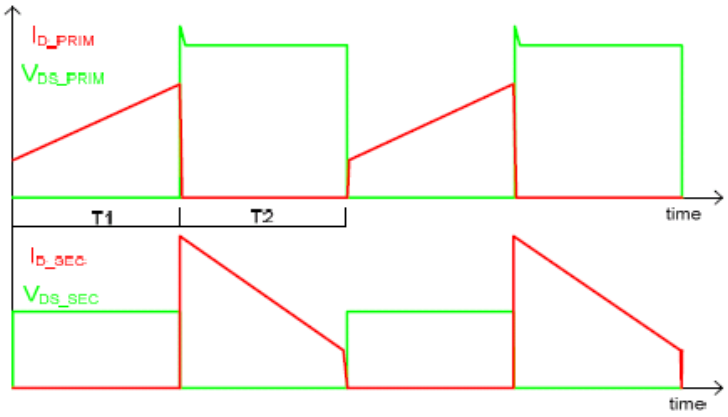


Figure 6: Primary and secondary currents and voltages for CCM mode

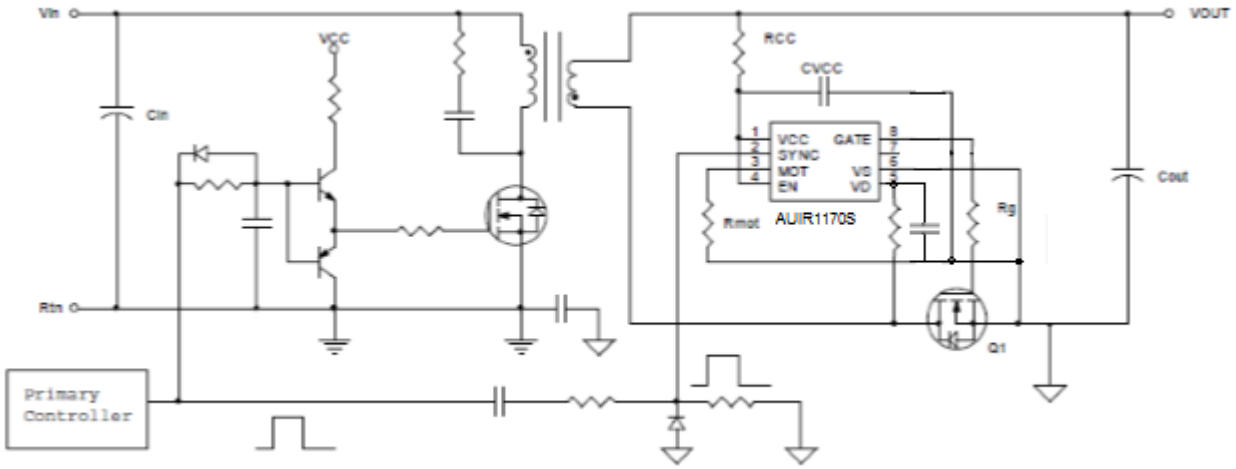


Figure 7: AUIRS1170 schematic in CCM mode Flyback

AUIRS1170 is designed to directly take the control information from primary side with capacitor coupling. A high voltage, low capacitance capacitor is used to send the primary gate driver signal to the SYNC pin. To have the circuit work properly, a Y cap is required between primary ground and secondary ground. No pulse transformer is required for the SYNC function, helps saving cost and PCB area.
The turn-off phase with SYNC control is shown in Figure 8.
In this case a blanking period is not applied; SYNC logic high will reset blanking time.

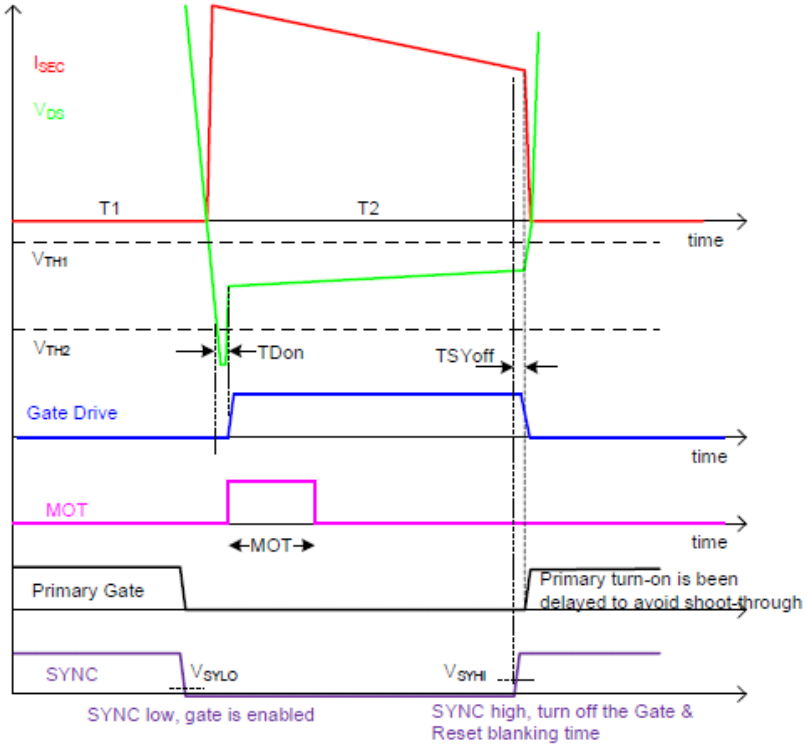


Figure 8: Secondary side CCM operation

Forward Application

The typical forward schematic with AUIRS1170 is shown in Figure 9. The operation waveform of SR in Forward is similar to the CCM operation of Flyback.

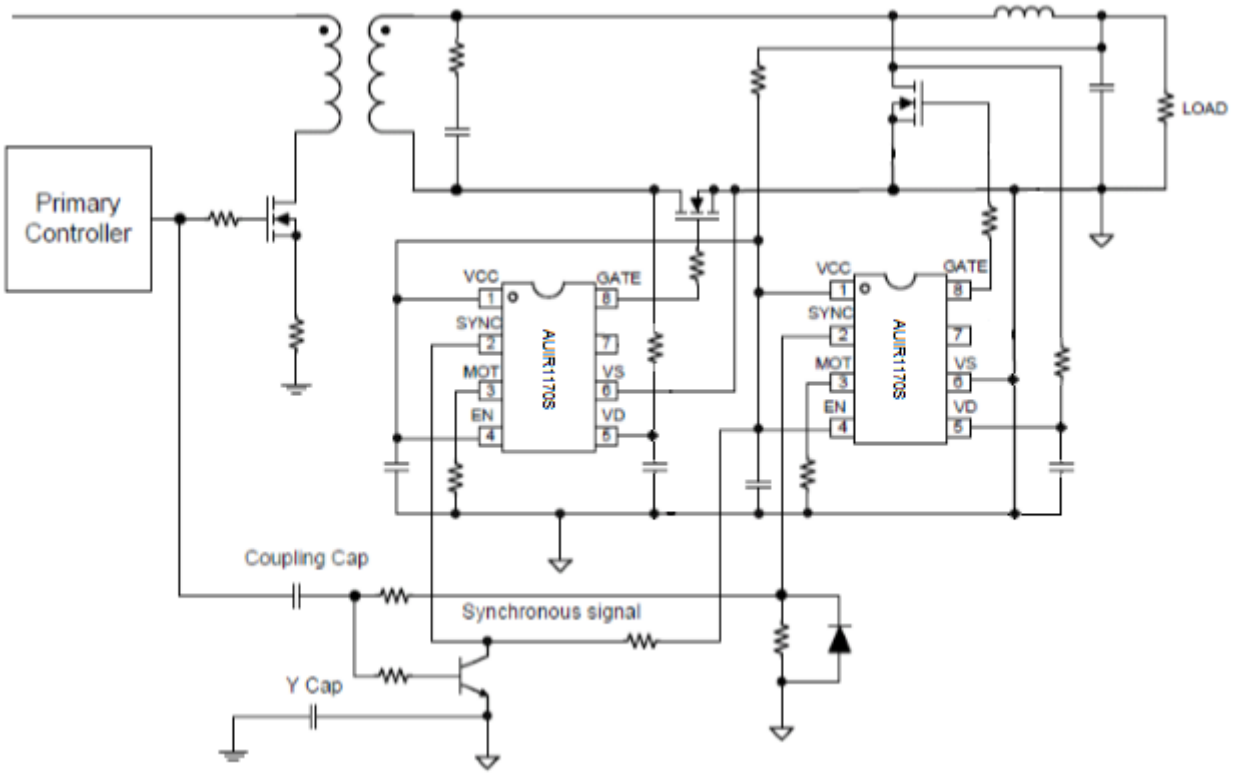


Figure 9: Forward application circuit

Resonant Half-Bridge Application

The typical application circuit of AUIRS1170 in LLC half-bridge is shown in Figure 10.

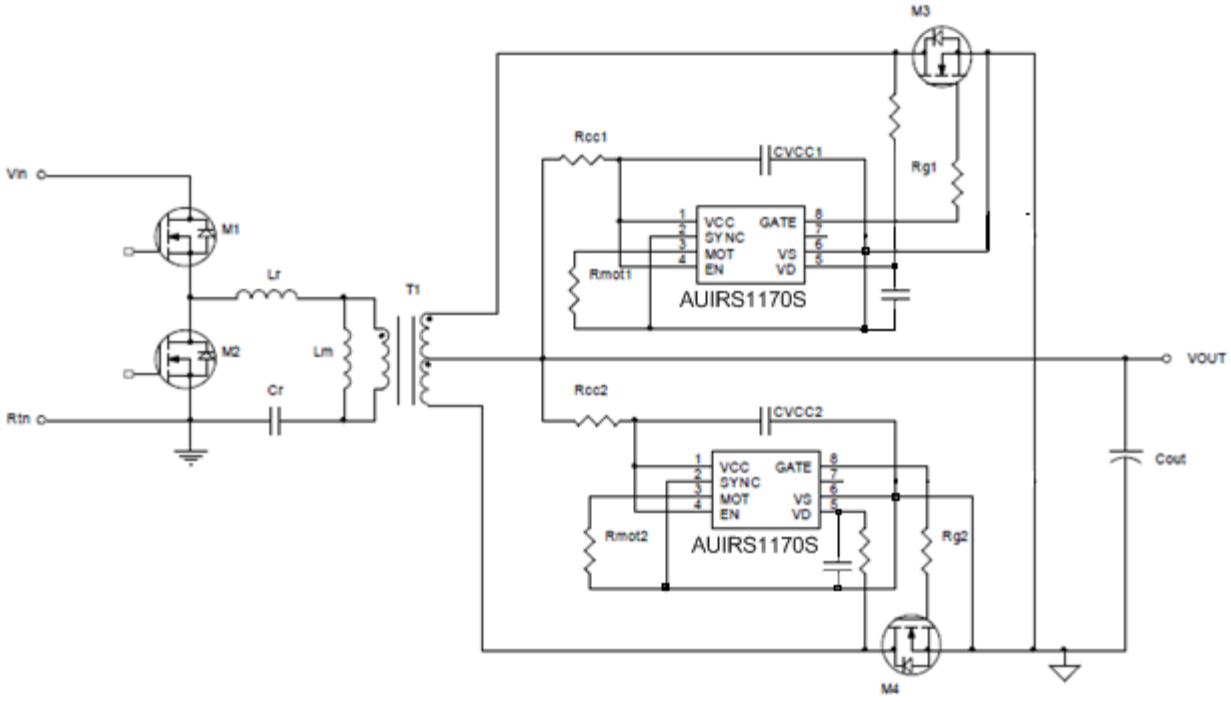


Figure 10: Resonant half-bridge application circuit

The SYNC pin can be tied to Vs in LLC converter. The turn-on phase and turn-off phase is similar to flyback converter except the current shape is sinusoid. The typical operation waveform can be found below.

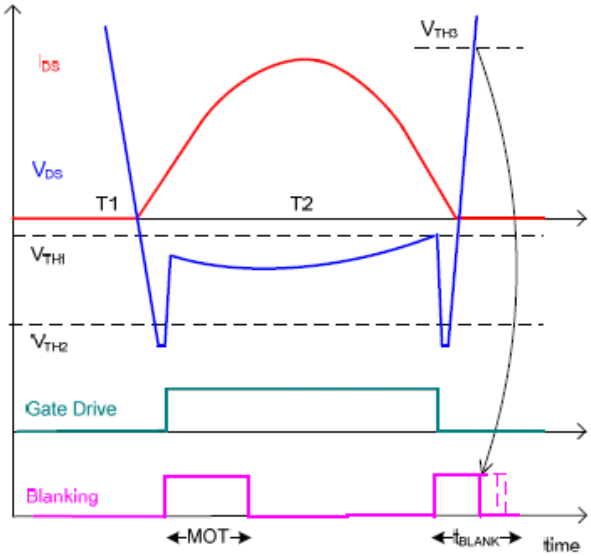


Figure 11: Resonant half-bridge operation waveforms (SYNC connected to Vs)

Application details

Special care has to be taken here in the selection of M3 and M4 mosfets rdson and Qg, because of the current shape. Being the current sinusoidal, a certain delay is expected from the time the M3 (M4) body diode will start conducting to the time the M3 (M4) channel will be closed. This depends on the di/dt and on the forward recovery time of the body diodes. In any case, it is necessary that diode forward voltage rises (in absolute value) above Vth2 before the gate drive is activated.
Because the forward recovery time of the state of the art mosfets is very short (few tens nsec) and forward recovery voltage may be several volts, this delay may be neglected, except in case of MHz operation.
So, in absence of any filter on pin Vd, the only significant delay at turn-on is due to the mosfet Qg, charged by the peak current of the IC gate driver output (3A typ).
On the other side, as deeply discussed in AN1205, some filter is needed on pin Vd, which delays the fall time at the IC Vd input; for that reason, AN1205 suggests the filter capacitor is quickly discharged trough a diode, whose anode is connected to pin Vd and whose cathode is connected to the mosfet drain terminal, as shown in fig.12:

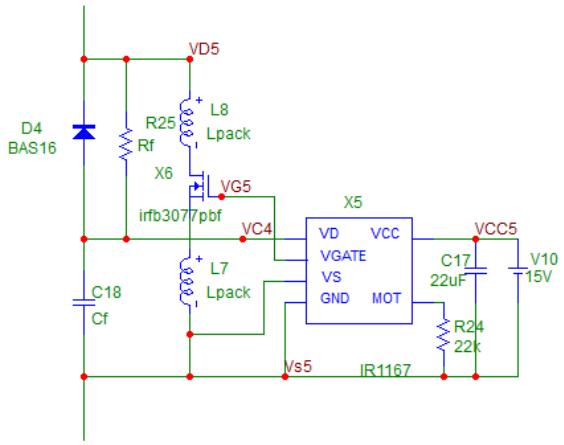


Fig.12: Vds filtering of noise generated by layout parasitics

At turn-off, because Vth1 is very low (few mV), very little delay is expected.
As said before, the turn-on delay introduced by the filter on Vd-Vs is deeply discussed in AN1205 and only few guidelines how to calculate the filter and the relevant delay are given here.
Moreover, an example of estimation of the delay introduced by M3 (M4) rdson and Qg is given.
To such delays, the delay introduced by the Vd-Vs filter has, of course, to be added.

Vds filtering

In resonant and high power applications the synch. rect. switch signal Vds may be not so clean, because of secondary stray inductances (see an example in figure 13 where dark blue is the voltage across the secondary switch, called S1; green is the total secondary current, flowing into the two alternate branches of the rectifier, S1 and S2; purple is the primary current and light blue the gate signal of the AUIRS1170S which drives S1).
Except when working at exactly the resonant frequency, there will always be a phase shift between the half (or full) bridge center tap voltage and the current. This is clearly visible in figure 13, where some extra Vds ringing appears in the middle of the Vds pulse, caused by the commutation of the primary switches.
This extra ringing on Vds, if not properly filtered, may induce false or premature commutations of the AUIRS1170S; to be more specific it may happen that at the primary switching transition the induced noise from primary to secondary forces the turn-off of the active synch. rect Fet. This effect is more evident at low output current when the signal across the synch. rect Fes is low.

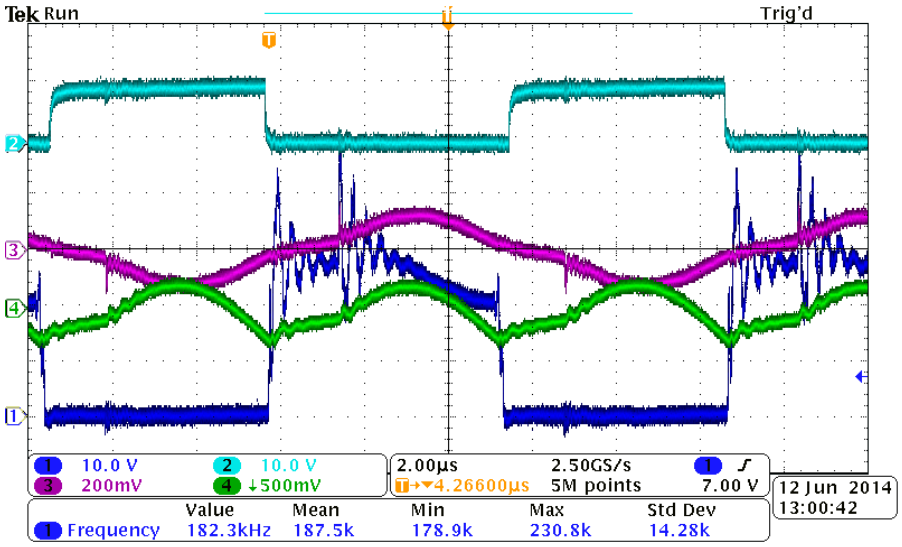


Figure 13: practical secondary waveforms in a LLC converter

To improve the noise rejection then a LP filter on Vds is suggested; the general rule is that filter cut-off frequency has to be set according to the fundamental frequency of the ringings (Fring): because it is a first order filter, its -3dB frequency shall be at least a decade below the ringing fundamental.
On the other side, the filter introduces delays at both turn-on and turn-off.
An example is shown in figure 14. A filter with a cut-off frequency of 1MHz (100pF - 1.5kOhm) introduces a turn-on delay of several hundred nsec (around 650ns).
Fortunately such delay can be easily compensated by introducing a diode in parallel to the filter resistance, which quickly discharges Cf during the high to low Vds transition.
The effect of such diode is shown in figure 15, where the turn-on delay is now only 134nsec.
Neglecting for a moment the compensation enabled by the diode, the delay cannot become a significant part of the switching half cycle. The delay introduced by the filter (0 to 90%) is 2.3 * R_f*C_f. Assuming as a starting point that the delay must stay at least below 20% of the half PWM period (Tsw/2), which is about half of the delay shown in Fig.14, we have that:

$$\frac{1}{2.3*R_f*C_f} \geq \frac{10}{Tsw} = 10 * Fsw \qquad [1]$$

The delay compensation forced by the diode will then further reduce the real delay, since the discharging equivalent resistance "Rd" of the diode in forward conduction will be used.
Then the final approximated formula to determine the RC filter pole value is the following:

$$\frac{2.3 * 10}{2 * \pi} Fsw \leq \frac{1}{2 * \pi * R_f C_f} = Fp \leq \frac{Fring}{10}$$

A final verification of the best working value has to be carried on in the real application and a good compromise has to be found case by case.

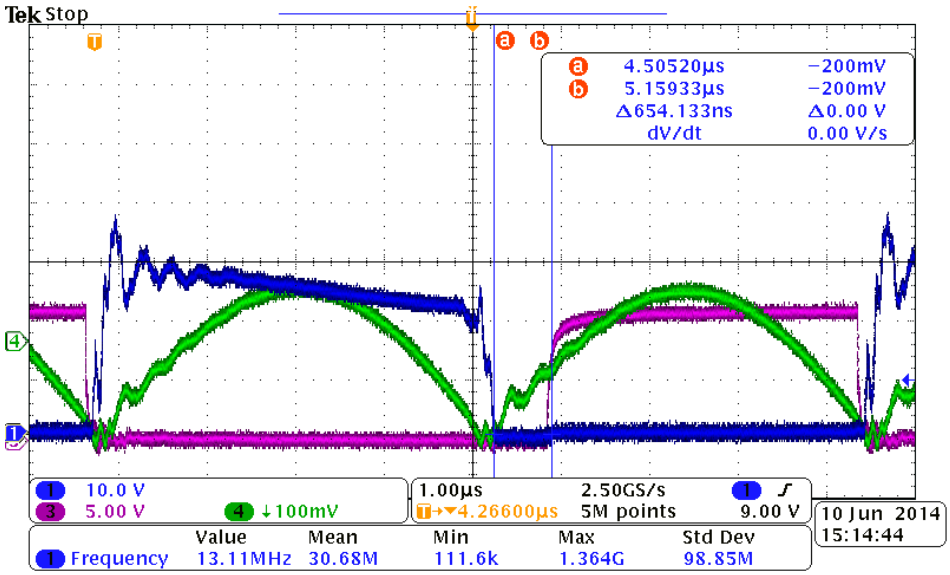


Figure 14: effect of Vds filter on turn-on delay.

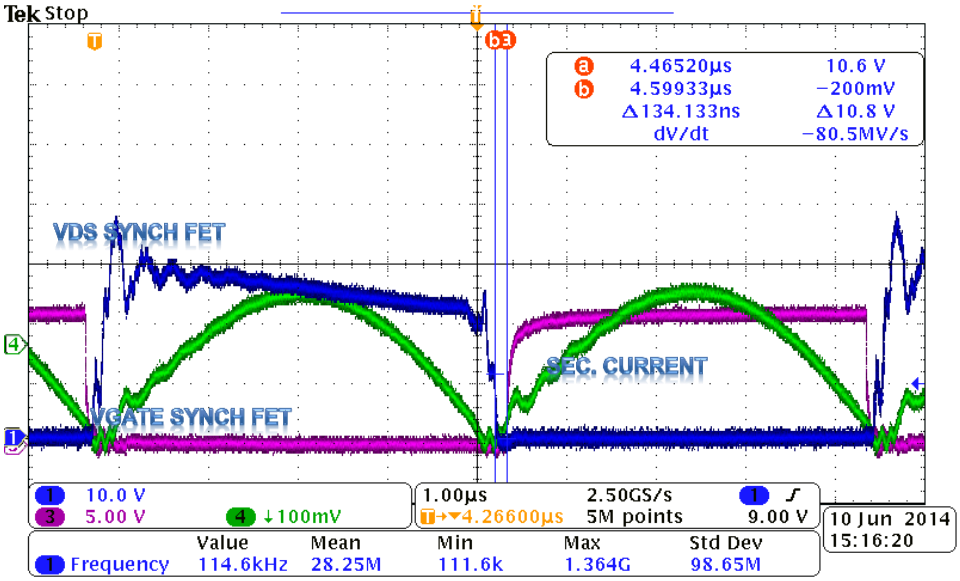


Figure 15: diode-discharge compensation of filter induced turn on delay

In all cases, the choice of R_f and C_f is not free. R_f is directly in series with pin Vd on the AUIRS1170S. Because the input Vd-Vs comparator is fed by an internal current source, adding too much external resistance may severely impact the turn-on threshold. Therefore a R_f value < 1.5k - 2k Ohm is recommended.

Turn-on delay and Mosfet selection
As said, the trigger of Vth2 threshold may be considered instantaneous, because of the forward recovery voltage of the body diode. After a time Tdon, Vgs will start rising. Because the mosfet is turned-on at zero voltage, there is no Miller plateau effect. Thus, the time the mosfet channel gets the whole current may be approximated as:

$$Tdelay_{on} = Tdon + Vgsth*Ciss/I_{Osource}$$

This delay is almost independent from the secondary current, provided the mosfet has enough transconductance. A more precise estimation is:

$$Tdelay - on = Tdon + \left(Vgsth * \frac{Ciss}{Iosource}\right)/(1 - gm * Ciss * 2 * \pi * \frac{Fsw}{Iosource} * Ipk)$$

Where gm is the mosfet transconductance (at low current levels) and Ipk is the secondary sinusoidal current peak value.

Worth to say that, to keep the mosfet channel in conduction, the rdson of the mosfet must not be too low!
In fact, if at the expiration of the MOT the channel voltage drop:

$$Vds = Rdson*i(T_{ONmin}) < Vth1$$

the gate pulse will be immediately terminated and the whole current will go back to the body diode.
A good rule of thumb is then to choose the Mosfet Rdson so that the voltage dropout across it will be around 100mV at max output current.

Turn-off
Turn-off is a bit more critical because, if too long, some cross conduction may occur in the output rectification.
Turn-off will actually be initiated before the current zero crossing, at the time Rdson*i(t) reaches Vth1.
This “anticipation” is given by:

$$Dt^{--} = Vth1/(Rdson*2*\pi*Fsw*Ipk)$$

After the time Tdoff, due to the IC internal propagation delay, the gate driver will start to discharge the mosfet Qg. The mosfet channel may be considered fully closed when Vgs approaches Vgs_{th}. Therefore:

$$Tfall = (Qg-Qgs_1)/I_{Osink}$$

Where Qg is the total gate charge and Qgs_1 the gate charge to get to the Vgs_{th}.

The total turn-off delay must then be

$$Tdelay_{off} = Tdoff + Tfall < Dt^{--}$$

This theoretical calculation helps to identify the optimum Rds-on and Qg of the matching synch. rect Fet, however an experimental verification is always needed to fine tune the application for proper operation.

Synch functionality in resonant applications

The SYNC pin also can be connected to a control signal for special turn-on and/or turn-off control.
Figure 16 is an example where the SYNC function is used to add some delay to the turn-on phase.
Figure 17 shows instead the use of synch to reset at the end of each cycle when Vds is too low to reach Vth3.

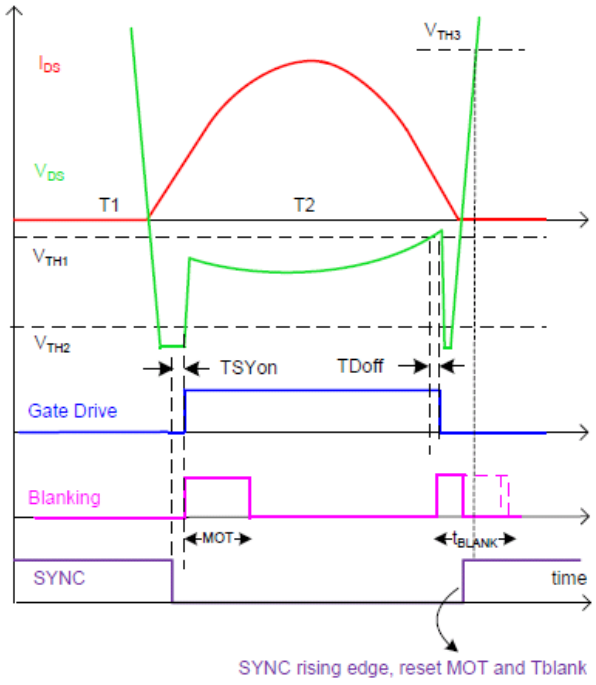


Figure 16: Resonant half-bridge with SYNC control

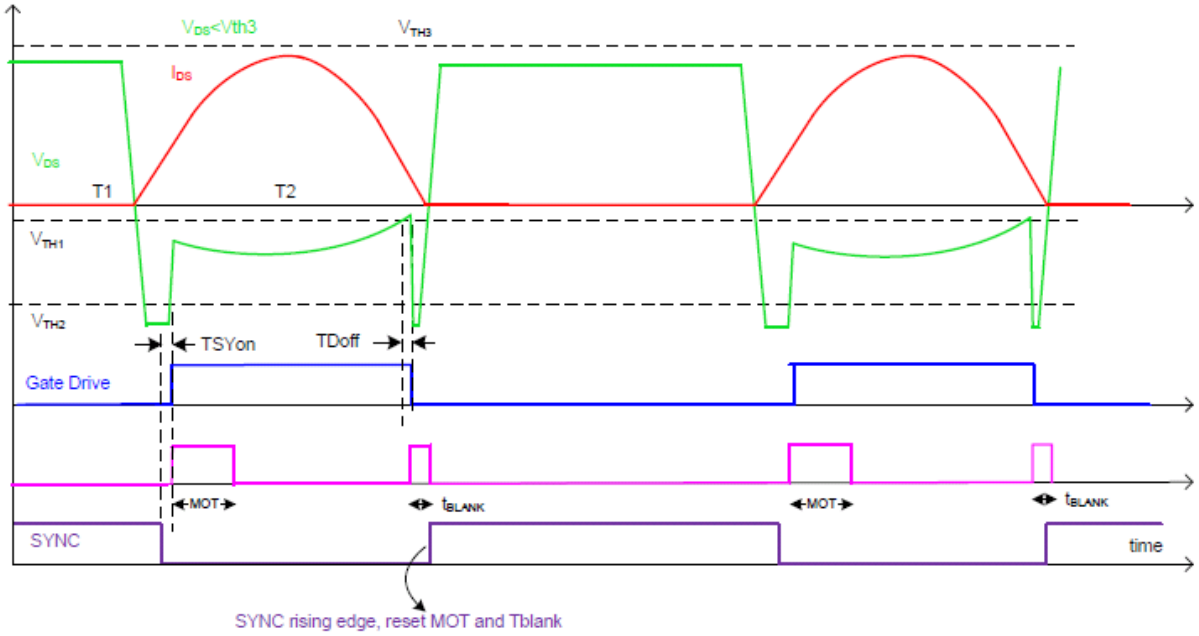


Figure 17: Reset by SYNC when VD<V_{th3}

MOT Protection Mode

The MOT protection prevents reverse current in SR MOSFET. This function works in all three topologies. Figure 18 is an example in Flyback converter.

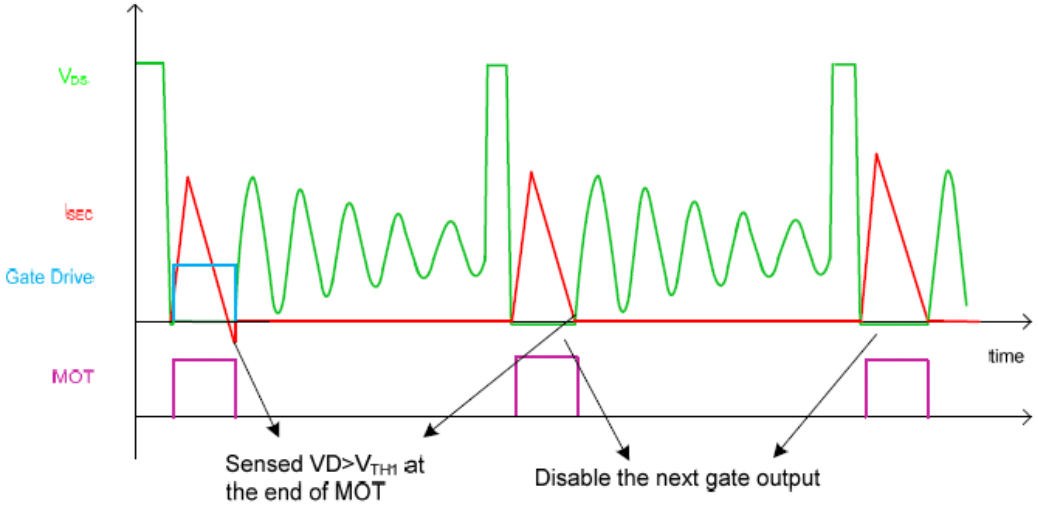


Figure 18: MOT Protection Mode

General Timing Waveforms

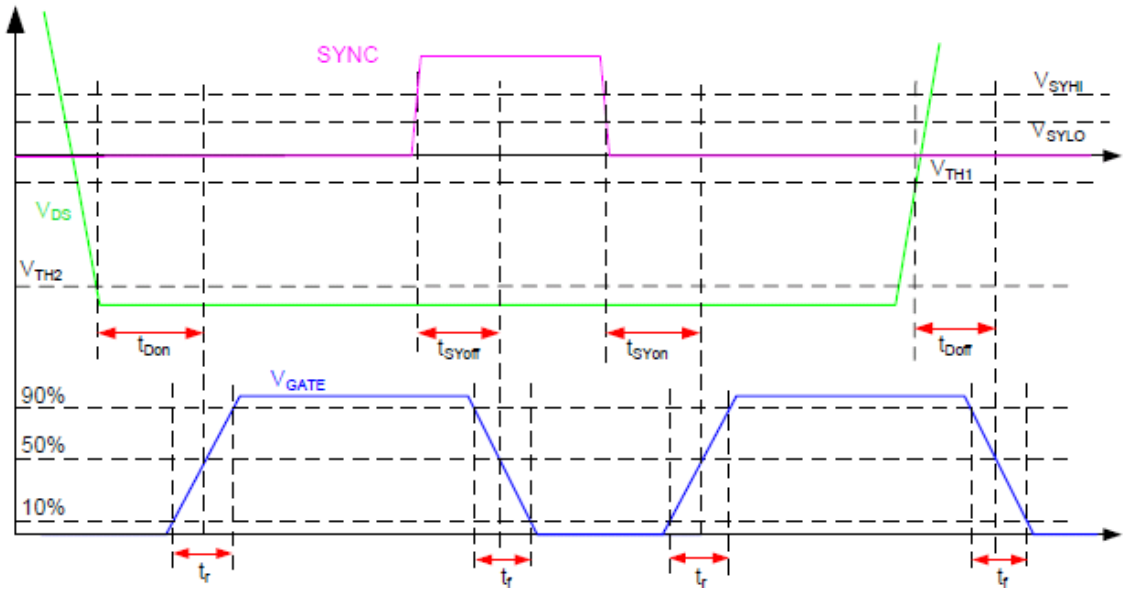


Figure 19: Timing waveforms

Suggested pcb layout and footprint

The exposed pad on the bottom side of the package has been introduced to improve the power dissipation capability of the device. It is weakly electrically connected to the IC substrate, which is at Vs potential. Therefore, special care has to be taken when designing the board layout.
Figure 20 below show two possible footprints. In both cases, the pad has no pcb traces to any signal. It may be connected to Vs (pin6), if needed for layout simplification.

Both layout examples use DirectFet™ as synch.rectification devices; as also reported in AN1205, it is important to have gate connections very similar to each other when several mosfets in parallel are used to carry high currents. To avoid different Tdon and Tdoff delays due to gate traces inductance.
In the bottom example, the gate connections are optimized from the above point of view.

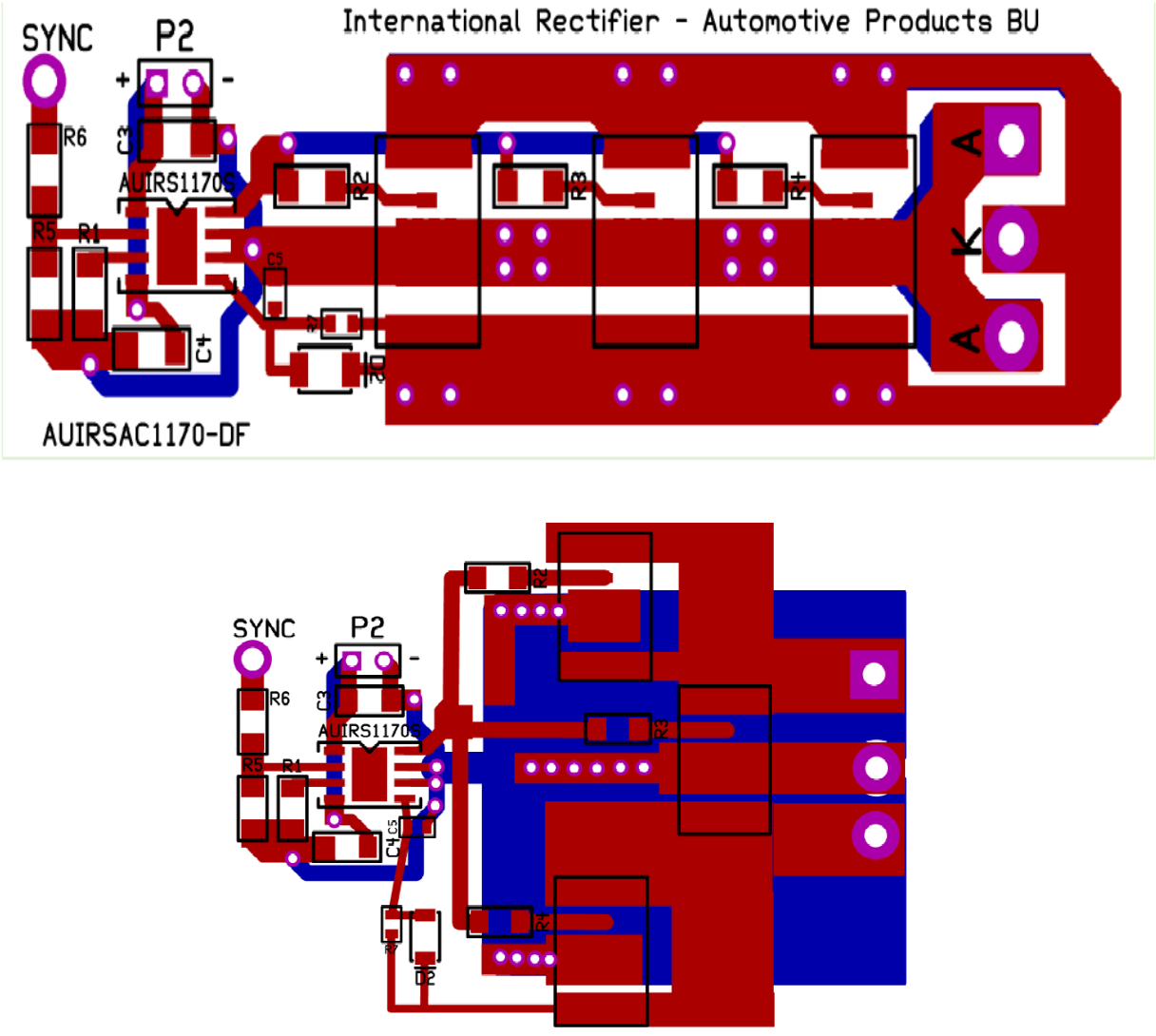
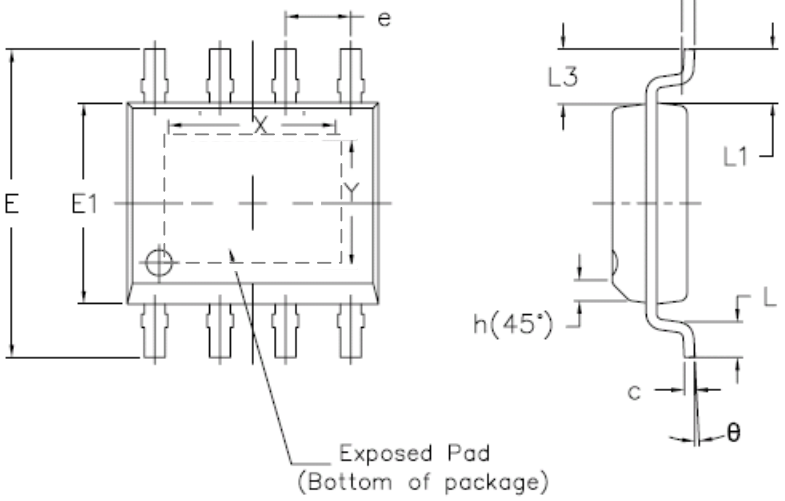
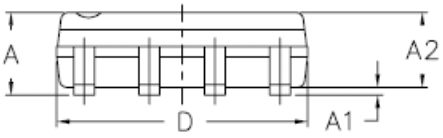


Figure 20: suggested footprints

Package Information

PSOP8L





SYMBOLS	DIMENSIONS			
	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A	—	1.75	—	0.0689
A1	0	0.10	0	0.0039
A2	1.25	—	0.0492	—
b	0.31	0.51	0.0122	0.0201
c	0.17	0.25	0.0067	0.0098
D	4.90BSC		0.1929BSC	
E	6.00BSC		0.2362BSC	
E1	3.90BSC		0.1535BSC	
e	1.27BSC		0.0500BSC	
h	0.25	0.50	0.0098	0.0197
L	0.40	1.27	0.0158	0.0500
L1	1.04REF		0.0409REF	
L2	0.25BSC		0.0098BSC	
L3	1.04REF		0.0409REF	
θ	0°	8°	0°	8°
OPTION2 X	3.300		0.1300	
OPTION2 Y	2.410		0.0950	

Qualification Information

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This part number passed Automotive qualification. Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		PSOP8L	MSL3
ESD	Human Body Model	Class 1A (500V)* (AEC-Q100-002, Rev. E)	
	Charged Device Model	C6 (1000V) (per AEC-Q100-011, Rev.C)	
IC Latch-UP Test		Class II, Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

* Limited by pin 5 (V_D), all other pins are rated at 1500V HBM.

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