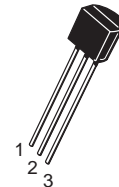
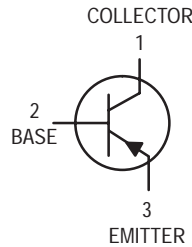


Amplifier Transistors

PNP Silicon

BC327,-16,-25
BC328,-16,-25



CASE 29-04, STYLE 17
TO-92 (TO-226AA)

MAXIMUM RATINGS

| Rating | Symbol | BC327 | BC328 | Unit |
|--|----------------|-------------|-------|------------------------------|
| Collector–Emitter Voltage | V_{CEO} | -45 | -25 | Vdc |
| Collector–Base Voltage | V_{CBO} | -50 | -30 | Vdc |
| Emitter–Base Voltage | V_{EBO} | -5.0 | | Vdc |
| Collector Current — Continuous | I_C | -800 | | mAdc |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 625 | 5.0 | mW mW/ $^\circ\text{C}$ |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 1.5 | 12 | Watt mW/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -55 to +150 | | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|------|---------------------------|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 200 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 83.3 | $^\circ\text{C}/\text{W}$ |

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|--|----------------|---------------|------------|--------|--------------|------|
| Collector–Emitter Breakdown Voltage ($I_C = -10\text{ mA}, I_B = 0$) | BC327 BC328 | $V_{(BR)CEO}$ | -45 -25 | — — | — — | Vdc |
| Collector–Emitter Breakdown Voltage ($I_C = -100\text{ }\mu\text{A}, I_E = 0$) | BC327 BC328 | $V_{(BR)CES}$ | -50 -30 | — — | — — | Vdc |
| Emitter–Base Breakdown Voltage ($I_E = -10\text{ }\mu\text{A}, I_C = 0$) | | $V_{(BR)EBO}$ | -5.0 | — | — | Vdc |
| Collector Cutoff Current ($V_{CB} = -30\text{ V}, I_E = 0$) ($V_{CB} = -20\text{ V}, I_E = 0$) | BC327 BC328 | I_{CBO} | — — | — — | -100 -100 | nAdc |
| Collector Cutoff Current ($V_{CE} = -45\text{ V}, V_{BE} = 0$) ($V_{CE} = -25\text{ V}, V_{BE} = 0$) | BC327 BC328 | I_{CES} | — — | — — | -100 -100 | nAdc |
| Emitter Cutoff Current ($V_{EB} = -4.0\text{ V}, I_C = 0$) | | I_{EBO} | — | — | -100 | nAdc |

BC327,-16,-25 BC328,-16,-25

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---------------|-------------------|-----|------|------|
| ON CHARACTERISTICS | | | | | |
| DC Current Gain ($I_C = -100\text{ mA}$, $V_{CE} = -1.0\text{ V}$) | h_{FE} | BC327/BC328 | 100 | — | 630 |
| | | BC327-16/BC328-16 | 100 | — | 250 |
| | | BC327-25/BC328-25 | 160 | — | 400 |
| ($I_C = -300\text{ mA}$, $V_{CE} = -1.0\text{ V}$) | | 40 | — | — | |
| Base-Emitter On Voltage ($I_C = -300\text{ mA}$, $V_{CE} = -1.0\text{ V}$) | $V_{BE(on)}$ | — | — | -1.2 | Vdc |
| Collector-Emitter Saturation Voltage ($I_C = -500\text{ mA}$, $I_B = -50\text{ mA}$) | $V_{CE(sat)}$ | — | — | -0.7 | Vdc |
| SMALL-SIGNAL CHARACTERISTICS | | | | | |
| Output Capacitance ($V_{CB} = -10\text{ V}$, $I_E = 0$, $f = 1.0\text{ MHz}$) | C_{ob} | — | 11 | — | pF |
| Current-Gain — Bandwidth Product ($I_C = -10\text{ mA}$, $V_{CE} = -5.0\text{ V}$, $f = 100\text{ MHz}$) | f_T | — | 260 | — | MHz |

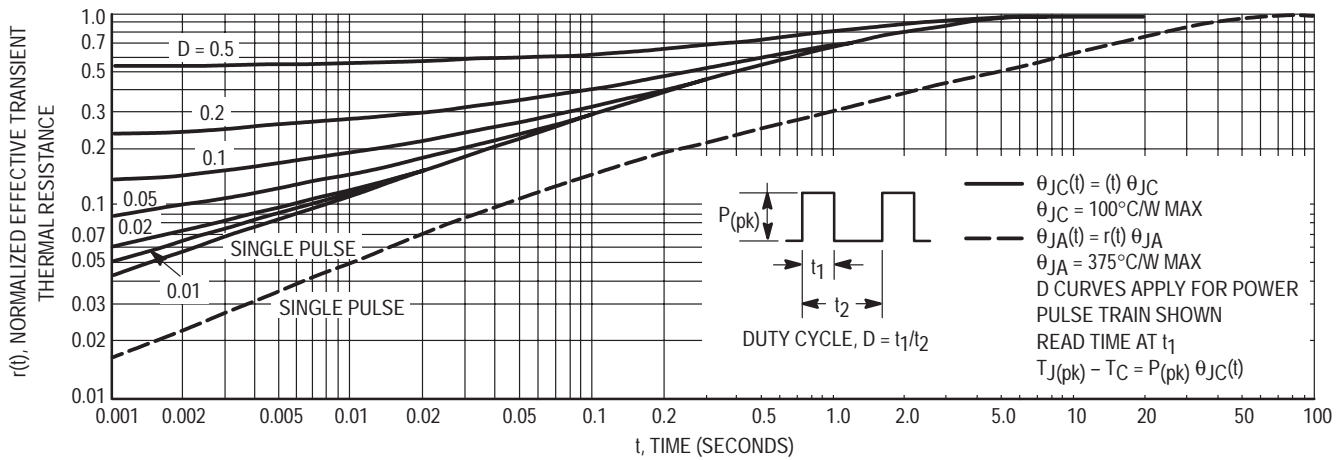


Figure 1. Thermal Response

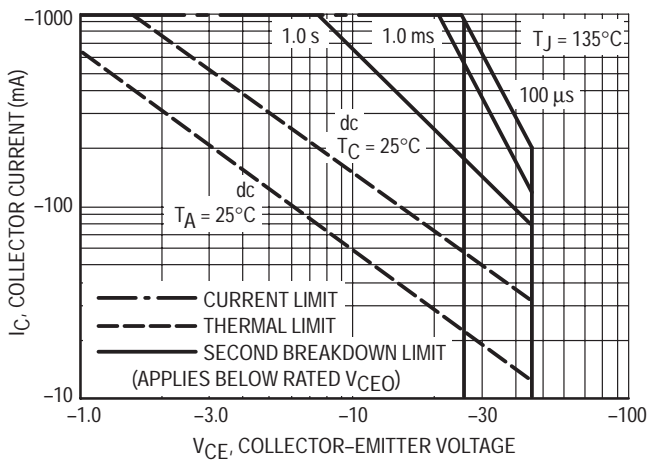


Figure 2. Active Region — Safe Operating Area

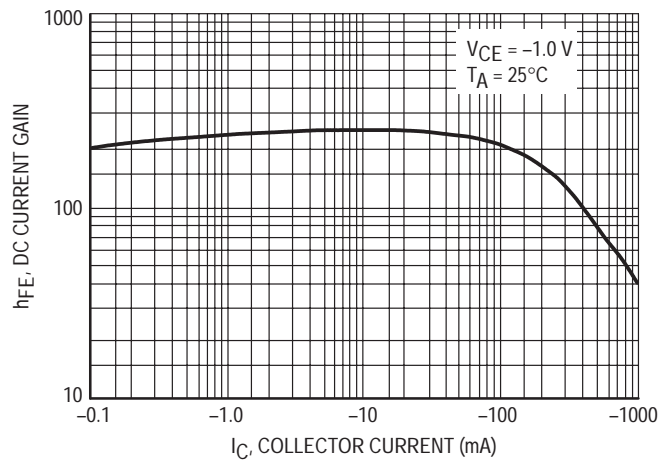


Figure 3. DC Current Gain

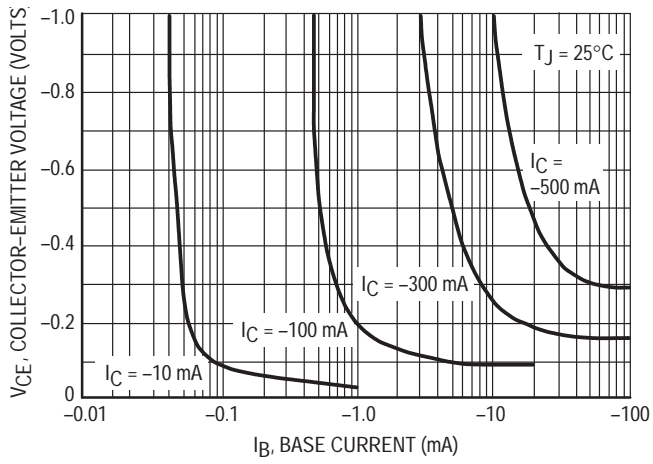


Figure 4. Saturation Region

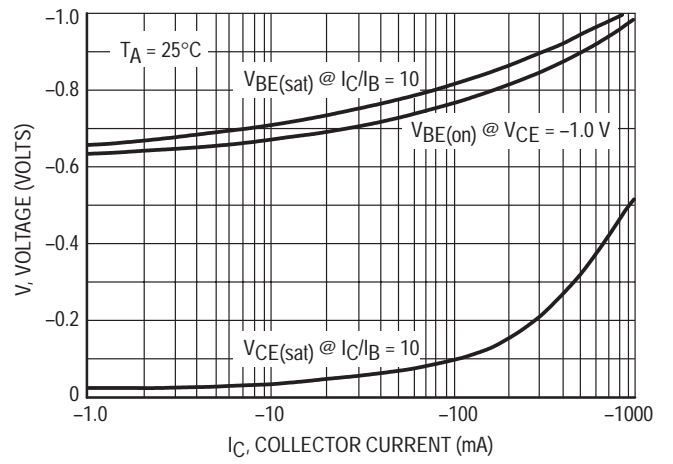


Figure 5. "On" Voltages

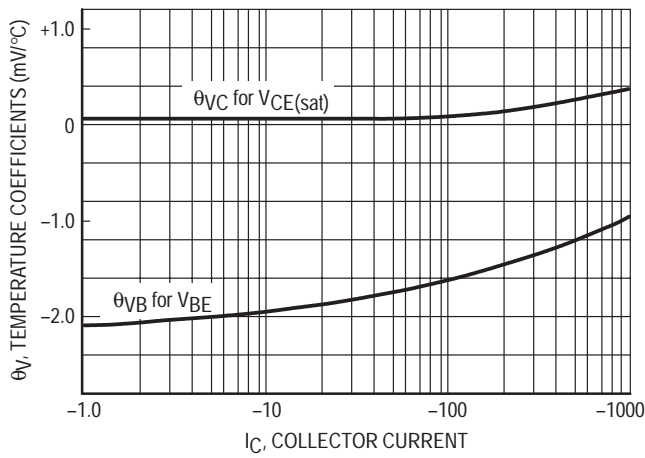


Figure 6. Temperature Coefficients

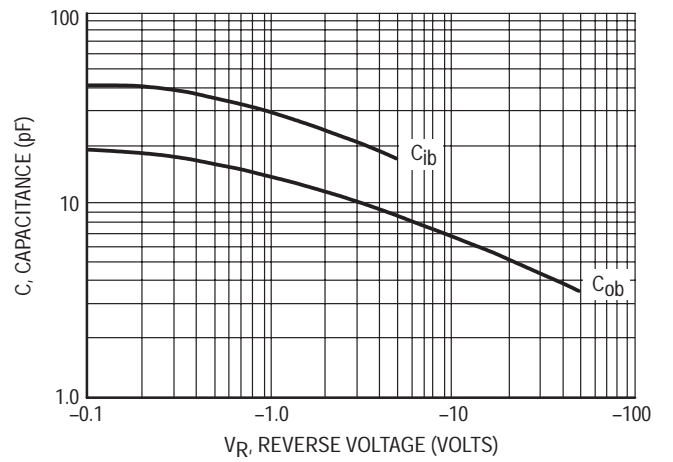


Figure 7. Capacitances

EMBOSSSED TAPE AND REEL

SOT-23, SC-59, SC-70/SOT-323, SC-90/SOT-416, SOT-223 and SO-16 packages are available only in Tape and Reel. Use the appropriate suffix indicated below to order any of the SOT-23, SC-59, SC-70/SOT-323, SOT-223 and SO-16 packages. (See Section 6 on Packaging for additional information).

- SOT-23: available in 8 mm Tape and Reel
Use the device title (which already includes the "T1" suffix) to order the 7 inch/3000 unit reel.
Replace the "T1" suffix in the device title with a "T3" suffix to order the 13 inch/10,000 unit reel.
- SC-59: available in 8 mm Tape and Reel
Use the device title (which already includes the "T1" suffix) to order the 7 inch/3000 unit reel.
Replace the "T1" suffix in the device title with a "T3" suffix to order the 13 inch/10,000 unit reel.
- SC-70/
SOT-323: available in 8 mm Tape and Reel
Use the device title (which already includes the "T1" suffix) to order the 7 inch/3000 unit reel.
Replace the "T1" suffix in the device title with a "T3" suffix to order the 13 inch/10,000 unit reel.
- SOT-223: available in 12 mm Tape and Reel
Use the device title (which already includes the "T1" suffix) to order the 7 inch/1000 unit reel.
Replace the "T1" suffix in the device title with a "T3" suffix to order the 13 inch/4000 unit reel.
- SO-16: available in 16 mm Tape and Reel
Add an "R1" suffix to the device title to order the 7 inch/500 unit reel.
Add an "R2" suffix to the device title to order the 13 inch/2500 unit reel.

RADIAL TAPE IN FAN FOLD BOX OR REEL

TO-92 packages are available in both bulk shipments and in Radial Tape in Fan Fold Boxes or Reels. Fan Fold Boxes and Radial Tape Reel are the best methods for capturing devices for automatic insertion in printed circuit boards.

- TO-92: available in Fan Fold Box
Add an "RLR" suffix and the appropriate Style code* to the device title to order the Fan Fold box.
- available in 365 mm Radial Tape Reel
Add an "RLR" suffix and the appropriate Style code* to the device title to order the Radial Tape Reel.

*Refer to Section 6 on Packaging for Style code characters and additional information on ordering requirements.

DEVICE MARKINGS/DATE CODE CHARACTERS

SOT-23, SC-59, SC-70/SOT-323, and the SC-90/SOT-416 packages have a device marking and a date code etched on the device. The generic example below depicts both the device marking and a representation of the date code that appears on the SC-70/SOT-323, SC-59 and SOT-23 packages.



The "D" represents a smaller alpha digit Date Code. The Date Code indicates the actual month in which the part was manufactured.

Tape and Reel Specifications and Packaging Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel-back” cover tape.

- Two Reel Sizes Available (7” and 13”)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, -1, -2
- SOD-123, SC-59, SC-70/SOT-323, SC-70ML/SOT-363, SOT-23, TSOP-6, in 8 mm Tape
- SOT-223 in 12 mm Tape
- SO-14, SO-16 in 16 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.



EMBOSSSED TAPE AND REEL ORDERING INFORMATION

| Package | Tape Width (mm) | Pitch (mm (inch)) | Reel Size (mm (inch)) | Devices Per Reel and Minimum Order Quantity | Device Suffix |
|-----------------|-----------------|-------------------------|-----------------------|---|---------------|
| SC-59 | 8 | 4.0 ± 0.1 (.157 ± .004) | 178 (7) | 3,000 | T1 |
| SC-70/SOT-323 | 8 | 4.0 ± 0.1 (.157 ± .004) | 178 (7) | 3,000 | T1 |
| | 8 | | 330 (13) | 10,000 | T3 |
| SO-14 | 16 | 8.0 ± 0.1 (.315 ± .004) | 178 (7) | 500 | R1 |
| | 16 | | 330 (13) | 2,500 | R2 |
| SO-16 | 16 | 8.0 ± 0.1 (.315 ± .004) | 178 (7) | 500 | R1 |
| | 16 | | 330 (13) | 2,500 | R2 |
| SOD-123 | 8 | 4.0 ± 0.1 (.157 ± .004) | 178 (7) | 3,000 | T1 |
| | 8 | | 330 (13) | 10,000 | T3 |
| SOT-23 | 8 | 4.0 ± 0.1 (.157 ± .004) | 178 (7) | 3,000 | T1 |
| | 8 | | 330 (13) | 10,000 | T3 |
| SOT-223 | 12 | 8.0 ± 0.1 (.315 ± .004) | 178 (7) | 1,000 | T1 |
| | 12 | | 330 (13) | 4,000 | T3 |
| SC-70ML/SOT-363 | 8 | 4.0 ± 0.1 (.157 ± .004) | 178 (7) | 3,000 | T1 |
| | 8 | | 178 (7) | 3,000 | T2 |
| TSOP-6 | 8 | 4.0 ± 0.1 (.157 ± .004) | 178 (7) | 3,000 | T1 |

EMBOSSED TAPE AND REEL DATA FOR DISCRETES

CARRIER TAPE SPECIFICATIONS



For Machine Reference Only
Including Draft and RADII
Concentric Around B_0



DIMENSIONS

| Tape Size | B_1 Max | D | D_1 | E | F | K | P_0 | P_2 | R Min | T Max | W Max |
|-----------|--------------------|--|-----------------------|---------------------------------|---------------------------------|------------------------|--------------------------------|--------------------------------|-----------------|-------------------|-------------------------------|
| 8 mm | 4.55 mm (.179") | 1.5 ± 0.1 mm -0.0 | 1.0 Min (.039") | 1.75 ± 0.1 mm (.069 ± .004") | 3.5 ± 0.05 mm (.138 ± .002") | 2.4 mm Max (.094") | 4.0 ± 0.1 mm (.157 ± .004") | 2.0 ± 0.1 mm (.079 ± .002") | 25 mm (.98") | 0.6 mm (.024") | 8.3 mm (.327") |
| 12 mm | 8.2 mm (.323") | 1.5 ± 0.1 mm (.059 ± .004") -0.0 | 1.5 mm Min (.060") | | 5.5 ± 0.05 mm (.217 ± .002") | 6.4 mm Max (.252") | | | | | 12 ± .30 mm (.470 ± .012") |
| 16 mm | 12.1 mm (.476") | | | | 7.5 ± 0.10 mm (.295 ± .004") | 7.9 mm Max (.311") | | | | | 16.3 mm (.642") |
| 24 mm | 20.1 mm (.791") | | | | 11.5 ± 0.1 mm (.453 ± .004") | 11.9 mm Max (.468") | | | | | 24.3 mm (.957") |

Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: If B_1 exceeds 4.2 mm (.165) for 8 mm embossed tape, the tape may not feed through all tape feeders.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 5.12-3.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



| Size | A Max | G | T Max |
|-------|---------------------|--|---------------------|
| 8 mm | 330 mm (12.992") | 8.4 mm + 1.5 mm, -0.0 (.33" + .059", -0.00) | 14.4 mm (.56") |
| 12 mm | 330 mm (12.992") | 12.4 mm + 2.0 mm, -0.0 (.49" + .079", -0.00) | 18.4 mm (.72") |
| 16 mm | 360 mm (14.173") | 16.4 mm + 2.0 mm, -0.0 (.646" + .078", -0.00) | 22.4 mm (.882") |
| 24 mm | 360 mm (14.173") | 24.4 mm + 2.0 mm, -0.0 (.961" + .070", -0.00) | 30.4 mm (1.197") |

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

TO-92 EIA, IEC, EIAJ

Radial Tape in Fan Fold Box or On Reel

Radial tape in fan fold box or on reel of the reliable TO-92 package are the best methods of capturing devices for automatic insertion in printed circuit boards. These methods of taping are compatible with various equipment for active and passive component insertion.

- Available in Fan Fold Box
- Available on 365 mm Reels
- Accommodates All Standard Inserters
- Allows Flexible Circuit Board Layout
- 2.5 mm Pin Spacing for Soldering
- EIA-468, IEC 286-2, EIAJ RC1008B

Ordering Notes:

When ordering radial tape in fan fold box or on reel, specify the style per Figures 3 through 8. Add the suffix "RLR" and "Style" to the device title, i.e. MPS3904RLRA. This will be a standard MPS3904 radial taped and supplied on a reel per Figure 9.

Fan Fold Box Information — Order in increments of 2000.

Reel Information — Order in increments of 2000.



US/European Suffix Conversions

| US | EUROPE |
|------|--------|
| RLRA | RL |
| RLRE | RL1 |
| RLRM | ZL1 |

TO-92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL



Figure 1. Device Positioning on Tape

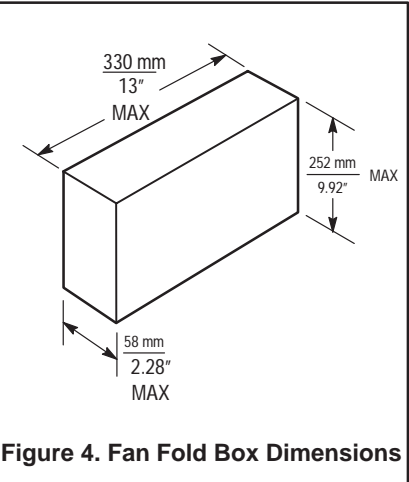
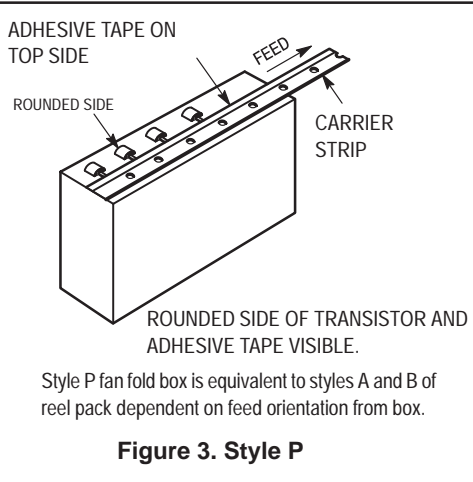
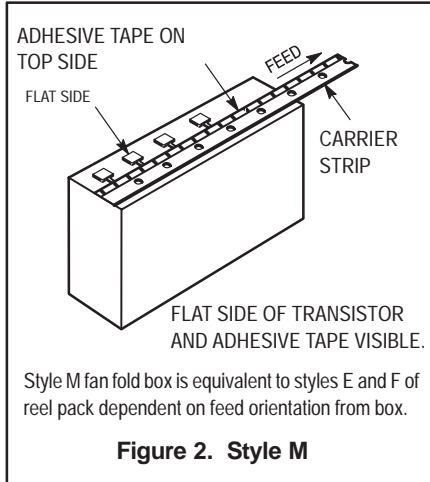
| Symbol | Item | Specification | | | |
|--------|--------------------------------------|---------------|---------|------------|------|
| | | Inches | | Millimeter | |
| | | Min | Max | Min | Max |
| D | Tape Feedhole Diameter | 0.1496 | 0.1653 | 3.8 | 4.2 |
| D2 | Component Lead Thickness Dimension | 0.015 | 0.020 | 0.38 | 0.51 |
| F1, F2 | Component Lead Pitch | 0.0945 | 0.110 | 2.4 | 2.8 |
| H | Bottom of Component to Seating Plane | .059 | .156 | 1.5 | 4.0 |
| H1 | Feedhole Location | 0.3346 | 0.3741 | 8.5 | 9.5 |
| H2A | Deflection Left or Right | 0 | 0.039 | 0 | 1.0 |
| H2B | Deflection Front or Rear | 0 | 0.051 | 0 | 1.0 |
| H4 | Feedhole to Bottom of Component | 0.7086 | 0.768 | 18 | 19.5 |
| H5 | Feedhole to Seating Plane | 0.610 | 0.649 | 15.5 | 16.5 |
| L | Defective Unit Clipped Dimension | 0.3346 | 0.433 | 8.5 | 11 |
| L1 | Lead Wire Enclosure | 0.09842 | — | 2.5 | — |
| P | Feedhole Pitch | 0.4921 | 0.5079 | 12.5 | 12.9 |
| P1 | Feedhole Center to Center Lead | 0.2342 | 0.2658 | 5.95 | 6.75 |
| P2 | First Lead Spacing Dimension | 0.1397 | 0.1556 | 3.55 | 3.95 |
| T | Adhesive Tape Thickness | 0.06 | 0.08 | 0.15 | 0.20 |
| T1 | Overall Taped Package Thickness | — | 0.0567 | — | 1.44 |
| T2 | Carrier Strip Thickness | 0.014 | 0.027 | 0.35 | 0.65 |
| W | Carrier Strip Width | 0.6889 | 0.7481 | 17.5 | 19 |
| W1 | Adhesive Tape Width | 0.2165 | 0.2841 | 5.5 | 6.3 |
| W2 | Adhesive Tape Position | .0059 | 0.01968 | .15 | 0.5 |

NOTES:

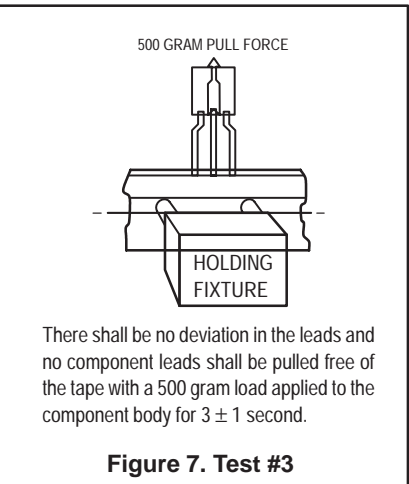
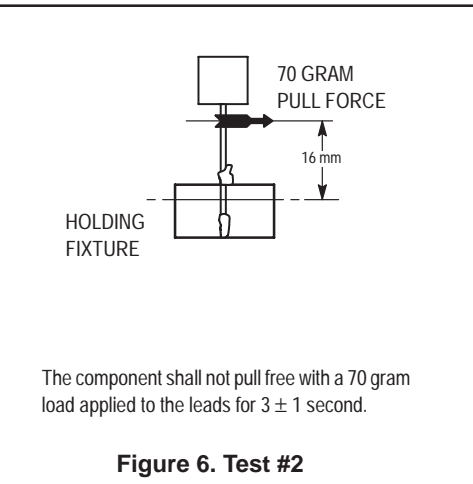
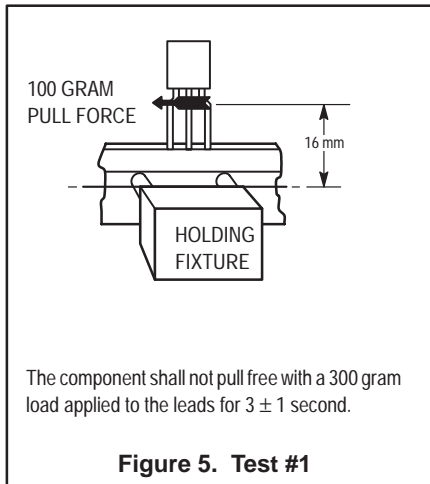
1. Maximum alignment deviation between leads not to be greater than 0.2 mm.
2. Defective components shall be clipped from the carrier tape such that the remaining protrusion (L) does not exceed a maximum of 11 mm.
3. Component lead to tape adhesion must meet the pull test requirements established in Figures 5, 6 and 7.
4. Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
5. Holddown tape not to extend beyond the edge(s) of carrier tape and there shall be no exposure of adhesive.
6. No more than 1 consecutive missing component is permitted.
7. A tape trailer and leader, having at least three feed holes is required before the first and after the last component.
8. Splices will not interfere with the sprocket feed holes.

TO-92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

FAN FOLD BOX STYLES

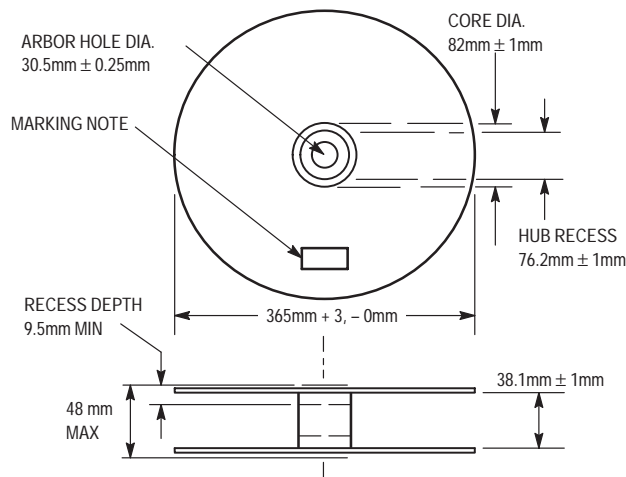


ADHESION PULL TESTS



TO-92 EIA RADIAL TAPE IN FAN FOLD BOX OR ON REEL

REEL STYLES



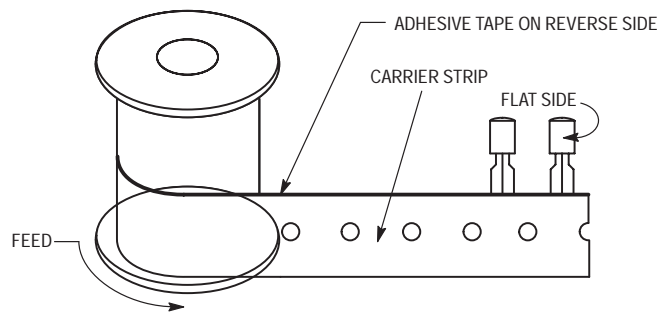
Material used must not cause deterioration of components or degrade lead solderability

Figure 8. Reel Specifications



Rounded side of transistor and adhesive tape visible.

Figure 9. Style A



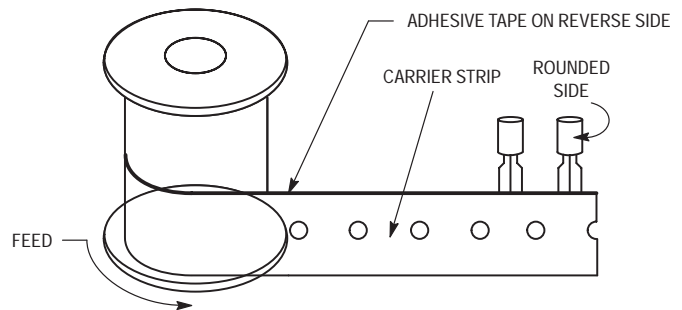
Flat side of transistor and carrier strip visible (adhesive tape on reverse side).

Figure 10. Style B



Flat side of transistor and adhesive tape visible.

Figure 11. Style E



Rounded side of transistor and carrier strip visible (adhesive tape on reverse side).

Figure 12. Style F

INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection inter-

face between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT-223 device, P_D is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{156^\circ\text{C/W}} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT-223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased.

Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 1.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

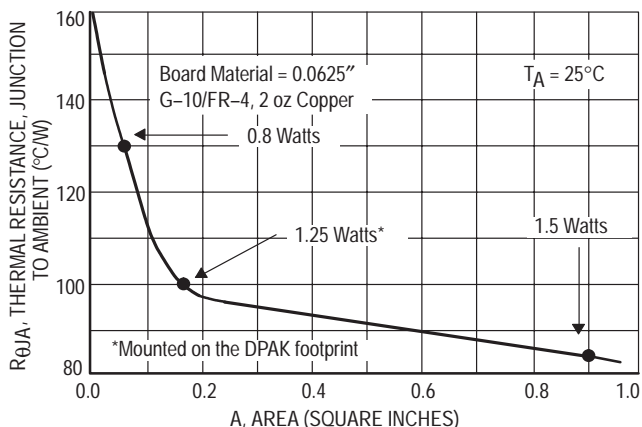


Figure 1. Thermal Resistance versus Drain Pad Area for the SOT-223 Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the

SOT-23, SC-59, SC-70/SOT-323, SC-90/SOT-416, SOD-123, SOT-223, SOT-363, SO-14, SO-16, and TSOP-6 packages, the stencil opening should be the same as the pad size or a 1:1 registration.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.

- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 2 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the

actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.



Figure 2. Typical Solder Heating Profile

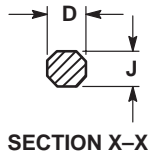
Footprints for Soldering





Package Outline Dimensions

Dimensions are in inches unless otherwise noted.

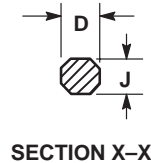
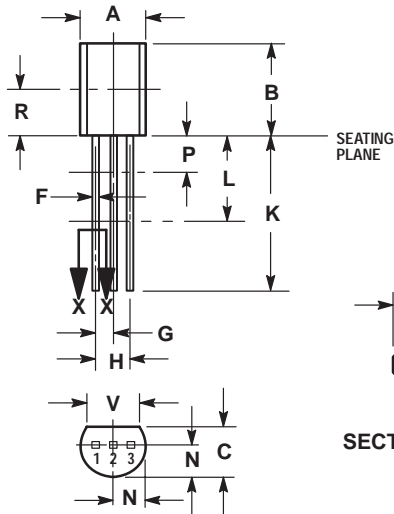


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
 4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.20 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.016 | 0.022 | 0.41 | 0.55 |
| F | 0.016 | 0.019 | 0.41 | 0.48 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.015 | 0.020 | 0.39 | 0.50 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.115 | --- | 2.93 | --- |
| V | 0.135 | --- | 3.43 | --- |

- | | | | | | |
|--|---|--|--|---|---|
| <p>STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR</p> | <p>STYLE 2: PIN 1. BASE 2. EMITTER 3. COLLECTOR</p> | <p>STYLE 3: PIN 1. ANODE 2. ANODE 3. CATHODE</p> | <p>STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE</p> | <p>STYLE 5: PIN 1. DRAIN 2. SOURCE 3. GATE</p> | <p>STYLE 7: PIN 1. SOURCE 2. DRAIN 3. GATE</p> |
| <p>STYLE 14: PIN 1. EMITTER 2. COLLECTOR 3. BASE</p> | <p>STYLE 15: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2</p> | <p>STYLE 17: PIN 1. COLLECTOR 2. BASE 3. EMITTER</p> | <p>STYLE 21: PIN 1. COLLECTOR 2. EMITTER 3. BASE</p> | <p>STYLE 22: PIN 1. SOURCE 2. GATE 3. DRAIN</p> | <p>STYLE 30: PIN 1. DRAIN 2. GATE 3. SOURCE</p> |

CASE 029-04 (TO-226AA) TO-92 PLASTIC



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
 4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.44 | 5.21 |
| B | 0.290 | 0.310 | 7.37 | 7.87 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.018 | 0.022 | 0.46 | 0.56 |
| F | 0.016 | 0.019 | 0.41 | 0.48 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.018 | 0.024 | 0.46 | 0.61 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.135 | --- | 3.43 | --- |
| V | 0.135 | --- | 3.43 | --- |

- | | | |
|---|--|---|
| <p>STYLE 1: PIN 1. EMITTER 2. BASE 3. COLLECTOR</p> | <p>STYLE 14: PIN 1. EMITTER 2. COLLECTOR 3. BASE</p> | <p>STYLE 22: PIN 1. SOURCE 2. GATE 3. DRAIN</p> |
|---|--|---|

CASE 029-05 (TO-226AE) TO-92 1-WATT PLASTIC

PACKAGE OUTLINE DIMENSIONS (continued)



NOTES:

1. PACKAGE CONTOUR OPTIONAL WITHIN DIA B AND LENGTH A. HEAT SLUGS, IF ANY, SHALL BE INCLUDED WITHIN THIS CYLINDER, BUT SHALL NOT BE SUBJECT TO THE MIN LIMIT OF DIA B.
2. LEAD DIA NOT CONTROLLED IN ZONES F, TO ALLOW FOR FLASH, LEAD FINISH BUILDUP, AND MINOR IRREGULARITIES OTHER THAN HEAT SLUGS.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 5.84 | 7.62 | 0.230 | 0.300 |
| B | 2.16 | 2.72 | 0.085 | 0.107 |
| D | 0.46 | 0.56 | 0.018 | 0.022 |
| F | --- | 1.27 | --- | 0.050 |
| K | 25.40 | 38.10 | 1.000 | 1.500 |

All JEDEC dimensions and notes apply.

**CASE 51-02
(DO-204AA)
DO-7**



SECTION X-X

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIM K MINIMUM.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.21 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.49 |
| D | 0.016 | 0.022 | 0.41 | 0.56 |
| F | 0.016 | 0.019 | 0.407 | 0.482 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.100 BSC | | 3.54 BSC | |
| J | 0.014 | 0.016 | 0.36 | 0.41 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.03 | 2.66 |
| P | --- | 0.050 | --- | 1.27 |
| R | 0.115 | --- | 2.93 | --- |
| V | 0.135 | --- | 3.43 | --- |

STYLE 1:
PIN 1. ANODE
2. CATHODE

**CASE 182-02
(T0-226AC) TO-92
PLASTIC**

PACKAGE OUTLINE DIMENSIONS (continued)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.1102 | 0.1197 | 2.80 | 3.04 |
| B | 0.0472 | 0.0551 | 1.20 | 1.40 |
| C | 0.0350 | 0.0440 | 0.89 | 1.11 |
| D | 0.0150 | 0.0200 | 0.37 | 0.50 |
| G | 0.0701 | 0.0807 | 1.78 | 2.04 |
| H | 0.0005 | 0.0040 | 0.013 | 0.100 |
| J | 0.0034 | 0.0070 | 0.085 | 0.177 |
| K | 0.0140 | 0.0285 | 0.35 | 0.69 |
| L | 0.0350 | 0.0401 | 0.89 | 1.02 |
| S | 0.0830 | 0.1039 | 2.10 | 2.64 |
| V | 0.0177 | 0.0236 | 0.45 | 0.60 |

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE

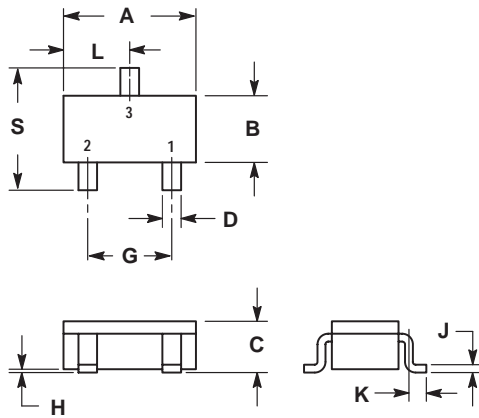
STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE-ANODE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

**CASE 318-08
(TO-236AB) SOT-23
PLASTIC**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|--------|
| | MIN | MAX | MIN | MAX |
| A | 2.70 | 3.10 | 0.1063 | 0.1220 |
| B | 1.30 | 1.70 | 0.0512 | 0.0669 |
| C | 1.00 | 1.30 | 0.0394 | 0.0511 |
| D | 0.35 | 0.50 | 0.0138 | 0.0196 |
| G | 1.70 | 2.10 | 0.0670 | 0.0826 |
| H | 0.013 | 0.100 | 0.0005 | 0.0040 |
| J | 0.09 | 0.18 | 0.0034 | 0.0070 |
| K | 0.20 | 0.60 | 0.0079 | 0.0236 |
| L | 1.25 | 1.65 | 0.0493 | 0.0649 |
| S | 2.50 | 3.00 | 0.0985 | 0.1181 |

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. N.C.
2. ANODE
3. CATHODE

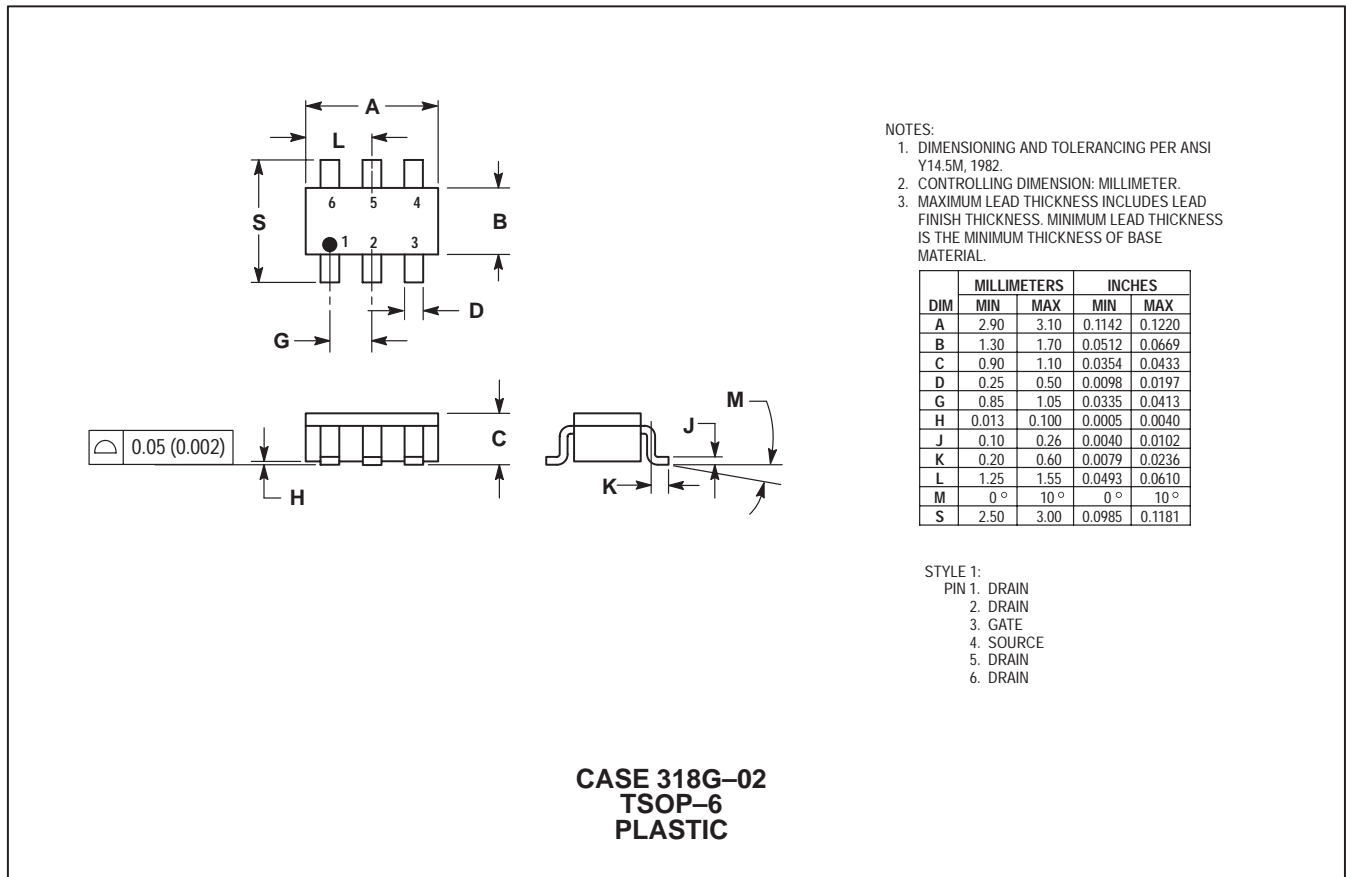
STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. N.C.
2. CATHODE
3. ANODE

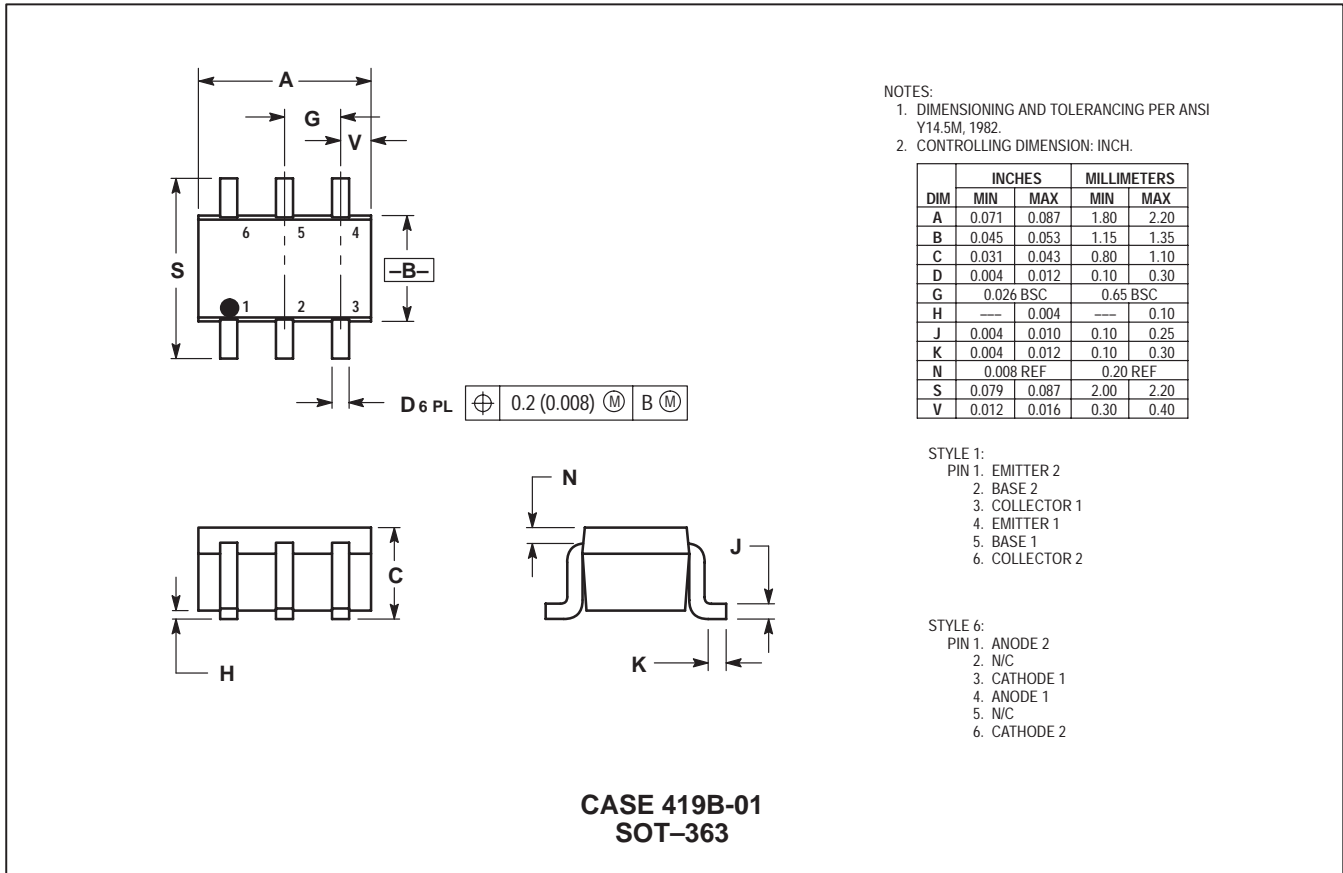
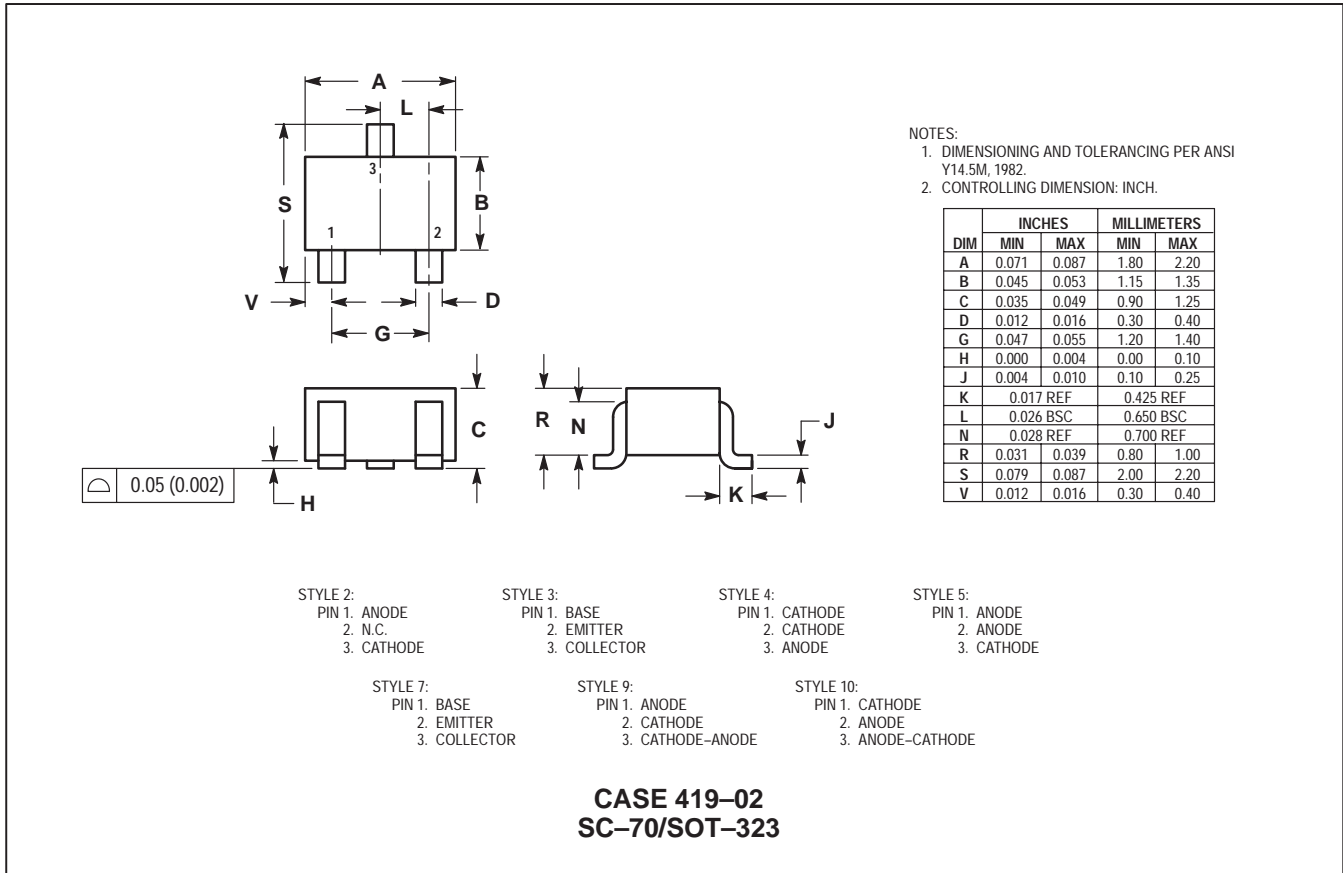
STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE

**CASE 318D-04
SC-59**

PACKAGE OUTLINE DIMENSIONS (continued)



PACKAGE OUTLINE DIMENSIONS (continued)



PACKAGE OUTLINE DIMENSIONS (continued)



PACKAGE OUTLINE DIMENSIONS (continued)

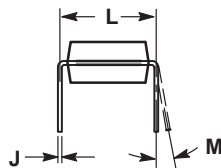
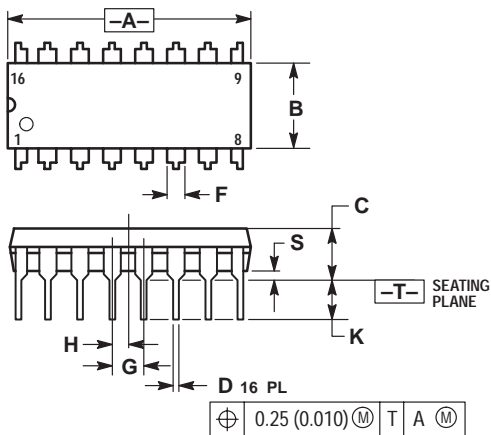


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | | 10° | |
| N | 0.015 | 0.039 | 0.39 | 1.01 |

CASE 646-06
14-PIN DIP
PLASTIC



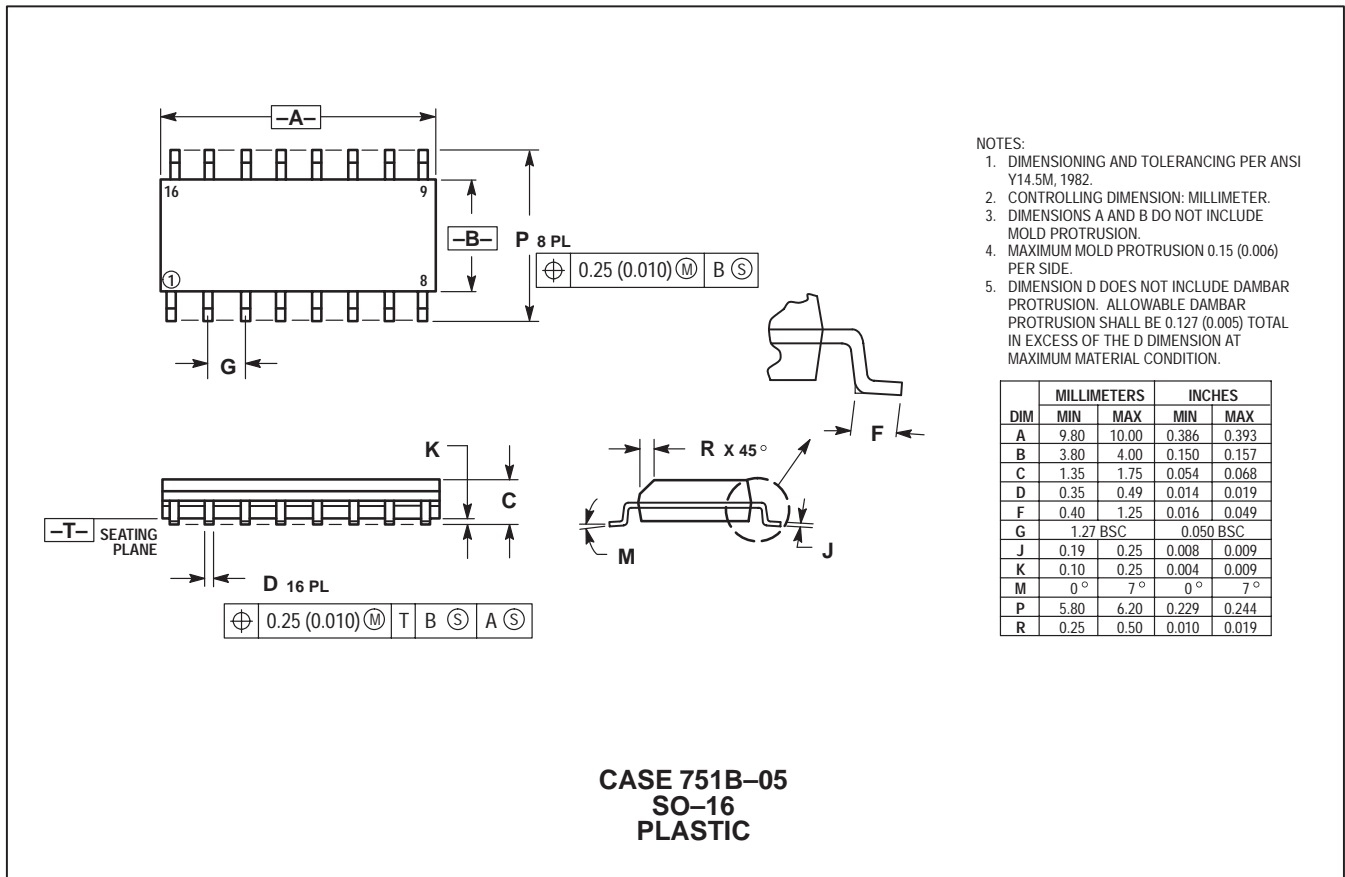
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | | 10° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

CASE 648-08
16-PIN DIP
PLASTIC

PACKAGE OUTLINE DIMENSIONS (continued)



OUTGOING QUALITY

The Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside the specification limits at the time of shipment. Motorola has established Six Sigma goals to improve its outgoing quality and will continue its "error free performance" focus to achieve its goal of zero parts per million (PPM) outgoing quality. Motorola's present quality level has led to vendor certification programs with many of its customers. These programs ensure a level of quality which allows the customer either to reduce or eliminate the need for incoming inspections.

AVERAGE OUTGOING QUALITY (AOQ) CALCULATION

$$AOQ = (\text{Process Average}) \bullet (\text{Probability of Acceptance}) \bullet (10^6) \text{ (PPM)}$$

- Process Average = $\frac{\text{Total Projected Reject Devices}}{\text{Total Number of Devices}}$
- Projected Reject Devices = $\frac{\text{Defects in Sample}}{\text{Sample Size}} \bullet \text{Lot Size}$
- Total Number of Devices = Sum of units in each submitted lot
- Probability of Acceptance = $1 \pm \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$
- 10^6 = Conversion to parts per million (PPM)

RELIABILITY DATA ANALYSIS

Reliability is the probability that a semiconductor device will perform its specified function in a given environment for a specified period. In other words, reliability is quality over time and environmental conditions. The most frequently used reliability measure for semiconductor devices is the failure rate (λ). The failure rate is obtained by dividing the number of failures observed by the product of the number of devices on test and the interval in hours, usually expressed as percent per thousand hours or failures per billion device hours (FITS). This is called a point estimate because it is obtained from observations on a portion (sample) of the population of devices.

To project from the sample to the population in general, one must establish confidence intervals. The application of confidence intervals is a statement of how "confident" one is that the sample failure rate approximates that for the population. To obtain failure rates at different confidence levels, it is necessary to make use of specific probability distributions. The chi-square (χ^2) distribution that relates observed and expected frequencies of an event is frequently used to establish confidence intervals. The relationship between failure rate and the chi-square distribution is as follows:

$$\lambda = \frac{\chi^2(\alpha, \text{d. f.})}{2t}$$

where:

- λ = failure rate
- χ^2 = chi-square function
- α = (100 – confidence level) / 100
- d.f. = degrees of freedom = $2r + 2$
- r = number of failures
- t = device hours

Chi-square values for 60% and 90% confidence intervals for up to 12 failures are shown in Table 1-1.

Table 1-1 – Chi-Square Table

| Chi-Square Distribution Function | | | |
|----------------------------------|-------------------|----------------------|-------------------|
| 60% Confidence Level | | 90% Confidence Level | |
| No. Fails | χ^2 Quantity | No. Fails | χ^2 Quantity |
| 0 | 1.833 | 0 | 4.605 |
| 1 | 4.045 | 1 | 7.779 |
| 2 | 6.211 | 2 | 10.645 |
| 3 | 8.351 | 3 | 13.362 |
| 4 | 10.473 | 4 | 15.987 |
| 5 | 12.584 | 5 | 18.549 |
| 6 | 14.685 | 6 | 21.064 |
| 7 | 16.780 | 7 | 23.542 |
| 8 | 18.868 | 8 | 25.989 |
| 9 | 20.951 | 9 | 28.412 |
| 10 | 23.031 | 10 | 30.813 |
| 11 | 25.106 | 11 | 33.196 |
| 12 | 27.179 | 12 | 35.563 |

The failure rate of semiconductor devices is inherently low. As a result, the industry uses a technique called accelerated testing to assess the reliability of semiconductors. During accelerated tests, elevated stresses are used to produce, in a short period, the same failure mechanisms as would be observed under normal use conditions. The objective of this testing is to identify these failure mechanisms and eliminate them as a cause of failure during the useful life of the product.

Temperature, relative humidity, and voltage are the most frequently used stresses during accelerated testing. Their relationship to failure rates has been shown to follow an Eyring type of equation of the form:

$$\lambda = A \exp(\phi/kT) \bullet \exp(B/RH) \bullet \exp(CE)$$

Where A, B, C, ϕ , and k are constants, more specifically B, C, and ϕ are numbers representing the apparent energy at which various failure mechanisms occur. These are called activation energies. "T" is the temperature, "RH" is the relative humidity, and "E" is the electric field. The most familiar form of this equation (shown on following page) deals with the first exponential term that shows an Arrhenius type relationship of the failure rate versus the junction temperature of semiconductors. The junction temperature is related to the ambient temperature through the thermal resistance and power dissipation. Thus, we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then by applying known acceleration factors, estimate the failure rates for lower junction.

The table on the following page shows observed activation energies with references.

**Table 1–2 – Time Dependent Failure Mechanisms in Semiconductor Devices
(Applicable to Discrete and Integrated Circuits)**

| Device Association | Process | Relevant Factors | Accelerating Factors | Typical Activation Energy in eV | Model | Reference |
|--|--|--------------------------------|----------------------|---|---------------------------------|-----------|
| Silicon Oxide Silicon–Silicon Oxide Interface | Surface Charges Inversion, Accumulation | Mobile Ions E/V, T | T, V | 1.0 | Fitch, et al. Peck | 1A 2 |
| | Oxide Pinholes | E/V, T | E, T | 0.7–1.0 (Bipolar) 1.0 (Bipolar) | 1984 WRS Hokari, et al. | 18 5 |
| | Dielectric Breakdown (TDDB) | E/V, T | E, T | 0.3–0.4 (MOS) 0.3 (MOS) | Domangue, et al. Crook, D.L. | 3 4 |
| | Charge Loss | E, T | E, T | 0.8 (MOS) EPROM | Gear, G. | 11 |
| Metallization | Electromigration | T, J | J, T | 1.0 Large grain Al (glassivated) | Nanda, et al. | 6 |
| | | Grain Size | | 0.5 Small grain Al | Black, J.R. | 7 |
| | | Doping | | 0.7 Cu–Al/Cu–Si–Al (sputtered) | Black, J.R. | 12 |
| | Corrosion Chemical Galvanic Electrolytic | Contamination | H, E/V, T | 0.6–0.7 (for electrolysis) E/V may have thresholds | Lycoudes, N.E. | 8 |
| Bond and Other Mechanical Interfaces | Intermetallic Growth | T, Impurities Bond Strength | T | 1.0 (Au/Al) | Fitch, W.T | 9 |
| Various Water Fab, Assembly, and Silicon Defects | Metal Scratches Mask Defects, etc. Silicon Defects | T, V | T, V | 0.5–0.7 eV | Howes, et al. | 10 |
| | | | | 0.5 eV | MMPD | 13 |

V = voltage; E = electric field; T = temperature; J = current density; H = humidity

NO. REFERENCE

| | |
|---|--|
| <p>1A 1.0 eV activation for leakage type failures. Fitch, W.T.; Greer, P.; Lycoudes, N.; "Data to Support 0.001%/1000 Hours for Plastic I/C's." Case study on linear product shows 0.914 eV activation energy which is within experimental error of 0.9 to 1.3 eV activation energies for reversible leakage (inversion) failures reported in the literature.</p> <p>1B 0.7 To 1.0 eV for oxide defect failures for bipolar structures. This is under investigation subsequent to information obtained from 1984 Wafer Reliability Symposium, especially for bipolar capacitors with silicon nitride as dielectric.</p> <p>2 1.0 eV activation for leakage type failures. Peck, D.S.; "New Concerns About Integrated Circuit Reliability" 1978 Reliability Physics Symposium.</p> <p>3 0.36 eV for dielectric breakdown for MOS gate structures. Domangue, E.; Rivera, R.; Shedard, C.; "Reliability Prediction Using Large MOS Capacitors", 1984 Reliability Physics Symposium.</p> <p>4 0.3 eV for dielectric breakdown. Crook, D.L.; "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", 1979 Reliability Physics Symposium.</p> <p>5 1.0 eV for dielectric breakdown. Hokari, Y.; et al.; IEDM Technical Digest, 1982.</p> | <p>6 1.0 eV for large grain Al–Si (compared to line width). Nanda, Vangard, GJ–P; Black, J.R.; "Electromigration of Al–Si Alloy Films", 1978 Reliability Physics Symposium.</p> <p>7 0.5 eV Al, 0.7 eV Cu–Al small grain (compared to line width). Black, J.R.; "Current Limitation of Thin Film Conductor" 1982 Reliability Physics Symposium.</p> <p>8 0.65 eV for corrosion mechanism. Lycoudes, N.E.; "The Reliability of Plastic Microcircuits in Moist Environments", 1978 Solid State Technology.</p> <p>9 1.0 eV for open wires or high resistance bonds at the pad bond due to Au–Al intermetallics. Fitch, W.T.; "Operating Life vs Junction Temperatures for Plastic Encapsulated I/C (1.5 mil Au wire)", unpublished report.</p> <p>10 0.7 eV for assembly related defects. Howes, M.G.; Morgan, D.V.; "Reliability and Degradation, Semiconductor Devices and Circuits" John Wiley and Sons, 1981.</p> <p>11 Gear, G.; "FAMOUS PROM Reliability Studies", 1976 Reliability Physics Symposium.</p> <p>12 Black, J.R.: unpublished report.</p> <p>13 Motorola Memory Products Division; unpublished report.</p> |
|---|--|

THERMAL RESISTANCE

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the junction temperatures low.

Electrical power dissipated in any semiconductor device is a source of heat. This heat source increases the temperature of the die about some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction depends on the packaging and mounting system's ability to remove heat generated in the circuit from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D \theta_{JA} \quad (2)$$

where:

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation, including effects of external loads when applicable

θ_{JC} = average thermal resistance, junction to case

θ_{CA} = average thermal resistance, case to ambient

θ_{JA} = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 devices.

Only two terms on the right side of equation (1) can be varied by the user, the ambient temperature and the device case-to-ambient thermal resistance, θ_{CA} . (To some extent the device power dissipation can also be controlled, but under recommended use the supply voltage and loading dictate a

fixed power dissipation.) Both system air flow and the package mounting technique affect the θ_{CA} thermal resistance term. θ_{JC} is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D \theta_{JC} \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

AIR FLOW

Air flow over the packages (due to a decrease in θ_{JC}) reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

For thermal resistance values for specific packages, see the Motorola Data Book or Design Manual for the appropriate device family or contact your local Motorola sales office.

ACTIVATION ENERGY

Determination of activation energies is accomplished by testing randomly selected samples from the same population at various stress levels and comparing failure rates due to the same failure mechanism. The activation energy is represented by the slope of the curve relating to the natural logarithm of the failure rate to the various stress levels.

In calculating failure rates, the comprehensive method is to use the specific activation energy for each failure mechanism applicable to the technology and circuit under consideration. A common alternative method is to use a single activation energy value for the "expected" failure mechanism(s) with the lowest activation energy.

RELIABILITY STRESS TESTS

The following are brief descriptions of the reliability tests commonly used in the reliability monitoring program. Not all of the tests listed are performed by each product division. Other tests may be performed when appropriate.

AUTOCLAVE (aka, PRESSURE COOKER)

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effect of galvanic corrosion. Autoclave is a highly accelerated and destructive test.

Typical Test Conditions: $T_A = 121^\circ\text{C}$, $\text{rh} = 100\%$, $p = 1$ atmosphere (15 psig), $t = 24$ to 96 hours

Common Failure Modes: Parametric shifts, high leakage and/or catastrophic

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing.

HIGH HUMIDITY HIGH TEMPERATURE BIAS (H3TB, H3TRB, or THB)

This is an environmental test designed to measure the moisture resistance of plastic encapsulated devices. A bias is applied to create an electrolytic cell necessary to accelerate corrosion of the die metallization. With time, this is a catastrophically destructive test.

Typical Test Conditions: $T_A = 85^\circ\text{C}$ to 95°C , $\text{rh} = 85\%$ to 95% , Bias = 80% to 100% of Data Book max. rating, $t = 96$ to 1750 hours

Common Failure Modes: Parametric shifts, high leakage and/or catastrophic

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing.

HIGH TEMPERATURE GATE BIAS (HTGB)

This test is designed to electrically stress the gate oxide under a bias condition at high temperature.

Typical Test Conditions: $T_A = 150^\circ\text{C}$, Bias = 80% of Data Book max. rating, $t = 120$ to 1000 hours

Common Failure Modes: Parametric shifts in gate leakage and gate threshold voltage

Common Failure Mechanisms: Random oxide defects and ionic contamination

Military Reference: MIL-STD-750, Method 1042

HIGH TEMPERATURE REVERSE BIAS (HTRB)

The purpose of this test is to align mobile ions by means of temperature and voltage stress to form a high-current leakage path between two or more junctions.

Typical Test Conditions: $T_A = 85^\circ\text{C}$ to 150°C , Bias = 80% to 100% of Data Book max. rating, $t = 120$ to 1000 hours

Common Failure Modes: Parametric shifts in leakage and gain

Common Failure Mechanisms: Ionic contamination on the surface or under the metallization of the die

Military Reference: MIL-STD-750, Method 1039

HIGH TEMPERATURE STORAGE LIFE (HTSL)

High temperature storage life testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures

Typical Test Conditions: $T_A = 70^\circ\text{C}$ to 200°C , no bias, $t = 24$ to 2500 hours

Common Failure Modes: Parametric shifts in leakage and gain

Common Failure Mechanisms: Bulk die and diffusion defects

Military Reference: MIL-STD-750, Method 1032

INTERMITTENT OPERATING LIFE (IOL)

The purpose of this test is the same as SSOL in addition to checking the integrity of both wire and die bonds by means of thermal stressing

Typical Test Conditions: $T_A = 25^\circ\text{C}$, $P_d =$ Data Book maximum rating, $T_{\text{ON}} = T_{\text{OFF}} = \Delta$ of 50°C to 100°C , $t = 42$ to 30000 cycles

Common Failure Modes: Parametric shifts and catastrophic

Common Failure Mechanisms: Foreign material, crack and bulk die defects, metallization, wire and die bond defects

Military Reference: MIL-STD-750, Method 1037

MECHANICAL SHOCK

This test is used to determine the ability of the device to withstand a sudden change in mechanical stress due to abrupt changes in motion as seen in handling, transportation, or actual use.

Typical Test Conditions: Acceleration = 1500 g's, Orientation = X_1, Y_1, Y_2 plane, $t = 0.5$ msec, Blows = 5

Common Failure Modes: Open, short, excessive leakage, mechanical failure

Common Failure Mechanisms: Die and wire bonds, cracked die, package defects

Military Reference: MIL-STD-750, Method 2015

MOISTURE RESISTANCE

The purpose of this test is to evaluate the moisture resistance of components under temperature/humidity conditions typical of tropical environments.

Typical Test Conditions: $T_A = -10^\circ\text{C}$ to 65°C , $rh = 80\%$ to 98% , $t = 24$ hours/cycles, cycle = 10

Common Failure Modes: Parametric shifts in leakage and mechanical failure

Common Failure Mechanisms: Corrosion or contaminants on or within the package materials. Poor package sealing

Military Reference: MIL-STD-750, Method 1021

SOLDERABILITY

The purpose of this test is to measure the ability of the device leads/terminals to be soldered after an extended period of storage (shelf life).

Typical Test Conditions: Steam aging = 8 hours, Flux = R, Solder = Sn60, Sn63

Common Failure Modes: Pin holes, dewetting, nonwetting

Common Failure Mechanisms: Poor plating, contaminated leads

Military Reference: MIL-STD-750, Method 2026

SOLDER HEAT

This test is used to measure the ability of a device to withstand the temperatures as may be seen in wave soldering operations. Electrical testing is the endpoint criterion for this stress.

Typical Test Conditions: Solder Temperature = 260°C , $t = 10$ seconds

Common Failure Modes: Parameter shifts, mechanical failure

Common Failure Mechanisms: Poor package design

Military Reference: MIL-STD-750, Method 2031

STEADY STATE OPERATING LIFE (SSOL)

The purpose of this test is to evaluate the bulk stability of the die and to generate defects resulting from manufacturing aberrations that are manifested as time and stress-dependent failures.

Typical Test Conditions: $T_A = 25^\circ\text{C}$, $P_D =$ Data Book maximum rating, $t = 16$ to 1000 hours

Common Failure Modes: Parametric shifts and catastrophic

Common Failure Mechanisms: Foreign material, crack die, bulk die, metallization, wire and die bond defects

Military Reference: MIL-STD-750, Method 1026

TEMPERATURE CYCLING (AIR TO AIR)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and transitions between temperature extremes. This testing will also expose excessive thermal mismatch between materials.

Typical Test Conditions: $T_A = -65^\circ\text{C}$ to 200°C , cycle = 10 to 4000

Common Failure Modes: Parametric shifts and catastrophic

Common Failure Mechanisms: Wire bond, cracked or lifted die and package failure

Military Reference: MIL-STD-750, Method 1051

THERMAL SHOCK (LIQUID TO LIQUID)

The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and sudden transitions between temperature extremes. This testing will also expose excessive thermal mismatch between materials.

Typical Test Conditions: $T_A = 0^\circ\text{C}$ to 100°C , cycle = 20 to 300

Common Failure Modes: Parametric shifts and catastrophic

Common Failure Mechanisms: Wire bond, cracked or lifted die and package failure

Military Reference: MIL-STD-750, Method 1056

VARIABLE FREQUENCY VIBRATION

This test is used to examine the ability of the device to withstand deterioration due to mechanical resonance.

Typical Test Conditions: Peak acceleration = 20 g's, Frequency range = 20 Hz to KHz, $t = 48$ minutes

Common Failure Modes: Open, short, excessive leakage, mechanical failure

Common Failure Mechanisms: Die and wire bonds, cracked die, package defects

Military Reference: MIL-STD-750, Method 2056

STATISTICAL PROCESS CONTROL

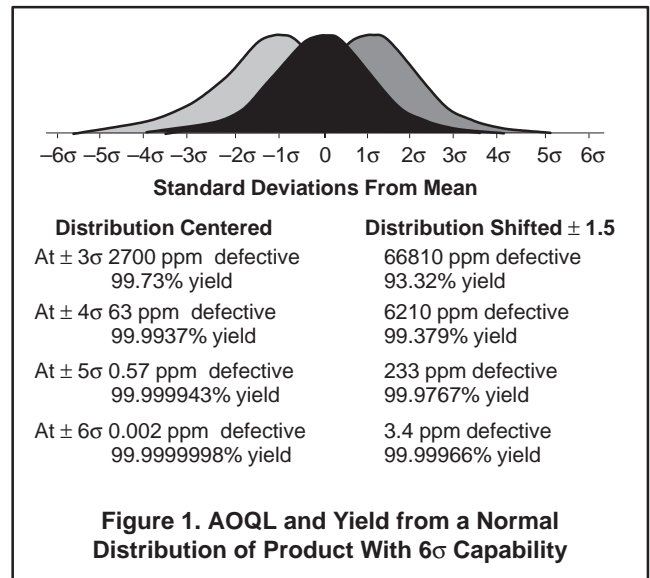
Communication Power & Signal Technologies Group (CPSTG) is continually pursuing new ways to improve product quality. Initial design improvement is one method that can be used to produce a superior product. Equally important to outgoing product quality is the ability to produce product that consistently conforms to specification. Process variability is the basic enemy of semiconductor manufacturing since it leads to product variability. Used in all phases of Motorola's product manufacturing, STATISTICAL PROCESS CONTROL (SPC) replaces variability with predictability. The traditional philosophy in the semiconductor industry has been adherence to the data sheet specification. Using SPC methods ensures that the product will meet specific process requirements throughout the manufacturing cycle. The emphasis is on defect prevention, not detection. Predictability through SPC methods requires the manufacturing culture to focus on constant and permanent improvements. Usually, these improvements cannot be bought with state-of-the-art equipment or automated factories. With quality in design, process, and material selection, coupled with manufacturing predictability, Motorola can produce world class products.

The immediate effect of SPC manufacturing is predictability through process controls. Product centered and distributed well within the product specification benefits Motorola with fewer rejects, improved yields, and lower cost. The direct benefit to Motorola's customers includes better incoming quality levels, less inspection time, and ship-to-stock capability. Circuit performance is often dependent on the cumulative effect of component variability. Tightly controlled component distributions give the customer greater circuit predictability. Many customers are also converting to just-in-time (JIT) delivery programs. These programs require improvements in cycle time and yield predictability achievable only through SPC techniques. The benefit derived from SPC helps the manufacturer meet the customer's expectations of higher quality and lower cost product.

Ultimately, Motorola will have Six Sigma capability on all products. This means parametric distributions will be centered within the specification limits, with a product distribution of plus or minus Six Sigma about mean. Six Sigma capability, shown graphically in Figure 1, details the benefit in terms of yield and outgoing quality levels. This compares a centered distribution versus a 1.5 sigma worst case distribution shift.

New product development at Motorola requires more robust design features that make them less sensitive to minor variations in processing. These features make the implementation of SPC much easier.

A complete commitment to SPC is present throughout Motorola. All managers, engineers, production operators, supervisors, and maintenance personnel have received multiple training courses on SPC techniques. Manufacturing has identified 22 wafer processing and 8 assembly steps considered critical to the processing of semiconductor products. Processes controlled by SPC methods that have shown significant improvement are in the diffusion, photolithography, and metallization areas.



To better understand SPC principles, brief explanations have been provided. These cover process capability, implementation, and use.

PROCESS CAPABILITY

One goal of SPC is to ensure a process is **CAPABLE**. Process capability is the measurement of a process to produce products consistently to specification requirements. The purpose of a process capability study is to separate the inherent **RANDOM VARIABILITY** from **ASSIGNABLE CAUSES**. Once completed, steps are taken to identify and eliminate the most significant assignable causes. Random variability is generally present in the system and does not fluctuate. Sometimes, the random variability is due to basic limitations associated with the machinery, materials, personnel skills, or manufacturing methods. Assignable cause inconsistencies relate to time variations in yield, performance, or reliability.

Traditionally, assignable causes appear to be random due to the lack of close examination or analysis. Figure 2 shows the impact on predictability that assignable cause can have. Figure 3 shows the difference between process control and process capability.

A process capability study involves taking periodic samples from the process under controlled conditions. The performance characteristics of these samples are charted against time. In time, assignable causes can be identified and engineered out. Careful documentation of the process is the key to accurate diagnosis and successful removal of the assignable causes. Sometimes, the assignable causes will remain unclear, requiring prolonged experimentation.

Elements which measure process variation control and capability are C_p and C_{pk} , respectively. C_p is the specification width divided by the process width or $C_p = (\text{specification width}) / 6\sigma$. C_{pk} is the absolute value of the closest specification value to the mean, minus the mean, divided by half the process width or $C_{pk} = |\text{closest specification} - \bar{x}| / 3\sigma$.

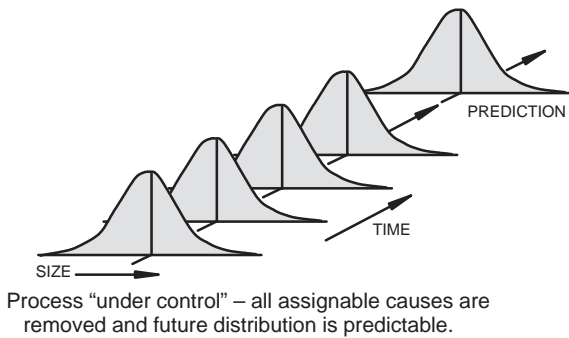


Figure 2. Impact of Assignable Causes on Process Predictable

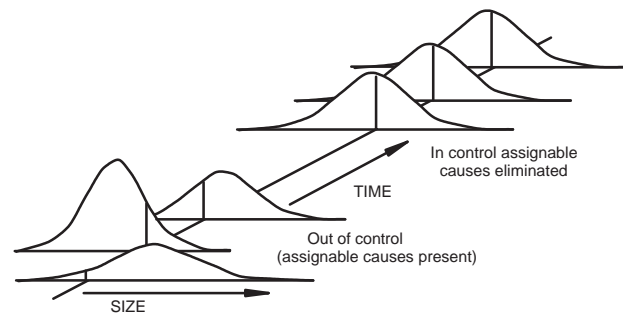


Figure 3. Difference Between Process Control and Process Capability

At Motorola, for critical parameters, the process capability is acceptable with a $Cpk = 1.50$ with continual improvement our goal. The desired process capability is a $Cpk = 2$ and the ideal is a $Cpk = 5$. Cpk , by definition, shows where the current production process fits with relationship to the specification limits. Off center distributions or excessive process variability will result in less than optimum conditions.

SPC IMPLEMENTATION AND USE

CPSTG uses many parameters that show conformance to specification. Some parameters are sensitive to process variations while others remain constant for a given product line. Often, specific parameters are influenced when changes to other parameters occur. It is both impractical and unnecessary to monitor all parameters using SPC methods. Only critical parameters that are sensitive to process variability are chosen for SPC monitoring. The process steps affecting these critical parameters must be identified as well. It is equally important to find a measurement in these process steps that correlates with product performance. This measurement is called a critical process parameter.

Once the critical process parameters are selected, a sample plan must be determined. The samples used for measurement are organized into **RATIONAL SUBGROUPS** of approximately two to five pieces. The subgroup size should be such that variation among the samples within the subgroup remain small. All samples must come from the same source e.g., the same mold press operator, etc. Subgroup data should

be collected at appropriate time intervals to detect variations in the process. As the process begins to show improved stability, the interval may be increased. The data collected must be carefully documented and maintained for later correlation. Examples of common documentation entries are operator, machine, time, settings, product type, etc.

Once the plan is established, data collection may begin. The data collected will generate \bar{X} and R values that are plotted with respect to time. \bar{X} refers to the mean of the values within a given subgroup, while R is the range or greatest value minus least value. When approximately 20 or more \bar{X} and R values have been generated, the average of these values is computed as follows:

$$\bar{\bar{X}} = (\bar{X}_1 + \bar{X}_2 + \bar{X}_3 + \dots) / K$$

$$\bar{R} = (R_1 + R_2 + R_3 + \dots) / K$$

where K = the number of subgroups measured.

The values of \bar{X} and R are used to create the process control chart. Control charts are the primary SPC tool used to signal a problem. Shown in Figure 4, process control charts show \bar{X} and R values with respect to time and concerning reference to upper and lower control limit values. Control limits are computed as follows:

$$R \text{ upper control limit} = UCLR = D_4 \bar{R}$$

$$R \text{ lower control limit} = LCLR = D_3 \bar{R}$$

$$\bar{X} \text{ upper control limit} = UCL\bar{X} = \bar{\bar{X}} + A_2 \bar{R}$$

$$\bar{X} \text{ lower control limit} = LCL\bar{X} = \bar{\bar{X}} - A_2 \bar{R}$$

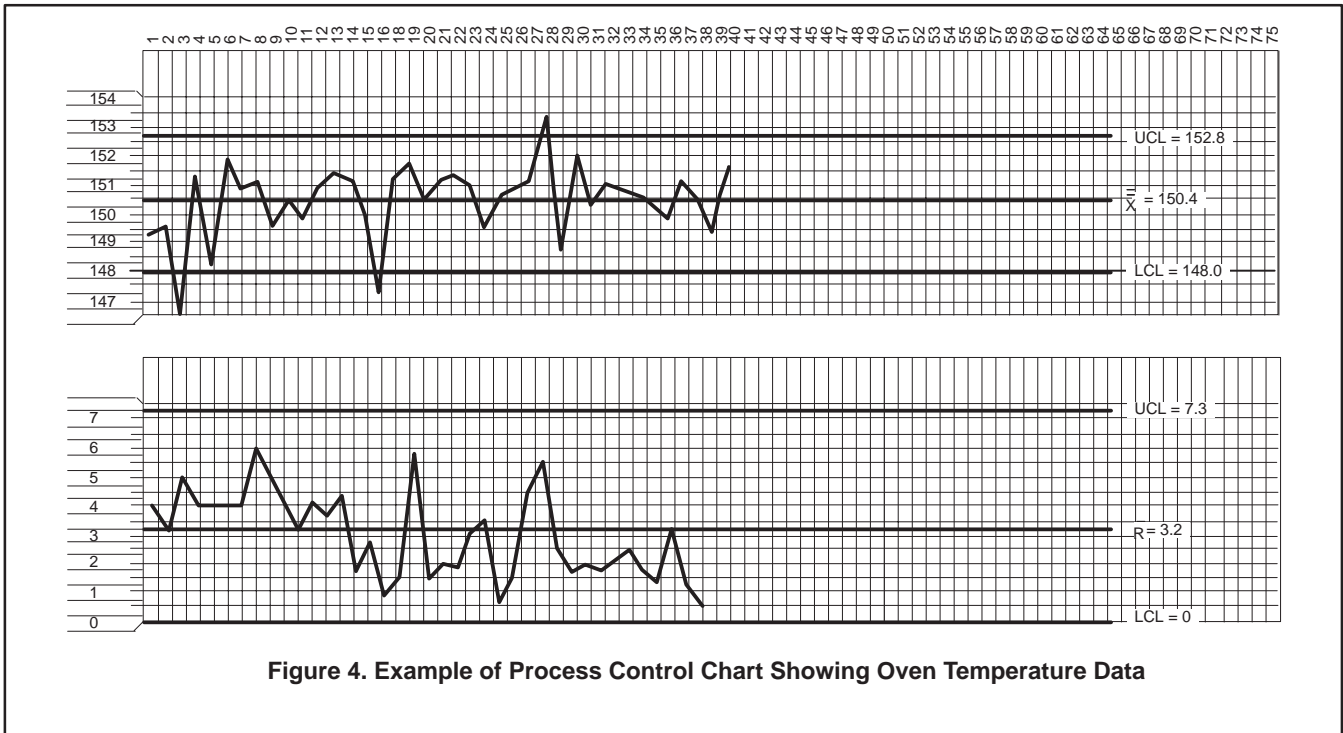


Figure 4. Example of Process Control Chart Showing Oven Temperature Data

Where D_4 , D_3 , and A_2 are constants varying by sample size, with values for sample sizes from 2 to 10 shown in the following partial table:

| n | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|-------|------|------|------|------|------|------|------|------|------|
| D_4 | 3.27 | 2.57 | 2.28 | 2.11 | 2.00 | 1.92 | 1.86 | 1.82 | 1.78 |
| D_3 | * | * | * | * | * | 0.08 | 0.14 | 0.18 | 0.22 |
| A_2 | 1.88 | 1.02 | 0.73 | 0.58 | 0.48 | 0.42 | 0.37 | 0.34 | 0.31 |

*For sample sizes below 7, the LCL_R would technically be a negative number; in those cases there is no lower control limit; this means that for a subgroup size 6, six "identical" measurements would not be unreasonable.

Control charts are used to monitor the variability of critical process parameters. The R chart shows basic problems with piece to piece variability related to the process. The X chart can often identify changes in people, machines, methods, etc. The source of the variability can be difficult to find and may require experimental design techniques to identify assignable causes.

Some general rules have been established to help determine when a process is **OUT-OF-CONTROL**. Figure 5 shows a control chart subdivided into zones A, B, and C corresponding to 3 sigma, 2 sigma, and 1 sigma limits respectively. In Figures 6 through 9 four of the tests that can be used to identify excessive variability and the presence of assignable causes are shown. As familiarity with a given process increases, more subtle tests may be employed successfully.

Once the variability is identified, the cause of the variability must be determined. Normally, only a few factors have a significant impact on the total variability of the process. The importance of correctly identifying these factors is stressed in the following example. Suppose a process variability depends on the variance of five factors A, B, C, D, and E. Each has a variance of 5, 3, 2, 1, and 0.4, respectively.

Since:

$$\sigma_{tot} = \sqrt{\sigma_A^2 + \sigma_B^2 + \sigma_C^2 + \sigma_D^2 + \sigma_E^2}$$

$$\sigma_{tot} = \sqrt{5^2 + 3^2 + 2^2 + 1^2 + (0.4)^2} = 6.3$$

If only D is identified and eliminated, then:

$$\sigma_{tot} = \sqrt{5^2 + 3^2 + 2^2 + (0.4)^2} = 6.2$$

This results in less than 2% total variability improvement. If B, C, and D were eliminated, then:

$$\sigma_{tot} = \sqrt{5^2 + (0.4)^2} = 5.02$$

This gives a considerably better improvement of 23%. If only A is identified and reduced from 5 to 2, then:

$$\sigma_{tot} = \sqrt{2^2 + 3^2 + 2^2 + 1^2 + (0.4)^2} = 4.3$$

Identifying and improving the variability from 5 to 2 yields a total variability improvement of nearly 40%.

Most techniques may be employed to identify the primary assignable cause(s). Out-of-control conditions may be correlated to documented process changes. The product may be analyzed in detail using best versus worst part comparisons or Product Analysis Lab equipment. Multi-variance analysis can be used to determine the family of variation (positional, critical, or temporal). Lastly, experiments may be run to test theoretical or factorial analysis. Whatever method is used, assignable causes must be identified and eliminated in the most expeditious manner possible.

After assignable causes have been eliminated, new control limits are calculated to provide a more challenging variability criteria for the process. As yields and variability improve, it may become more difficult to detect improvements because they become much smaller. When all assignable causes have been eliminated and the points remain within control limits for 25 groups, the process is said to be in a state of control.

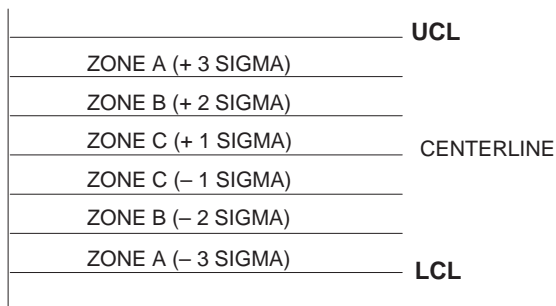


Figure 5. Control Chart Zones

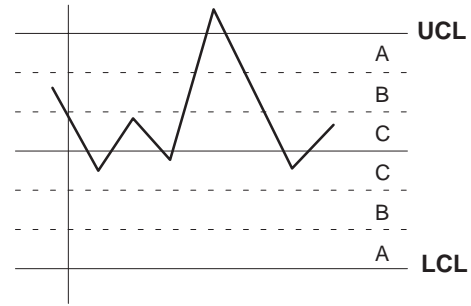


Figure 6. One Point Outside Control Limit Indicating Excessive Variability

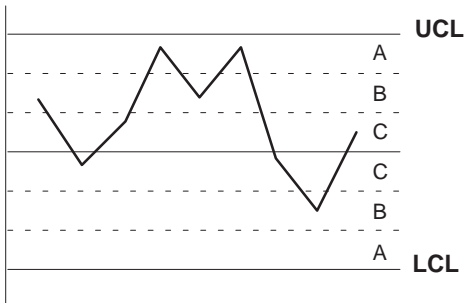


Figure 7. Two Out of Three Points in Zone A or Beyond Indicating Excessive Variability

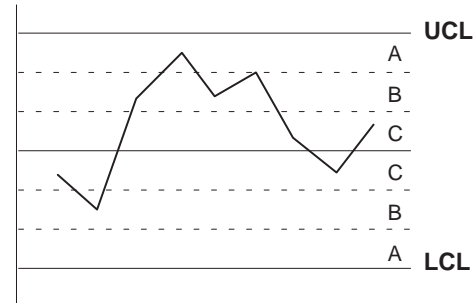


Figure 8. Four Out of Five Points in Zone B or Beyond Indicating Excessive Variability

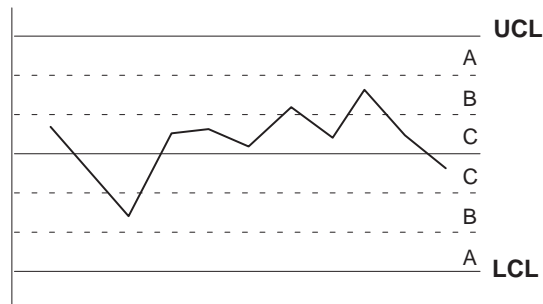


Figure 9. Seven Out of Eight Points in Zone C or Beyond Indicating Excessive Variability

SUMMARY

Motorola is committed to the use of STATISTICAL PROCESS CONTROLS. These principles, used throughout manufacturing have already resulted in many significant improvements to the processes. Continued dedication to the

SPC culture will allow Motorola to reach the Six Sigma and zero defect capability goals. SPC will further enhance the commitment to **TOTAL CUSTOMER SATISFACTION**.

REPLACEMENT DEVICES

| DEVICE | REPLACEMENT | DEVICE | REPLACEMENT | DEVICE | REPLACEMENT |
|---------|-------------|----------|-------------|-----------|-------------|
| 1N5139 | MV2101 | 2N3053A | MPSA05 | BC560B | BC560C |
| 1N5139A | MV2101 | 2N3244 | 2N4403 | BC849ALT1 | BC848ALT1 |
| 1N5140 | MMBV2103LT1 | 2N3250 | 2N4403 | BC850ALT1 | BC848ALT1 |
| 1N5140A | MMBV2103LT1 | 2N3251 | MPS2907A | BC857CLT1 | BC857ALT1 |
| 1N5141 | MMBV2104LT1 | 2N3251A | MPS2907A | BCY70 | MPS2222A |
| 1N5141A | MMBV2104LT1 | 2N3467 | MPSA56 | BCY71 | MPS2222A |
| 1N5142 | MMBV2105LT1 | 2N3468 | MPSA56 | BCY72 | MPS2222A |
| 1N5142A | MMBV2105LT1 | 2N3497 | 2N5401 | BDB01D | BDB01C |
| 1N5143 | MMBV2105LT1 | 2N3500 | 2N5551 | BDB02D | BDB02C |
| 1N5143A | MMBV2105LT1 | 2N3501 | 2N5551 | BDC02D | BDC01D |
| 1N5144 | MMBV2107LT1 | 2N3546 | MPSH17 | BDC05 | MPSW42 |
| 1N5144A | MMBV2107LT1 | 2N3634 | 2N5401 | BF244A | 2N3819 |
| 1N5145 | MMBV2108LT1 | 2N3635 | 2N5401 | BF244B | 2N3819 |
| 1N5145A | MMBV2108LT1 | 2N3636 | MPSA92 | BF245 | BF245A |
| 1N5146 | MMBV2109LT1 | 2N3637 | MPSA92 | BF245A | BF245A |
| 1N5146A | MV2109 | 2N3700 | MPSA06 | BF245B | BF245A |
| 1N5147 | MV2111 | 2N3799 | MPSA18 | BF245C | BF245A |
| 1N5147A | MV2111 | 2N3947 | MPS2222A | BF246A | BF245A |
| 1N5441A | MV2101 | 2N3963 | MPSA18 | BF246B | BF245A |
| 1N5443A | MV2103 | 2N3964 | MPSA18 | BF247B | BF245A |
| 1N5444A | MV2104 | 2N4014 | MPS2222A | BF256B | BF256A |
| 1N5445A | MV2105 | 2N4032 | MPS2907A | BF256C | BF256A |
| 1N5449A | MV2108 | 2N4033 | MPSA56 | BF258 | BF422 |
| 1N5450A | MV2109 | 2N4036 | MPSA56 | BF374 | BC338 |
| 1N5451A | MV2111 | 2N4037 | MPSA56 | BF391 | MPSA42 |
| 1N5452A | MV2111 | 2N4126 | MPS4126 | BF392 | MPSA42 |
| 1N5453A | MV2111 | 2N4265 | 2N4264 | BF492 | MPSA92 |
| 1N5455A | MV2115 | 2N4405 | MPS8599 | BF493 | MPSA92 |
| 2N697 | MPSA20 | 2N4407 | MPS8599 | BFW43 | 2N5401 |
| 2N718A | MPSA05 | 2N4931 | MPSA92 | BSP20AT1 | BF720T1 |
| 2N720A | MPSA06 | 2N5086 | 2N5087 | BSS71 | MPSA42 |
| 2N930 | MPSA18 | 2N5668 | 2N3819 | BSS72 | MPSA42 |
| 2N930A | MPSA18 | 2N5669 | 2N3819 | BSS73 | MPSA42 |
| 2N956 | MPSA05 | 2N5670 | 2N3819 | BSS74 | MPSA92 |
| 2N1613 | 2N4410 | 2N6431 | MPSA42 | BSS75 | MPSA92 |
| 2N1711 | MPSA05 | 2N6433 | MPSA92 | BSS76 | MPSA92 |
| 2N1893 | MPSA06 | 2N6516 | 2N6517 | BSS89 | BS107 |
| 2N2102 | 2N4410 | BA582T1 | MMBV3401LT1 | BSV16-10 | MPS2907A |
| 2N2218A | MPS2222A | BC107 | BC237 | BSX20 | MPS2369A |
| 2N2219 | MPS2222A | BC107A | BC237 | CV12253 | MPSA06 |
| 2N2219A | MPS2222A | BC107B | BC237 | IRFD110 | BSS123LT1 |
| 2N2222 | MPS2222 | BC108 | | IRFD113 | MMBF170LT1 |
| 2N2222A | MPS2222A | BC109C | BC3338 | IRFD120 | BSS123LT1 |
| 2N2270 | MPSA05 | BC140-10 | MPSW06 | IRFD123 | MMBF170LT1 |
| 2N2369 | MPS2369 | BC140-16 | MPSW06 | IRFD210 | MMFT107T1 |
| 2N2369A | MPS2369A | BC141-10 | MPSW06 | IRFD213 | MMFT107T1 |
| 2N2484 | 2N5087 | BC141-16 | MPSW06 | IRFD220 | MMFT107T1 |
| 2N2895 | MPSA06 | BC160-16 | MPSW56 | IRFD223 | MMFT107T1 |
| 2N2896 | 2N5551 | BC161-16 | MPSW56 | IRFD9120 | BSS123LT1 |
| 2N2904 | MPS2907 | BC177 | BC547 | IRFD9123 | 2N7002LT1 |
| 2N2904A | MPS2907A | BC177A | BC547A | J111 | J111RLRA |
| 2N2905 | MPS2907 | BC177B | BC547B | J113 | J113RL1 |
| 2N2905A | MPS2907A | BC238 | BC238B | J203 | 2N5458 |
| 2N2906 | MPS2907 | BC309B | BC308C | J300 | 2N5486 |
| 2N2906A | MPS2907A | BC393 | MPSA92 | J305 | MMBF5484LT1 |
| 2N2907 | MPS2907 | BC394 | MPSA42 | MAD130P | BAS16LT1 |
| 2N2907A | MPS2907A | BC450 | MPSA92 | MAD1103P | BAS16LT1 |
| 2N3019 | MPSA06 | BC450A | MPSA92 | MAD1107P | BAS16LT1 |
| 2N3020 | MPSA06 | BC546A | BC546B | MAD1108P | BAS16LT1 |
| 2N3053 | MPSA20 | BC559 | BC559B | MAD1109P | BAS16LT1 |

REPLACEMENT DEVICES

| DEVICE | REPLACEMENT | DEVICE | REPLACEMENT | DEVICE | REPLACEMENT |
|-------------|-------------|--------------|--------------|----------|-------------|
| MM3001 | 2N5551 | MPS6530 | MPS6530RLRM | MV2114 | MV2115 |
| MM3725 | MPS2222A | MPS6531 | MPS6530RLRM | MVAM108 | MMBV2109LT1 |
| MM4001 | 2N5401 | MPS6562 | MPS6651 | MVAM109 | MMBV2109LT1 |
| MMAD1106 | BAS16LT1 | MPS6568A | MPS918 | MVAM115 | MMBV2109LT1 |
| MMBF4856LT1 | MMBF4391LT1 | MPS6571 | MPSA18 | MVAM125 | MMBV2109LT1 |
| MMBF4860LT1 | MMBF5457LT1 | MPS6595 | MPS3563 | PBF259 | MMBT6517LT1 |
| MMBF5459LT1 | MMBF5457LT1 | MPS8093 | 2N4402 | PBF259S | MMBT6517LT1 |
| MMBF5486LT1 | 2N5486 | MPSA16 | MPSA17 | PBF259RS | MMBT6517LT1 |
| MMBT8599LT1 | MMBT5551LT1 | MPSH04 | MPSH17 | PBF493 | MMBTA92LT1 |
| MMBV2104LT1 | MMBV2103LT1 | MPSH07A | MPSH17 | PBF493R | MMBTA92LT1 |
| MMPQ3799 | MMPQ3725 | MPSH20 | MPSH17 | PBF493RS | MMBTA92LT1 |
| MMSV3401T1 | MMBV3401LT1 | MPSH24 | MPSH17 | PBF493S | MMBTA92LT1 |
| MPF970 | MMBFJ175LT1 | MPSH34 | MPSH17 | VN1706L | MMFT107T1 |
| MPF971 | MMBFJ175LT1 | MPSH69 | MPSH81 | | |
| MPF3821 | MMBF5457LT1 | MSA1022-BT1 | MSA1022-CT1 | | |
| MPF3822 | MMBF5457LT1 | MSB709-ST1 | MSB709-RT1 | | |
| MPF4856 | MPF4391RLRA | MSB710-QT1 | MSB710-RT1 | | |
| MPF4857 | 2N5639 | MSB1218A-ST1 | MSB1218A-RT1 | | |
| MPF4858 | J112 | MSC1621T1 | MSD602-RT1 | | |
| MPF4859 | 2N5638RLRA | MSC2404-CT1 | MSC2295-CT1 | | |
| MPF4860 | 2N5638RLRA | MSD1819A-ST1 | MSD1819A-RT1 | | |
| MPF4861 | J112 | MV1620 | MV2101 | | |
| MPQ6501 | MPQ6502 | MV1624 | MMBV2103LT1 | | |
| MPS3638 | MPS3638A | MV1636 | MV2108 | | |
| MPS3866 | BF224 | MV1640 | MV2109 | | |
| MPS4123 | MPS4124 | MV1642 | MV2111 | | |
| MPS4125 | MPS4126 | MV1644 | MV2111 | | |
| MPS4258 | MPS3640 | MV2103 | MMBV2103LT1 | | |
| MPS5771 | MPS3640 | MV2107 | MV2108 | | |
| MPS6520 | MPS6521 | MV2113 | MV2111 | | |