

### Features

- $\mu$ POL™ package with output inductor included
- Small size: 3.3mm x 3.3mm x 1.5mm
- Continuous 6A load capability
- Plug and play: no external compensation required
- Programmable operation using the I<sup>2</sup>C serial bus
- Wide input voltage range: 4.5–16V
- Adjustable output voltage: 0.6–2.5V,  $\pm 0.5\%$  initial accuracy
- Enabled input, programmable under-voltage lock-out (UVLO) circuit
- Open-drain power-good indicator
- Built-in protection features
- Operating temperature from -40°C to +125°C
- Lead-free and halogen-free
- Compliant with EU Directives REACH and RoHS 6

### Applications

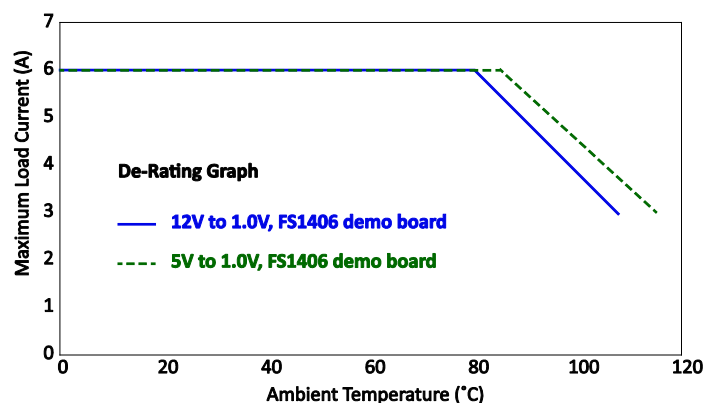
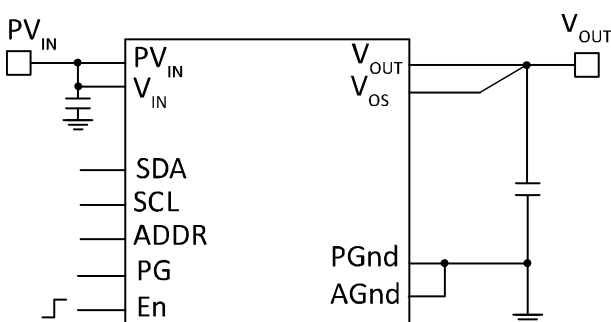
- Storage applications
- Telecom and networking applications
- Industrial applications
- Server applications
- Distributed point-of-load power architectures
- Computing peripheral voltage regulation
- General DC-DC conversion

### Description

The FS1406 is an easy-to-use, fully integrated and highly efficient micro-point-of-load ( $\mu$ POL™) voltage regulator. The on-chip pulse-width modulation (PWM) controller and integrated MOSFETs, plus incorporated inductor and capacitors, result in an extremely compact and accurate regulator. The low-profile package is suitable for automated assembly using standard surface-mount equipment.

Developed by a cross-functional engineering team, the design exemplifies best practice and uses class-leading technologies. From early in the integrated circuit design phase, designers worked with application and packaging engineers to select compatible technologies and implement them in ways that reduce compromise. The ability to program aspects of the FS1406's operation using the Inter-Integrated Circuit (I<sup>2</sup>C) protocol is unique in this class of product. Developing and optimizing all of these elements together has yielded the smallest, most efficient and fully featured 6A  $\mu$ POL™ currently available.

The built-in protection features include pre-biased start-up, soft-start protection, over-voltage protection, thermally compensated over-current protection with hiccup mode, thermal shut-down with auto-recovery.



## Pin configuration

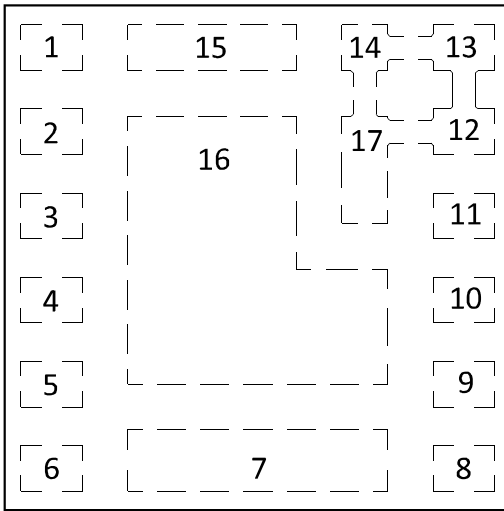


Figure 1 Pin layout (top view)

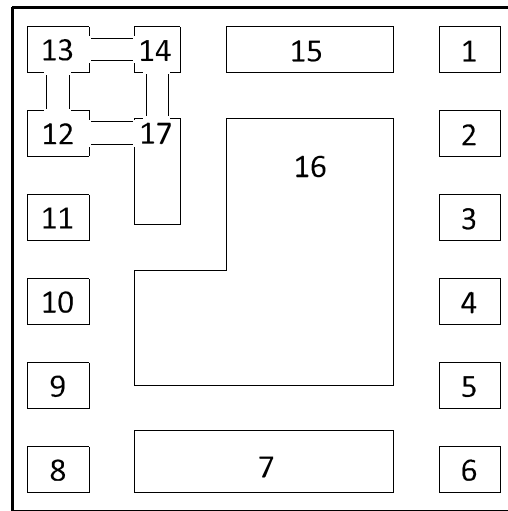


Figure 2 Pin layout (bottom view)

## Pin functions

Pin Number	Name	Description
1	SDA	<b>I<sup>2</sup>C Data Serial Input/Output line.</b> Pull up to bus voltage with a 4.99k $\Omega$ resistor.
2	PG	<b>Power Good status.</b> Open drain of an internal MOSFET. Pull up to $V_{CC}$ – pin 10 or an external bias voltage (Figure 7) – with a 49.9k $\Omega$ resistor.
3	En	<b>Enable.</b> Switches the FS1406 on and off. Can be used with two external resistors to set an external UVLO (Figure 6).
4	SCL	<b>I<sup>2</sup>C Clock line.</b> Pull up to bus voltage with a 4.99k $\Omega$ resistor.
5	$V_{OS}$	<b><math>V_{OUT}</math> sense pin.</b> Connect directly to the regulator output ( $V_{OUT}$ ).
6	ADDR	<b>Address.</b> Connect to AGnd through a resistor to program FS1406 address (page 16).
7	$V_{OUT}$	<b>Regulator output voltage.</b> Place output capacitors between this pin and PGnd (pin 8).
8, 16	PGnd	<b>Power ground.</b> Serves as a separate ground for the MOSFETs. Connect to the power ground plane in the application.
9	AGnd	<b>Signal ground.</b> Serves as the ground for the internal reference and control circuitry.
10	$V_{CC}$	<b>Supply voltage.</b> May be an input bias for an external $V_{CC}$ voltage or the output of the internal LDO regulator.
11	$V_{IN}$	<b>Input voltage.</b> Input for the internal LDO regulator.
12,13,14,17	$PV_{IN}$	<b>Power input voltage.</b> Input for the MOSFETs.
15	$V_{SW}$	<b>Test point for internal <math>V_{SW}</math>.</b> Connect to an isolated pad on the PCB.

## Block diagram

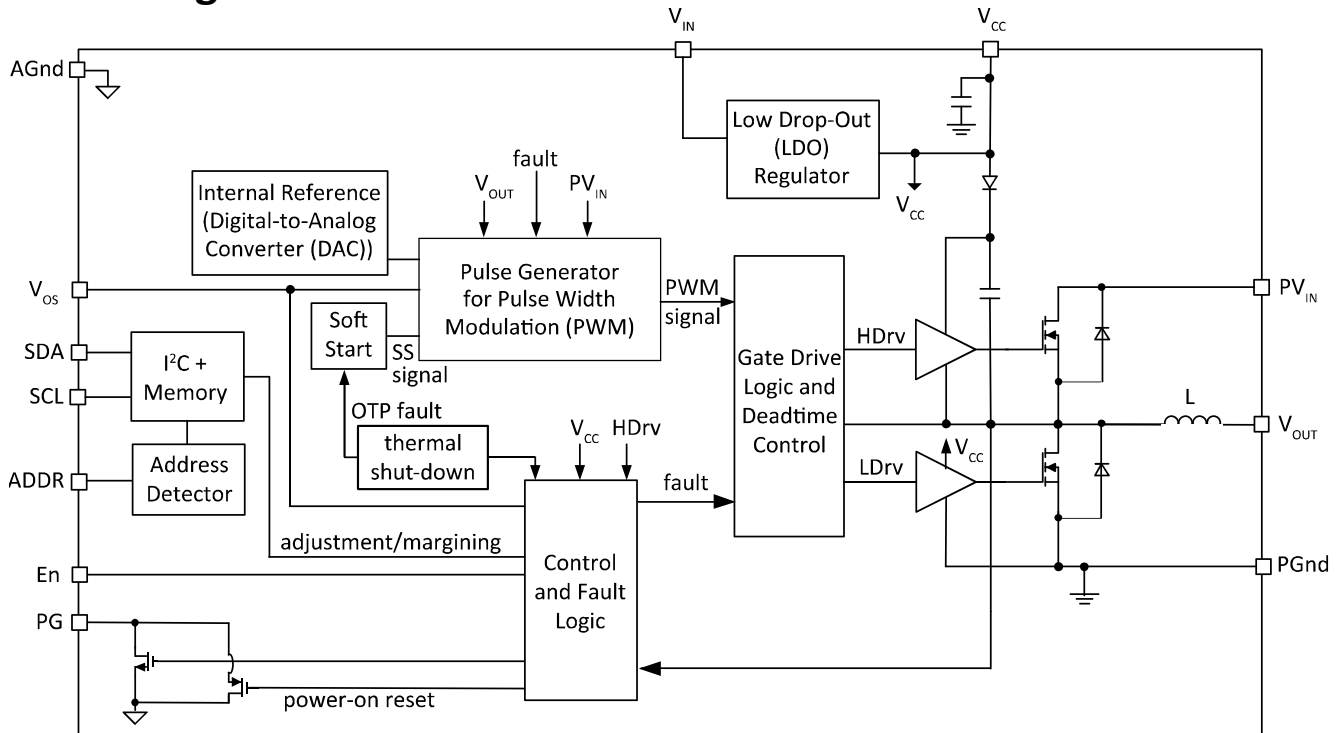


Figure 3 FS1406  $\mu$ POL™

## Typical applications

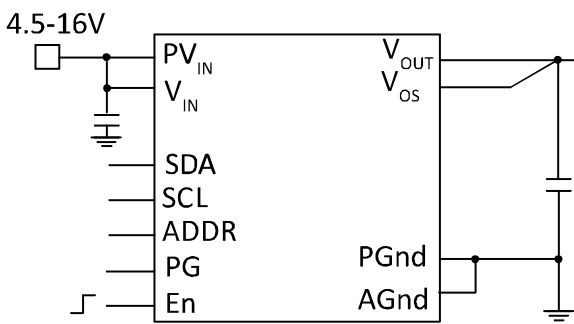


Figure 4 Single supply applications circuit

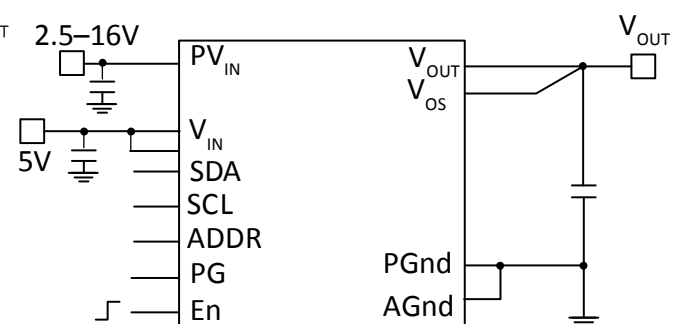


Figure 5 Dual supply applications circuit

## Absolute maximum ratings

**Warning:** Stresses beyond those shown may cause permanent damage to the FS1406.

**Note:** Functional operation of the FS1406 is not implied under these or any other conditions beyond those stated in the FS1406 specification.

Reference	Range
$PV_{IN}$ , $V_{IN}$ , En to PGnd	-0.3V to 18V (Note 1, page 9)
$V_{CC}$ to PGnd	-0.3V to 6V (Note 2, page 9)
$V_{OS}$ to AGnd	-0.3V to $V_{CC}$ (Note 2, page 9)
PG to AGnd	-0.3V to $V_{CC}$ (Note 2, page 9)
PGnd to AGnd	-0.3V to +0.3V
ESD Classification	2kV (HBM JESD22-A114)
Moisture Sensitivity Level	MSL 3 (JEDEC J-STD-020D)

Thermal Information	Range
Junction-to-Ambient Thermal Resistance $\Theta_{JA}$	22.6°C/W
Junction to PCB Thermal Resistance $\Theta_{J-PCB}$	2.36°C/W
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C
Note:	$\Theta_{JA}$ : FS1406 evaluation board and JEDEC specifications JESD 51-2A $\Theta_{J-c}$ (bottom) : JEDEC specification JESD 51-8

## Order information

### Package details

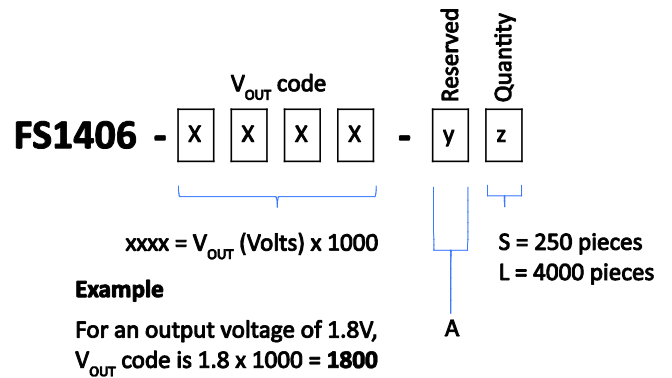
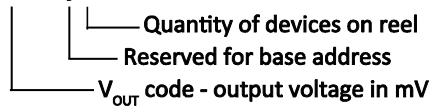
The FS1406 uses a  $\mu$ POL™ 3.3 mm x 3.3 mm package delivered in tape-and-reel format (Figure 34), with either 250 or 4000 devices on a reel.

### Standard part numbers

Output voltages of 0.6V to 2.5V are available.

V <sub>OUT</sub>	Part numbers	
	250 devices on a reel	4000 devices on a reel
0.60	FS1406-0600-AS	FS1406-0600-AL
0.70	FS1406-0700-AS	FS1406-0700-AL
0.75	FS1406-0750-AS	FS1406-0750-AL
0.80	FS1406-0800-AS	FS1406-0800-AL
0.90	FS1406-0900-AS	FS1406-0900-AL
1.00	FS1406-1000-AS	FS1406-1000-AL
1.05	FS1406-1050-AS	FS1406-1050-AL
1.10	FS1406-1100-AS	FS1406-1100-AL
1.20	FS1406-1200-AS	FS1406-1200-AL
1.80	FS1406-1800-AS	FS1406-1800-AL
2.50	FS1406-2500-AS	FS1406-2500-AL

### FS1406-xxxx-yz



## Recommended operating conditions

Definition	Symbol	Min	Max	Units
Input Voltage Range with External $V_{CC}$ (Note 3, Note 5)	$PV_{IN}$	2.5	16	V
Input Voltage Range with Internal LDO (Note 4, Note 5)	$PV_{IN}, V_{IN}$	4.5	16	
Supply Voltage Range (Note 2)	$V_{CC}$	4.5	5.5	
Output Voltage Range	$V_O$	0.6	2.5	
Continuous Output Current Range	$I_O$	0	6	A
Operating Junction Temperature	$T_J$	-40	125	$^{\circ}C$

## Electrical characteristics

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V, 0^{\circ}C < T < 125^{\circ}C$							
Typical values are specified at $T_A = 25^{\circ}C$							
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
<b>Supply Current</b>							
$V_{IN}$ Supply Current (Standby)	$I_{IN(Standby)}$	Enable low		1		mA	
$V_{IN}$ Supply Current (Static)	$I_{IN(Static)}$	No switching, $En = 2V$		2			
$V_{IN}$ Supply Current (Dynamic)	$I_{IN(Dyn)}$	$En$ high, $V_{IN} = 12V, V_{OUT} = 1.8V, F_{SW} = 2MHz$		19	25		
<b>Soft-Start</b>							
Soft-Start Rate	$SS_{Rate}$ (default)	(Note 7)		0.5			V/ms
<b>Output Voltage</b>							
Output Voltage Range	$V_{OUT}$ (default)			1.8			V
	V (resolution)	$V_{OUT} \leq 1.8V$		5			mV
		$V_{OUT} > 1.8V$		10			
Accuracy		$T_J = 25^{\circ}C, PV_{IN} = 12V, V_{OUT} = 1.8V$ (Note 6)		$\pm 0.5$			%
		$25^{\circ}C < T_J < 125^{\circ}C, PV_{IN} = 12V, 0.6V \leq V_{OUT} < 1.0V$ (Note 6)	-1.2		+1.2		
		$25^{\circ}C < T_J < 125^{\circ}C, PV_{IN} = 12V, 1.0V \leq V_{OUT} \leq 2.5V$ (Note 6)	-1		+1		
<b>On-Time Timer Control</b>							
On Time	$T_{ON}$	$PV_{IN} = 12V, V_{OUT} = 1.8V, F_{SW} = 2MHz$	70	80	90	ns	
Minimum On-Time	$T_{ON(MIN)}$	(Note 7)		50			
Minimum Off-Time	$T_{OFF(MIN)}$	$PV_{IN} = 1.8V, V_{OUT} = 1.8V, F_{SW} = 2MHz$		220	256		
<b>Internal Low Drop-Out (LDO) Regulator</b>							
LDO Regulator Output Voltage	$V_{CC}$	$5.5V < V_{IN} = 16V, 0 - 20mA$	4.9	5.2	5.5	V	
		$4.5V \leq V_{IN} < 5.5V, 0 - 20mA$	4.3				
Line Regulation	$V_{LN}$	$5.5V < V_{IN} = 16V, 20mA$			50	mV	
Load Regulation	$V_{LD}$	$0 - 20mA$			100		
Short Circuit Current	$I_{SHORT}$	(Note 7)		70			mA

ELECTRICAL CHARACTERISTICS						
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T < 125^{\circ}C$						
Typical values are specified at $T_A = 25^{\circ}C$						
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Thermal Shut-Down</b>						
Thermal Shut-Down	TSD (default)			145		$^{\circ}C$
Hysteresis				25		
<b>Under-Voltage Lock-Out</b>						
$V_{CC}$ Start Threshold	$V_{CC\_UVLO(START)}$	$V_{CC}$ Rising Trip Level	3.7	4.0	4.2	V
$V_{CC}$ Stop Threshold	$V_{CC\_UVLO(STOP)}$	$V_{CC}$ Falling Trip Level	3.6	3.8	3.95	
Enable Threshold	$En(HIGH)$	Ramping Up	1.1	1.2	1.3	
	$En(LOW)$	Ramping Down	0.9	1	1.06	
Input Impedance	$R_{EN}$		500	1000	1500	k $\Omega$
<b>Current Limit</b>						
Current Limit Threshold	$I_{OC}$ (default)	$T_J = 25^{\circ}C$ , $PV_{IN} = 12V$ , $V_{OUT} = 1.8V$	7.2	7.8	8.5	A
Hiccup Blanking Time	$T_{BLK(HICCUP)}$			20		ms
<b>Over-Voltage Protection</b>						
Output Over-Voltage Protection Threshold	$V_{OVP}$ (default)	OVP Detect (Note 7), $V_{OUT} = 1.8V$	115	120	125	$V_{OS}\%$
Output Over-voltage Protection Delay	$T_{OVPDEL}$			5		$\mu s$
<b>Power Good (PG)</b>						
Power Good Upper Threshold	$V_{PG(UPPER)}$ (default)	$V_{OUT}$ Rising to 1.8V	85	90	95	$V_{OS}\%$
Power Good Hysteresis	$V_{PG(LOWER)}$	$V_{OUT}$ Falling from 1.8V		5		
Power Good Sink Current	$I_{PG}$	$PG = 0.5V$ , $En = 2V$		9		mA

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T < 125^{\circ}C$							
Typical values are specified at $T_A = 25^{\circ}C$							
Parameter	Symbol	Conditions	Fast-mode		Fast-mode Plus		Unit
$I^2C$ parameters		(Note 7 for all parameters)	Min	Max	Min	Max	
$I^2C$ bus voltage	$V_{BUS}$		1.8	5.5	1.8	5.5	V
LOW-level input voltage	$V_{IL}$		-0.5	$0.3V_{BUS}$	-0.5	$0.3V_{BUS}$	
HIGH-level input voltage	$V_{IH}$		$0.7V_{BUS}$		$0.7V_{BUS}$		
Hysteresis	$V_{HYS}$		$0.05V_{BUS}$		$0.05V_{BUS}$		
LOW-level output voltage 1	$V_{OL1}$	(open-drain or open-collector) at 3mA sink current; $V_{DD} > 2V$ ,	0	0.4	0	0.4	
LOW-level output voltage 2	$V_{OL2}$	(open-drain or open-collector) at 2mA sink current; $V_{DD} \leq 2V$ ,	0	$0.2V_{BUS}$	0	$0.2V_{BUS}$	
LOW-level output current	$I_{OL}$	$V_{OL} = 0.4V$ ,	3	-	3	-	mA
		$V_{OL} = 0.6V$	6	-	6	-	

ELECTRICAL CHARACTERISTICS							
Unless otherwise stated, these specifications apply over: $4.5V < PV_{IN} = V_{IN} < 16V$ , $0^{\circ}C < T < 125^{\circ}C$							
Typical values are specified at $T_A = 25^{\circ}C$							
Parameter	Symbol	Conditions	Fast-mode		Fast-mode Plus		Unit
$I^2C$ parameters		(Note 7 for all parameters)	Min	Max	Min	Max	
Output fall time	$T_{OF}$	From $V_{IHmin}$ to $V_{ILmax}$	$20 \times (V_{BUS}/5.5 V)$	250	$20 \times (V_{BUS}/5.5 V)$	125	ns
Pulse width of spikes that must be suppressed by the input filter	$T_{SP}$		0	50	0	50	
Input current each I/O pin	$I_I$		-10	10	-10	10	$\mu A$
Capacitance for each I/O pin	$C_I$		-	10	-	10	pF
SCL clock frequency	$F_{SCL}$		0	400	0	1000	kHz
Hold time (repeated) START condition	$T_{HD;STA}$	After this time, the first clock pulse is generated	0.6	-	0.26	-	$\mu s$
LOW period of the SCL clock	$T_{LOW}$		1.3	-	0.5	-	
HIGH period of the SCL clock	$T_{HIGH}$		0.6	-	0.26	-	
Set-up time for a repeated START condition	$T_{SU;STA}$		0.6	-	0.26	-	
Data hold time	$T_{HD;DAT}$	$I^2C$ -bus devices	0	-	0	-	ns
Data set-up time	$T_{SU;DAT}$		100	-	50	-	
Rise time of SDA and SCL signals	$T_R$		20	300	-	120	
Fall time of SDA and SCL signals	$T_F$		$20 \times (V_{DD}/5.5 V)$	300	$20 \times (V_{DD}/5.5 V)$	120	$\mu s$
Set-up time for STOP condition	$T_{SU;STO}$		0.6	-	0.26	-	
Bus free time between a STOP and START condition	$T_{BUF}$		1.3	-	0.5	-	pF
Capacitive load for each bus line	$C_B$		-	400	-	550	
Data valid time	$T_{VD;DAT}$		-	0.9	-	0.45	$\mu s$
Data valid acknowledge time	$T_{VD;ACK}$		-	0.9	-	0.45	
Noise margin at the LOW level	$V_{NL}$	For each connected device, including hysteresis	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
Noise margin at the HIGH level	$V_{NH}$		$0.2V_{DD}$	-	$0.2V_{DD}$	-	
SDA timeout	$T_{TO}$		200		200		$\mu s$

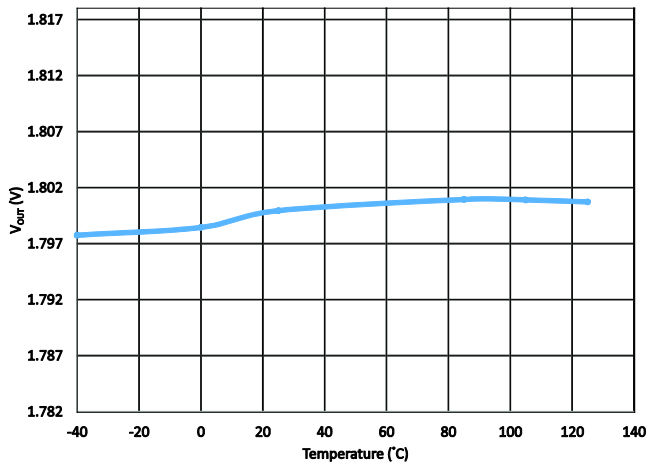


**Notes**

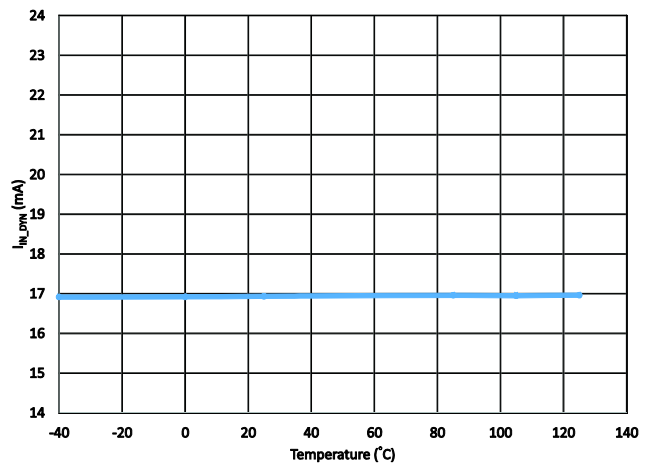
- 1 PGnd pin and AGnd pin are connected together
- 2 Must not exceed 6V
- 3  $V_{IN}$  is connected to  $V_{CC}$  to bypass the internal Low Drop-Out (LDO) regulator
- 4  $V_{IN}$  is connected to  $PV_{IN}$  (for single-rail applications with  $PV_{IN}=V_{IN}=4.5V-5.5V$ )
- 5 Maximum switch node voltage should not exceed 22V
- 6 Hot and cold temperature performance is assured by correlation using statistical quality control, but not tested in production; performance at 25°C is tested and guaranteed in production environment
- 7 Guaranteed by design but not tested in production

## Temperature characteristics

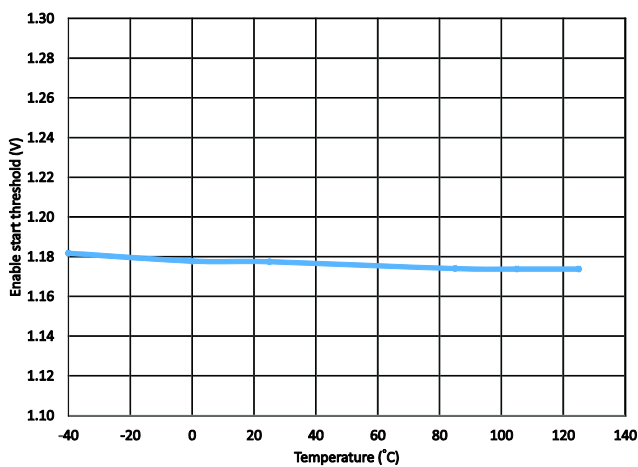
Output Voltage



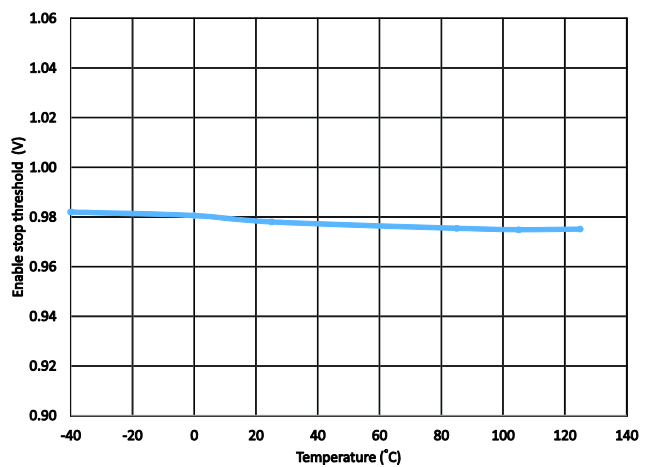
V<sub>IN</sub> Supply Current (Dynamic)



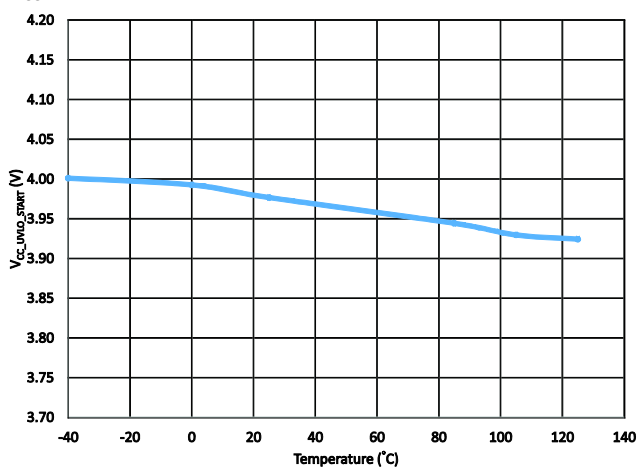
Enable Start Threshold



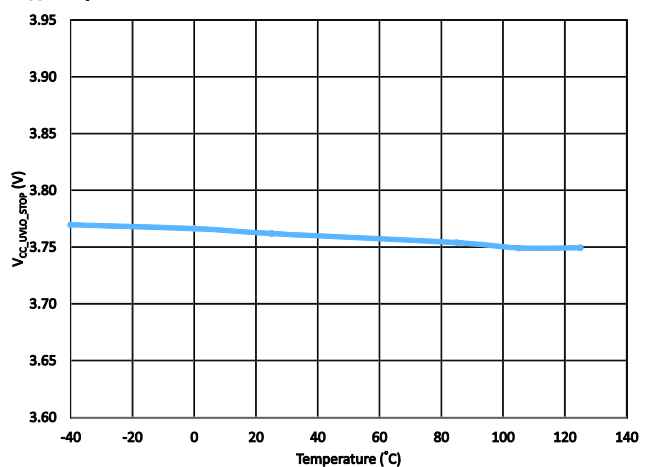
Enable Stop Threshold



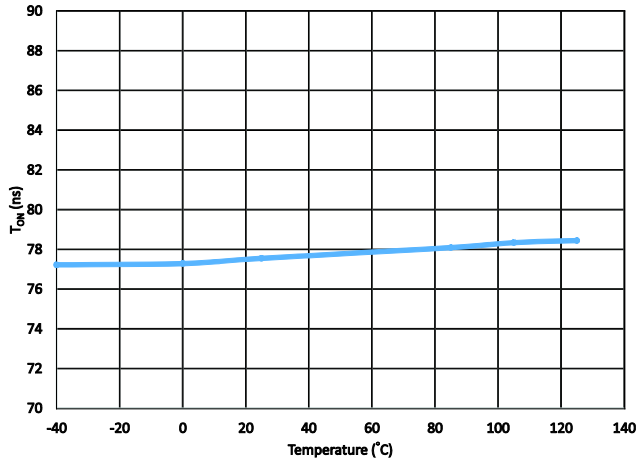
V<sub>CC</sub> Start Threshold



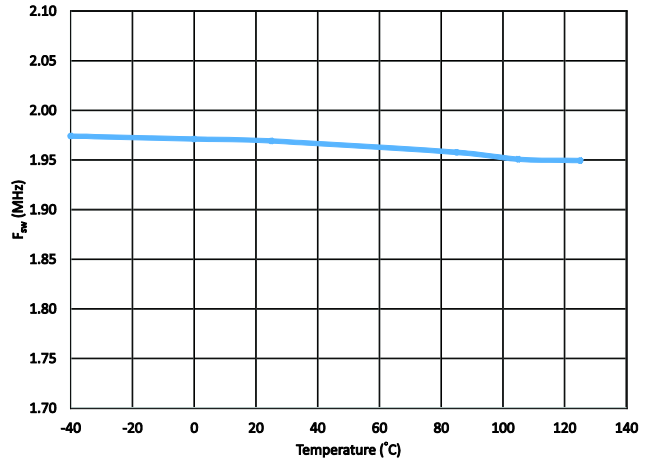
V<sub>CC</sub> Stop Threshold



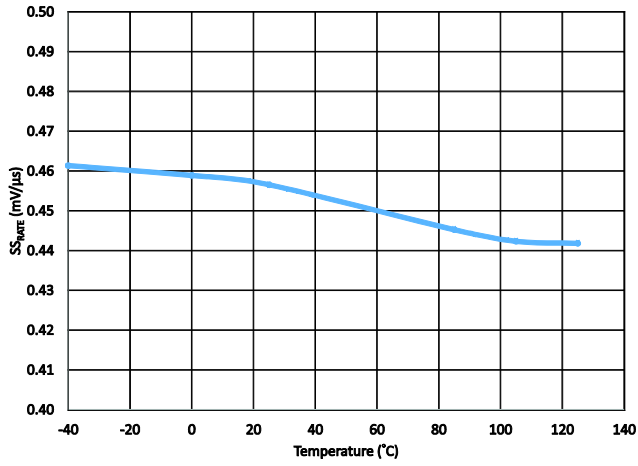
**On Time**



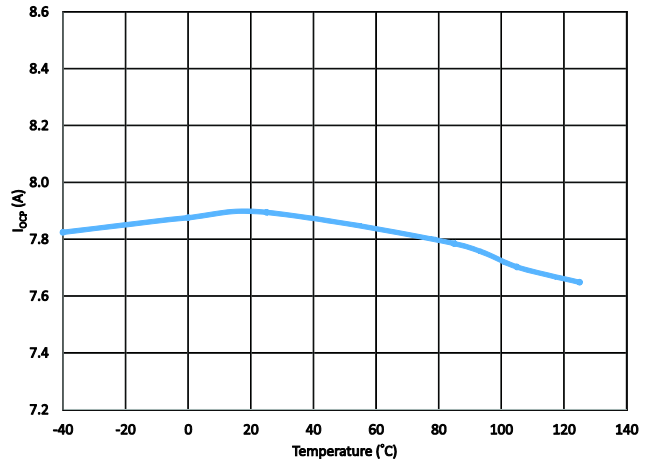
**Switching Frequency**



**Soft-Start Rate**



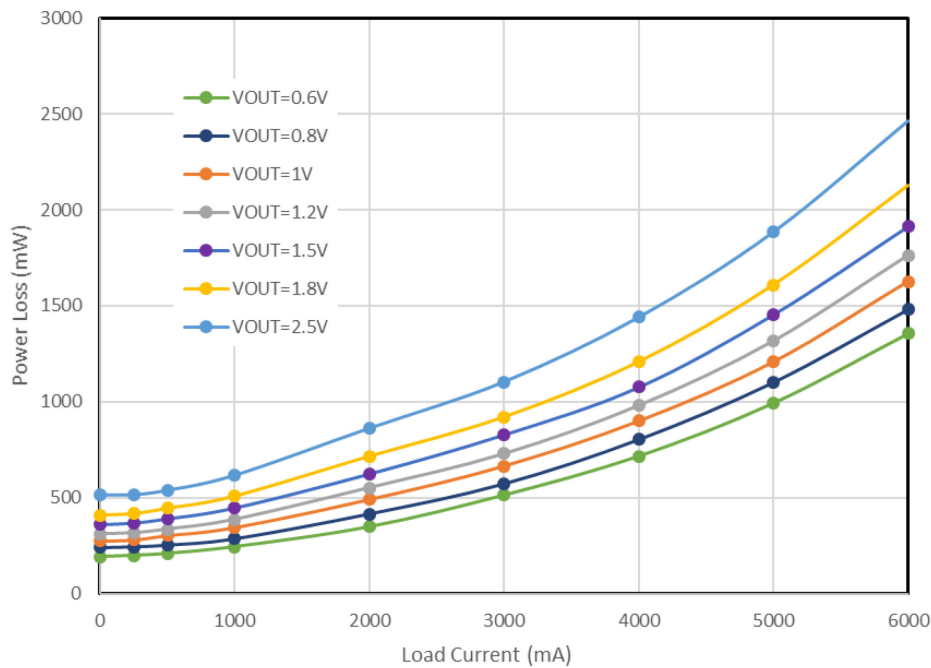
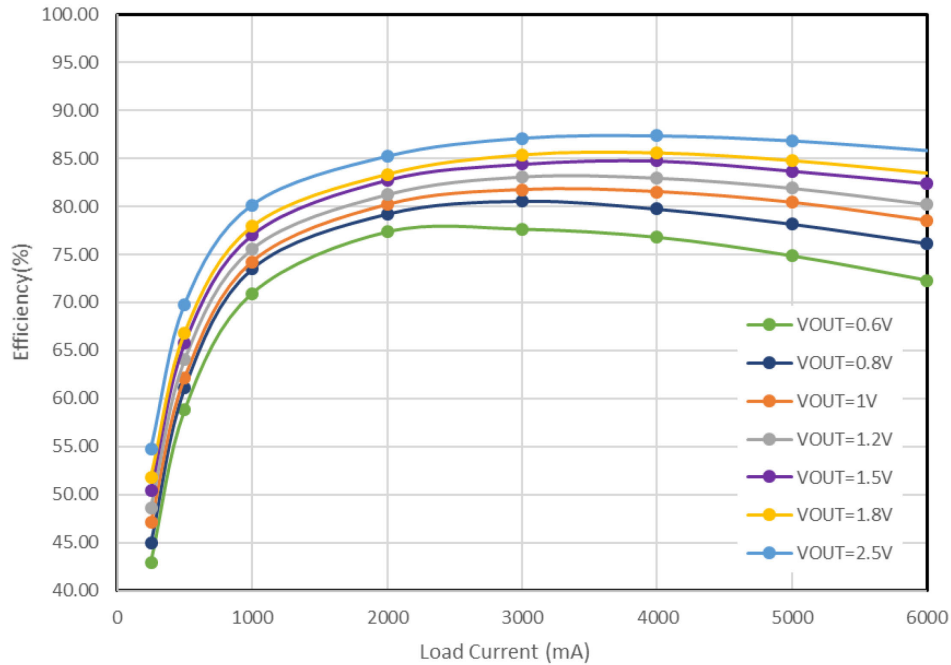
**Current Limit Threshold**



## Efficiency characteristics

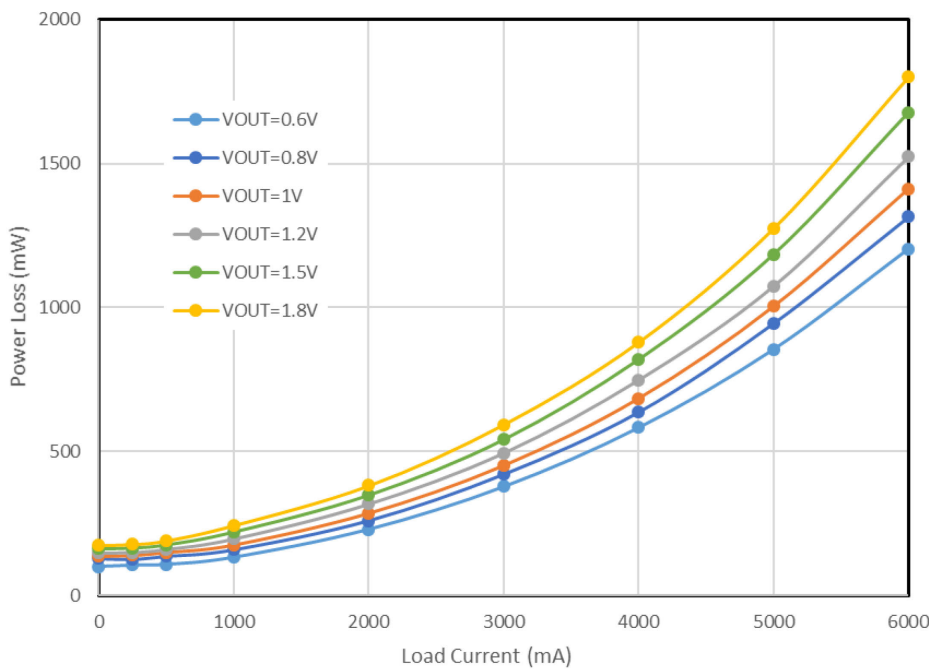
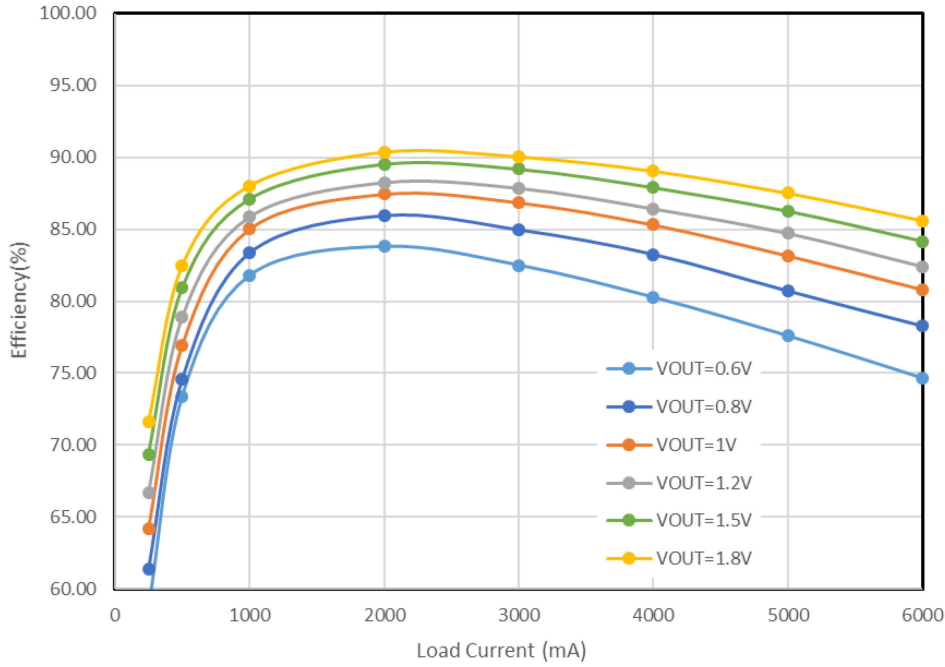
### Typical efficiency and power loss at $PV_{IN} = 12V$

$PV_{IN} = 12V$ , Internal LDO used,  $I_O = 0A-6A$ , room temperature, no air flow, all losses included



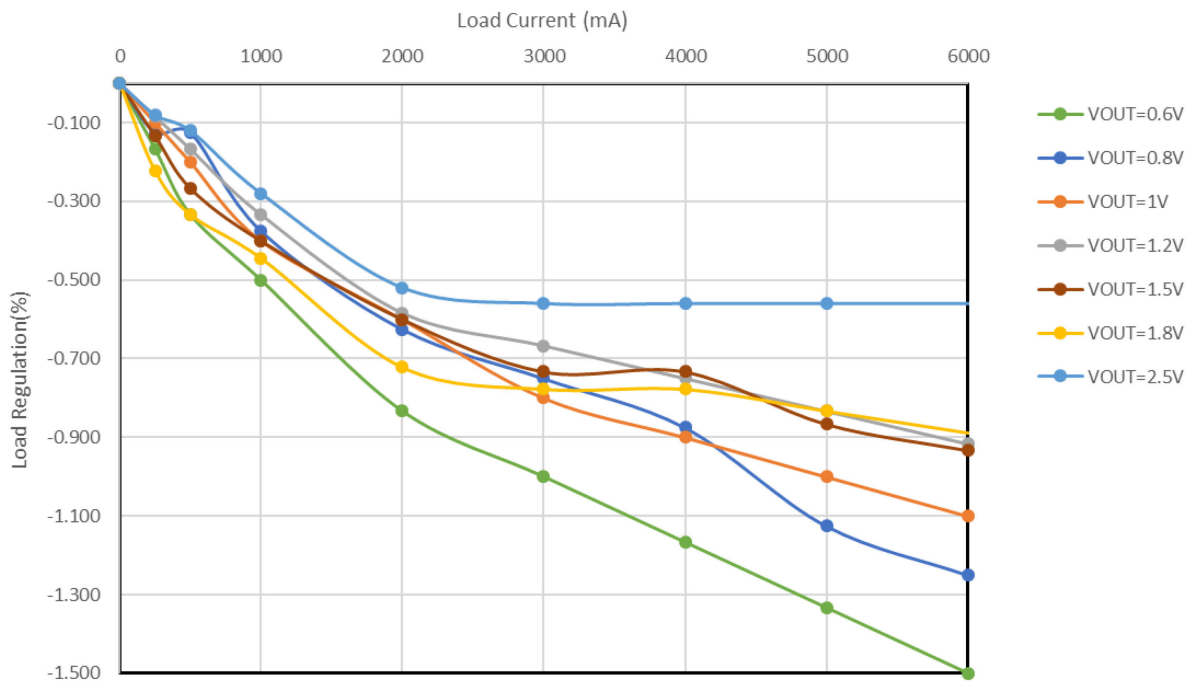
### Typical efficiency and power loss at $PV_{IN} = 5V$

$PV_{IN} = V_{IN} = V_{CC} = 5V$ ,  $I_o = 0A-6A$ , room temperature, no air flow, all losses included

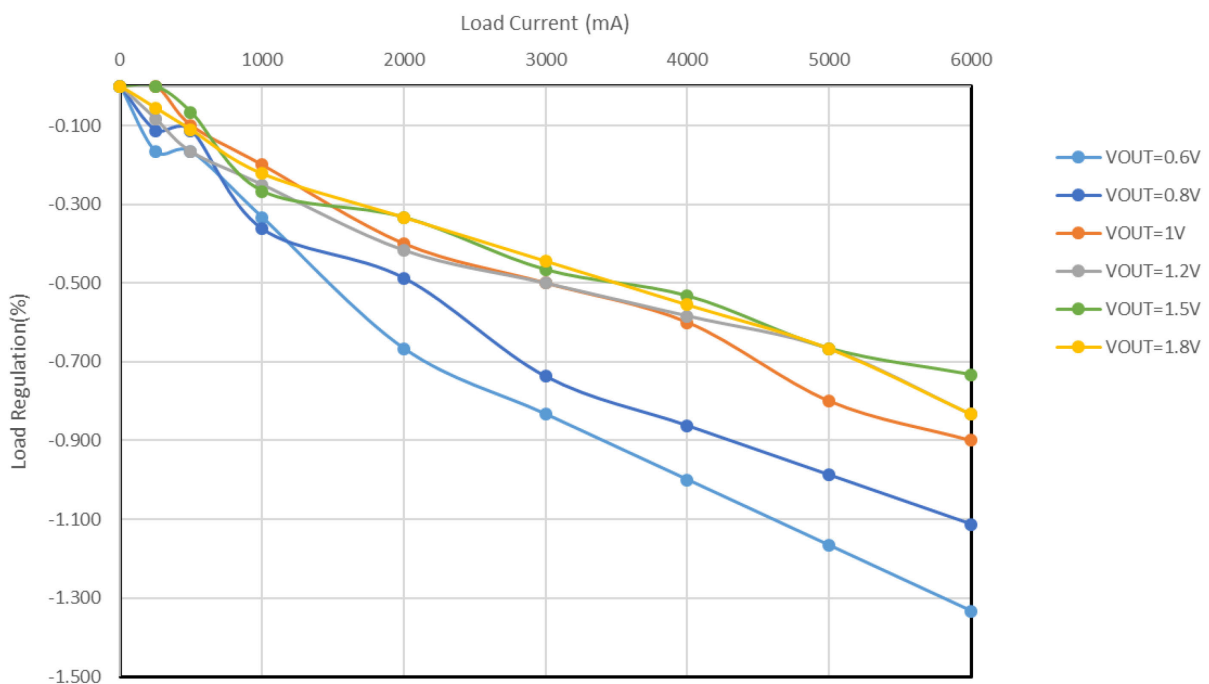


## Typical load regulation

$PV_{IN} = 12V$ , internal LDO used,  $I_o = 0A-6A$ , room temperature, no air flow



$PV_{IN} = V_{IN} = V_{CC} = 5V$ ,  $I_o = 0A-6A$ , room temperature, no air flow, all losses included



## Applications information

### Overview

The FS1406 is an easy-to-use, fully integrated and highly efficient DC/DC regulator. Aspects of its operation, including output voltage and system optimization parameters, can be programmed using the I<sup>2</sup>C protocol. It uses a proprietary modulator to deliver fast transient responses. The modulator has internal stability compensation so that it can be used in a wide range of applications, with various types of output capacitors, without loop stability issues.

### Bias voltage

The FS1406 has an integrated Low Drop-Out (LDO) regulator, providing the DC bias voltage for the internal circuitry. The typical LDO regulator output voltage is 5.2V. For internally biased single-rail operation, the V<sub>IN</sub> pin should be connected to the PV<sub>IN</sub> pin (Figure 6). If an external bias voltage is used, the V<sub>IN</sub> pin should be connected to the V<sub>CC</sub> pin to bypass the internal LDO regulator (Figure 7).

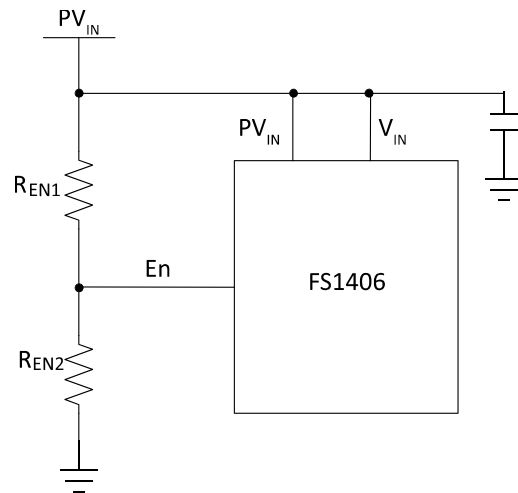
The supply voltage (internal or external) rises with V<sub>IN</sub> and does not need to be enabled using the En pin. Consequently, I<sup>2</sup>C communication can begin as soon as:

- V<sub>CC\_UVLO</sub> start threshold is exceeded
- Memory contents are loaded
- Initialization is complete
- Address offset is read

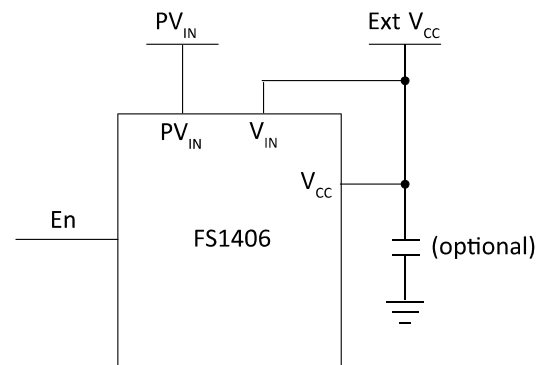
**Note:** Until initialization is complete, a small leakage current ( $\approx 3.4\mu\text{A}$ ) will flow from the device into the output. This may significantly pre-bias the output voltage in applications with long V<sub>IN</sub>/V<sub>CC</sub> rise times. To prevent this, a small load capable of sinking 3.4 $\mu\text{A}$  should be connected in such applications.

The I<sup>2</sup>C bus may be pulled up either to V<sub>CC</sub> or to a system I<sup>2</sup>C bus voltage. The FS1406 offers two ranges for the I<sup>2</sup>C bus voltage, defined by the user register bit **Bus\_voltage\_sel**.

Register	Bits	Name/Description
0x1A	[1]	<b>Bus_voltage_sel</b> 0:1.8–2.5V, 1: 3.3–5V



**Figure 6** Single supply configuration: internal LDO regulator, adjustable PV<sub>IN\_UVLO</sub>



**Figure 7** Using an external bias voltage

## I<sup>2</sup>C base address and offsets

The FS1406 has a user register called **Base\_address**[7:0] stored in memory that sets its base I<sup>2</sup>C address. The default base address is 0x08. An offset of 0-3 is then defined by connecting the ADDR pin to the AGnd pin either directly or through a resistor. An address detector reads the resistance of the connection at startup and uses it to set the offset, which is added to the base I<sup>2</sup>C address to set the address at which the I<sup>2</sup>C master device will communicate with the FS1406.

To select offsets of 0 to 3, connect the pins as follows:

- **0** – 0 $\Omega$  (short ADDR to AGnd)
- **+1** – 10k $\Omega$
- **+2** – 20k $\Omega$
- **+3** – >30.1k $\Omega$

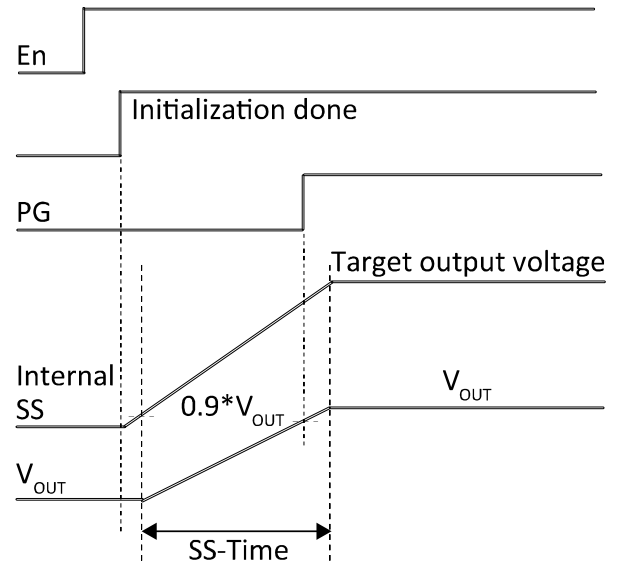
## Soft-start and target output voltage

The FS1406 has an internal digital soft-start circuit to control output voltage rise-time and limit current surge at start-up. When  $V_{CC}$  exceeds its start threshold ( $V_{CC\_UVLO(START)}$ ), the FS1406 exits reset mode; this initiates loading of the contents of the non-volatile memory into the working registers and calculates the address offset as described above.

Once initialization is complete and the Enable (En) pin has been asserted (Figure 8), the internal reference soft-starts to the target output voltage at the rate defined by the user register bit **SS\_rate**.

Register	Bits	Name/Description
0x14	[3]	<b>SS_rate</b> 0: 0.5mV/ $\mu$ s (default), 1: 1 mV/ $\mu$ s

During initial start-up, the FS1406 operates with a minimum of high-drive (HDrv) pulses until the output voltage increases (see Switching frequency, minimum on-time and off-time on page 18). On-time is increased until  $V_{OUT}$  reaches the target value defined by the user register bit **Vout\_high\_byte** and user register **Vout\_low\_byte**[7:0].



**Figure 8** Theoretical operational waveforms during soft-start

Register	Bits	Name/Description
0x12	[0]	<b>Vout_high_byte</b>
0x13	[7:0]	<b>Vout_low_byte</b>

$V_{OUT}$  is set in increments of 5mV for target voltages up to 1.8V, and 10mV increments for target output voltages from 1.8V to 2.5V. Use the following equation to calculate the  $V_{OUT}$  code to enter into **Vout\_high\_byte** and **Vout\_low\_byte**[7:0]:

$$Vout_{code} = \frac{Vout_{target} - \frac{0.4 \times resolution}{0.005}}{resolution}$$

All voltages and resolutions are in Volts.

For example:

To set  $V_{OUT} = 1V$  ( $\leq 1.8V$ , resolution of 5mV):

$$Vout_{code} = \frac{1 - \frac{0.4 \times 0.005}{0.005}}{0.005} = 120$$

120 is 078 in hexadecimal, therefore:

Set **Vout\_high\_byte** to 0

Set **Vout\_low\_byte** to 78 or (01111000)<sub>b</sub>



To set  $V_{OUT} = 2.5V$  ( $>1.8V$ , resolution of  $10mV$ ):

$$V_{out\_code} = \frac{2.5 - \frac{0.4 \times 0.01}{0.005}}{0.01} = 170$$

170 is 0AA in hexadecimal, therefore:

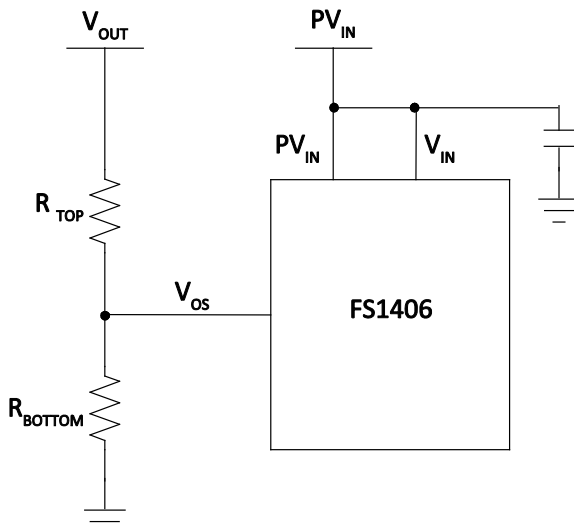
Set **Vout\_high\_byte** to 0

Set **Vout\_low\_byte** to AA or  $(10101010)_b$

Over-current protection (OCP) and over-voltage protection (OVP) is enabled during soft-start to protect the FS1406 from short circuits and excess voltages respectively.

For maximum system accuracy, the recommended way to set the output voltage is by programming the user registers with the appropriate code. For optimum performance when using this approach, the change in output voltage should not exceed  $\pm 20\%$  of the pre-set default output voltage.

However, another option is to combine an FS1406 pre-programmed to  $0.6V$  with a feedback resistor divider (Figure 9). This gives system designers the flexibility to design all the power rails in the system across the entire output voltage range ( $0.6-2.5V$ ) using a single part, at the expense of a worst-case error of no more than an additional  $-1\%$ .



**Figure 9** Setting the output voltage with an external resistor divider

The equation below describes the appropriate resistor divider selection to set the output voltage using a FS1406 programmed to  $0.6V$ .

$$\frac{R_{TOP}}{R_{BOTTOM}} = 1.745V_{OUT} - 1.047$$

It is recommended that system designers place a capacitor of  $4.7pF$  to  $47pF$  in parallel with  $R_{TOP}$ , for which a value of  $40.2k\Omega$  is recommended. The recommended value for  $R_{BOTTOM}$  depends on the output voltage, as shown in the following table.

$V_{OUT}$ (V)	$R_{BOTTOM}$ (k $\Omega$ )	$V_{OUT}$ (V)	$R_{BOTTOM}$ (k $\Omega$ )
0.650	464	1.550	24.3
0.700	232	1.600	23.2
0.720	191	1.650	22.1
0.750	154	1.700	21
0.780	127	1.750	20
0.800	115	1.800	19.1
0.850	90.9	1.850	18.2
0.880	82.4	1.900	17.8
0.900	76.8	1.950	16.9
0.950	64.9	2.000	16.5
1.000	57.6	2.050	15.8
1.050	51.1	2.100	15.4
1.100	46.4	2.150	14.7
1.150	42.2	2.200	14.3
1.200	38.3	2.250	14
1.250	35.7	2.300	13.7
1.300	33.2	2.350	13.3
1.350	30.9	2.400	12.7
1.400	28.7	2.450	12.4
1.450	27.4	2.500	12.1
1.500	25.6		

## Pre-biased start-up

The FS1406 can start up into a pre-charged output smoothly, without causing oscillations and disturbances of the output voltage. When it starts up in this way, the Control and Synchronous MOSFETs are forced off until the internal Soft-Start (SS) signal exceeds the sensed output voltage at the  $V_{OS}$  pin. Only then is the first gate signal of the Control MOSFET generated, followed by complementary turn on of the Synchronous MOSFET. The Power Good (PG) function is not active until this point.

## Shut-down mechanisms

The FS1406 has two shut-down mechanisms:

- *Hard shut-down or decay according to load*  
Initiated by de-asserting the En pin. Both drivers switch off and the digital-to-analog converter (DAC) and soft-start are pulled down instantaneously.
- *Soft-Stop or controlled ramp down*  
Initiated by setting user register bit **SoftStopEnable** to 1 *and* user register bit **SoftDisable** to 1. The SS signal falls to 0 at the same rate as it rises during start-up; the drivers are disabled only when it reaches 0. The output voltage then follows the SS signal down to 0.

The **SoftDisable** bit must not be toggled while the part is enabled and switching. Instead, for applications requiring soft-stop, this bit must be set to 1 and, with the En pin asserted, the **SoftStopEnable** bit must be toggled to soft-start or soft-stop the device.

By default, both the **SoftDisable** bit and the **SoftStopEnable** bit are 0, which means that soft-stop operation is disabled by default.

Register	Bits	Name/Description
0x14	[2]	<b>SoftStopEnable</b>
0x1C	[3]	<b>SoftDisable</b>

## Switching frequency, minimum on-time and off-time

The switching frequency of the FS1406 depends on the output voltage. For an output voltage of 1.8V, the switching frequency is nominally 2MHz.

When the output voltage is set by programming the user registers, the appropriate switching frequency is also programmed at the factory. When the output voltage is set using an external resistor divider, the switching frequency automatically adjusts to the appropriate value:

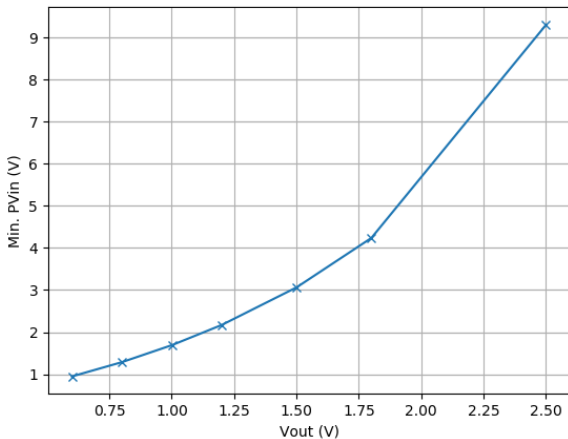
$$F_{sw} = 650kHz \times \frac{V_{OUT}}{0.6}$$

Therefore, with either method, system designers need not concern themselves with selecting the switching frequency and have one fewer design task to manage.

When input voltage is high relative to target output voltage, the Control MOSFET is switched on for shorter periods. The shortest period for which it can reliably be switched on is defined by minimum on-time ( $T_{ON(MIN)}$ ). During start-up, when the output voltage is very small, the FS1406 operates with minimum on-time.

When input voltage is low relative to target output voltage, the Control MOSFET is switched on for longer periods. The shortest period for which it can be switched off is defined by minimum off-time ( $T_{OFF(MIN)}$ ). The Synchronous MOSFET stays on during this period and its current is detected for over-current protection. This dictates the minimum input voltage that can still allow the device to regulate its output at the target voltage.

Figure 10 shows the minimum input voltage required for some typical output voltages. This curve assumes typical efficiency numbers; since it is affected by efficiency, system designers should validate the values in their own applications.



Note:  $V_{IN} = V_{CC} = 5V$  for  $PV_{IN} < 4.2V$

Figure 10 Minimum input voltage requirements

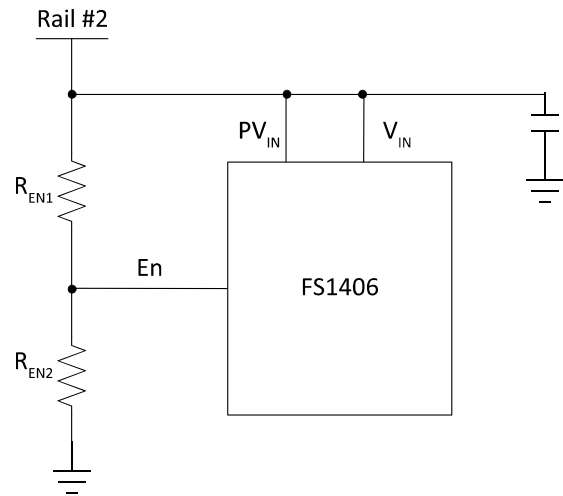


Figure 11 En pin used to monitor other rails for sequencing purposes

## Enable (En) pin

The Enable (En) pin has several functions:

- It is used to switch the FS1406 on and off. It has a precise threshold, which is internally monitored by the UVLO circuit. If it is left floating, an internal  $1M\Omega$  resistor pulls it down to prevent the FS1406 being switched on unintentionally.
- It can be used to implement a precise input voltage UVLO. The input of the En pin is derived from the  $PV_{IN}$  voltage by a set of resistive dividers,  $R_{EN1}$  and  $R_{EN2}$  (Figure 6). Users can program the UVLO threshold voltage by selecting different ratios. This is a useful feature that stops the FS1406 regulating when  $PV_{IN}$  is lower than the desired voltage.
- It can be directly connected to  $PV_{IN}$  without external resistive dividers for some space-constrained designs. This is a useful feature for standalone start-up, when no logic signal is available to enable the FS1406.
- It can be used to monitor other rails for a specific power sequencing scheme (Figure 11).

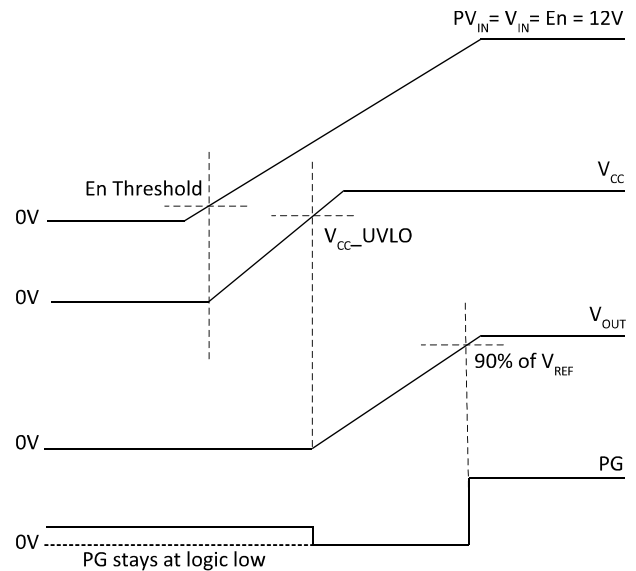
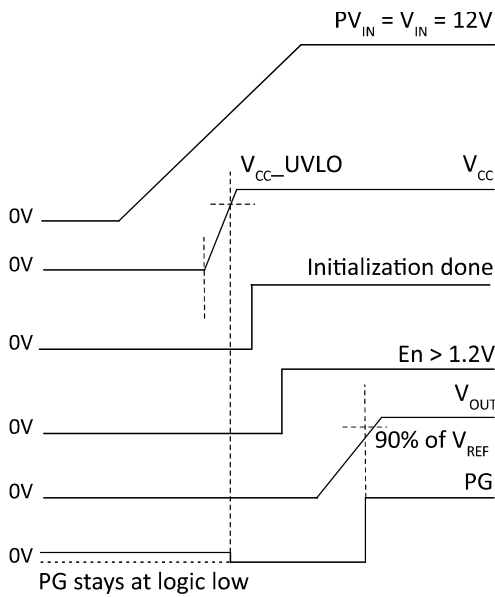


Figure 12 Start-up:  $PV_{IN}$ ,  $V_{IN}$  and En pins tied together, PG pin pulled up to an external supply



**Figure 13 Start-up: En pin asserted after  $PV_{IN}$  and  $V_{IN}$ , PG pin pulled up to an external supply**

For  $V_{OUT}$  to start up as defined by the soft-start rate requires correct sequencing:

- $PV_{IN}$  must start up before  $V_{CC}$  and/or Enable.
- $PV_{IN}$  must ramp down only after  $V_{CC}$  has ramped down below its UVLO threshold and/or Enable has been de-asserted.

## Over-current protection (OCP)

Over-current protection (OCP) is provided by sensing the current through the  $R_{DS(on)}$  of the Synchronous MOSFET. When this current exceeds the OCP threshold, a fault condition is generated. This method provides several benefits:

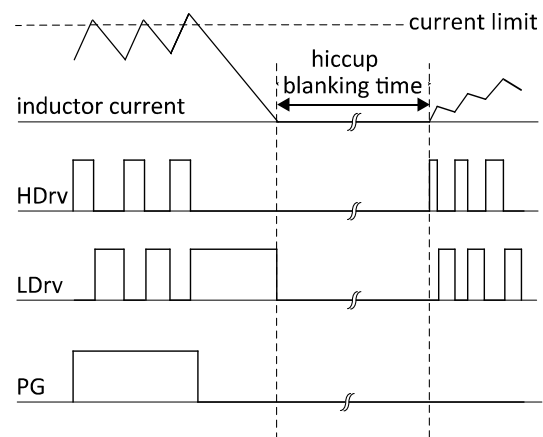
- Provides accurate overcurrent protection without reducing converter efficiency (the current sensing is lossless)
- Reduces cost by eliminating a current-sense resistor
- Reduces any layout-related noise issues.

The OCP threshold is defined by the user register bits **OCSet**.

Register	Bits	Name/Description
0x15	[2:0]	<b>OCSet</b> 2:8A (default), 1:6A, 0: 4A

The threshold is internally compensated so that it remains almost constant at different ambient temperatures.

When the current exceeds the OCP threshold, the PG and SS signals are pulled low. The Synchronous MOSFET remains on until the current falls to 0, then the FS1406 enters hiccup mode (Figure 14). Both the Control MOSFET and the Synchronous MOSFET remain off for the hiccup-blanking time. After this time, the FS1406 tries to restart. If an over-current fault is still detected, the preceding actions are repeated. The FS1406 remains in hiccup mode until the over-current fault is remedied.



**Figure 14 Illustration of OCP in hiccup mode**

## Over-voltage protection (OVP)

Over-voltage protection (OVP) is provided by sensing the voltage at the  $V_{OS}$  pin. When  $V_{OS}$  exceeds the output OVP threshold for longer than the output OVP delay (typically  $5\mu s$ ), a fault condition is generated.

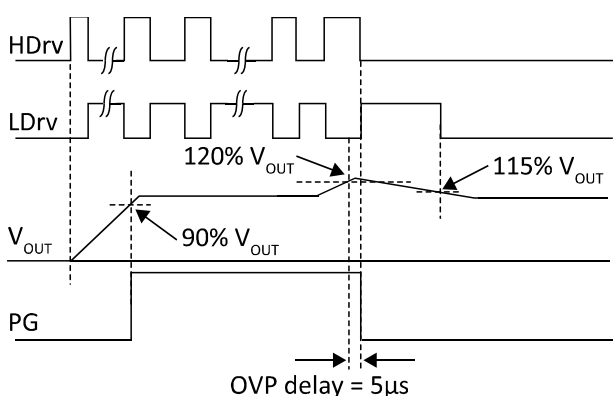
The OVP threshold is defined by the user register bits **OV\_Threshold**.

Register	Bits	Name/Description
0x17	[1:0]	<b>OV_Threshold</b> 0:105% of $V_{OUT}$ 1:110% of $V_{OUT}$ 2:115% of $V_{OUT}$ 3:120% of $V_{OUT}$ (default)

The Control MOSFET is switched off immediately and the PG pin is pulled low. The Synchronous MOSFET is switched on to discharge the output capacitor.

The Control MOSFET remains latched off until reset by cycling either VCC or En. The voltage at the VOS pin falling below the output OVP threshold (with 5% hysteresis) does not switch on the Control MOSFET but it does switch off the Synchronous MOSFET to prevent build-up of negative current.

Figure 15 shows a timing diagram for over-voltage protection.



**Figure 15 Illustration of latched OVP**

## Over-temperature protection (OTP)

Temperature sensing is provided inside the FS1406. The OTP threshold is defined by the user register bits **OT\_Threshold**.

Register	Bits	Name/Description
0x19	[1:0]	<b>OT_Threshold</b> 0:75°C 1: 85°C 2: 125°C 3: 145°C (default)

When the threshold is exceeded, thermal shut-down switches off both MOSFETs and resets the internal soft-start, but the internal LDO regulator is still in operation.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the OTP threshold.

## Power Good (PG)

Power Good (PG) behavior is defined by the user register bits **PGControl** and **PG\_Threshold**.

Register	Bits	Name/Description
0x18	[1:0]	<b>PG_Threshold</b> 0:80% of $V_{OUT}$ 1: 85% of $V_{OUT}$ 2: 90% of $V_{OUT}$ (default) 3: 95% of $V_{OUT}$
0x14	[0]	<b>PG_Control</b> 1:Threshold based (default) 0: DAC based

### PG\_Threshold bit

The user register bit **PG\_Threshold** defines the PG threshold as a percentage of  $V_{OUT}$ . Hysteresis of 5% is applied to this, giving a lower threshold.

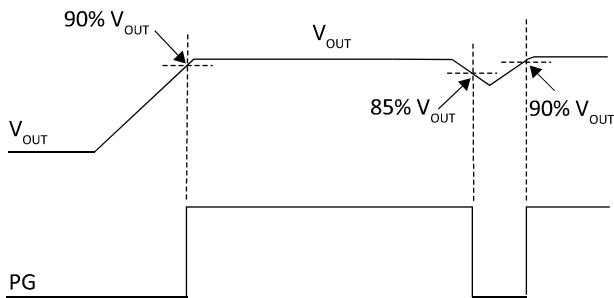
When  $V_{OS}$  rises above the upper threshold, the PG signal is pulled high. When  $V_{OS}$  drops below the lower threshold, the PG signal is pulled low.

### PGControl bit set to 1 (default)

Figure 16 shows PG behavior in this situation.

The behavior is the same at start-up and during normal operation. The PG signal is asserted when:

- $V_{EN}$  and  $V_{CC}$  are both above their thresholds
- No fault has occurred (including over-current, over-voltage and over-temperature)
- $V_{OUT}$  is within the target range (determined by continuously monitoring whether  $V_{OS}$  is above the PG threshold)



**Figure 16 PG signal when PGControl bit=1**

### PGControl bit set to 0

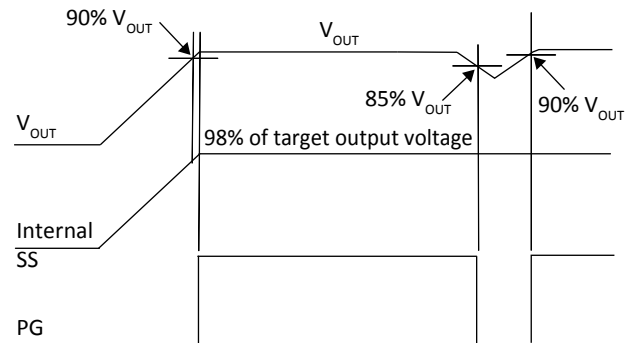
Figure 17 shows PG behavior in this situation.

In normal operation, the PG signal behaves in the same way as when the **PGControl** bit is 1.

At start-up, however, the PG signal is asserted after soft-start is within 2% of target output voltage, not when  $V_{OS}$  exceeds the upper PG threshold.

For pre-biased start-up, the PG signal is not active until the first gate signal of the Control MOSFET is generated.

FS1406 also integrates an additional PMOS in parallel to the NMOS internally connected to the PG pin (Figure 3). This PMOS allows the PG signal to stay at logic low, even if  $V_{CC}$  is low and the PG pin is pulled up to an external voltage not  $V_{CC}$  (Figure 12 and Figure 13).



**Figure 17 PG signal when PGControl bit=0**

## Design example

Let us now consider a simple design example, using the FS1406 for the following design parameters:

- $PV_{IN} = V_{IN} = 12V$
- $V_{OUT} = 1.8V$
- $F_{SW} = 2MHz$
- $C_{OUT} = 2 \times 22\mu F$
- $C_{IN} = 2 \times 22\mu F$
- Ripple Voltage =  $\pm 1\% * V_{OUT}$
- $\Delta V_{OUT(MAX)} = \pm 3\% * V_{OUT}$   
(for 50% load transient)

### Input capacitor

The input capacitor selected for this design must:

- Handle the peak and root mean square (RMS) input currents required by the FS1406
- Have low equivalent series resistance and inductance (ESR and ESL) to reduce input voltage ripple

MLCCs (multi-layer ceramic capacitors) are ideal. Typically, in 0805 case size, they can handle 2A RMS current with less than 5°C temperature rise.

For a buck converter operating at duty cycle  $D$  and output current  $I_O$ , the RMS value of the input current is:

$$I_{RMS} = I_O \sqrt{D(1-D)}$$

In this application,  $I_O = 6A$  and  $D = \frac{V_{OUT}}{PV_{IN}} = 0.15$

Therefore,  $I_{RMS} = 2.14A$  and we can select two 22 $\mu F$  16V ceramic capacitors for the input capacitors (C3216X5R1C226M160AB from TDK).

If the FS1406 is not located close to the 12V power supply, a bulk capacitor (68–330 $\mu F$ ) may be used in addition to the ceramic capacitors.

For  $V_{IN}$ , which is the input to the LDO, it is recommended to use a 1 $\mu F$  capacitor very close to the pin. The  $V_{IN}$  pin should be connected to  $PV_{IN}$  through a 2.7 $\Omega$  resistor. Together, the 2.7 $\Omega$  resistor and 1 $\mu F$  capacitor filter noise on  $PV_{IN}$ .

### Output voltage and output capacitor

The FS1406 is supplied pre-programmed and factory-trimmed in a closed loop to the target voltage specified for the part number. As a result, no external resistor divider is required and resistor tolerances are eliminated from the error budget.

The design requires minimal output capacitance to meet the target output voltage ripple and target maximum output voltage deviation under load transient conditions.

For the FS1406, the minimum number of output capacitors required to achieve target peak-to-peak  $V_{OUT}$  ripple is:

$$N_{MIN} = 4.09 \times \frac{\frac{(1-D)}{8CF_{SW}} + ESR(1-D) + \frac{ESL \times F_{SW} \times (1-D)^2}{D}}{\Delta V_{OUTripple(p-p)}}$$

where:

- $N_{MIN}$  = minimum number of output capacitors
- $D$  = duty cycle
- $C$  = equivalent capacitance of each output capacitor
- $F_{SW}$  = switching frequency
- $ESR$  = equivalent series resistance of each output capacitor
- $ESL$  = equivalent series inductance of each output capacitor
- $\Delta V_{OUTripple(p-p)}$   
= target peak-to-peak  $V_{OUT}$  ripple

This design uses C2012X5R0J226K125AB from TDK; this is a 22 $\mu F$  MLCC, 0805 case size, rated at 6.3V. At 1.8V, accounting for DC bias and AC ripple derating, it has an equivalent capacitance of 12 $\mu F$  ( $C$ ). Equivalent series resistance is 3m $\Omega$  ( $ESR$ ) and equivalent series inductance is 0.44nH ( $ESL$ ).

Putting these parameters into the equation gives:

$$N_{MIN} = 1.27$$

To meet the maximum voltage deviation  $\Delta V_{o,max}$  under a  $\Delta I_o$  load transient, the minimum required number of output capacitors is:

$$\frac{0.244 \times \Delta I_o^2}{\Delta V_{o,max} \times F_{sw} \times C}$$

where:

- $\Delta I_o$  = load step
- $\Delta V_{OUT,max}$  = target maximum voltage deviation
- $F_{sw}$  = switching frequency
- $C$  = equivalent capacitance of each output capacitor

Again, using  $C = 12\mu\text{F}$ , it can be seen that the minimum number of output capacitors required is 0.4.

In our design intended for space-constrained applications, therefore, we use two C2012X5R0J226K125AB capacitors.

It should be noted here that the calculation for the minimum number of output capacitors under a load transient makes some assumptions:

- a) No ESR or ESL
- b) Converter can saturate its duty cycle instantly
- c) No latency
- d) Step load (infinite slew rate)

Assumptions (a), (b) and (c) are liberal, whereas (d) is conservative. Therefore, in a real application, additional capacitance may be required to meet transient requirements and should be carefully considered by the system designer.

The typical application waveforms in Figure 26 and Figure 27 show the steady state  $V_{OUT}$  ripple as well as the voltage deviation in response to a 50% load transient. These waveforms show that the selection of two  $22\mu\text{F}$  capacitors meets the design criteria.

It should be noted that even in the absence of a target  $V_{OUT}$  ripple or target maximum voltage deviation under load transient, at least one  $22\mu\text{F}$  capacitor is still required in order to ensure stable operation without excessive jitter.

Up to six  $22\mu\text{F}$  capacitors may be used in the design. If more capacitance is required, it is recommended to use a capacitor with relatively high ESR ( $>3\text{m}\Omega$ ) such as POSCAP or specialty polymer capacitors.

Figure 18 shows the minimum required output capacitance as a function of the output voltage. For an output voltage of 1V, the minimum capacitor requirement is dictated by the load transient specifications ( $< \pm 3\% V_{OUT}$ ). For output voltages above 1V, the output voltage ripple specification dominates ( $< \pm 1\%$ ).

### V<sub>CC</sub> capacitor selection

FS1406 uses an on-package  $V_{CC}$  capacitor to ensure effective high-frequency bypassing. However, especially for applications that use an external  $V_{CC}$  supply, it is recommended that system designers place a  $2.2\mu\text{F}/0603/\text{X7R}/10\text{V}$  capacitor on the application board as close as possible to the  $V_{CC}$  pin.



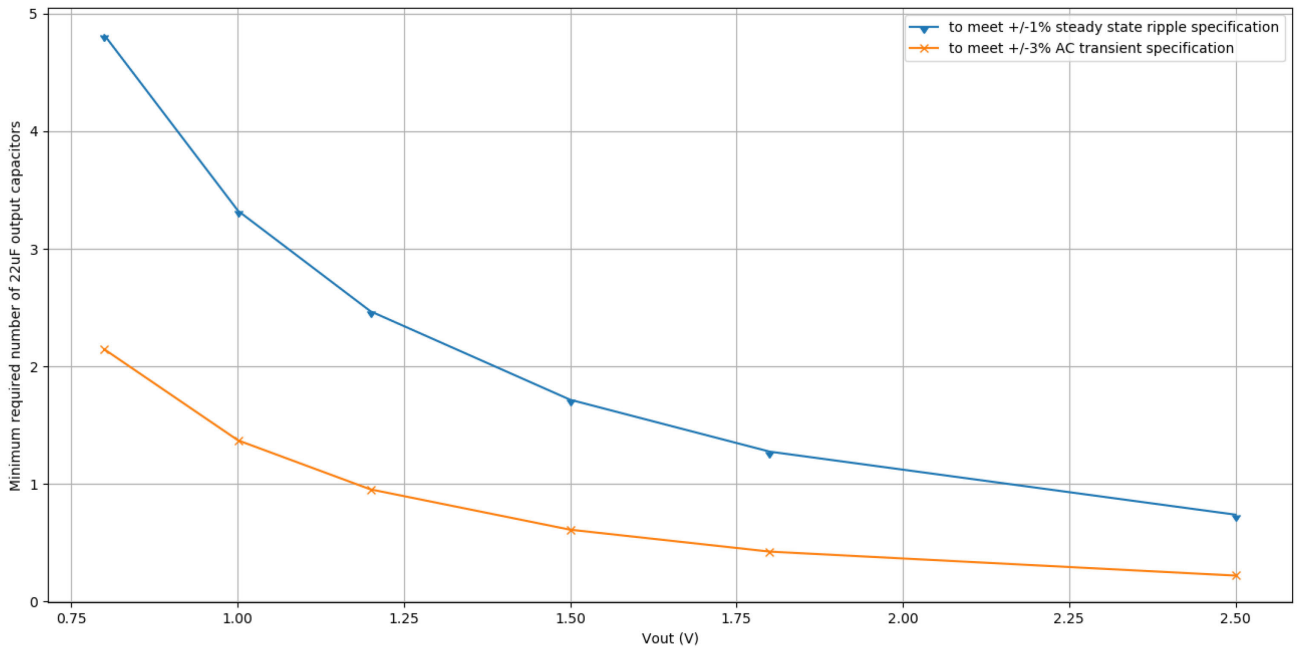


Figure 18 Minimum output capacitance

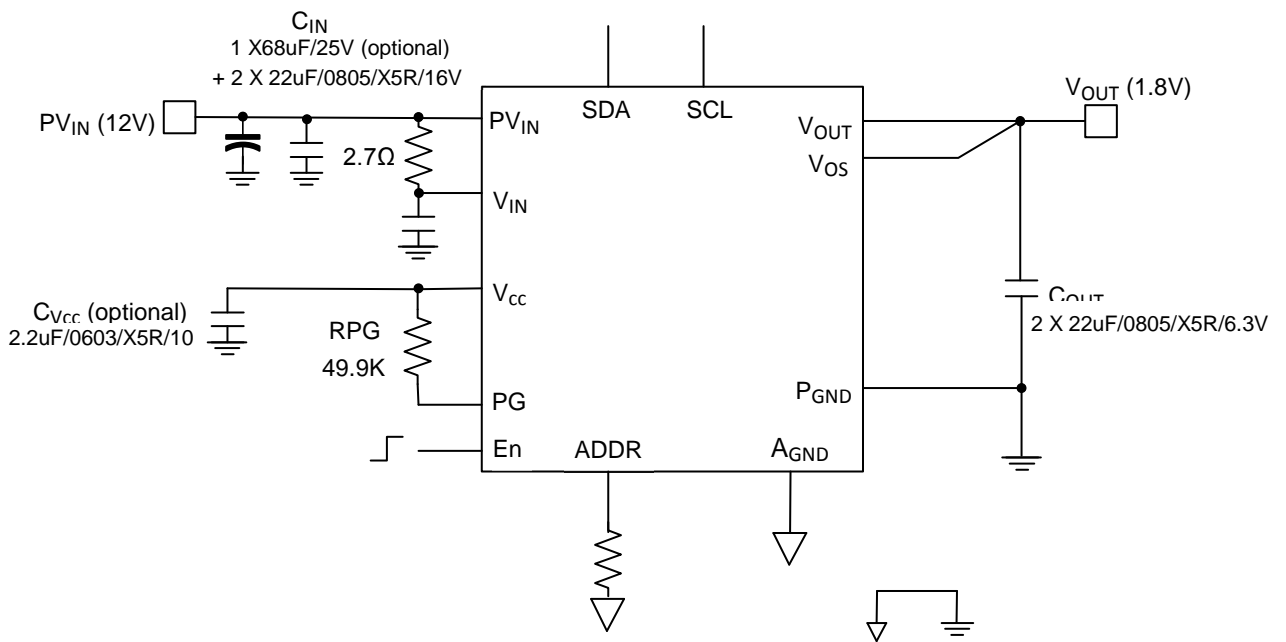


Figure 19 Application circuit for a single supply, PV<sub>IN</sub>=12V, V<sub>OUT</sub>=1.8V, 6A

## Typical operating waveforms

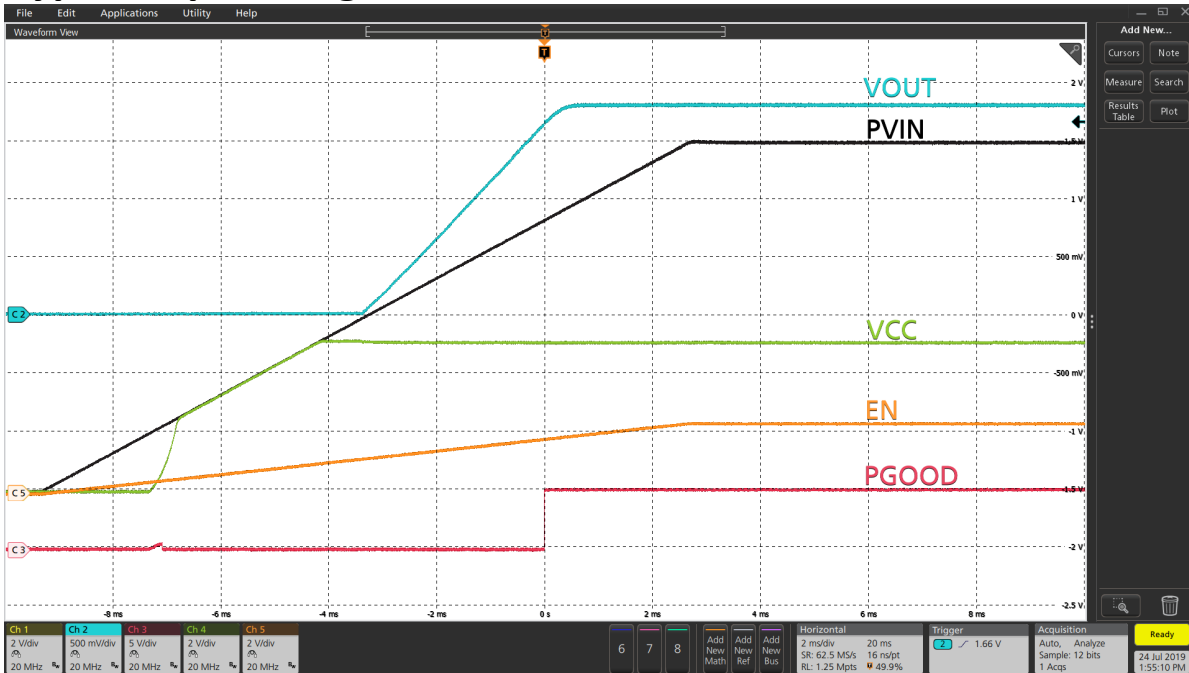


Figure 20 Startup with no load (Ch1:PV<sub>IN</sub>, Ch2: V<sub>OUT</sub>, Ch3: PGood, Ch4:V<sub>CC</sub> Ch5: Enable)

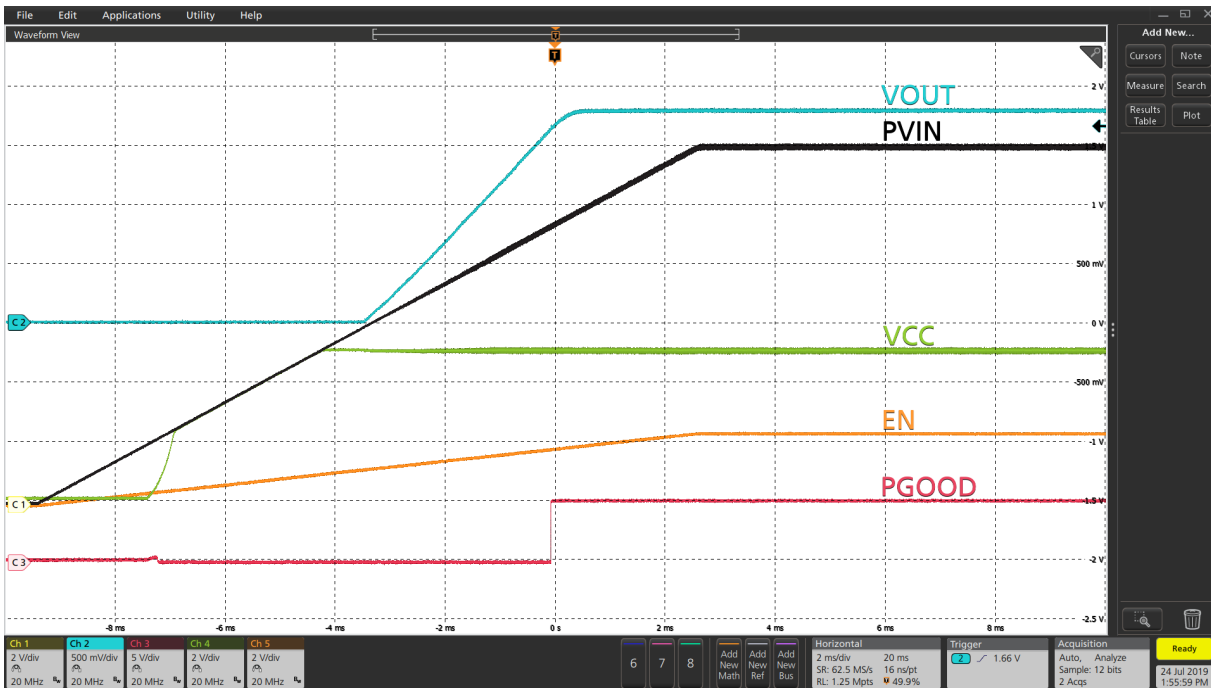
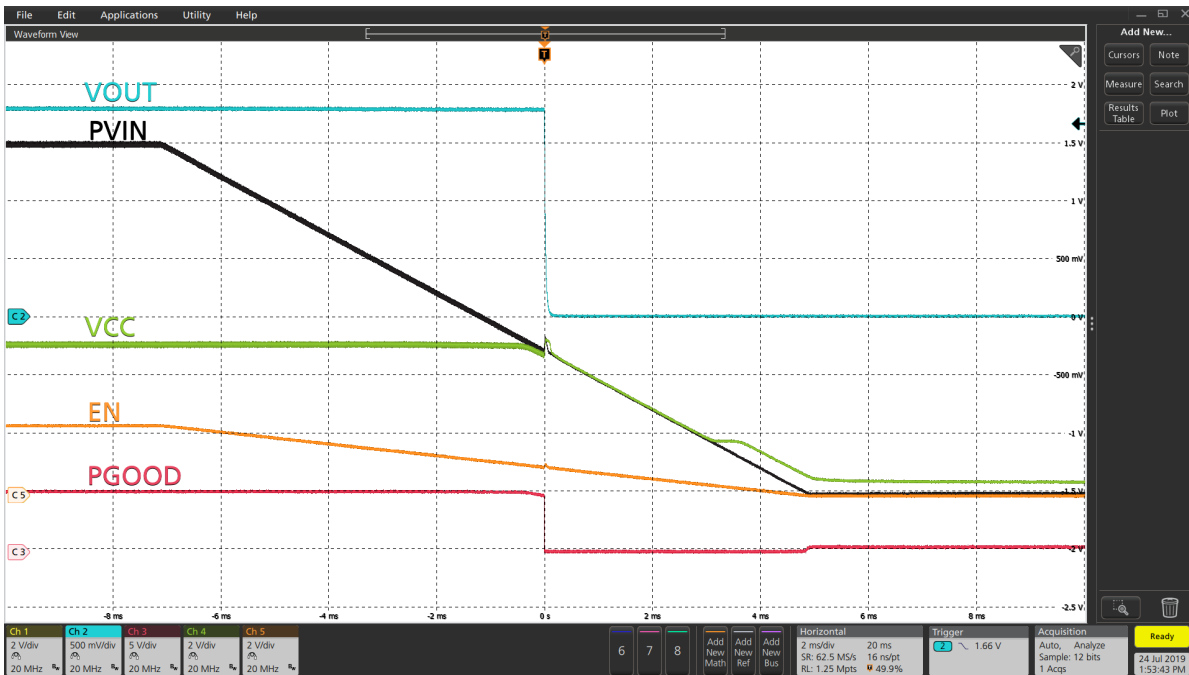
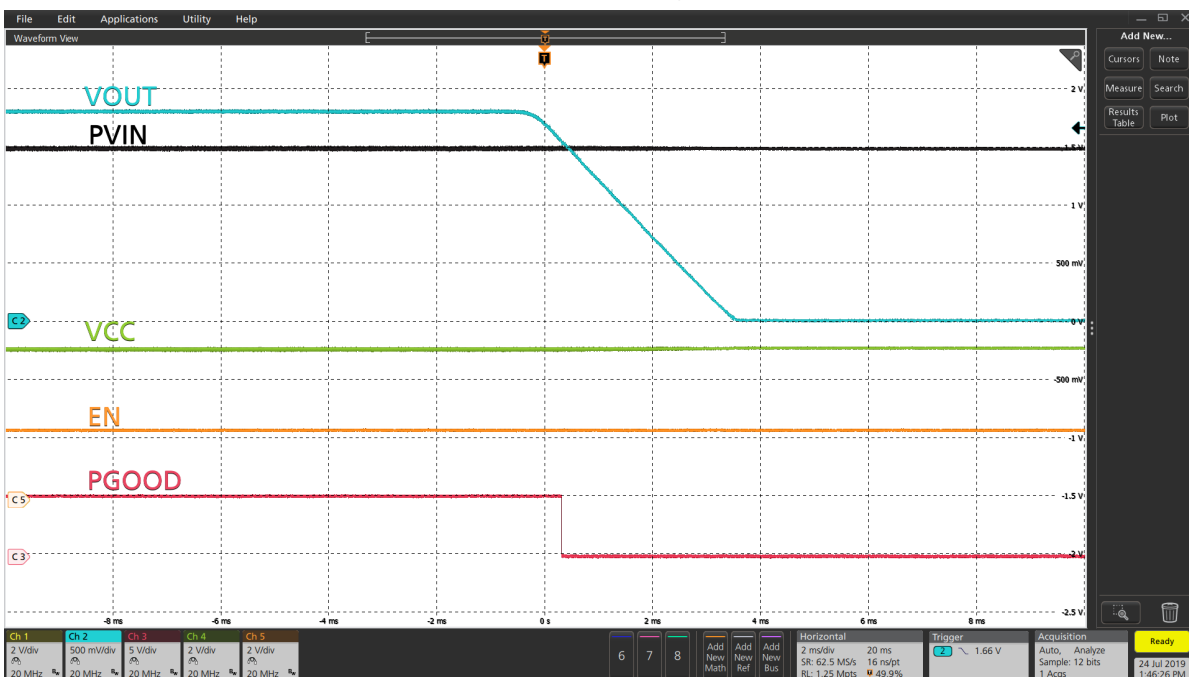


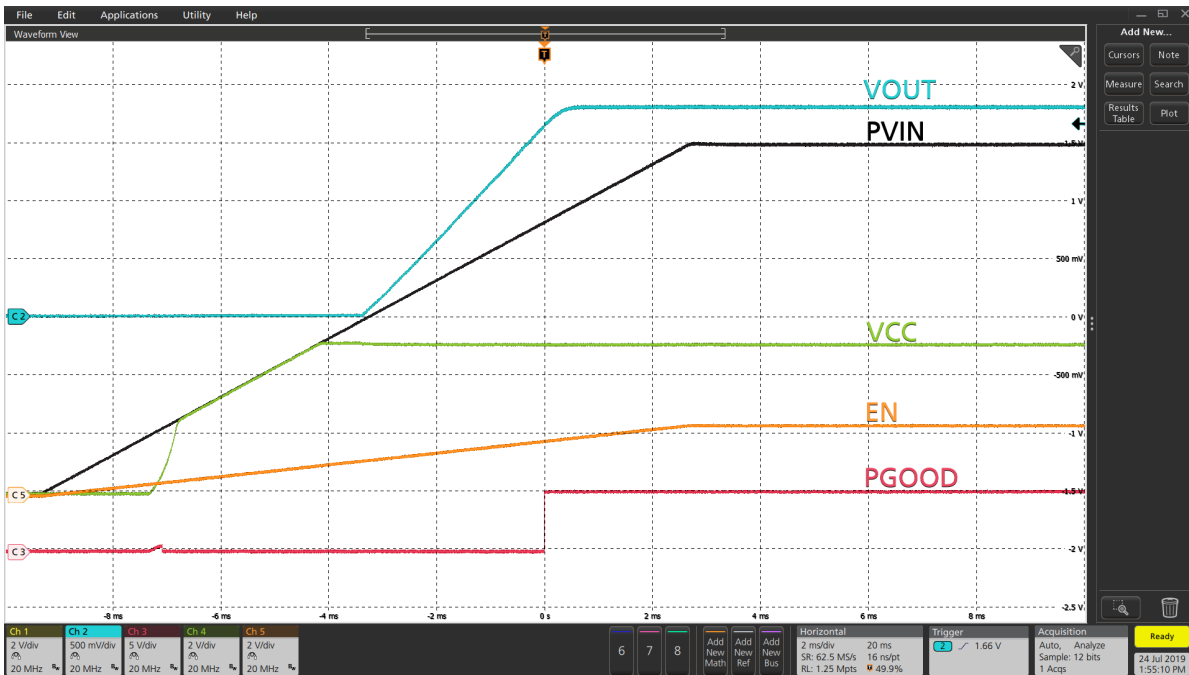
Figure 21 Startup with 6 A load (Ch1:PV<sub>IN</sub>, Ch2: V<sub>OUT</sub>, Ch3: PGood, Ch4:V<sub>CC</sub> Ch5: Enable)



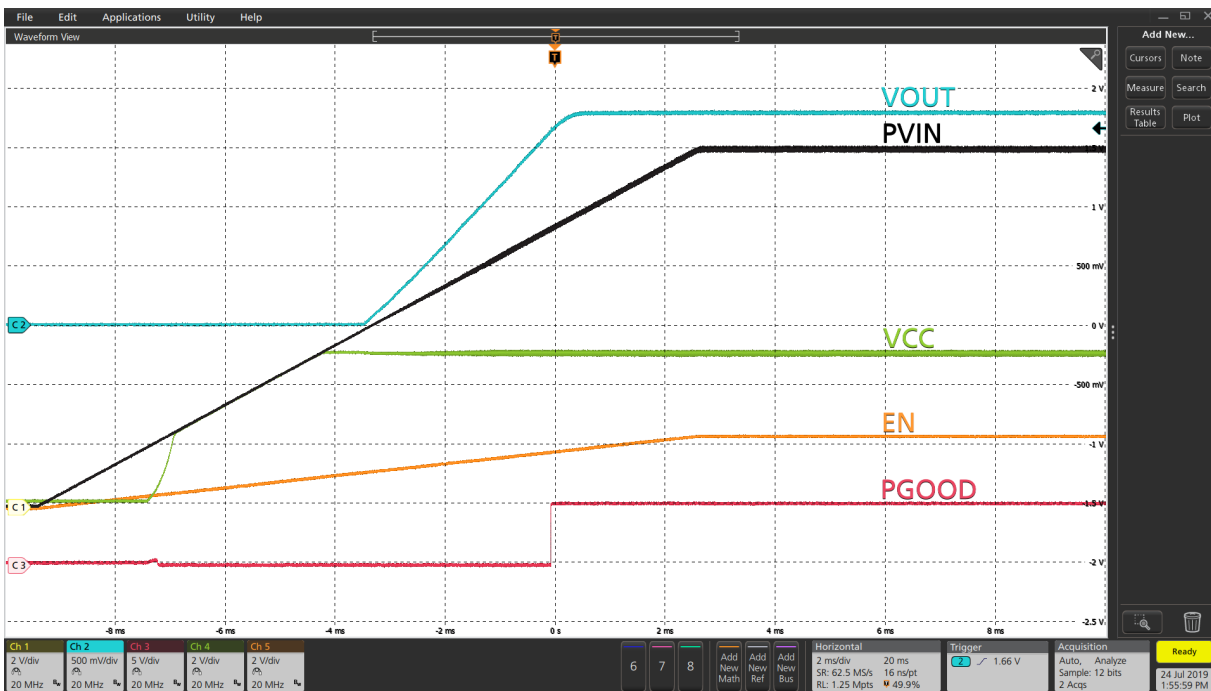
**Figure 22 Shutdown with Enable de-assertion at 6A load (Ch1:PV<sub>IN</sub>, Ch2: V<sub>OUT</sub>, Ch3: PGood, Ch4:V<sub>CC</sub>, Ch5: Enable)**



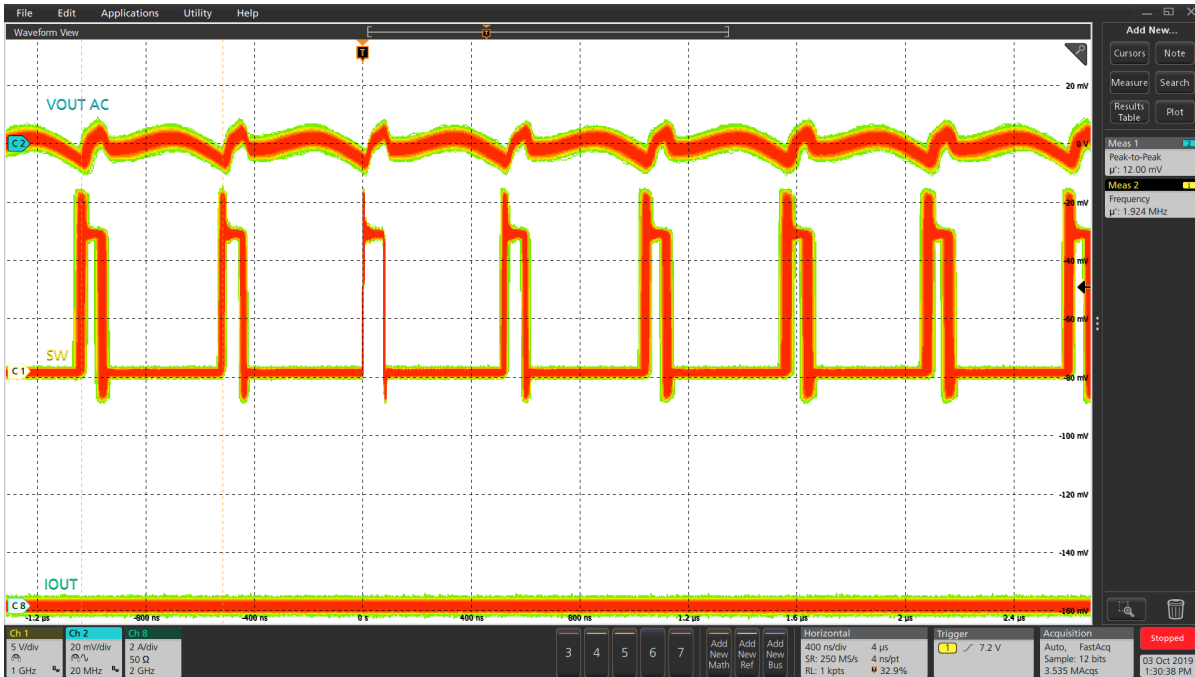
**Figure 23 Soft turn off at no load (Ch1:PV<sub>IN</sub>, Ch2: V<sub>OUT</sub>, Ch3: PGood, Ch4:V<sub>CC</sub>, Ch5: Enable)**



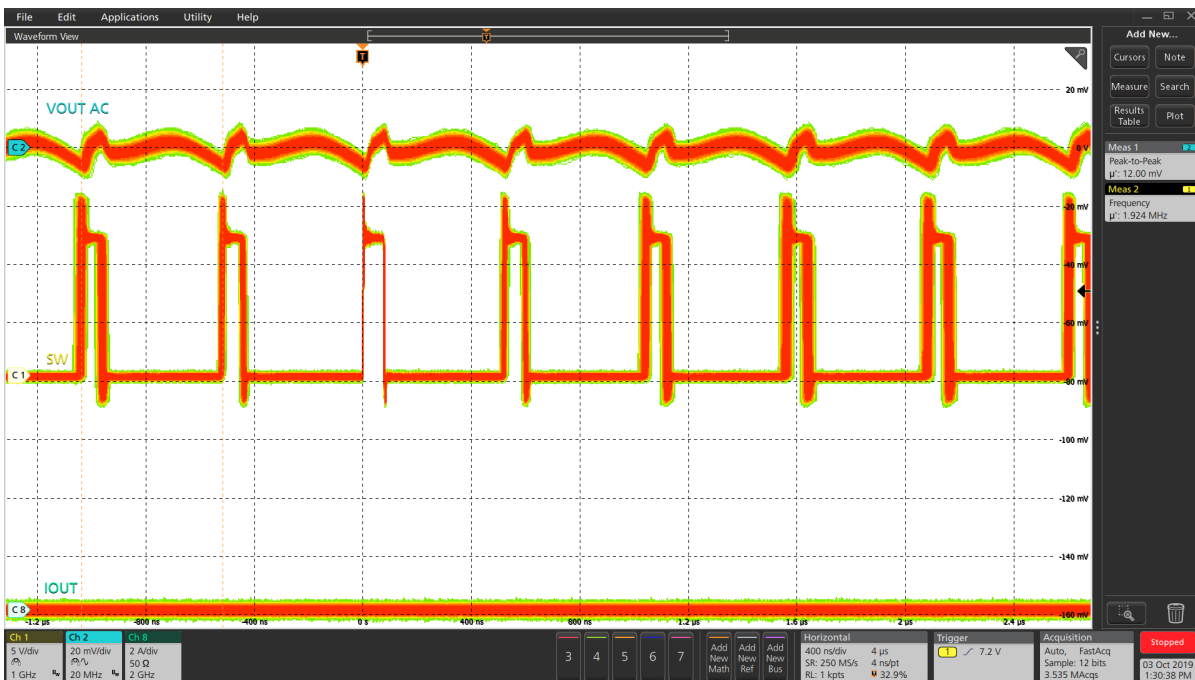
**Figure 24 Startup with no load (Ch1:PV<sub>IN</sub>, Ch2: V<sub>OUT</sub>, Ch3: PGood, Ch4:V<sub>CC</sub> Ch5: Enable)**



**Figure 25 Startup with 6 A load (Ch1:PV<sub>IN</sub>, Ch2: V<sub>OUT</sub>, Ch3: PGood, Ch4:V<sub>CC</sub> Ch5: Enable)**



**Figure 26**  $V_O$  ripple at 0A (Ch8:I<sub>o</sub>, Ch1: Sw, Ch2: V<sub>OUT</sub>), Peak-Peak  $V_O$  ripple=12mV



**Figure 27**  $V_O$  ripple at 6A (Ch8:I<sub>o</sub>, Ch1: Sw, Ch2: V<sub>out</sub>), Peak-Peak  $V_O$  ripple=15.19mV

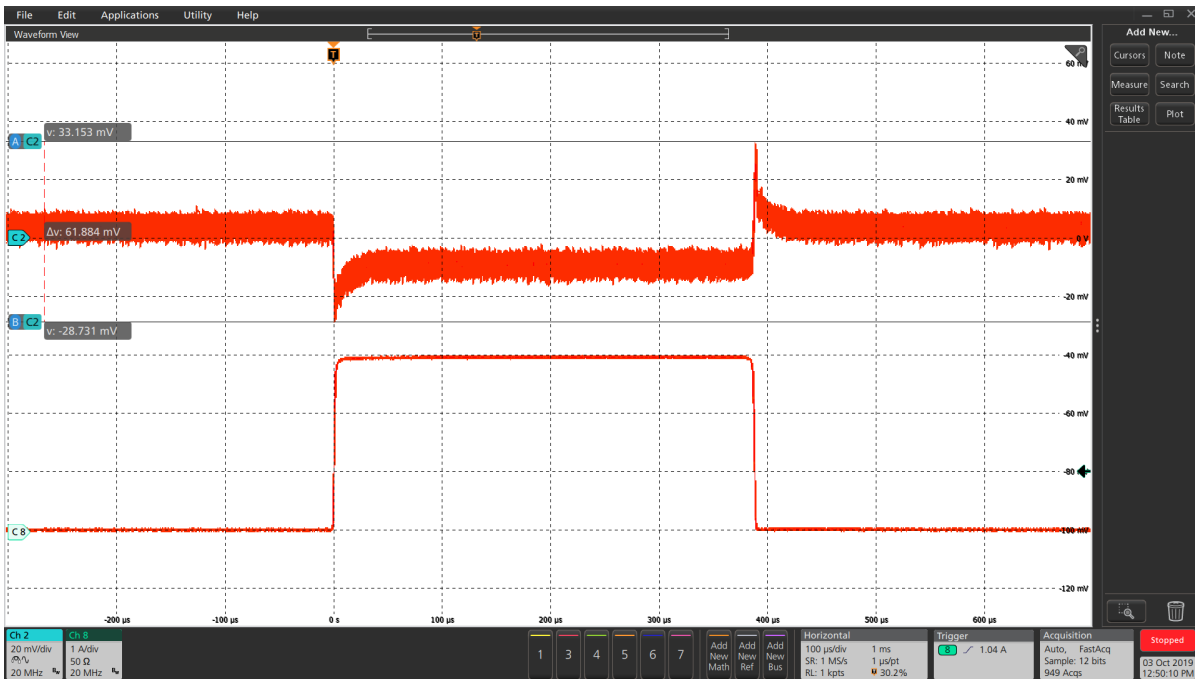


Figure 28 Transient response 0A to 3A (Ch6:  $I_O$ , Ch2:  $V_{OUT}$ ), peak-peak deviation=62mV

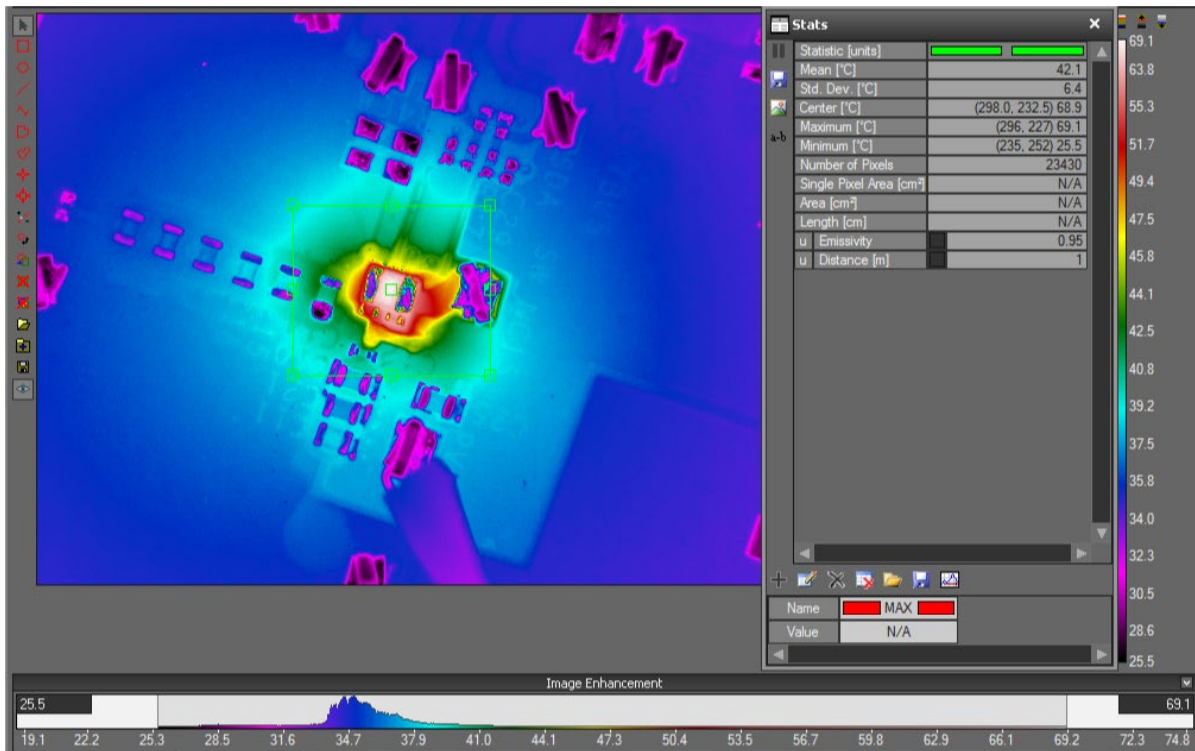


Figure 29 Thermal image at  $PV_{IN} = 12V$ ,  $V_{OUT} = 1.8V$ ,  $I_O = 6A$ , room temperature, no airflow, FS1406 maximum temperature = 69°C

## Layout recommendations

FS1406 is a highly integrated device with very few external components, which simplifies PCB layout. However, to achieve the best performance, these general PCB design guidelines should be followed:

- Bypass capacitors, including input/output capacitors and the  $V_{CC}$  bypass capacitor (if used), should be placed as close as possible to the FS1406 pins.
- Output voltage should be sensed with a separated trace directly from the output capacitor.
- Analog ground and power ground are connected through a single-point connection.
- To aid thermal dissipation, the PGnd pad should be connected to the power ground plane using vias. Copper-filled vias are preferred but plated-through-hole vias are acceptable, provided that they are not filled with resin or covered with solder mask.
- Adequate numbers of vias should be used to make connections between layers, especially for the power traces.
- To minimize power losses and thermal dissipation, wide copper polygons should be used for input and output power connections.
- SCL and SDA traces must be at least 10mil wide, with 20–30mil spacing between them.

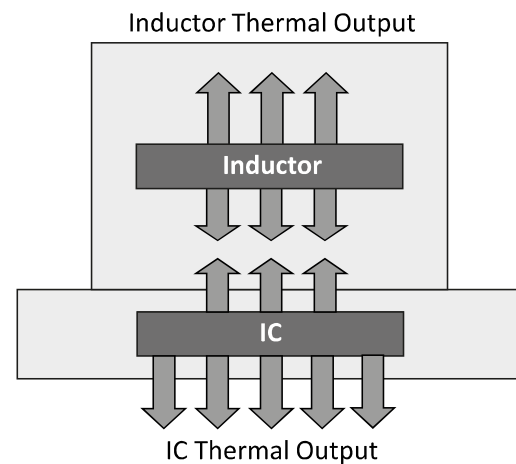
## Thermal considerations

The FS1406 has been thermally tested and modelled in accordance with JEDEC specifications JESD 51-2A and JESD 51-8. It has been tested using a 4-layer application PCB, with thermal vias under the device to assist cooling (for details of the PCB, refer to the application notes).

The FS1406 has two significant sources of heat:

- The power MOSFET section of the IC
- The inductor

The IC is well coupled to the PCB, which provides its primary cooling path. Although the inductor is also connected to the PCB, its primary cooling path is through convection. The cooling process for both heat sources is ultimately through convection. The PCB can be seen as a heat-spreader or, to some degree, a heat-sink.



**Figure 30 Heat sources in the FS1406**

Figure 31 shows the thermal resistances in the FS1406, where:

- $\Theta_{JA}$  is the measure of natural convection from the assembled test sample within a confined enclosure of approximately 30x30x30cm. The air is passive within this environment and the only air movement is due to convection from the device on test.
- $\Theta_{Jcbottom}$  is the heat flow from the IC to the bottom of the package, to which it is well coupled. The testing method adopts the method outlined in JESD 51-8, where the test PCB is clamped between cold plates at defined distances from the device.
- $\Theta_{Jctop}$  is theoretically the heat flow from the IC to the top of the package. This is not representative for the FS1406 for two reasons: firstly, it is not the primary conduction path of the IC and, more importantly, the inductor is positioned directly over the IC. As the inductor is a heat source, generating a similar amount of heat to the IC, a meaningful value for junction-to-case (top) cannot be derived.

The values of the thermal resistances are:

- $\Theta_{JA} = 22.6^{\circ}\text{C/W}$
- $\Theta_{Jcbottom} = 2.36^{\circ}\text{C/W}$

Although these values indicate how the FS1406 compares with similar point-of-load products tested using the same conditions and specifications, they cannot be used to predict overall thermal performance. For accurate modeling of the  $\mu$ POL<sup>TM</sup>'s interaction with its environment, computational fluid dynamics (CFD) simulation software is needed to calculate combined routes of conduction and convection simultaneously.

Note: In all tests, airflow has been considered as passive or static; applications using forced air may achieve a greater cooling effect.

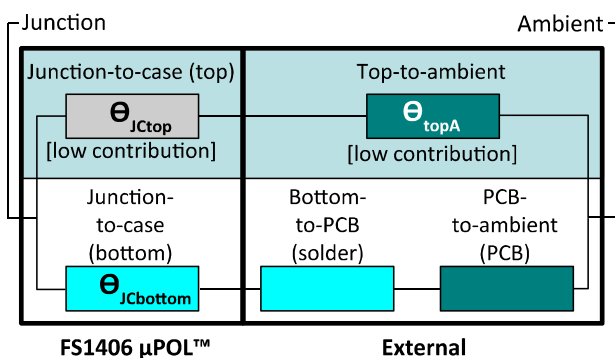


Figure 31 Thermal resistances of the FS1406



## I<sup>2</sup>C protocol

S = Start bit  
 P = Stop bit  
 A = Ack  
 N = Nack

W = Write bit ('1')  
 R = Read ('0')  
 Sr = Repeated start

White bits = Issued by master  
 Grey bits = Sent by slave (FS140x)

### Write transaction

1            7            1   1            8            1            8            1   1

S	Slave Address	W	A	Register Address	A	Data Byte	A	P
---	---------------	---	---	------------------	---	-----------	---	---

### Read transaction

1            7            1   1            8            1   1            7            1   1            8            1   1

S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A	Data Byte	N	P
---	---------------	---	---	------------------	---	----	---------------	---	---	-----------	---	---

## Reflow profiles

TDK does not recommend specific reflow profiles for use with its  $\mu$ PoL products. Many factors influence the selection of an ideal reflow profile. Each PCB should be profiled in accordance with the solder paste manufacturer’s recommendations.

Figure 32 shows reflow profiles similar to the one that has been used successfully in mounting  $\mu$ PoL products to PCBs. The linear profile is recommended as a starting point. The soak profile can be useful in two situations:

- For PCBs with uneven loads (areas of high and low component density) – the soak profile allows more time for the PCB to reach an even temperature over its entire area.
- For PCBs with surfaces that are more difficult to solder – the soak profile allows the flux more time to act on the surfaces to be soldered.

To ensure that TDK’s  $\mu$ PoL products can be soldered using standard lead-free reflowing parameters, they have been tested using reflow profiles with peak temperatures up to 260°C. Most solder paste manufacturers do not recommend using profiles with peak temperatures over 250°C.

To ensure that TDK’s  $\mu$ PoL products solder well within lead-free environments, they are finished with ENiG (Electroless-Nickel-Gold). The nickel can be considered as a barrier layer: it forms a thin but reliable intermetallic with tin. This is in contrast to copper, which dissolves quickly in tin-rich lead-free solders: one reflow operation may dissolve 4 $\mu$ m of copper, potentially causing problems.

When profiling the PCB, remember that many components (not only TDK’s  $\mu$ PoL products) may use surface finishes that contain nickel. Profiles that use temperatures above 220°C for very short times, which may have been derived to reduce copper consumption, may not give sufficient time for nickel to form a good intermetallic layer.

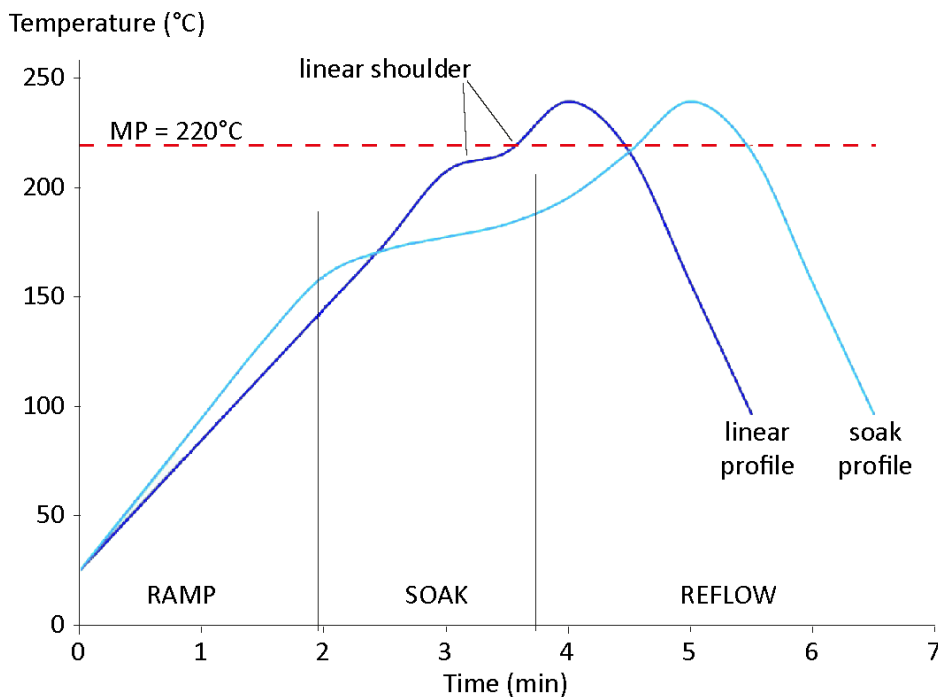


Figure 32 Reflow profile

## Package description

The FS1406 is designed for use with standard surface-mount technology (SMT) population techniques. It has a positive (raised) footprint, with the pads being higher than the surrounding substrate. The finish on the pads is ENiG.

As a result of these properties, the FS1406 works extremely well in lead-free environments. The surface wets easily and the positive footprint accommodates processing variations.

Note: Refer to the Design Guidelines for more information about TDK's  $\mu$ POL<sup>TM</sup> package series.

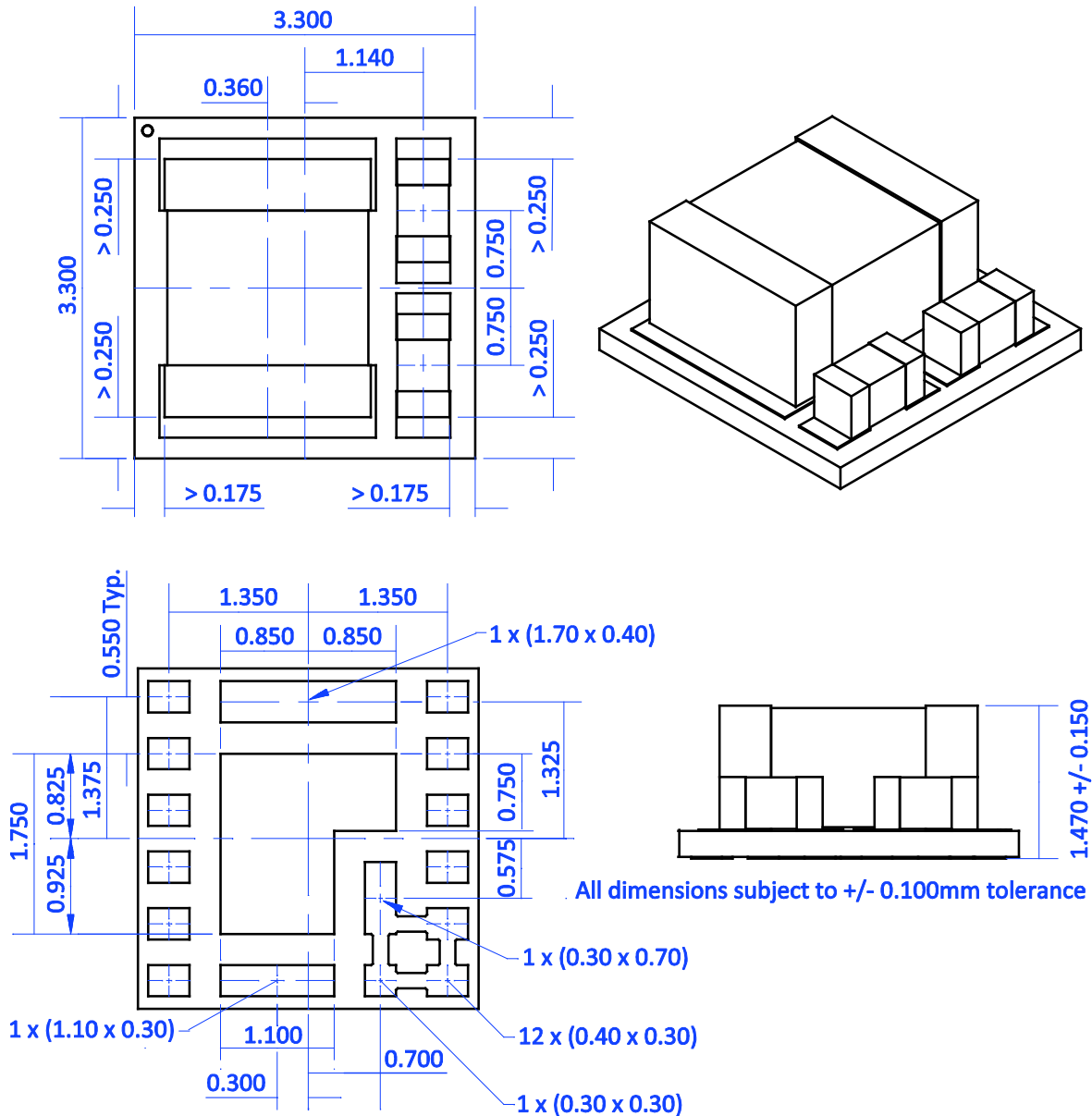
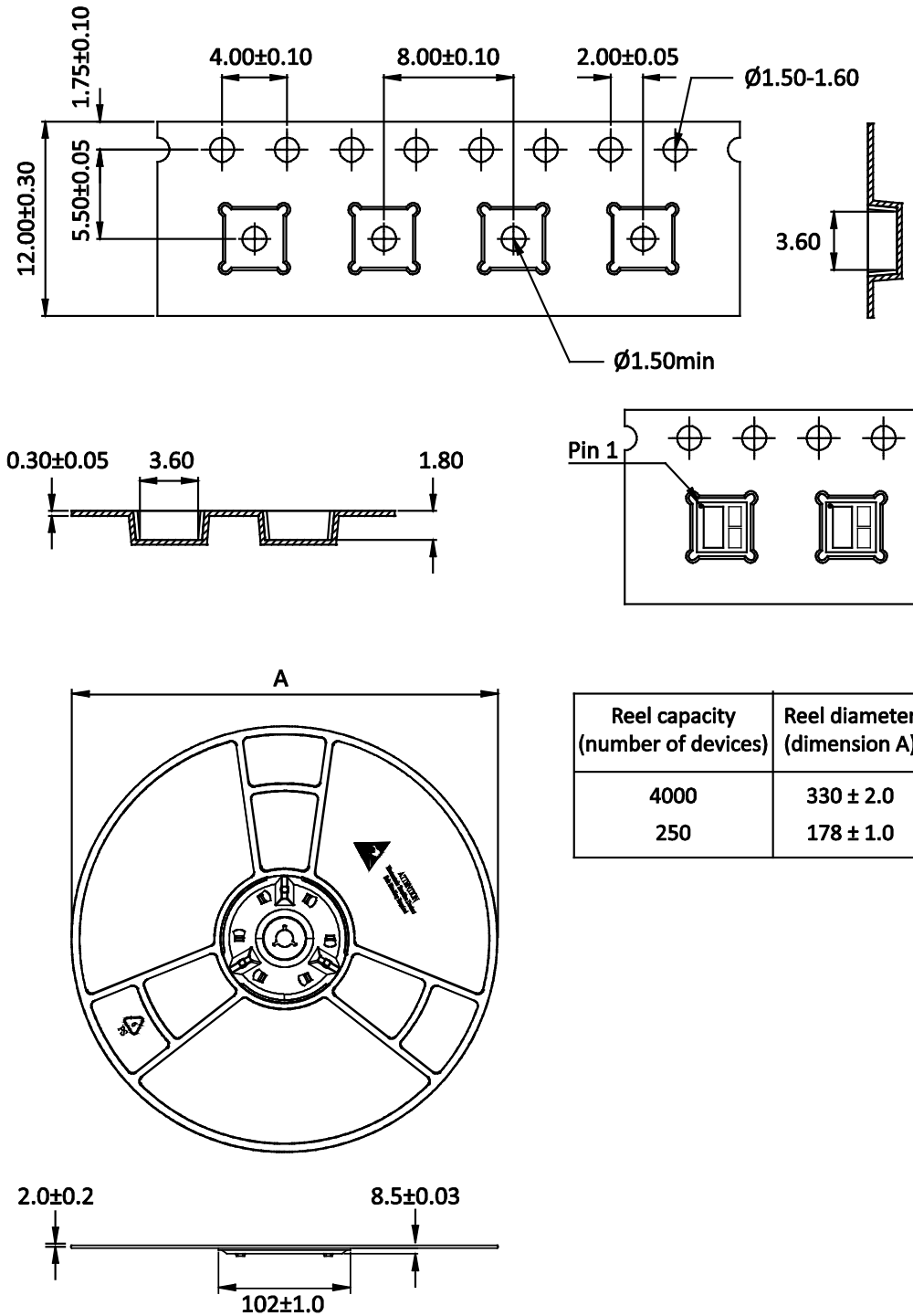


Figure 33 Dimensioned drawings



**Figure 34** Tape and reel pack