

M74HC244P**M74HC244DWP****OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER****DESCRIPTION**

The M74HC244 is a semiconductor integrated circuit consisting of two blocks of 3-state non-inverting buffers each with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output: ($I_{OL}=6\text{mA}$, $I_{OH}=-6\text{mA}$)
- High-speed: 10ns typ. ($C_L=50\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation: $20\mu\text{W}/\text{package (max)}$ ($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- High noise margin: 30% of V_{CC} , min ($V_{CC}=4.5\text{V}$, 6V)
- Capable of driving 15 LSTTL loads
- Wide operating voltage range: $V_{CC}=2\sim6\text{V}$
- Wide operating temperature range: $T_a=-40\sim+85^\circ\text{C}$

APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTIONAL DESCRIPTION

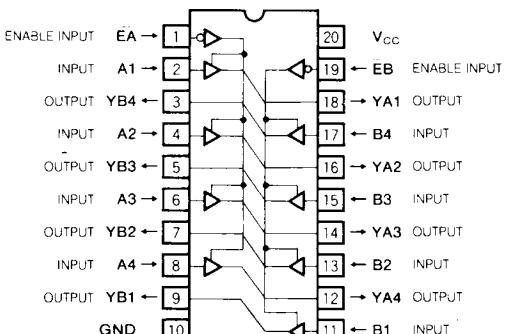
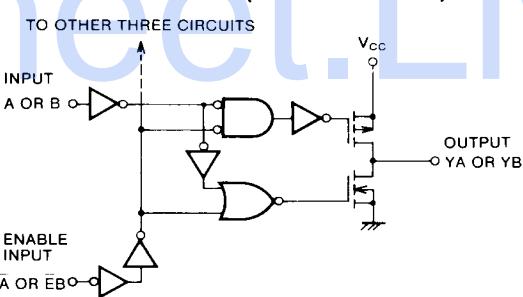
Use of silicon gate technology allows the M74HC244 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244.

The M74HC244 consists of two independent blocks with each block containing four buffers.

When enable input E is low and input A (or B) is low then output Y will become low. However, if A (or B) is high then Y will become high.

When E is high then all outputs within the block will become high-impedance state, irrespective of A (or B).

All eight buffer circuits can be controlled simultaneously by connecting \bar{EA} and \bar{EB} of the two blocks.

PIN CONFIGURATION (TOP VIEW)Outline 20P4
20P2V**LOGIC DIAGRAM (EACH BUFFER)****FUNCTION TABLE (Note 1)**

Inputs		Outputs
A, B	EA, EB	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -40\sim+85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7.0	V
V_i	Input voltage		-0.5~ $V_{CC}+0.5$	V
V_o	Output voltage		-0.5~ $V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_i < 0\text{V}$	-20	mA
		$V_i > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_o < 0\text{V}$	-20	mA
		$V_o > V_{CC}$	20	
I_o	Output current, per output pin		± 35	mA
I_{cc}	Supply/GND current	V_{CC}, GND	± 75	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature range		-65~+150	°C

Note 2 : M74HC244DWP, $T_a = -40\sim+80^\circ\text{C}$ and $T_a = 80\sim85^\circ\text{C}$ are derated at $-7\text{mW}/\text{C}$

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER**RECOMMENDED OPERATING CONDITIONS** ($T_a = -40\sim+85^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature range	-40		+85	°C
t_r, t_f	Input risetime, falltime	$V_{CC} = 2.0\text{V}$	0	1000	ns
		$V_{CC} = 4.5\text{V}$	0	500	
		$V_{CC} = 6.0\text{V}$	0	400	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits					Unit
			25°C			-40~+85°C		
V_{IH}	High-level input voltage	$V_O = V_{CC}-0.1\text{V}$ $ I_O = 20\mu\text{A}$	2.0	1.5			1.5	V
			4.5	3.15			3.15	
			6.0	4.2			4.2	
V_{IL}	Low-level input voltage	$V_O = 0.1\text{V}, V_{CC}-0.1\text{V}$ $ I_O = 20\mu\text{A}$	2.0			0.5	0.5	V
			4.5			1.35	1.35	
			6.0			1.8	1.8	
V_{OH}	High-level output voltage	$V_I = V_{IH}, V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9		1.9	V
			$I_{OH} = -20\mu\text{A}$	4.5	4.4		4.4	
			$I_{OH} = -20\mu\text{A}$	6.0	5.9		5.9	
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	$I_{OL} = -6.0\text{mA}$	4.5	4.18		4.13	V
			$I_{OL} = -7.8\text{mA}$	6.0	5.68		5.63	
			$I_{OL} = 20\mu\text{A}$	2.0		0.1	0.1	
I_{IH}	High-level input current	$V_I = 6\text{V}$	$I_{OL} = 20\mu\text{A}$	4.5		0.1	0.1	μA
			$I_{OL} = 20\mu\text{A}$	6.0		0.1	0.1	
			$I_{OL} = 20\mu\text{A}$	6.0		0.1	0.1	
I_{IL}	Low-level input current	$V_I = 0\text{V}$	$I_{OL} = 6.0\text{mA}$	4.5		0.26	0.33	μA
			$I_{OL} = 7.8\text{mA}$	6.0		0.26	0.33	
I_{OZH}	Off-state high-level output current	$V_I = V_{IH}, V_{IL}, V_O = V_{CC}$	$I_{OL} = 6.0\text{mA}$		0.5		5.0	μA
			$I_{OL} = 7.8\text{mA}$			-0.5	-5.0	
I_{OZL}	Off-state low-level output current	$V_I = V_{IH}, V_{IL}, V_O = \text{GND}$	$I_{OL} = 6.0\text{mA}$			-0.5	-5.0	μA
			$I_{OL} = 7.8\text{mA}$					
I_{CC}	Quiescent supply current	$V_I = V_{CC}, \text{GND}, I_O = 0\mu\text{A}$	$I_{OL} = 6.0\text{mA}$			4.0	40.0	μA
			$I_{OL} = 7.8\text{mA}$					

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^\circ C$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L = 50\text{pF}$ (Note 4)			10	ns
t_{THL}					10	
t_{PLH}					20	
t_{PHL}					20	
t_{PLZ}	Output disable time from low-level and high-level ($\bar{EA} - YA$, $\bar{EB} - YB$)	$C_L = 5 \text{ pF}$ (Note 4)			25	ns
t_{PHZ}					25	
t_{PZL}	Output enable time to low-level and high-level ($EA - YA$, $EB - YB$)	$C_L = 50\text{pF}$ (Note 4)			28	ns
t_{PZH}					28	

SWITCHING CHARACTERISTICS ($V_{CC} = 2\text{--}6V$, $T_a = -40\text{--}+85^\circ C$)

Symbol	Parameter	Test conditions	Limits					Unit
			25°C		-40~+85°C			
	$V_{CC}(\text{V})$	Min	Typ	Max	Min	Max		
t_{TLH}	Low-level to high-level and high-level to low-level output transition time	$C_L = 50\text{pF}$ (Note 4)	2.0		60		75	ns
t_{THL}			4.5		12		15	
t_{PLH}			6.0		10		13	
t_{PHL}	Low-level to high-level and high-level to low-level output propagation time ($A - YA$, $B - YB$)	$C_L = 50\text{pF}$ (Note 4)	2.0		60		75	ns
t_{PLZ}			4.5		12		15	
t_{PHZ}			6.0		10		13	
t_{PZL}			2.0		115		145	
t_{PZH}			4.5		23		29	
t_{PLZ}			6.0		20		25	
t_{PLH}	$C_L = 150\text{pF}$ (Note 4)		2.0		115		145	ns
t_{PHL}			4.5		23		29	
t_{PZL}			6.0		20		25	
t_{PZH}			2.0		165		208	
t_{PLZ}			4.5		33		42	
t_{PHZ}			6.0		28		35	
t_{PLH}	$C_L = 50\text{pF}$ (Note 4)		2.0		165		208	ns
t_{PHL}			4.5		33		42	
t_{PZL}			6.0		28		35	
t_{PZH}			2.0		150		189	
t_{PLZ}			4.5		30		38	
t_{PHZ}			6.0		26		32	
t_{PLH}	$C_L = 50\text{pF}$ (Note 4)		2.0		150		189	ns
t_{PHL}			4.5		30		38	
t_{PZL}			6.0		26		32	
t_{PZH}			2.0		150		189	
t_{PLZ}			4.5		30		38	
t_{PHZ}			6.0		26		32	
C_I	Input capacitance					10	10	pF
C_O	Three-state output capacitance	$EA = V_{CC}$, $EB = V_{CC}$				15	15	
C_{PD}	Power dissipation capacitance (Note 3)					57		

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per buffer)

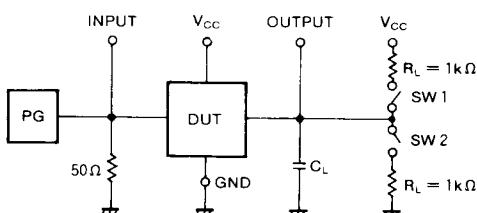
The power dissipated during operation under no-load conditions is calculated using the following formula:

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$$



OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

Note 4 : Test Circuit



Parameter	SW 1	SW 2
t_{TLH}, t_{THL}	Open	Open
t_{PLH}, t_{PHL}	Close	Open
t_{PLZ}	Open	Close
t_{PHZ}	Close	Open
t_{PZL}	Open	Open
t_{PZH}	Open	Close

(1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r = 6\text{ns}$, $t_f = 6\text{ns}$ (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.**TIMING DIAGRAM**