

# MC100LVELT22

## 3.3V Dual LVTTTL/LVCMOS to Differential LVPECL Translator

The MC100LVELT22 is a dual LVTTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

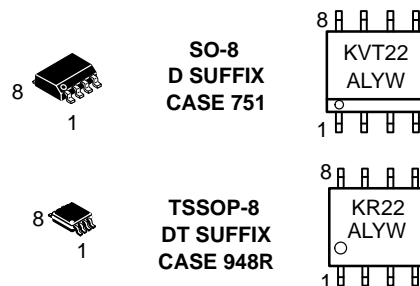
- 350 ps Typical Propagation Delay
- <100 ps Output-to-Output Skew
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $GND = 0\text{ V}$
- When Unused TTL Input is left Open, Q Output will Default High



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAMS\*



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional marking information, see Application Note AND8002/D.

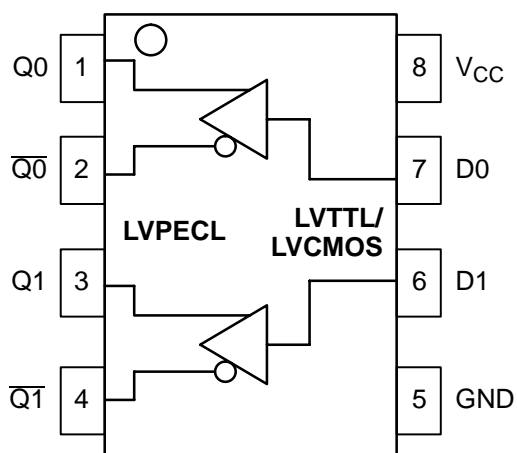
### ORDERING INFORMATION

Device	Package	Shipping**
MC100LVELT22D	SO-8	98 Units/Rail
MC100LVELT22DR2	SO-8	2500 Units/Reel
MC100LVELT22DT	TSSOP-8	98 Units/Rail
MC100LVELT22DTR2	TSSOP-8	2500 Units/Reel

\*\*For additional tape and reel information, see Brochure BRD8011/D.

Datasheet.Live

## MC100LVELT22



**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

### PIN DESCRIPTION

PIN	FUNCTION
Qn, $\overline{Qn}$	LVPECL Differential Outputs
D0, D1	LVTTTL/LVCMOS Inputs
V <sub>CC</sub>	Positive Supply
GND	Ground

### ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model
	> 4 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	164
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

# MC100LVELT22

## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		7	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	7	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	SO-8 SO-8	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	SO-8	41 to 44 ± 5%	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	TSSOP-8	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

## LVPECL DC CHARACTERISTICS V<sub>CC</sub> = 3.3 V; GND = 0.0 V (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>CC</sub>	Power Supply Current			28			28			29	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 4)	2275		2420	2275		2420	2275		2420	mV
V <sub>OL</sub>	Output LOW Voltage (Note 4)	1490		1680	1490		1680	1490		1680	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

3. Output parameters vary 1:1 with V<sub>CC</sub>. V<sub>CC</sub> can vary ±0.15 V.

4. Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

## LVTTTL/LVC MOS INPUT DC CHARACTERISTICS V<sub>CC</sub> = 3.3 V; T<sub>A</sub> = -40°C to 85°C (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>IN</sub> = 2.7 V
I <sub>IHH</sub>	Input HIGH Current			100	μA	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>IL</sub>	Input LOW Current			-0.2	mA	V <sub>IN</sub> = 0.5 V
V <sub>IK</sub>				-1.2	V	I <sub>IN</sub> = -18 mA
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	

5. V<sub>CC</sub> can vary ±0.15 V.

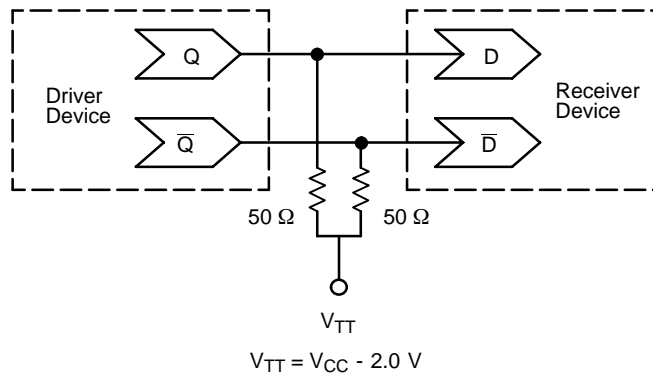
## AC CHARACTERISTICS V<sub>CC</sub> = 3.3 V; GND = 0.0 V (Note 6)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>max</sub>	Maximum Toggle Frequency				350						MHz
t <sub>PLH</sub>	Propagation Delay (Note 7)	200	350	600	200	350	600	200	350	600	ps
t <sub>skew</sub>	Skew Output-to-Output Part-to-Part		30	100 400		30	100 400		30	100 400	ps
t <sub>JITTER</sub>	Random Clock Jitter (RMS)					1.6					ps
t <sub>r</sub> /t <sub>f</sub>	Output Rise/Fall Time (20-80%)	200		550	200		500	200		500	ps

6. V<sub>CC</sub> can vary ±0.15 V.

7. Specifications for standard TTL input signal.

## MC100LVELT22



**Figure 1. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020 - Termination of ECL Logic Devices.)**

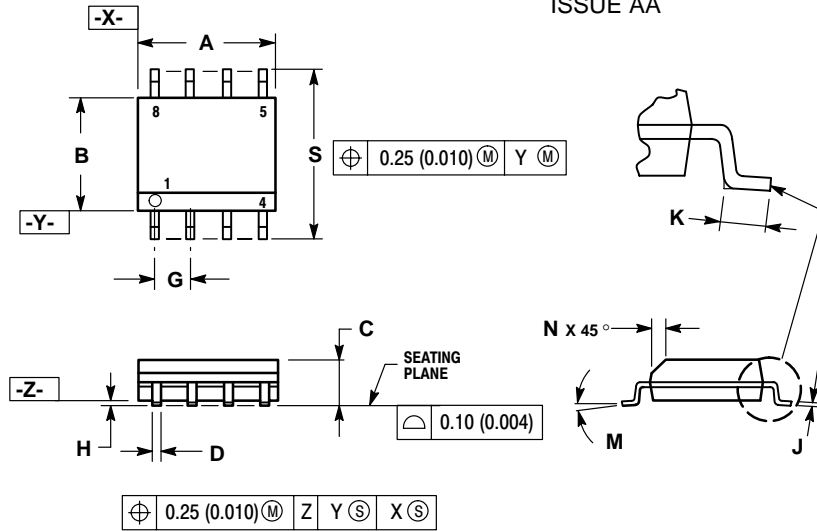
### Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices
- AND8090** - AC Characteristics of ECL Devices

# MC100LVELT22

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-07  
ISSUE AA



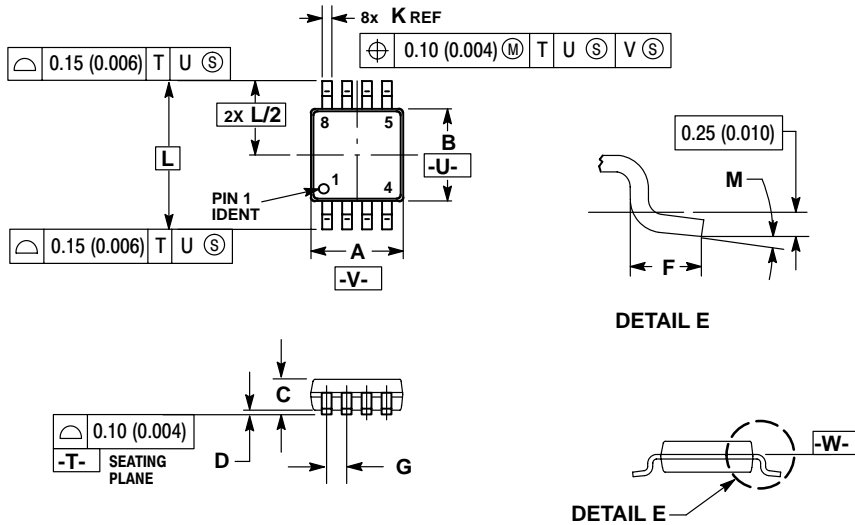
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

# MC100LVELT22

## PACKAGE DIMENSIONS


TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.