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DSP56F801EVMUM/D
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56F801 Evaluation Module

Hardware User's Manual

MOTOROLA digital dna

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Preface

This reference manual describes in detail the hardware on the 56F801 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Motorola 56F801 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction -** provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary -** describes in detail the 56F801hardware.
- **Appendix A, 56F801EVM Schematics -** contains the schematics of the 56F801EVM.
- **Appendix B, 56F801EVM Bill of Material -** provides a list of the materials used on the 56F801EVM board.

Suggested Reading

More documentation on the 56F801 and the 56F801EVM kit may be found at URL:

http://www.motorola.com/semiconductors

Notation Conventions

This manual uses the following notational conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	$\overline{WE}$ $\overline{OE}$	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a "$" symbol	$0FF0 $80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter "b" attached to the number	b1010 b0011	
Blue Text	Linkable on-line	...refer to Chapter 7, License	
Bold	Reference sources, paths, emphasis	...see: **http://www.motorola.com/**	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

A/D Analog-to-Digital
D/A Digital-to-Analog
EVM Evaluation Module
GPIO General Purpose Input and Output Port
IC Integrated Circuit
JTAG Joint Test Action Group, a bus protocol/interface used for test and debug
LQFP Low-profile Quad Flat Pack
MPIO Multi Purpose Input and Output Port, shares package pins with other peripherals on the chip and can function as a GPIO
OnCE™ On-Chip Emulation, a debug bus and port created by Motorola to enable designers to create a low-cost hardware interface for a professional-quality debug environment
PCB Printed Circuit Board

PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface Port
SRAM	Static Random Access Memory

References

The following sources were referenced to produce this manual:

[1] *DSP56800 Family Manual*, Motorola, DSP56800FM/D

[2] *DSP56F801/803/805/807 User's Manual*, Motorola, DSP56F801-7UM/D

[3] *56F801 Technical Data*, Motorola, DSP56F801/D

Chapter 1
Introduction

The 56F801EVM is used to demonstrate the abilities of the 56F801 and to provide a hardware tool allowing the development of applications that use the 56F801.

The 56F801EVM is an evaluation module board that includes a 56F801 part, peripheral expansion connectors, external memory and a JTAG interface. The expansion connectors are for signal monitoring and user feature expandability.

The 56F801EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the 56F801EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full-speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the device's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the chip are available to the user.

1.1 56F801EVM Architecture

The 56F801EVM facilitates the evaluation of various features present in the 56F801 part. The 56F801EVM can be used to develop real-time software and hardware products based on the 56F801. The 56F801EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The 56F801EVM is flexible enough to allow a user to fully exploit the 56F801's features to optimize the performance of their product, as shown in **Figure 1-1**.

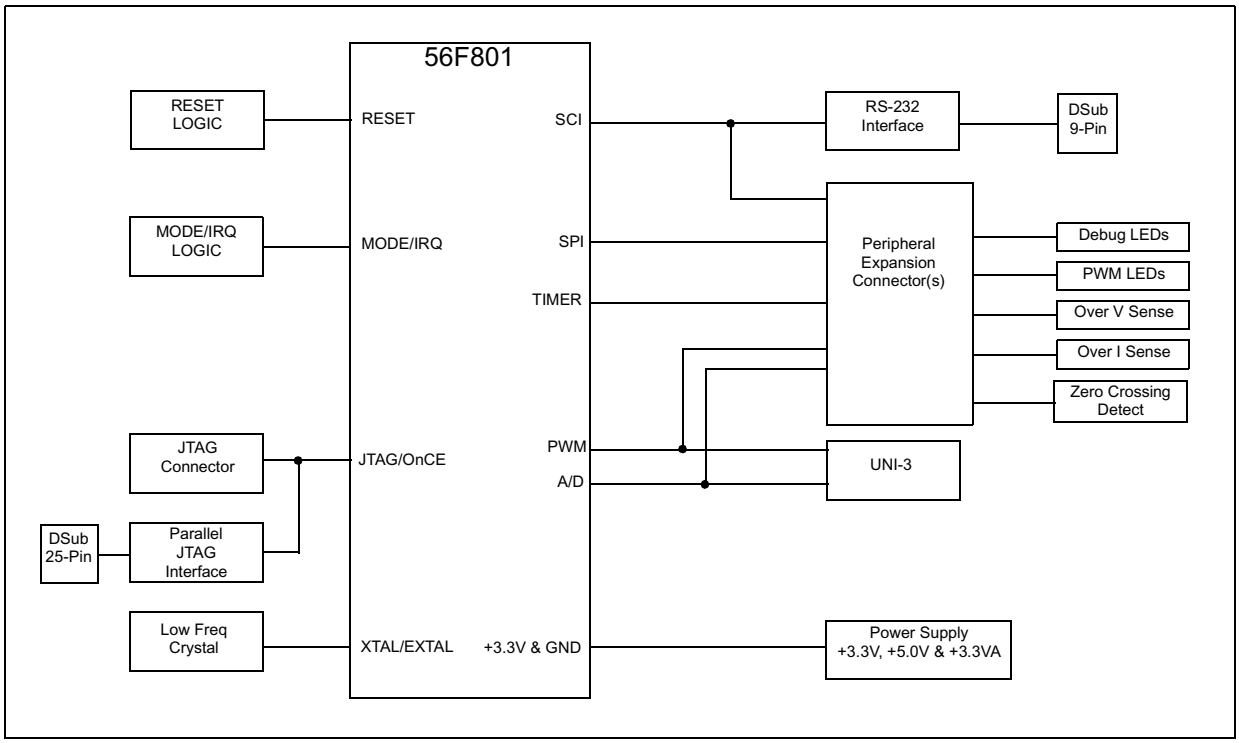

Figure 1-1. Block Diagram of the 56F801EVM

1.2 56F801EVM Configuration Jumpers

Nine jumper groups, (JG1-JG9), shown in **Figure 1-2**, are used to configure various features on the 56F801EVM board. **Table 1-1** describes the default jumper group settings.

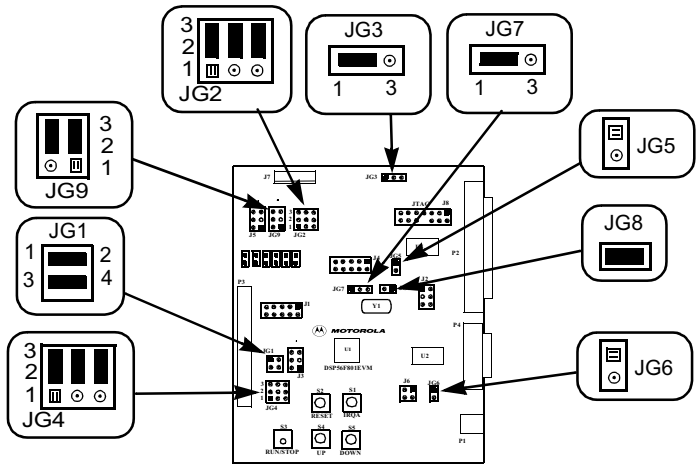

Figure 1-2. 56F801EVMJumper Reference

Table 1-1. 56F801EVM Default Jumper Options

Jumper Group	Comment	Jumpers Connections
JG1	UNI-3 serial selected	1–2, 3–4
JG2	Encoder Input Selected	2–3, 5–6 & 8–9
JG3	UNI-3 Over-Voltage Selected for FAULT0	1–2
JG4	UNI-3 3-Phase Current Sense Selected as inputs to A/D	2–3, 5–6 & 8–9
JG5	Enable on-board Parallel JTAG Host/Target Interface	NC
JG6	Enable RS-232 output	NC
JG7	Use on-board EXTAL crystal input for hybrid controller oscillator	1-2
JG8	Use on-board XTAL crystal input for hybrid controller oscillator	1–2
JG9	Encoder Input Selected to TD1 and TD2	2–3, 5–6

1.3 56F801EVM Connections

An interconnection diagram is shown in **Figure 1-3** for connecting the PC and the external +12V DC power supply to the 56F801EVM board.

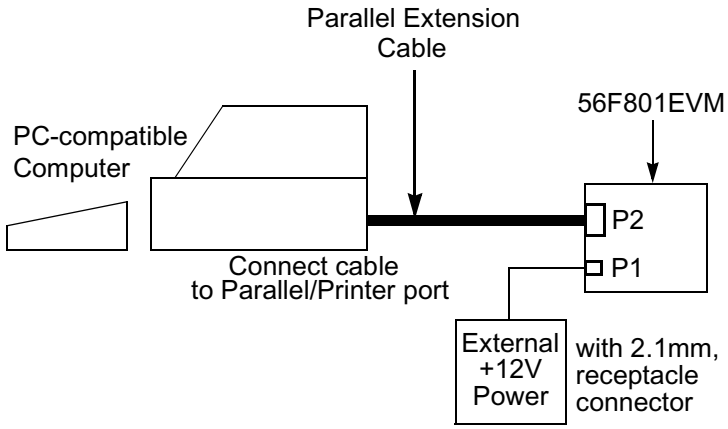

Figure 1-3. Connecting the 56F801EVM Cables

Perform the following steps to connect the 56F801EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer.
2. Connect the other end of the parallel extension cable to P2, shown in **Figure 1-3**, on the 56F801EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 4.0A power supply is not plugged into a 120V AC power source.
4. Connect the 2.1mm output power plug from the external power supply into P1, shown in **Figure 1-3**, on the 56F801EVM board.
5. Apply power to the external power supply. The green Power-On LED, LED8, will illuminate when power is correctly applied.

Chapter 2
Technical Summary

The 56F801EVM is designed as a versatile hybrid controller development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, servo and motor control, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F801 device, combined with the Hall-Effect/Quadrature Encoder interface, motor zero crossing logic, motor bus over-current logic, motor bus over-voltage logic and parallel JTAG interface, makes the 56F801EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F801 processor.

The main features of the 56F801EVM, with board and schematic reference designators include:

- 56F801 16-bit +3.3V hybrid controller operating at 80MHz [U1]
- 8.00MHz crystal oscillator for frequency generation [Y1]
- Optional external oscillator frequency input connector [JG7 and JG8]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J8]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P2]
- RS-232 interface for easy connection to a host processor [U2 and P4]
- Connector to allow the user to connect their own SCI / MPIO-compatible peripheral [J6]
- Connector to allow the user to connect their own SPI / MPIO-compatible peripheral [J3]
- Connector to allow the user to connect their own PWM or MPIO-compatible peripheral [J1]
- Connector to allow the user to connect their own Timer D/ MPIO-compatible peripheral [J5]

- Connector to allow the user to attach their own A/D port-compatible peripheral [J4]
- On-board power regulation from an external 12V DC-supplied power input [P1]
- Light Emitting Diode (LED) power indicator [LED8]
- One on-board real-time user debugging LED [LED7]
- Six on-board PWM monitoring LEDs [LED1-6]
- UNI-3 Motor interface [P3]
  - — Encoder/Hall-Effect interface and selector [JG2 & JG9]
  - — Over-Voltage sensing [U6]
  - — Over-Current sensing [U6]
  - — Back-EMF sensing and selector [JG4]
  - — Zero Crossing detection and selector [JG2 & JG9]
  - — Pulse Width Modulation
- Manual RESET push button [S2]
- Manual interrupt push button for $\overline{\text{IRQA}}$ [S1]
- General purpose push-button on AN6 for Speed UP [S4]
- General purpose push button on AN6 for Speed DOWN [S5]
- General purpose toggle switch for RUN/STOP control(AN7) [S3]

2.1 56F801

The 56F801EVM uses a Motorola DSP56F801FV80 part, designated as U1 on the board and in the schematics. This part will operate at a maximum speed of 80MHz. A full description of the 56F801, including functionality and user information, is provided in these documents:

- *56F801 Technical Data*, (DSP56F801/D)**:** Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements and available packaging.
- *DSP56F801/803/805/807 User's Manual*, (DSP56F801-7UM/D): Provides an overview description of the hybrid controller and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control/status register descriptions for each subsystem.
- *DSP56F800 Family Manual*, (DSP56F800FM/D): Provides a detailed description of the core processor, including internal status and control registers and a detailed description of the family instruction set.

Refer to these documents for detailed information about chip functionality and operation. They can be found on this URL:

http://www.motorola.com/semiconductors

2.2 RS-232 Serial Communications

The 56F801EVM provides an RS-232 interface by the use of an RS-232 level converter, (Maxim MAX3245EEAI, designated as U2). Refer to the RS-232 schematic diagram in **Figure 2-3**. The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232 compatible signal levels and connects to the host's serial port via connector P4. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The pinout of connector P4 is listed in **Table 2-1**. The RS-232 level converter/transceiver can be disabled by placing a jumper at JG6.

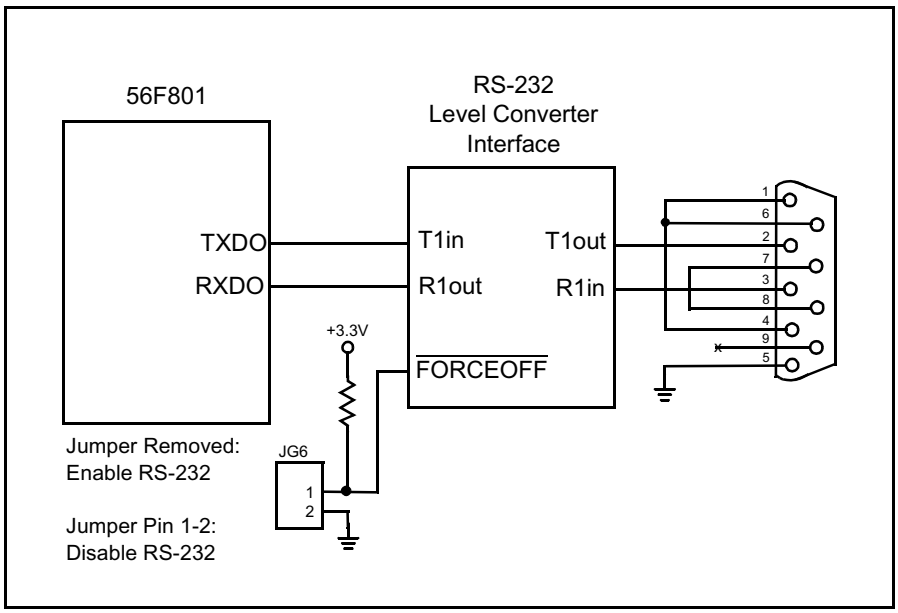

Figure 2-1. Block Diagram of the RS-232 Interface

Table 2-1. RS-232 Serial Connector Description

P4			
Pin #	**Signal**	**Pin #**	**Signal**
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD	7	Jumper to 8
3	RXD	8	Jumper to 7
4	Jumper to 1 & 6	9	N/C
5	GND		

2.3 Clock Source

The 56F801EVM uses an 8.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. The 56F801 uses its internal PLL to multiply the input frequency by 10, to achieve its 80MHz maximum operating frequency. An external oscillator source can be connected to the device by using the oscillator bypass connector, JG7 and JG8; see **Figure 2-2**.

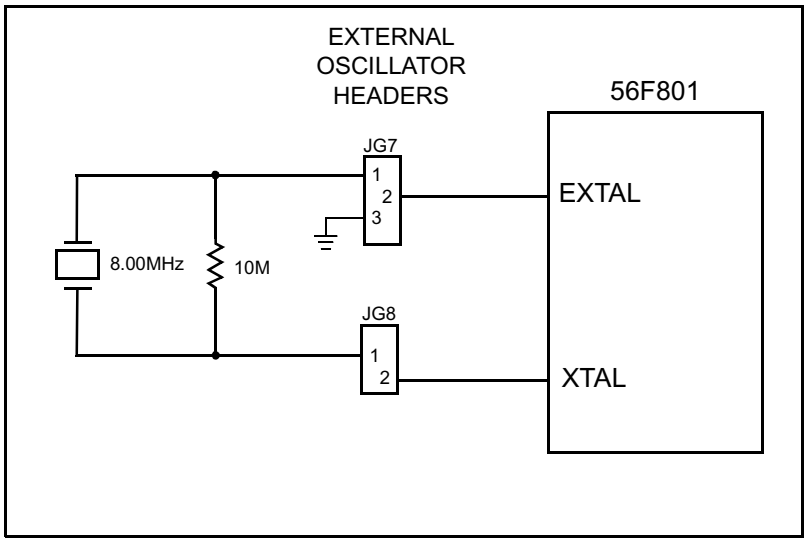

Figure 2-2. Block Diagram of the Clock Interface

2.4 Debug LEDs

One on-board Light-Emitting Diode (LED) is provided to allow real-time debugging for user programs. This LED allows the programmer to monitor program execution without having to stop the program during debugging; refer to **Figure 2-3**. This user LED, designated LED7, is controlled by the MOSI signal. Setting the MOSI to a Logic One value will turn on the LED.

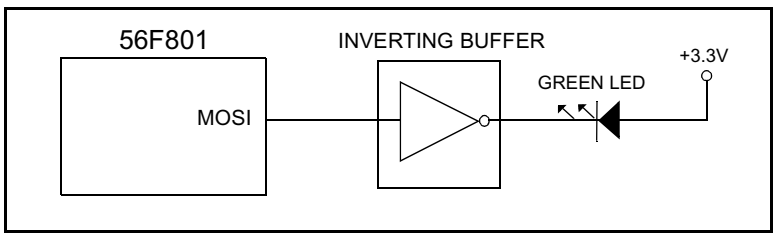

Figure 2-3. Block Diagram of the Debug LED Interface

2.5 Debug Support

The 56F801EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.5.1 JTAG Connector

The JTAG connector on the 56F801EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F801's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. **Table 2-2** shows the pin-out for this connector.

Table 2-2. JTAG Connector Description

J8			
Pin #	**Signal**	**Pin #**	**Signal**
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	NC	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG5. Reference **Table 2-3** for this jumper's selection options.

Table 2-3. Parallel JTAG Interface Disable Jumper Selection

JG5	Comment
No jumpers	On-board Parallel JTAG Interface Enabled
1–2	Disable on-board Parallel JTAG Interface

2.5.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P2, allows the 56F801 to communicate with a Parallel Printer Port on a Windows PC; reference **Figure 2-4**. By using this connector, the user can download programs and work with the 56F801's registers. **Table 2-4** shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG5 should be removed, as shown in **Table 2-3**.

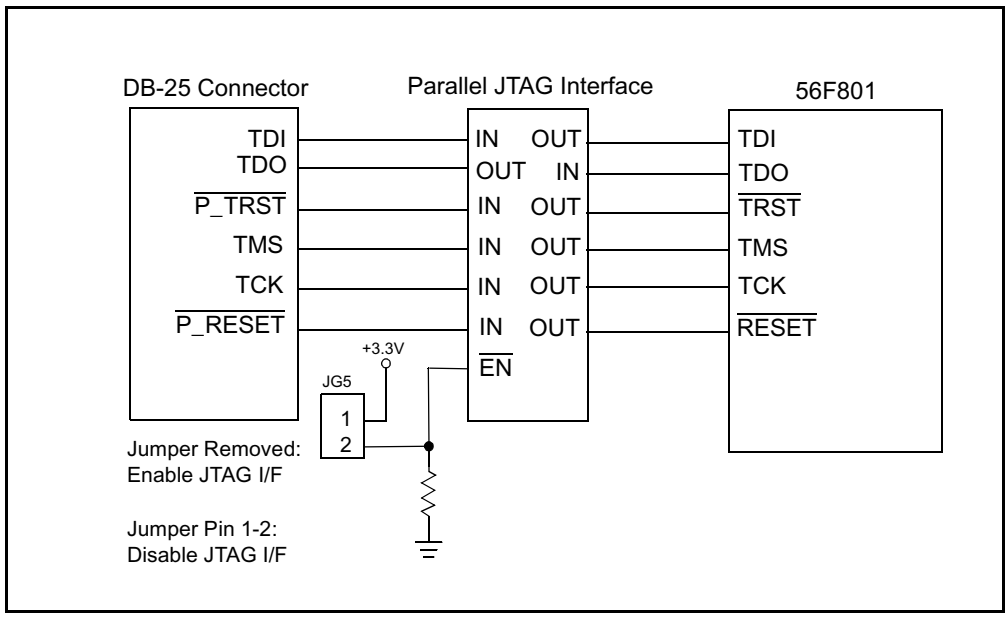

Figure 2-4. Block Diagram of the Parallel JTAG Interface

Table 2-4. Parallel JTAG Interface Connector Description

P2			
Pin #	**Signal**	**Pin #**	**Signal**
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	NC
4	PORT_TCK	17	NC
5	PORT_TDI	18	GND
6	$\overline{\text{PORT\_TRST}}$	19	GND
7	NC	20	GND
8	PORT_IDENT	21	GND

Table 2-4. Parallel JTAG Interface Connector Description

P2			
Pin #	**Signal**	**Pin #**	**Signal**
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

2.6 External Interrupt

One on-board push-button switch is provided for external interrupt generation, as shown in **Figure 2-5**. S1 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. This switch allows the user to generate interrupts for his user-specific programs.

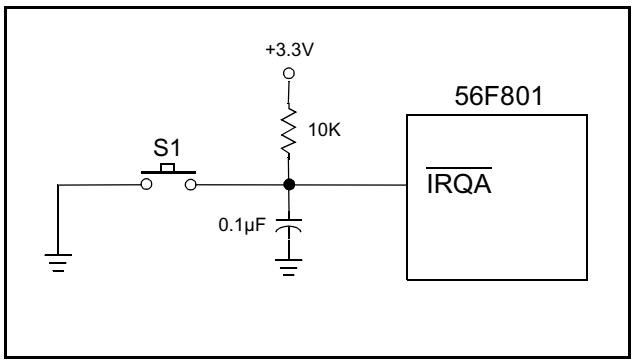

Figure 2-5. Block Diagram of the User Interrupt Interface

2.7 Reset

Logic is provided on the 56F801 to generate a clean Power-On RESET signal. Additional, reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button; refer to **Figure 2-6**.

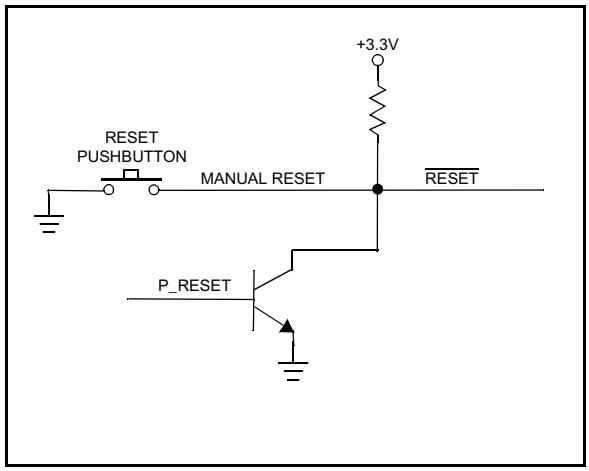

Figure 2-6. Block Diagram of the RESET Interface

2.8 Power Supply

The main power input to the 56F801EVM, +12V DC at 4.0A, is through a 2.1mm coax power jack. A 4.0A power supply is provided with the 56F801EVM; however, less than 300mA is required by the EVM. The remaining current is available for user motor control applications when connected to an optional motor power stage board. The 56F801EVM provides +3.3V DC voltage regulation for the controller, parallel JTAG interface and supporting logic; refer to **Figure 2-7**. Power applied to the 56F801EVM is indicated with a Power-On LED, referenced as LED8.

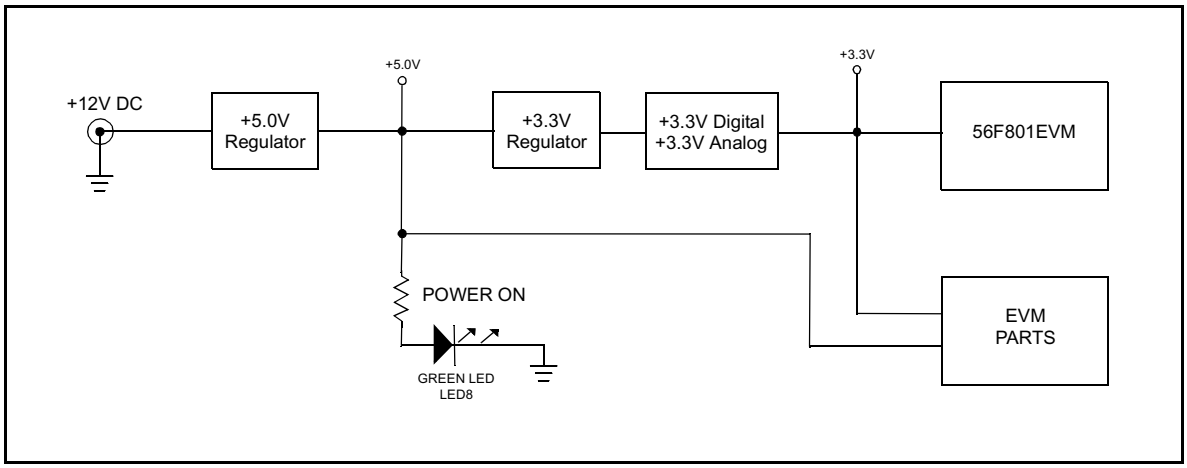

Figure 2-7. Block Diagram of the Power Supply

2.9 UNI-3 Interface

Motor control signals from a family of motor driver boards can be connected to the EVM board via the UNI-3 connector/interface. The UNI-3 connector/interface contains all of the signals needed to drive and control the motor drive boards. These signals are connected to various groups of the hybrid controller's input and output ports; A/D, TIMER and PWM. The header, JG4, is used to select between the Back-EMF and Motor Phase Current signals. Refer to **Table 2-5** for the pin out of the UNI-3 connector, P3.

Table 2-5. UNI-3 Connector Description

P3			
Pin #	**Signal**	**Pin #**	**Signal**
1	PWM_AT	2	Shield
3	PWM_AB	4	Shield
5	PWM_BT	6	Shield
7	PWM_BB	8	Shield
9	PWM_CT	10	Shield
11	PWM_CB	12	GND
13	GND	14	+5.0V DC
15	+5.0V DC	16	Analog +3.3V DC
17	Analog GND	18	Analog GND
19	Analog +15V DC	20	Analog -15V DC
21	Motor DC Bus Voltage Sense	22	Motor DC Bus Current Sense
23	Motor Phase A Current Sense	24	Motor Phase B Current Sense
25	Motor Phase C Current Sense	26	Motor Drive Temperature Sense
27	NC	28	Shield
29	Motor Drive Brake Control	30	Serial COM
31	PFC PWM	32	PFC Inhibit
33	PFC Zero Cross	34	Zero Cross A
35	Zero Cross B	36	Zero Cross C

Table 2-5. UNI-3 Connector Description (Continued)

P3			
Pin #	**Signal**	**Pin #**	**Signal**
37	Shield	38	Back-EMF Phase A Sense
39	Back-EMF Phase B Sense	40	Back-EMF Phase C Sense

2.10 Speed Up/Down Switches and Run/Stop Switch

Two push-button switches are connected to form the Speed UP/DOWN logic via a set of resistors to the A/D Port's signal AN6. The resistors create a voltage divider network presenting unique voltage to the A/D port when each push button is pressed. A RUN/STOP toggle switch is connected to A/D Port's signal AN7. Refer to **Figure 2-8**.

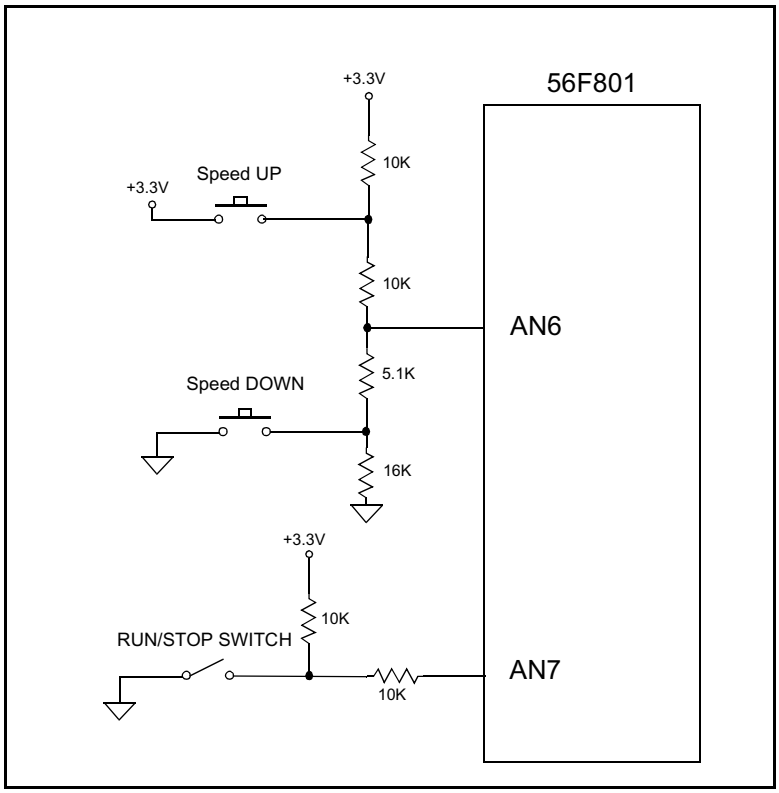

Figure 2-8. RUN/STOP and General Purpose Switches

2.11 Motor Control PWM Signals and LEDs

The 56F801 has one dedicated PWM unit. The PWM unit's lines are connected to the UNI-3 interface connector and to a set of six PWM LEDs via inverting buffers. The inverting buffers are used to isolate and drive the device's PWM's outputs to the PWM LEDs. The PWM LEDs indicate the status of PWM's signals, as shown in **Figure 2-9**. The PWM signals are routed to a header, J1, and are available for use by the end user.

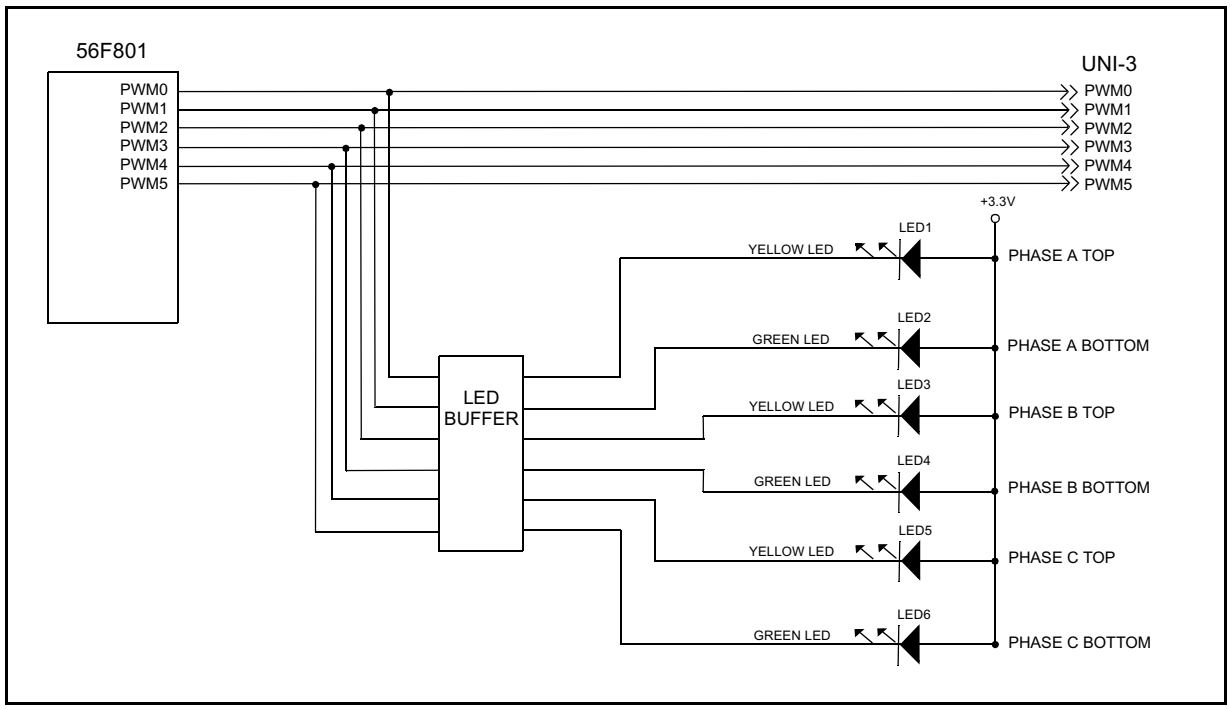

Figure 2-9. PWM Interface and LEDs

2.12 Motor Protection Logic

The 56F801EVM contains a UNI-3 connector that interfaces with various motor drive boards. The device can sense error conditions generated by the motor power stage boards via signals on the UNI-3 connector. The motor driver board's Motor Supply DC Bus Voltage, Current and Motor Phase Currents are sensed on the power stage board. The conditioned signals are transferred to the board via the UNI-3 connector. These analog input signals are compared to a limit set by trimpots. If the input analog signals are greater than the limit set by the trimpot, a controller digital voltage-compatible +3.3V DC fault signal is generated.

2.12.1 UNI-3 Motor Protection Logic

The UNI-3 DC Bus Over-Voltage or the UNI-3 DC Bus Over-Current signal can be connected to the hybrid controller's PWM fault input, FAULT0. Jumper JG3 provides the selection; reference **Figure 2-10** and **Table 2-6**.

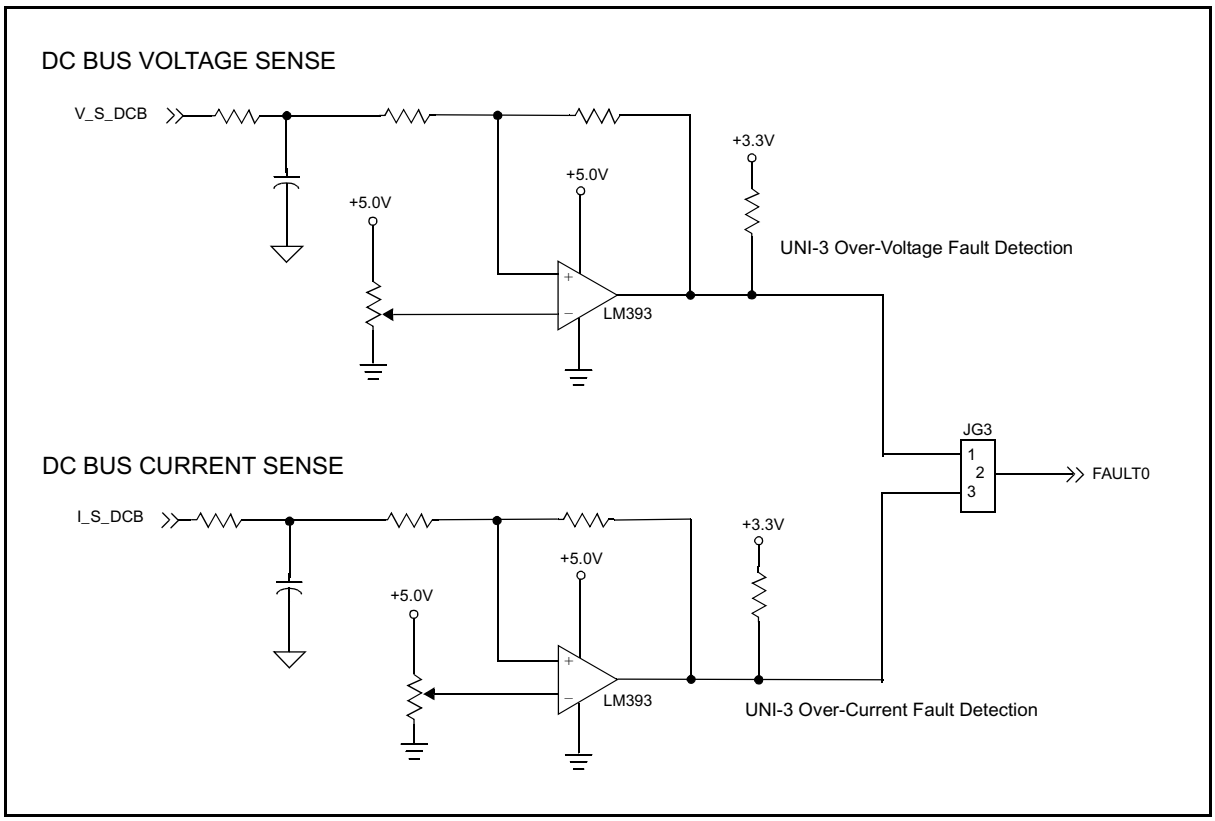

Figure 2-10. FAULT0 Selection Circuit

Table 2-6. FAULT0 Source Selection Jumper

JG3	Comment
1–2	DC Bus Over-Voltage Sense input
2–3	DC Bus Over-Current Sense input

2.13 Back-EMF and Motor Phase Current Sensing

The UNI-3 connector supplies Back-EMF and Motor Phase Current signals from the three phases of a motor attached to a motor drive unit. The Back-EMF signals on the UNI-3 connector are derived from a resistor divider network contained in the motor drive unit. These resistors divide down the attached motor's Back-EMF voltages to a 0 to +3.3V level. The Motor Phase Current signals are derived from current sense resistors. Both of these signal groups are then routed to a group of header pins, JG4, that allow the end user to select which signal group the device's A/D will monitor; reference **Figure 2-11**.

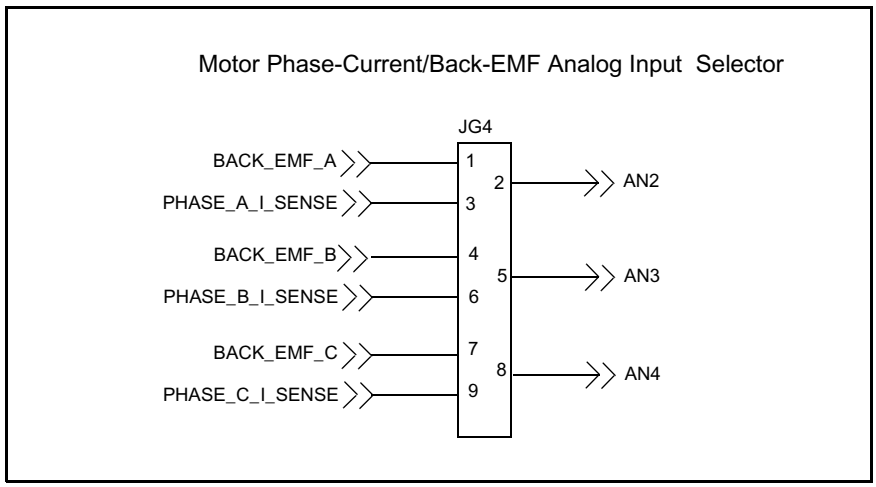

Figure 2-11. Back-EMF or Motor Phase Current Sense Signals

2.14 Quadrature Encoder/Hall-Effect Interface

The 56F801EVM board contains a Quadrature Encoder/Hall-Effect interface connected to the device's Timer D port signals, TD1 and TD2. The circuit is designed to accept +3.0V to +5.0V encoder or Hall-Effect sensor inputs. Input noise filtering is supplied on the input path for the Quadrature Encoder/Hall-Effect interface. **Figure 2-12** shows the encoder interface.

2.15 Zero-Crossing Detection

An attached UNI-3 motor drive board contains logic that can send out pulses when the phase voltage of an attached 3-phase motor drops to zero. The motor drive board circuits generate a 0 to +5.0V DC pulse via voltage comparators. The resulting pulse signals are sent to a set of jumper blocks shared with the Encoder/Hall-Effect interface. The jumper blocks allow the selection of Zero-Crossing signals or Quadrature Encoder/Hall-Effect signals. When in operation, the hybrid controller will only monitor one set of signals, Encoder/Hall-Effect or Zero-Crossing. **Figure 2-12** contains the Zero-Crossing and Encoder/Hall circuits.

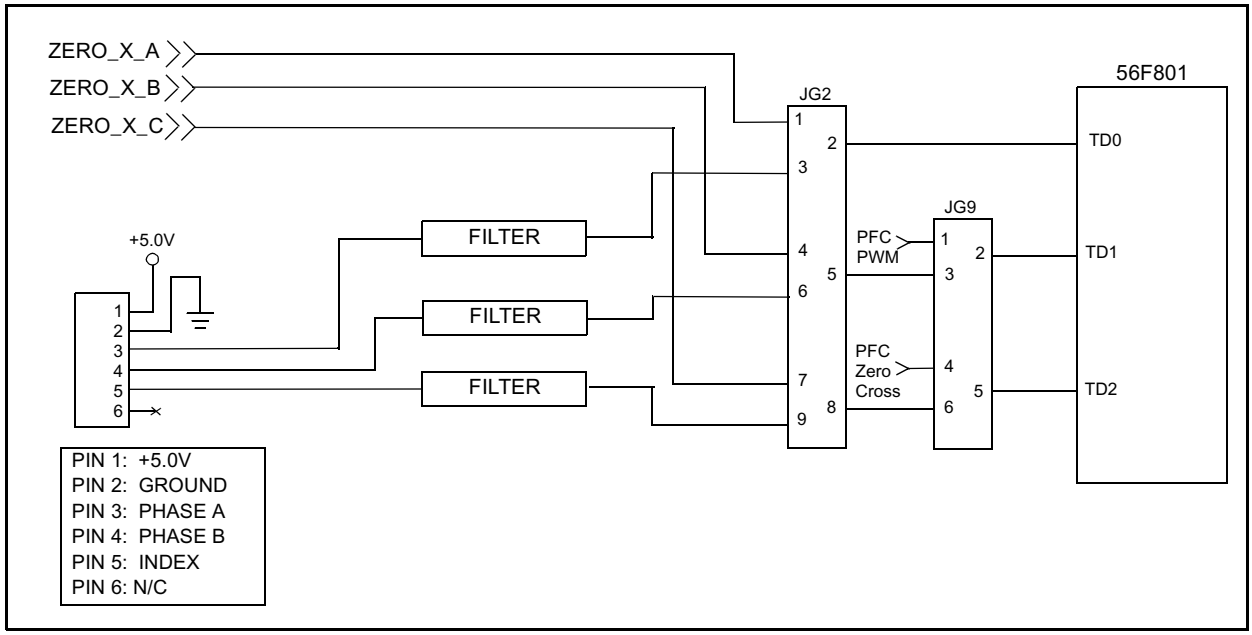

Figure 2-12. Zero-Crossing Encoder Interface

2.16 Peripheral Connectors

The EVM board contains a group of Peripheral Expansion Connectors used to gain access to the resources of the 56F801. These signal groups have Expansion Connectors:

- Timer Channel D
- A/D Input Port
- Serial Communications Port
- Serial Peripheral Port
- PWM Port
- External Control Lines

2.16.1 External Control Signal Expansion Connector

The External Control Signal connector contains the device's external interrupt and Reset control signal lines. Refer to **Table 2-7** for the names of these signals.

Table 2-7. External Control Signal Connector Description

J2			
Pin #	**Signal**	**Pin #**	**Signal**
1	$\overline{\text{IRQA}}$	2	$\overline{\text{RESET}}$
3	N/C	4	$\overline{\text{DE}}$
5	GND	6	+3.3V

2.16.2 Timer Channel D Expansion Connector

The Timer Channel D port is an MPIO port attached to the Timer D expansion connector. Refer to **Table 2-8** for the signals attached to the connector.

Table 2-8. Timer D Connector Description

J5			
Pin #	**Signal**	**Pin #**	**Signal**
1	TD0	2	TD1
3	TD2	4	N/C
5	GND	6	+3.3V

2.16.3 A/D Port Expansion Connector

The 8-channel Analog-to-Digital conversion port is attached to this connector. See **Table 2-9** for the connection information.

Table 2-9. A/D Port Connector Description

J4			
Pin #	**Signal**	**Pin #**	**Signal**
1	AN0	2	AN1
3	AN2	4	AN3
5	AN4	6	AN5
7	AN6	8	AN7
9	GNDA	10	+3.3VA

2.16.4 Serial Communications Port Expansion Connector

The Serial Communications Port, SCI0, is attached to this connector. See **Table 2-10** for the connection information.

Table 2-10. SCI0 Connector Description

J6			
Pin #	**Signal**	**Pin #**	**Signal**
1	TXD	2	RXD
3	GND	4	+3.3V

Appendix A
56F801EVM Schematics

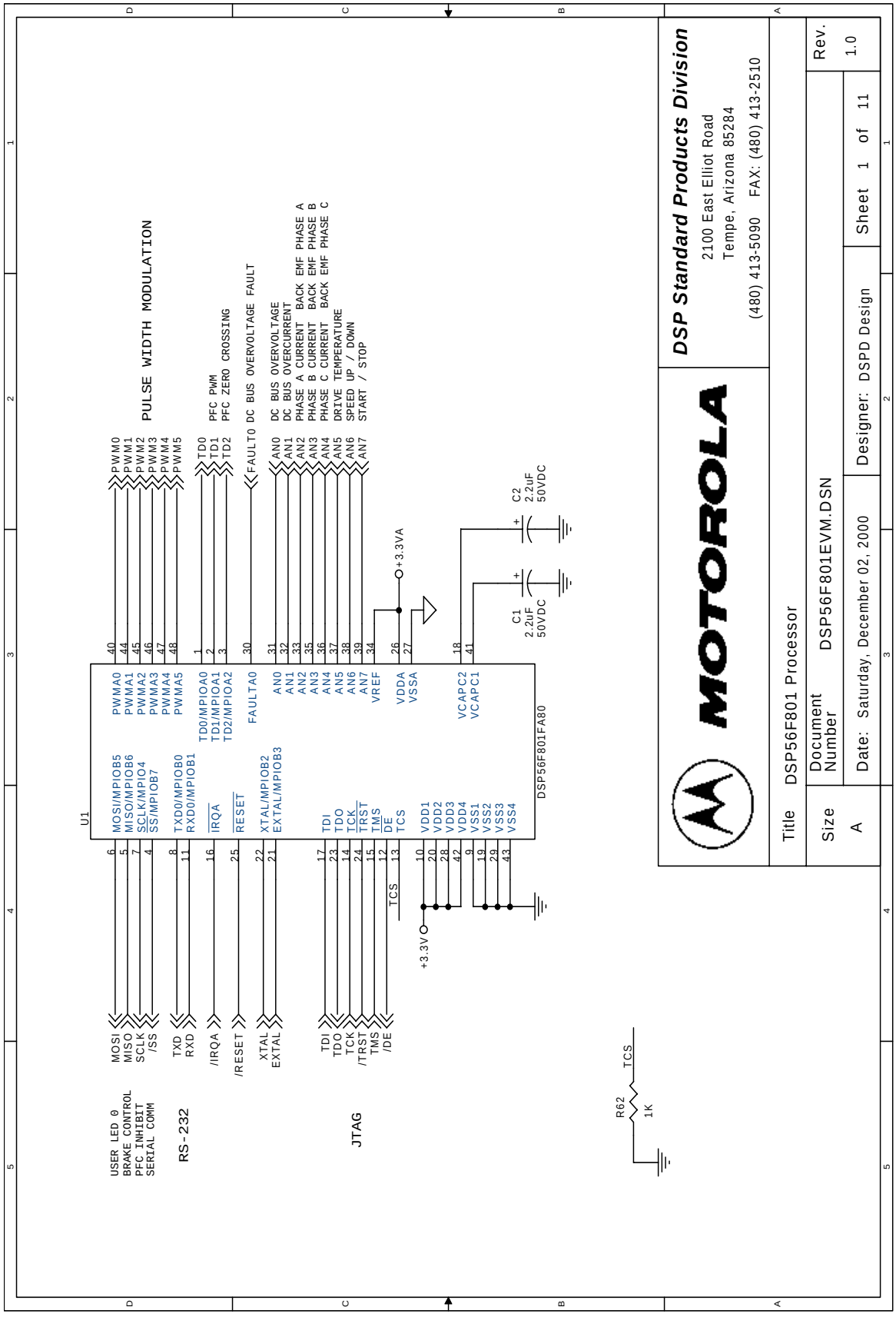

Figure A-1. 56F801 Processor

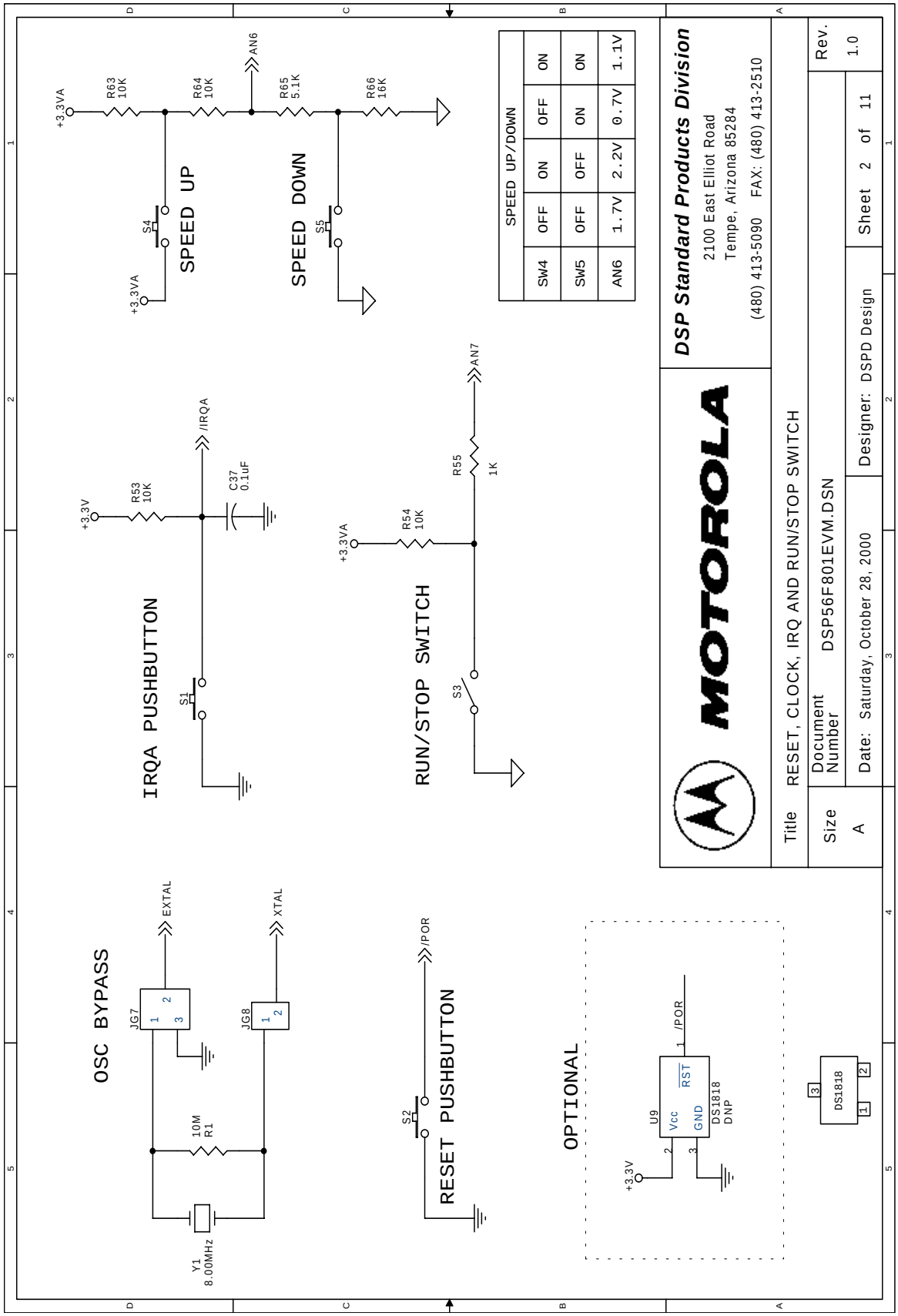

Figure A-2. Reset, Mode, Clock, IRQ and RUNun/Stop Switch

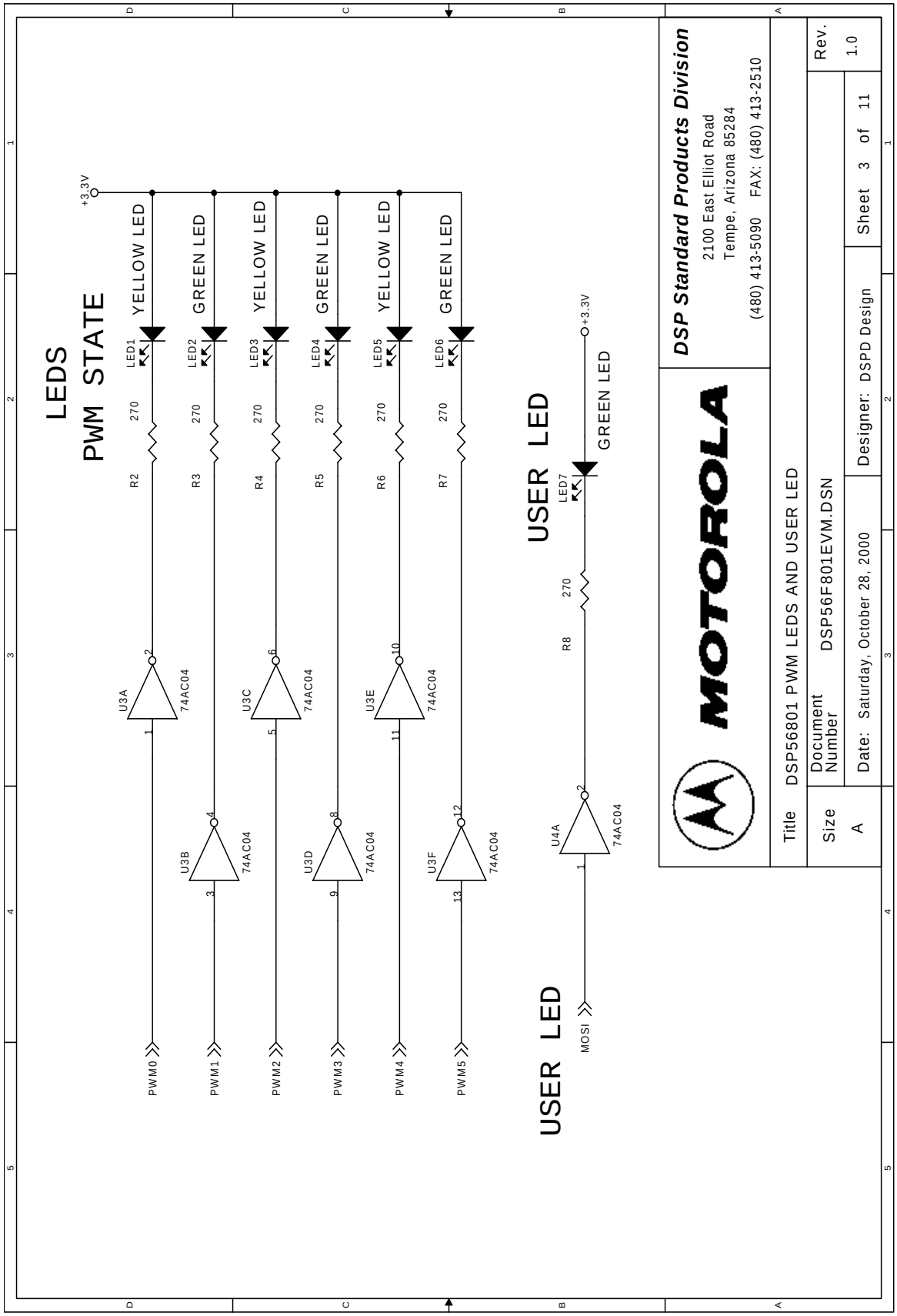

Figure A-3. 56F801 PWM LEDs and User LED

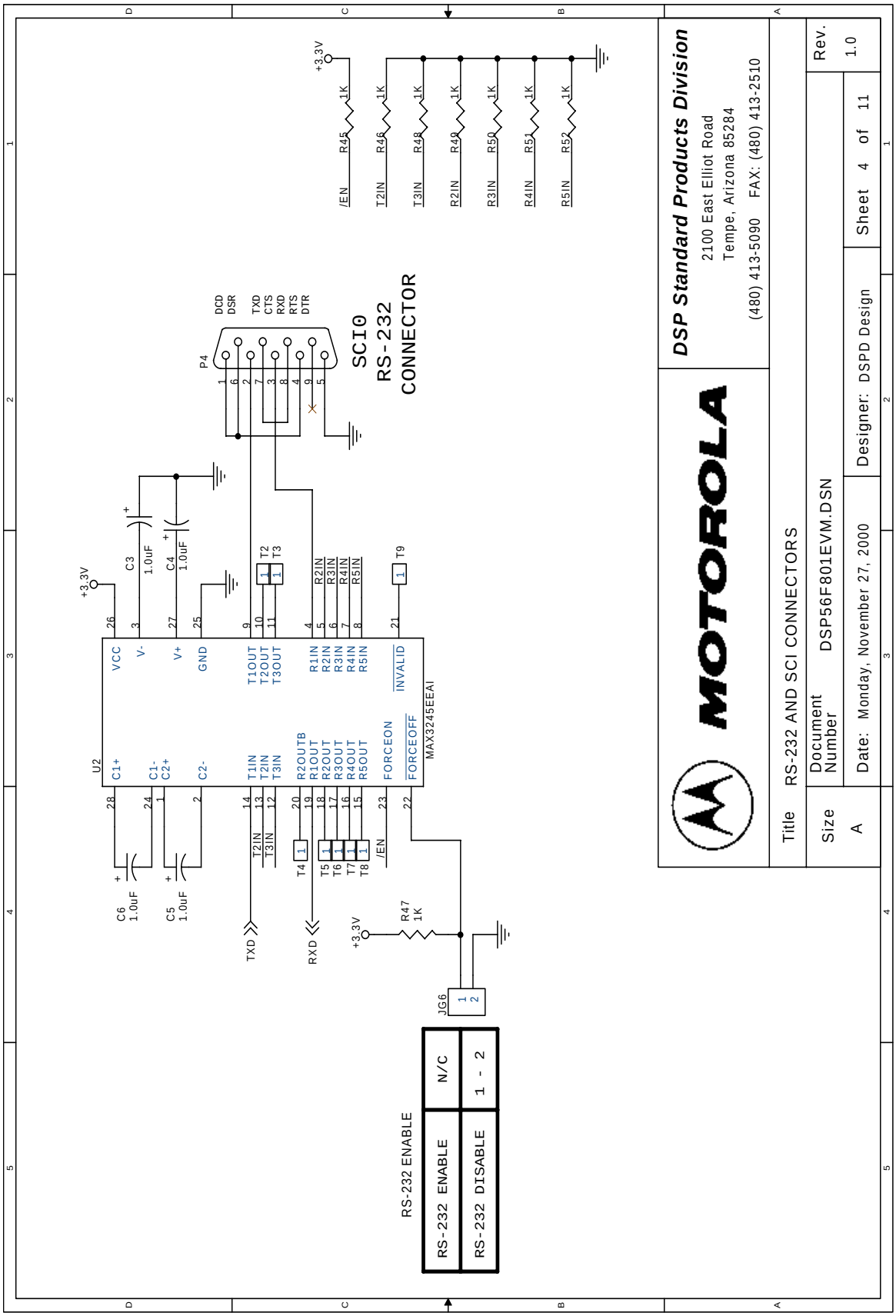

Figure A-4. RS-232 and SCI Connectors

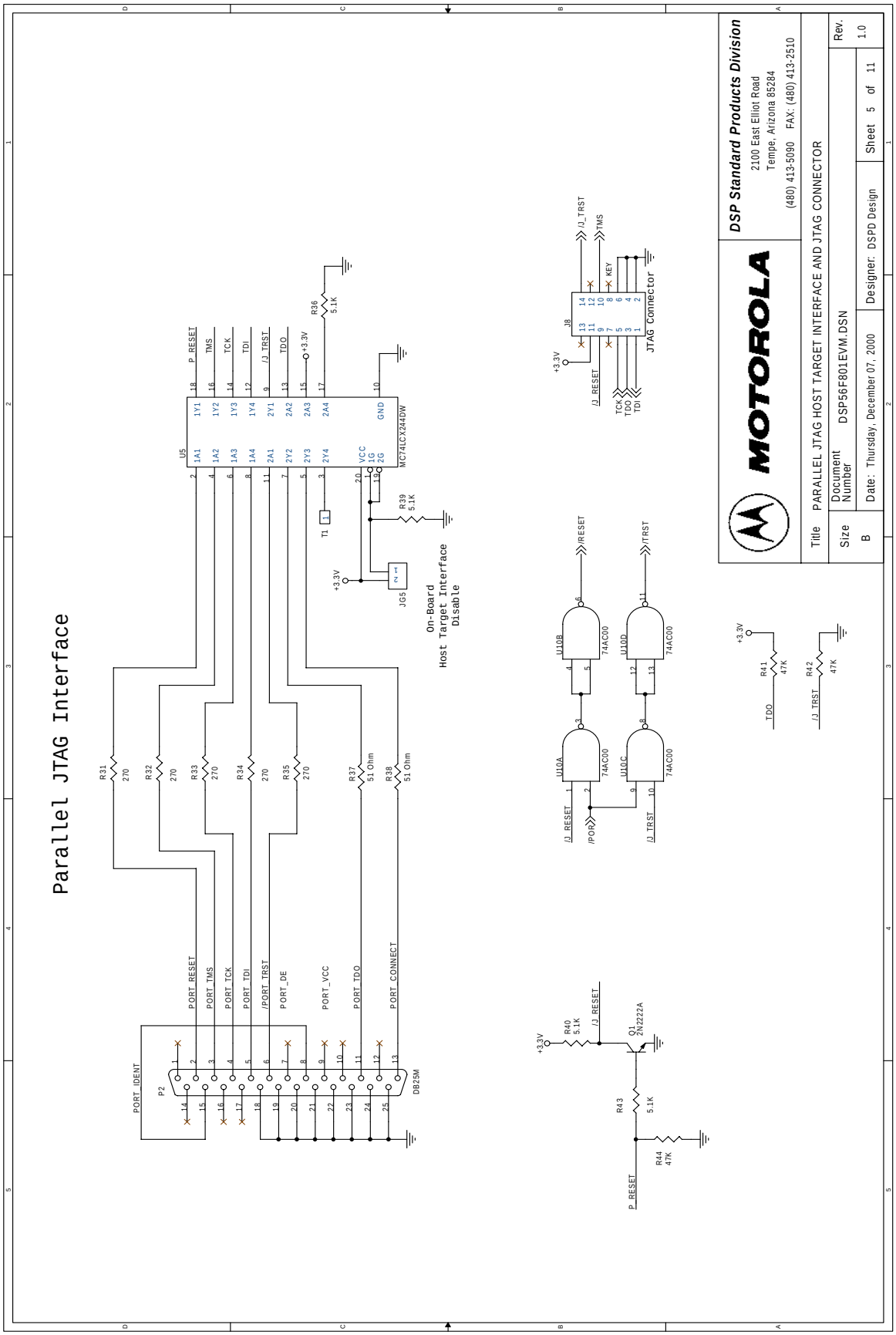

Figure A-5. Parallel JTAG Host Target Interface and JTAG Connector

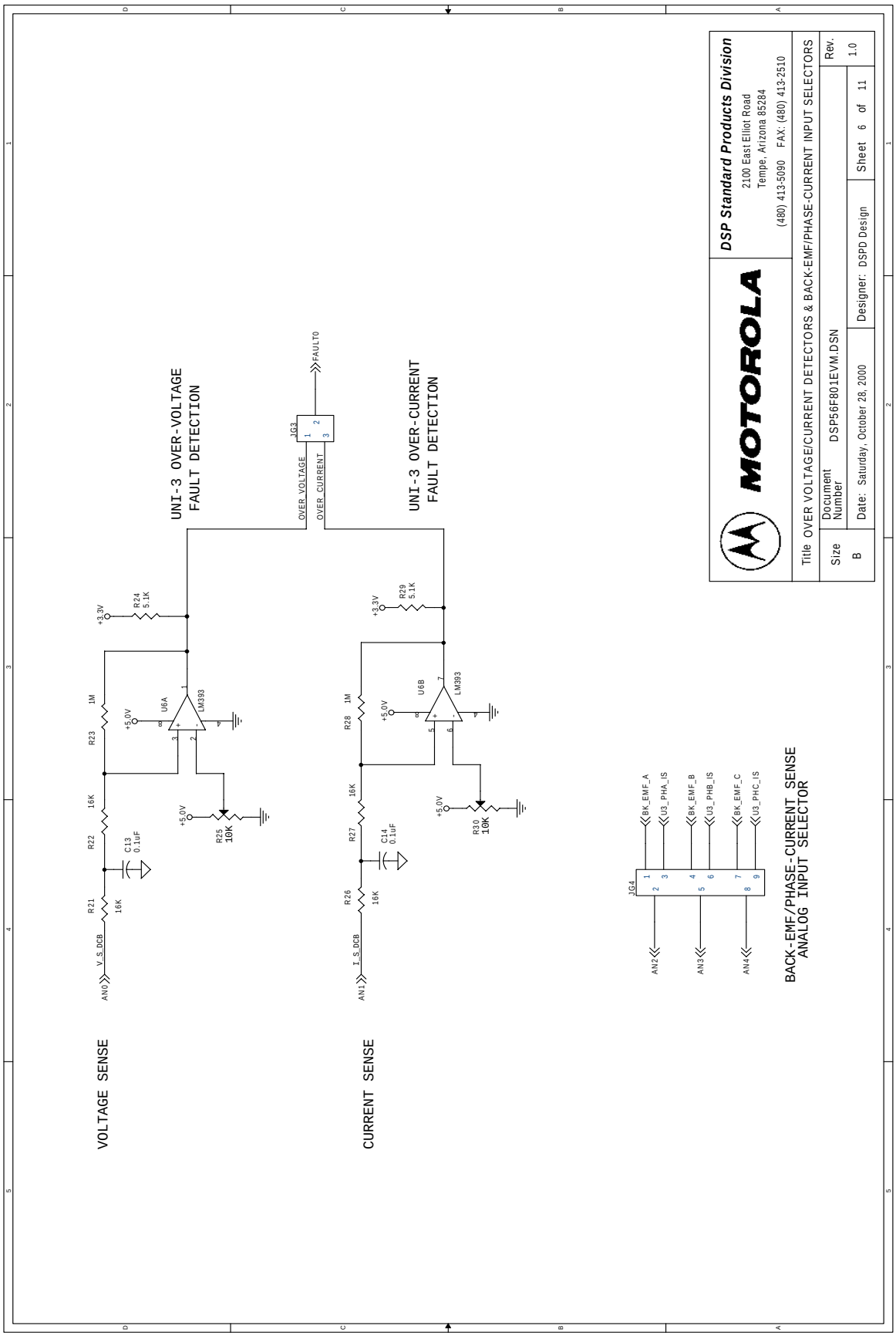

Figure A-6. Over-Voltage/Current Detectors & Back-EMF/Phase-Current Input Selectors

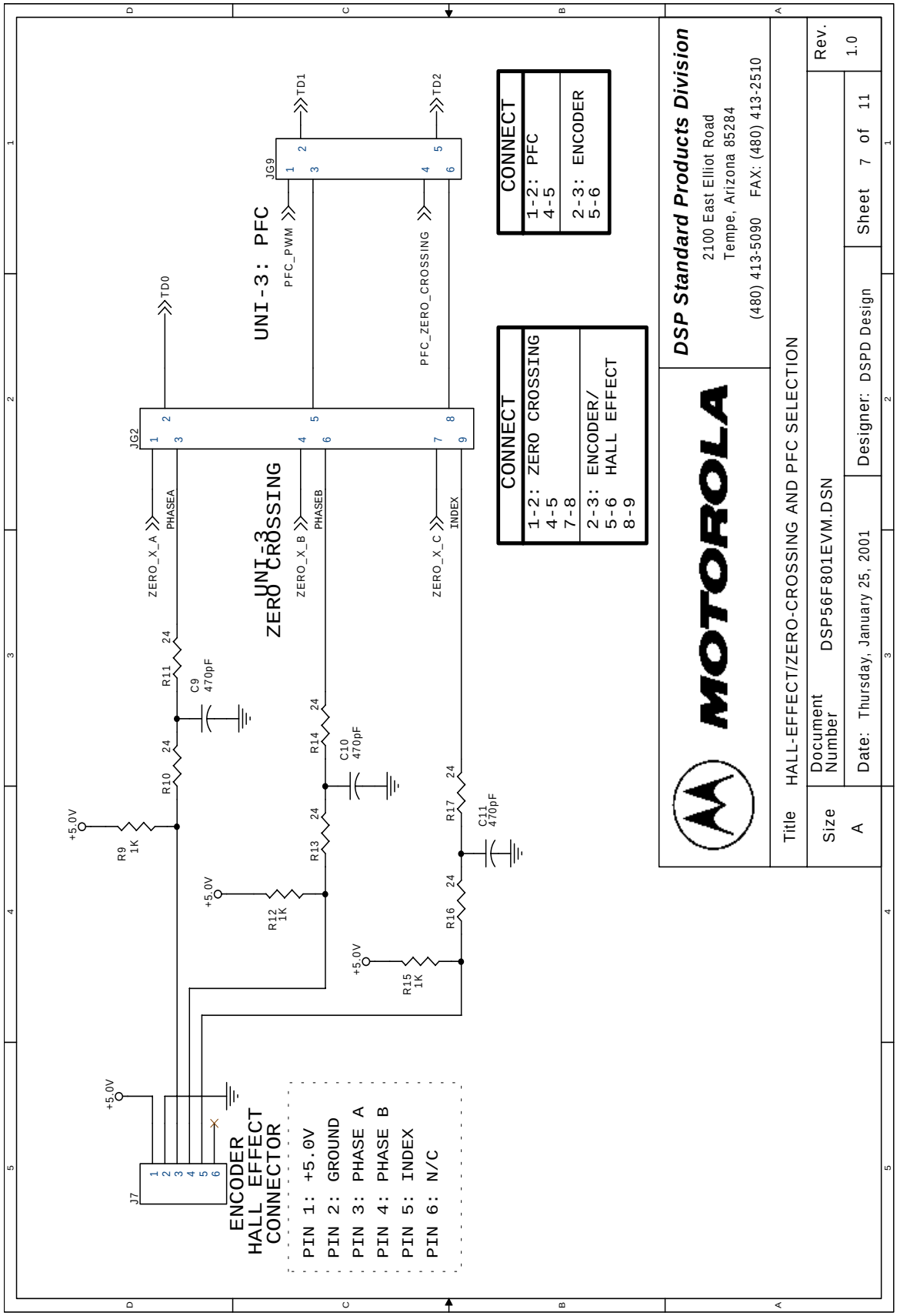

Figure A-7. Hall-Effect/Zero-Crossing and PFC Selection

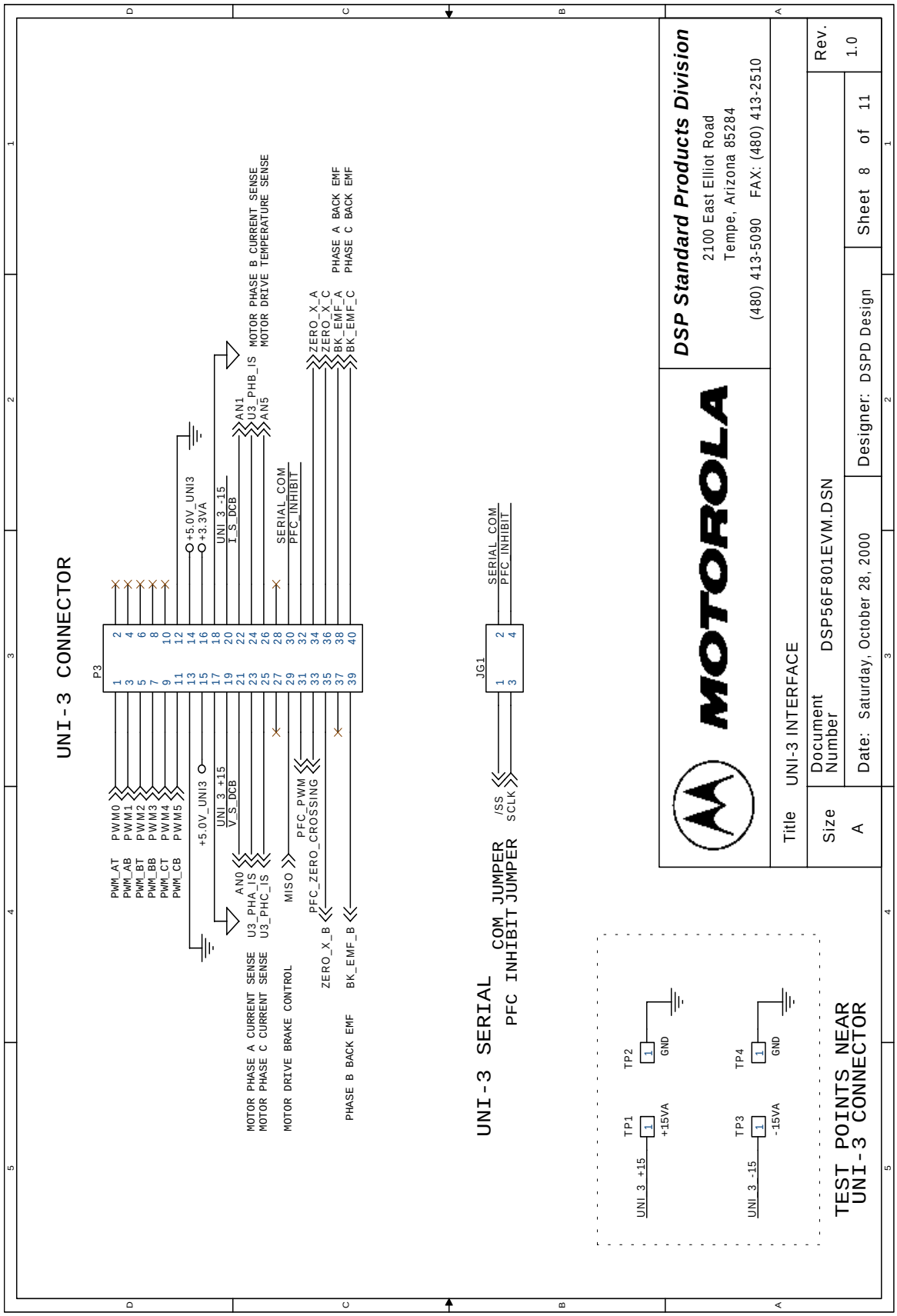

Figure A-8. UNI-3 Interface

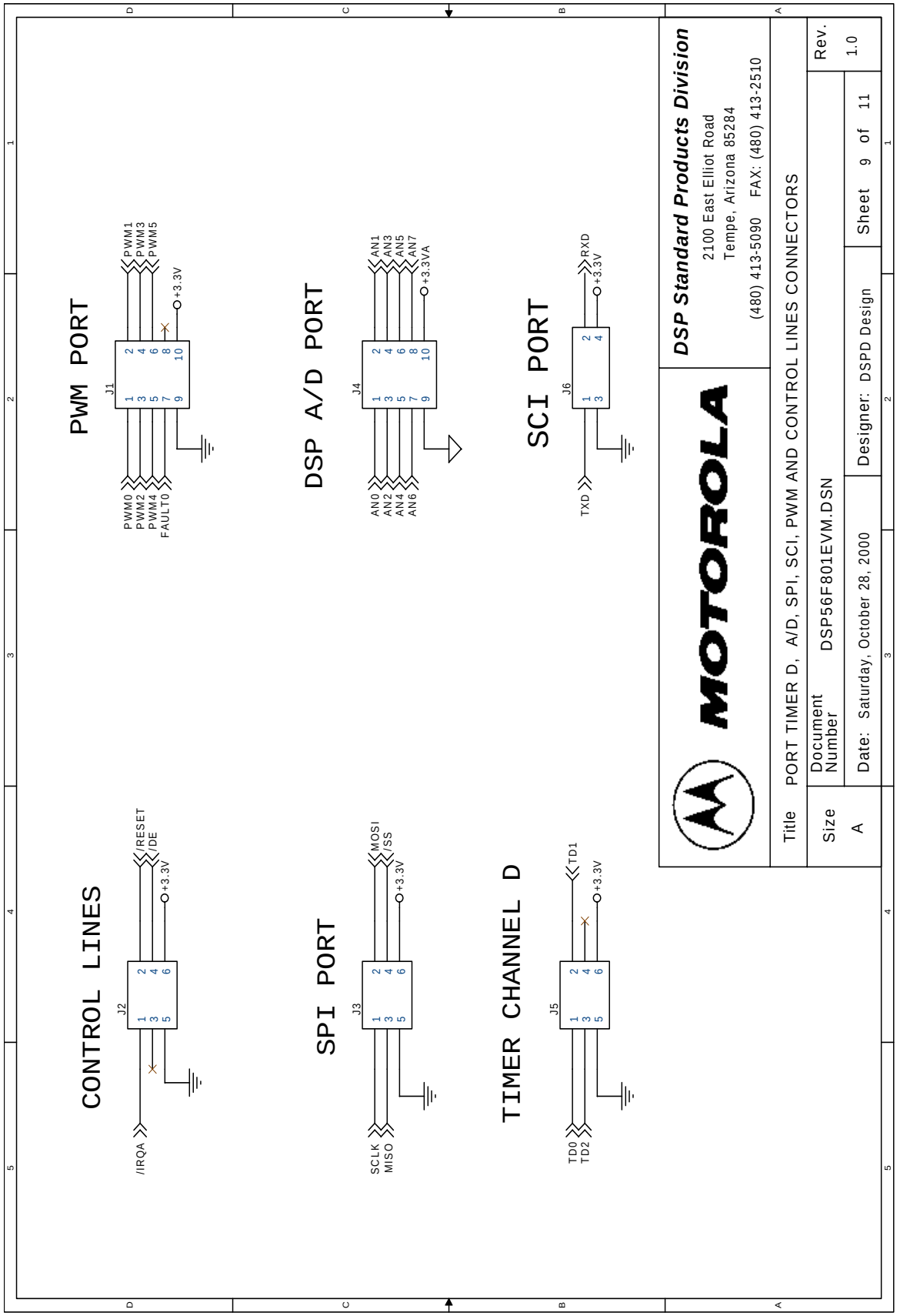

Figure A-9. Port Timer D, A/D, SPI, SCI, PWM and Control Line Connectors

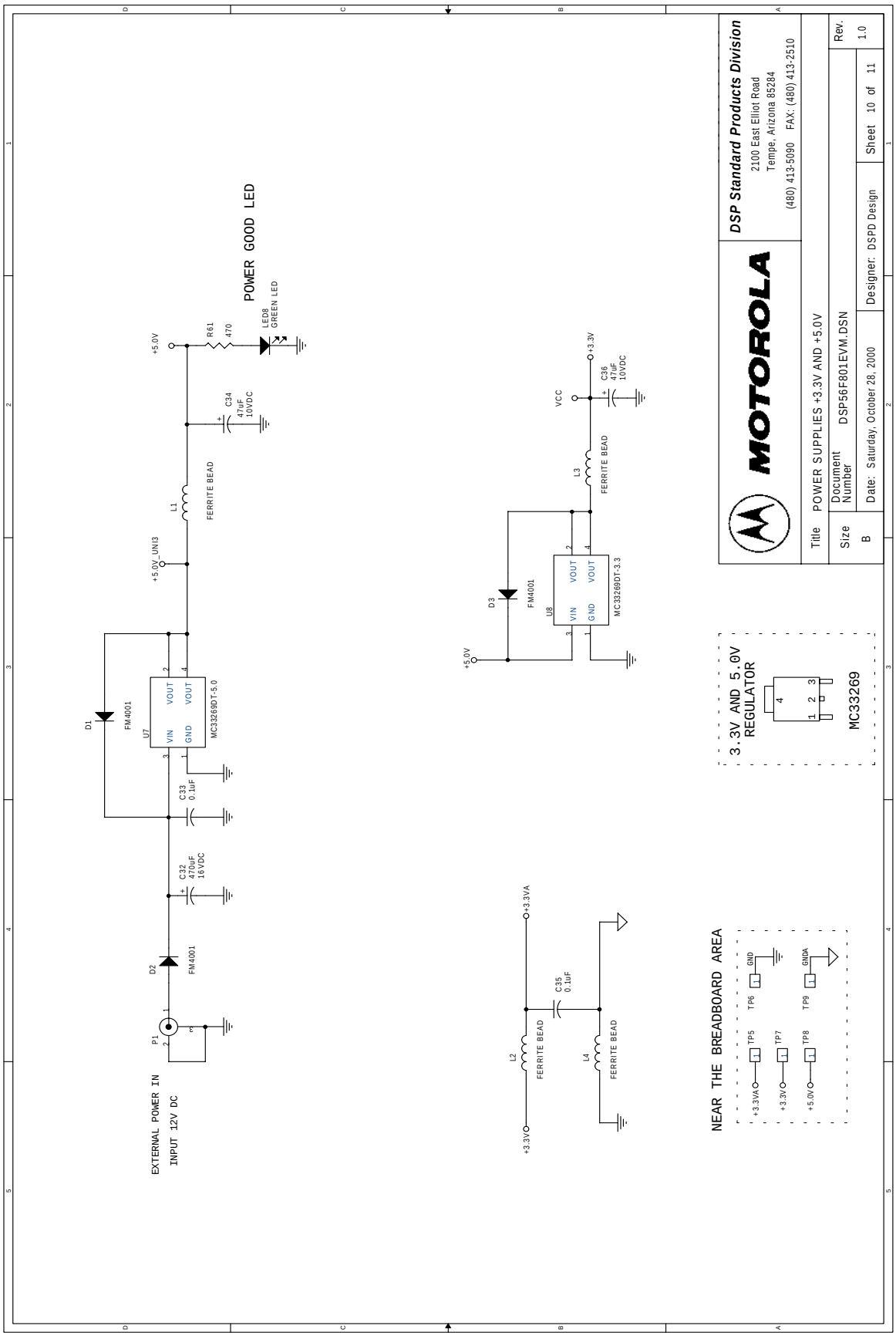

Figure A-10. Power Supplies +3.3V and +5.0V

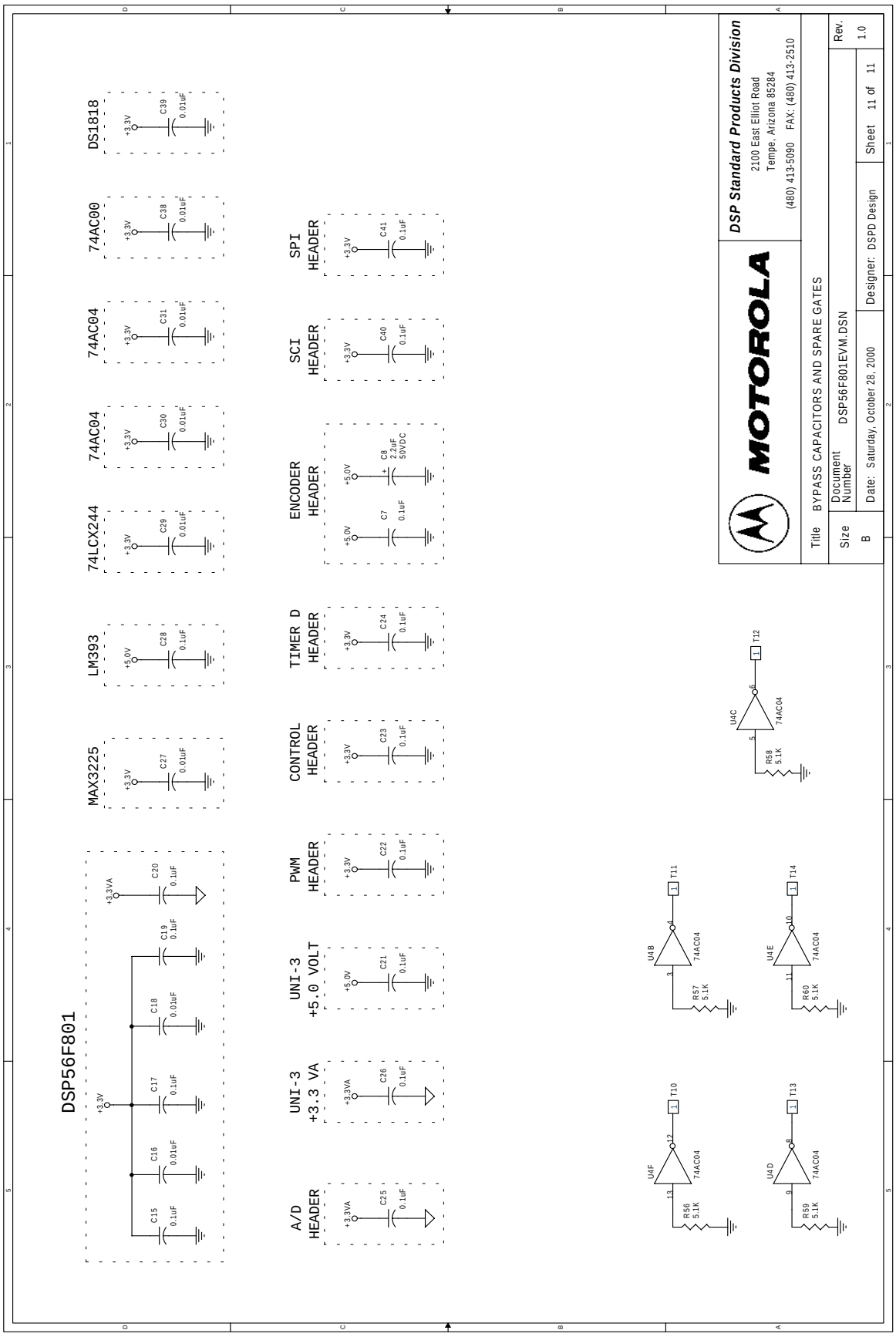

Figure A-11. Bypass Capacitors and Spare Gates

Appendix B
56F801EVM Bill of Material

Qty	Description	Ref. Designators	Vendor Part #
Integrated Circuits			
1	DSP56F801FA80	U1	Motorola, DSP56F801FA80
1	MAX3245	U2	Maxim, MAX3245EEAI
2	74AC04	U3, U4	Fairchild, 74AC04SC
1	74LCX244	U5	ON Semiconductor, MC74LCX244DW
1	LM393	U6	National, LM393M
1	MC33269DT-5.0	U7	ON Semiconductor, MC33269DT-5.0
1	MC33269DT-3.3	U8	ON Semiconductor, MC33269DT-3.3
1	74AC00	U10	Fairchild, 74AC00SC
Resistors			
5	16K Ω	R21, R22, R26, R27, R66	SMEC, RC73L2A16KOHMJT
2	1M Ω	R23, R28	SMEC, RC73L2A1MOHMJT
12	5.1K Ω	R24, R29, R36, R39, R40, R43, R56-R60, R65	SMEC, RC73L2A5.1KOHMJT
4	10K Ω	R53, R54, R63, R64	SMEC, RC73L2A10KOHMJT
2	51 Ω	R37, R38	SMEC, RC73L2A51OHMJT
3	47K Ω	R41, R42, R44	SMEC, RC73L2A47KOHMJT
1	470 Ω	R61	SMEC, RC73L2A470OHMJT
1	10M Ω	R1	SMEC, RC73L2A10MOHMJT
13	1K Ω	R9, R12, R15, R45-R52, R55, R62	SMEC, RC73L2A1KOHMJT
12	270 Ω	R2-R8, R31-R35	SMEC, RC73L2A270OHMJT
6	24 Ω	R10, R11, R13, R14, R16, R17	SMEC, RC73L2A24OHMJT

Qty	Description	Ref. Designators	Vendor Part #
Potentioneters			
2	10K Ω	R25, R30	BC/MEPCOPAL, ST4B103CT
Inductors			
4	1.0mH	L1, L2, L3, L4	Panasonic, EXC-ELSA35V
LEDs			
3	Yellow LED	LED1, LED3, LED5	Hewlett-Packard, HSMY-C650
5	Green LED	LED2, LED4, LED6, LED7, LED8	Hewlett-Packard, HSMG-C650
Diode			
3	FM4001	D1, D2, D3	Diodes, US1ADICT
Capacitors			
3	2.2µF, +50V DC	C1, C2, C8	NICHICON, UWX1H2R2MCR2GB
19	0.1µF	C7, C13-C15, C17, C19-C26, C28, C33, C35, C37, C40, C41	SMEC, MCCE104K2NR-T1
1	470µF, +16V DC	C32	ELMA, RV-16V471MH10R
2	47µF, +16V DC	C34, C36	ELMA, RV2-16V470M-R
3	470pF	C9-C11	SMEC, MCCE471J2NO-T1
8	0.01uF	C16, C18, C27, C29-C31, C38, C39	SMEC, MCCE103K2NR-T1
4	1.0uF, +50V DC	C3-C6	NICHICON, UWX1H010MCR1GB
Jumpers			
2	3 × 1 Bergstick	JG3, JG7	SAMTEC, TSW-103-07-S-S
3	1 × 2 Bergstick	JG5, JG6, JG8	SAMTEC, TSW-102-07-S-S
2	3 x 3 Bergstick	JG2, JG4	SAMTEC, TSW-103-07-S-T
2	5 x 2 Bergstick	J1, J4	SAMTEC, TSW-105-07-S-D
1	7 x 2 Bergstick	J8	SAMTEC, TSW-107-07-S-D
1	6 x 1 MTA	J7	AMP, MTA 640456-6
2	2 x 2 Bergstick	JG1, J6	SAMTEC, TSW-102-07-S-D
1	20 x 2 Shrouded	P3	3M, 2540-6002UB

Qty	Description	Ref. Designators	Vendor Part #
		Test Points	
9	1 × 1 Bergstick	TP1 - TP9	Samtec, TSW-101-07-S-S
		Crystals	
1	8.00MHz Crystal	Y1	CTS, ATS08ASM-T
		Connectors	
1	2.1mm coax Power Connector	P1	Switch Craft, RAPC-722
1	DB25M Connector	P2	AMPHENOL, 617-C025P-AJ121
1	20 x 2 Shrouded	P3	3M, 2540-6002UB
1	DE9F Connector	P4	AMPHENOL, 617-C009S-AJ120
		Switches	
4	SPST Pushbutton	S1, S2, S4, S5	Panasonic, EVQ-PAD05R
1	SPDT Toggle	S3	C&K, GT11MSCKE
		Transistors	
1	2N2222A	Q1	ZETEX, FMMT2222ACT
		Miscellaneous	
13	Shunt	SH1–SH13	Samtec, SNT-100-BL-T
4	Rubber Feet	RF1–RF4	3M, SJ5018BLKC

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