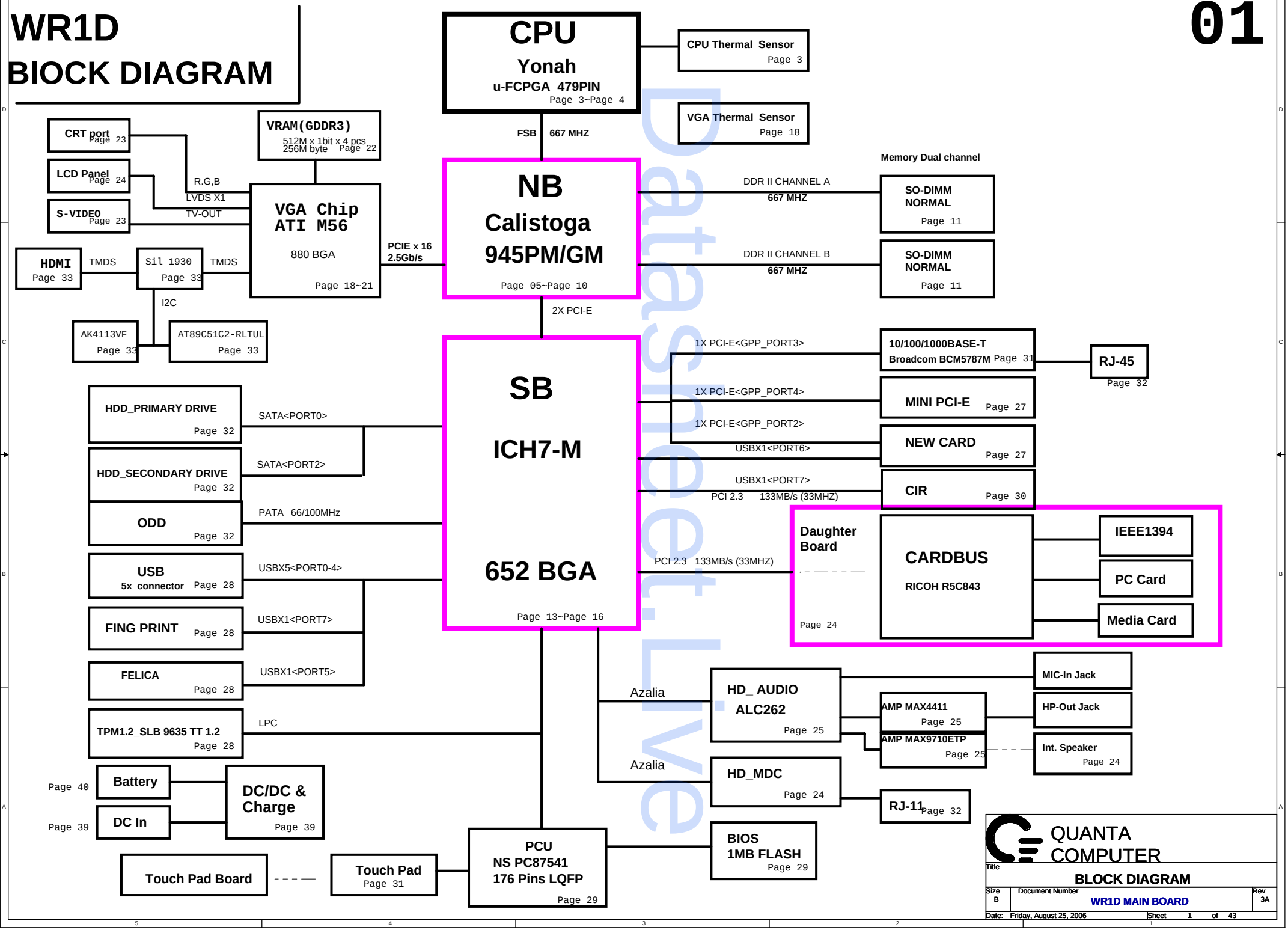
WR1D
BIOCK DIAGRAM

01



QUANTA COMPUTER

Title	BLOCK DIAGRAM	
Size B	Document Number WR1D MAIN BOARD	Rev 3A
Date: Friday, August 25, 2006	Sheet 1 of 43	

WR1D Schematic Ver :3A

02

1. Schematic Page Description :

QUANTA COMPUTER

Title	PAGE LIST		
Size: Custom	Document Number: WR1D MAIN BOARD		Rev: 3A
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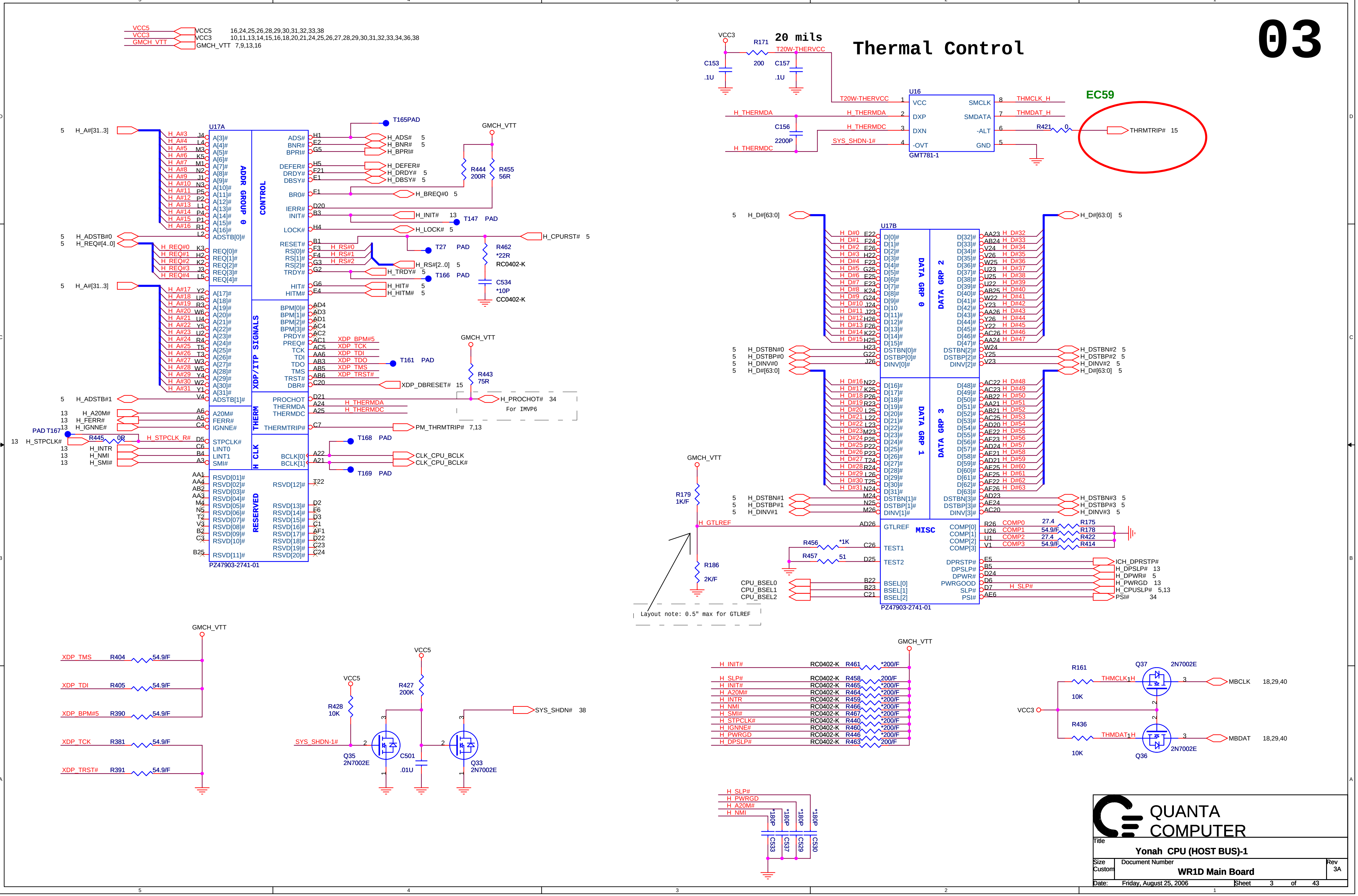
CHIP	
Port 0	BCM5751M LAN

Thermal Control



VCC5 16,24,25,26,28,29,30,31,32,33,38
VCC3 10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38
GMCH_VTT 7,9,13,16
20 mils
R171 200
C153 .1U
C157 .1U
T20W-THERVCC
U16
GMT781-1
VCC
DXP
DXN
-OVT
SMCLK
SMDATA
-ALT
GND
H_THERMDA
H_THERMDC
SYS_SHDN-1#
C156 2200P
THMCLK_H
THMDAT_H
R421 0
THRMTRIP# 15
EC59
U17A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
H_A#[31..3]
H_ADSTB#0
H_REQ#[4..0]
H_ADSTB#1
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
PAD T167
R445 0R
T165PAD
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BREQ#0
H_INIT#
T147 PAD
H_LOCK#
H_CPURST#
T27 PAD
H_RS#[2..0]
H_TRDY#
T166 PAD
H_HIT#
H_HITM#
R444 200R
R455 56R
R462 *22R RC0402-K
C534 *10P CC0402-K
XDP_BPM#5
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST#
T161 PAD
XDP_DBRESET# 15
R443 75R
H_PROCHOT# 34
For IMVP6
PM_THRMTRIP# 7,13
T168 PAD
CLK_CPU_BCLK
CLK_CPU_BCLK#
T169 PAD
U17B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
H_D#[63:0]
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
H_DINV#2
H_DSTBN#3
H_DSTBP#3
H_DINV#3
R179 1K/F
H_GTLREF
R186 2K/F
Layout note: 0.5" max for GTLREF
R456 *1K
R457 51
COMP0
COMP1
COMP2
COMP3
R175 27.4
R178 54.9/F
R422 27.4
R414 54.9/F
ICH_DPRSTP#
H_DPSLP# 13
H_DPWR# 5
H_PWRGD 13
H_CPUSLP# 5,13
PSI# 34
H_SLP#
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
XDP_TMS R404 54.9/F
XDP_TDI R405 54.9/F
XDP_BPM#5 R390 54.9/F
XDP_TCK R381 54.9/F
XDP_TRST# R391 54.9/F
R428 10K
R427 200K
Q35 2N7002E
Q33 2N7002E
C501 .01U
SYS_SHDN# 38
H_INIT# RC0402-K R461 *200/F
H_SLP# RC0402-K R458 200/F
H_INIT# RC0402-K R465 *200/F
H_A20M# RC0402-K R464 *200/F
H_INTR RC0402-K R459 *200/F
H_NMI RC0402-K R466 *200/F
H_SMI# RC0402-K R467 *200/F
H_STPCLK# RC0402-K R440 *200/F
H_IGNNE# RC0402-K R460 *200/F
H_PWRGD RC0402-K R446 *200/F
H_DPSLP# RC0402-K R463 200/F
R161 10K
R436 10K
Q37 2N7002E
Q36 2N7002E
THMCLK_H
THMDAT_H
MBCLK 18,29,40
MBDAT 18,29,40
C533 *180P
C537 *180P
C529 *180P
C530 *180P

QUANTA COMPUTER

Title	Yonah CPU (HOST BUS)-1
Size: Custom	Document Number: WR1D Main Board — Rev 3A
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GMCH_VTT → GMCH_VTT 7,9,13,16
CPU_CORE → CPU_CORE 34
VCC1.5 → VCC1.5 7,8,14,16,27,38

GMCH_VTT: C506 330U/2.5V/7343/R=12, C510 0.1U, C504 0.1U, C515 0.1U, C494 0.1U, C493 0.1U

GMCH_VTT: C503 0.1U, C519 0.1U, C485 0.1U, C498 0.1U, C500 0.1U

CPU_CORE: C528 0.1U, C525 0.1U, C478 0.1U, C526 0.1U, C484 0.1U

CPU_CORE: C527 0.1U, C538 0.1U, C476 0.1U, C477 0.1U, C536 0.1U

10U/6.3V/X5R(CC0805)
5 mOhm*35

---> 10U/4V/X5R(CC0603)
Murata

CPU_CORE: C469 10U, C531 10U, C472 10U, C474 10U, C532 10U

CPU_CORE, CPU_CORE

U17C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	V6
E12	VCC[036]	VCCP[02]	G21
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA	B26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AF5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AF4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AF2
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]	VCCSENSE	AF7
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AF7

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GMCH_VTT → C505 330U

VCC1.5 → C535 0.01U, C539 10U

VCC1.5 → B26

near PIN B26

CPU_VID0 34
CPU_VID1 34
CPU_VID2 34
CPU_VID3 34
CPU_VID4 34
CPU_VID5 34
CPU_VID6 34

CPU_CORE → R380 100/F → VCCSENSE 34

R375 100/F → VSSSENSE 34

GMCH_VTT: C509 0.1U, C520 0.1U, C516 0.1U, C486 0.1U, C487 0.1U, C514 0.1U

U17D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
A26	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	AF3
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	AF24

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QUANTA COMPUTER

Title: Yonah CPU (POWER/NC)-2

Size: B | Document Number: WR1D MAIN BOARD | Rev: 3A

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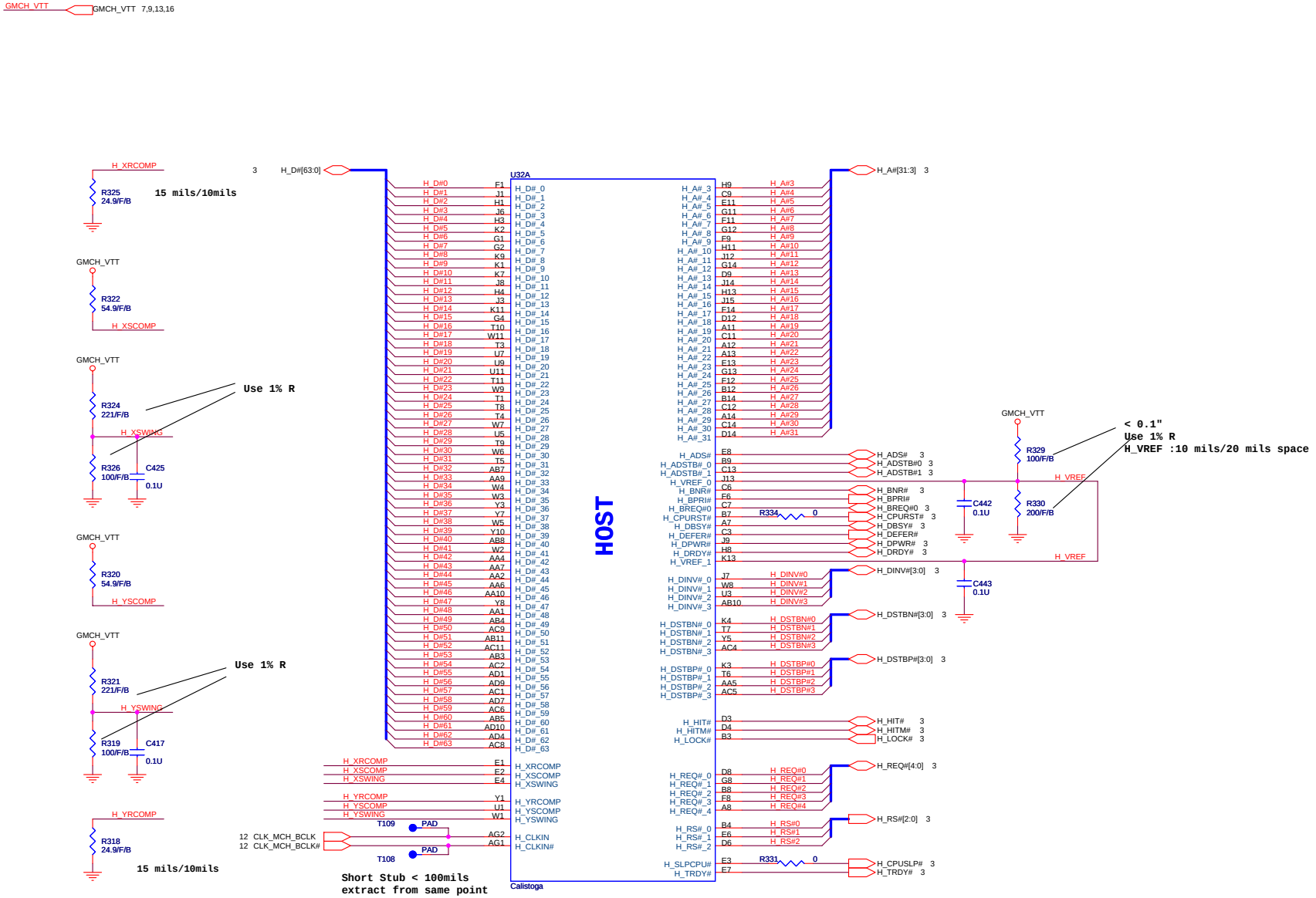

QUANTA COMPUTER			
Title: Calistoga HOST 1/6			
Size: Custom	Document Number: WR1D MAIN BOARD		Rev: 3A
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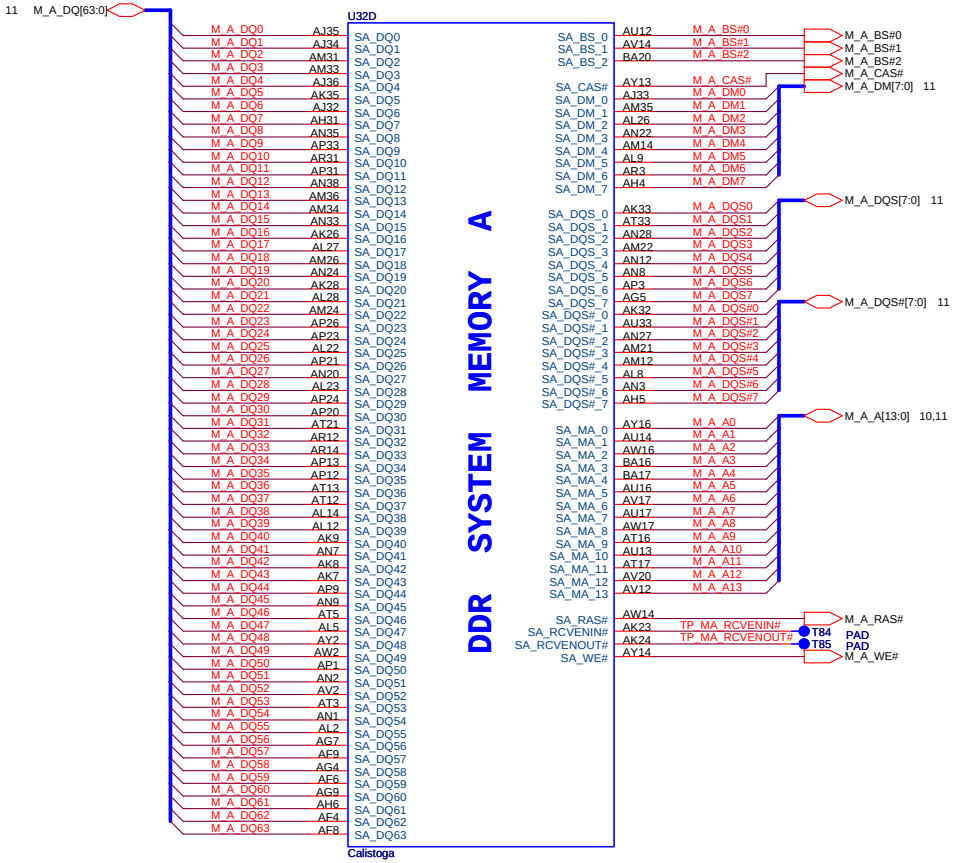
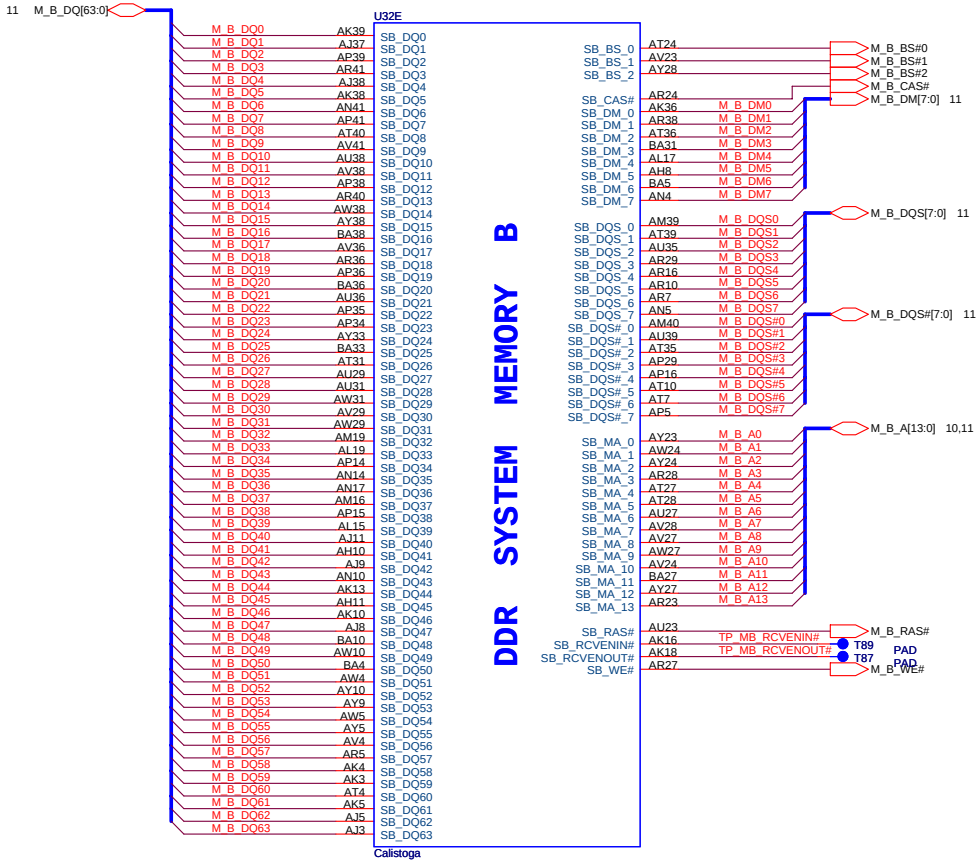
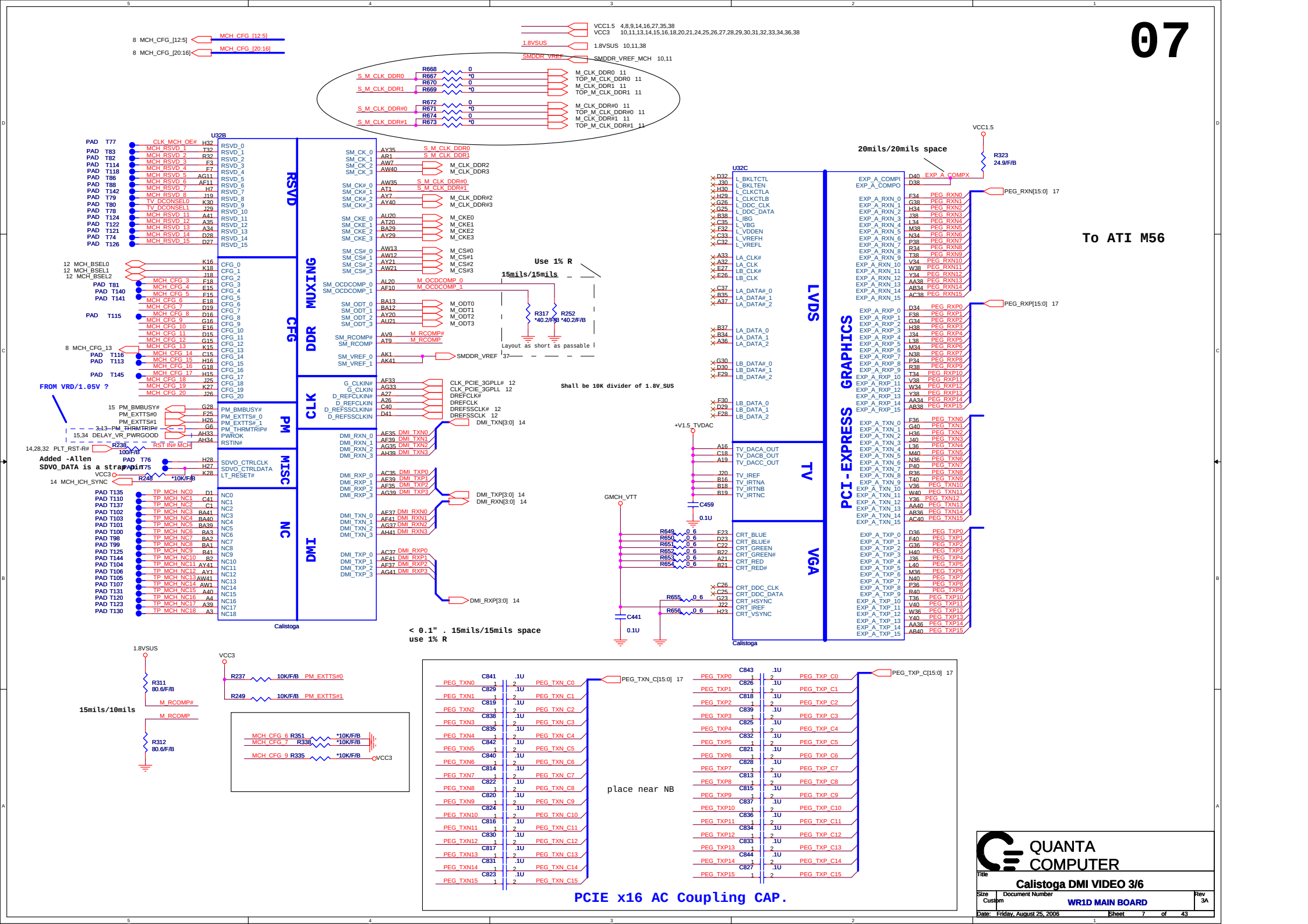




QUANTA COMPUTER

Title	Calistoga DDRII 2/6	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
Date: Friday, August 25, 2006	Sheet 6 of 43	



QUANTA COMPUTER

Title: Calistoga DMI VIDEO 3/6

Size	Document Number	Rev
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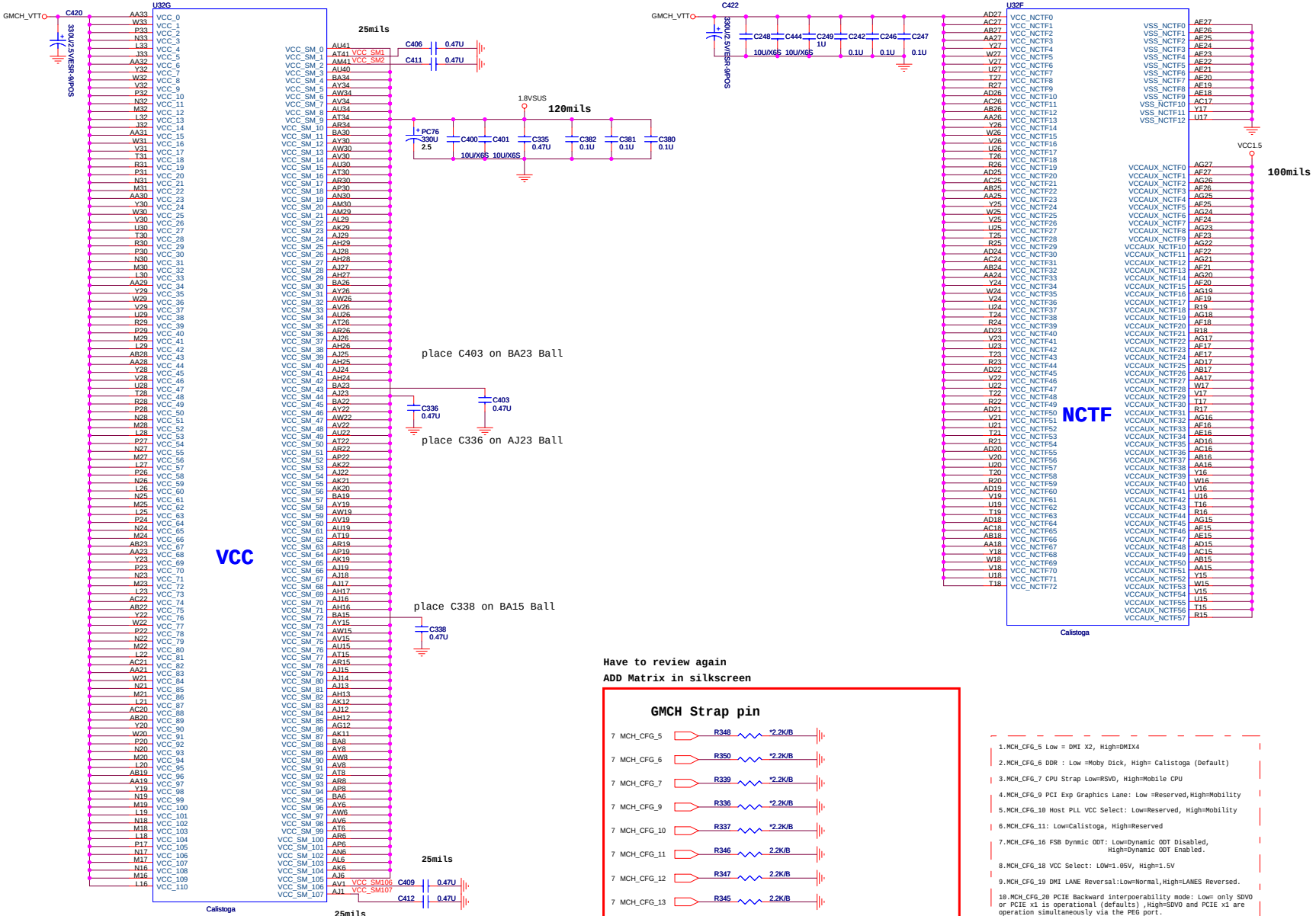
GMCH_VTT
VCC1.5
VCC3
1.8VSUS

GMCH_VTT 7,9,13,16
VCC1.5 4,7,9,14,16,27,35,38
VCC3 10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38
1.8VSUS 10,11,38



Have to review again
ADD Matrix in silkscreen

GMCH Strap pin

7 MCH_CFG_5	R348	*2.2K/B	
7 MCH_CFG_6	R350	*2.2K/B	
7 MCH_CFG_7	R339	*2.2K/B	
7 MCH_CFG_9	R336	*2.2K/B	
7 MCH_CFG_10	R337	*2.2K/B	
7 MCH_CFG_11	R346	2.2K/B	
7 MCH_CFG_12	R347	2.2K/B	
7 MCH_CFG_13	R345	2.2K/B	
7 MCH_CFG_16	R349	*2.2K/B	
7 MCH_CFG_18	R234	1K/F/B CFG_RSVD_0_R	R235 *0/B VCC3
7 MCH_CFG_19	R251	*1K/F/B	VCC3
7 MCH_CFG_20	R250	*1K/F/B	VCC3

1.MCH_CFG_5 Low = DMI X2, High=DMIX4

2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)

3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU

4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility

5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility

6.MCH_CFG_11: Low=Calistoga, High=Reserved

7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.

8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V

9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.

10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

QUANTA COMPUTER

Title: Calistoga Power&Strap 4/6

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VCC1.5 — VCC1.5 — 7,8,14,16,27,38
VCC2.5 — VCC2.5 — 18,20,38
VCC3 — VCC3 — 10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38

U32H

POWER

Calistoga

Shall Add more bypass caps for 1.05V

VTT_56 , VTT_71 and 72 are attached with 0.1u seperated .Checking

80mils

60mils

40mils

RC0805

Oreginal FCM2012C-181 "CX000181008"

QUANTA COMPUTER

Title: Calistoga Power 2 5/6

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

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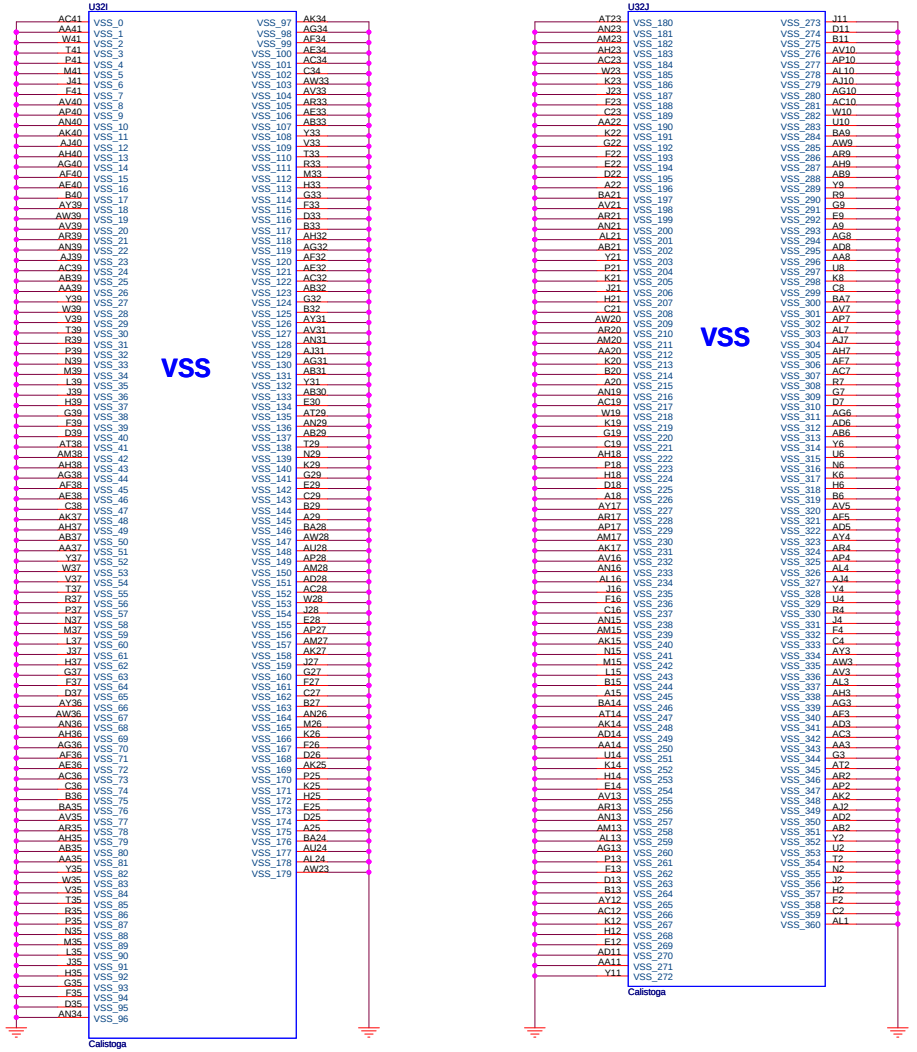
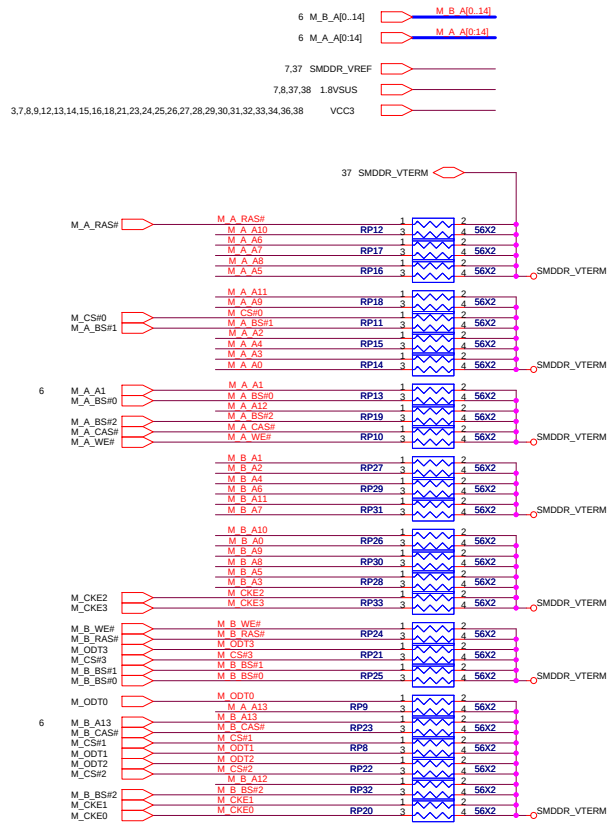
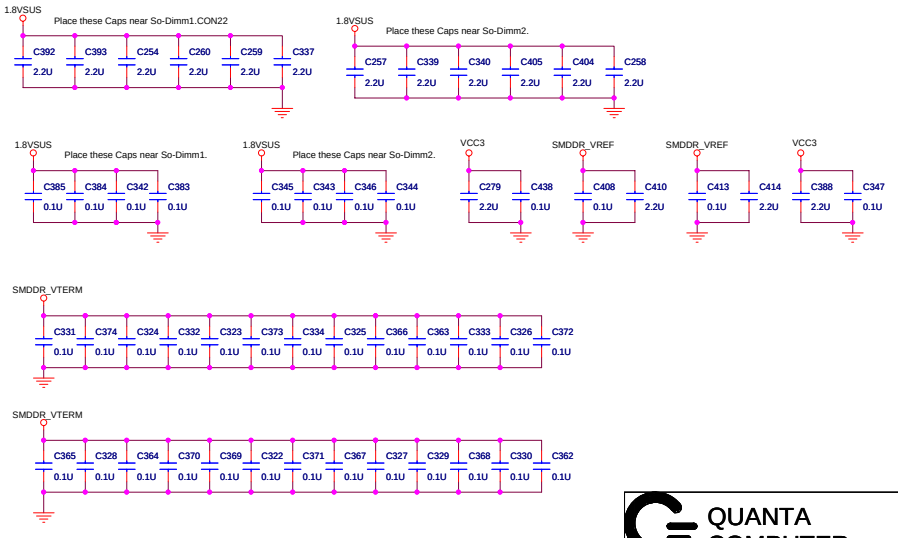


DDR Terminal Resistor



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



QUANTA COMPUTER

Title: **Calistoga GND 6/6&DDR Terminal Resistors**

Size	Document Number	Rev
C	WR1D MAIN BOARD	3A

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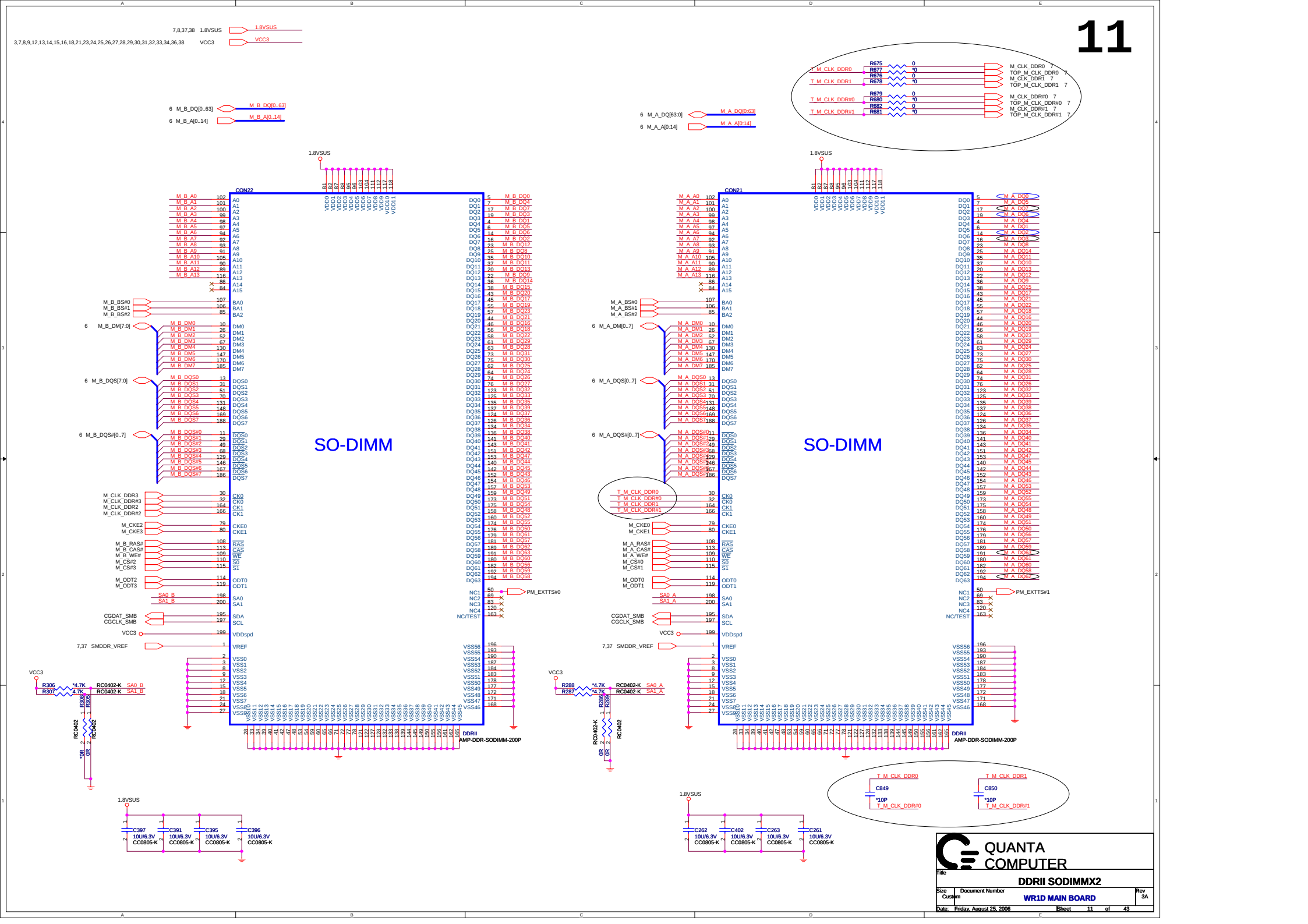

QUANTA COMPUTER

Title: DDRII SODIMMX2

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 3A

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Place these termination to close CK410M.

Place these termination to close CK410M.

FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	200	100	33	

SMbus address D2

ITP_EN: select pin functionality
"0" : SRC pair
"1" : CPU_ITP pair

DREFSSCLK Frequency Select.
"0" : 96MHz "1" : 100MHz

Stuff 0 ohm for 533MHz, NC for 667MHz

Title	EXT CLK GEN
Size	B
Document Number	WR1D MAIN BOARD
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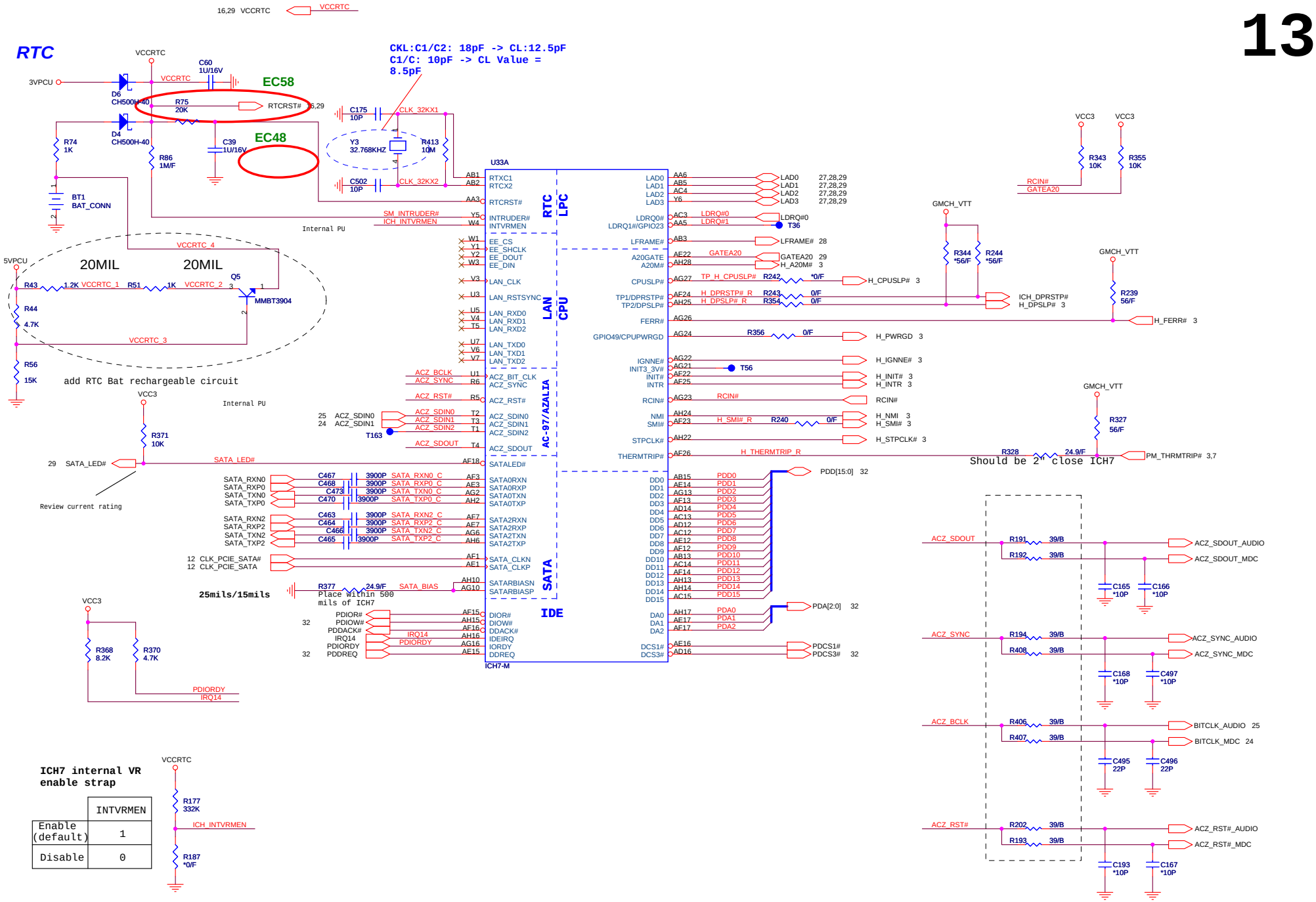
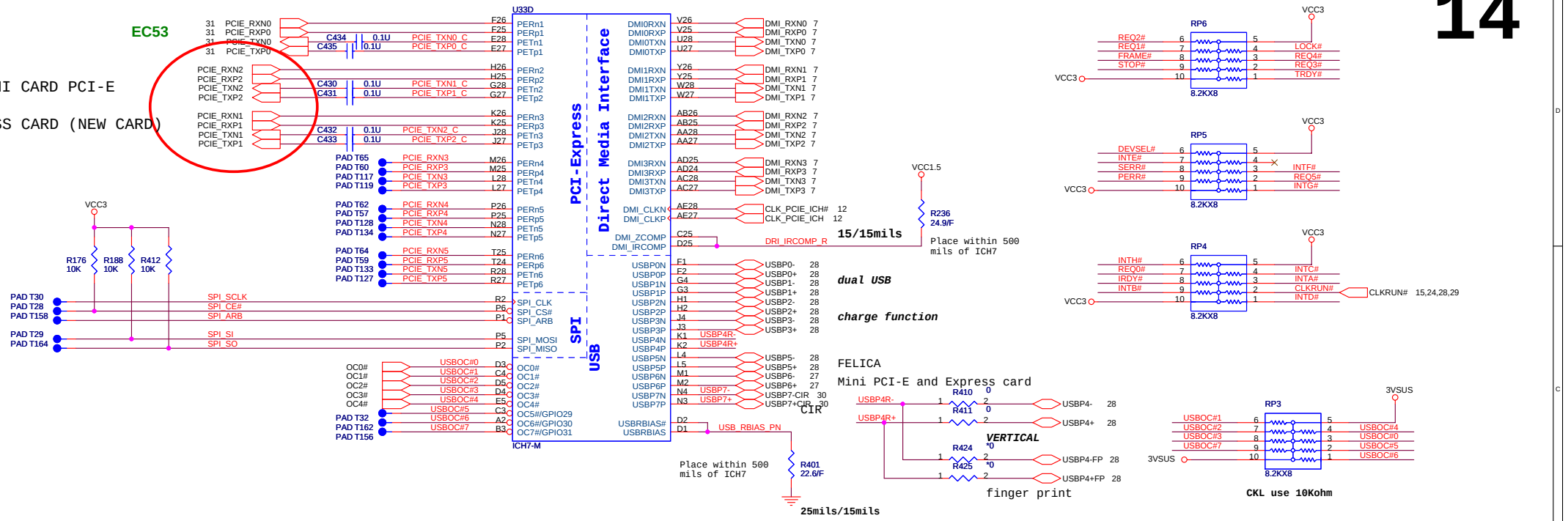

RTC
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
EC58
EC48
add RTC Bat rechargeable circuit
20MIL
20MIL
Internal PU
Review current rating
25mils/15mils
Should be 2" close ICH7
U33A
ICH7-M
RTC
LPC
CPU
LAN
AC-97/AZALIA
SATA
IDE
ICH7 internal VR enable strap
INTVRMEN
Enable (default) 1
Disable 0
QUANTA COMPUTER
ICH7-M HOST (1/4)
WR1D MAIN BOARD
Friday, August 25, 2006

EC53

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ3# / GNT3#	INT B/C/G#
Relteck Lan	AD16	REQ2# / GNT2#	INT C#

QUANTA COMPUTER

Title: ICH7-M PCI E (2/4)

Size: Custom | Document Number: WR1D MAIN BOARD | Rev: 2A

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16,27,31,38 RVCC3

R376
No stuff-->boot
Stuff-->No boot

3VPCU
RVCC3
R226 *0/F
R225 0/F
SCLK0 R224 2.2K
SDATA0 R221 2.2K

RVCC3
RI# R332 10K
SMB_LINK_ALERT# R340 10K
SMLINK0 R342 10K
SMLINK1 R341 10K
EXTSMI# R359 10K
WAKE_SCI# R333 10K
SMB_ALERT# R352 10K

RVCC3
DNBSWON# R358 10K
SYS_RST# R229 10K
WAKE# R213 1K
PM_BATLOW# R357 8.2K

VCC3
CLKRUN# R372 8.2K
SERIRQ R360 8.2K
SATA2GP R369 8.2K
SATA3GP R210 8.2K
RUNTIME_SCI# R R212 10K
BOARD_ID1 R228 8.2K
BOARD_ID0 R232 8.2K

to Clock Gen & DIMM

SYS_RST is suspend rail

VCC3
R367 *1K/F
26 ACZ_SPKR

VCC3
R245 *10K/F
R378 *10K/F
12 PM_STPPCI#
12 PM_STPCPU#
No ASF support
R379 0/F
R246 0/F

VCC3
R363 10K/F
3 THRMTRIP#

VCC3
R247 10K
29 SCI# KBSMI#
R207 0/F
R364 0/F

U33C
ICH7-M

SMB
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#

SYS GPIO
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8

GPIO

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

Clocks
CLK14
CLK48
SUSCLK

Power MGT
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39

12,27,29 SCLK0
12,27,29 SDATA0
T139
T138
T143
T129
28 SUS_STAT#
3 XDP_DBRESET#
R366 0/F
7 PM_BMBUSY#
T146
PM_STPPCI_ICH#
PM_STPCPU_ICH#
27 BIOS_WP#
R89 0/F
BIOS_REC_R
FWH_MFG_MODE_R
14,24,28,29 CLKRUN#
T47
T160
27,31 WAKE#
14,24,28,29 SERIRQ
VR_PWRGD_CK410
RUNTIME_SCI# R
EXTSMI# R

SMBCLK C22
SDATA0 B22
SMB_LINK_ALERT# A26
SMLINK0 B25
SMLINK1 A25
RI# A28
SPKR A19
SUS_STAT# A27
SYS_RST# A22
GPIO0/BM_BUSY# AB18
GPIO11/SMBALERT# B23
PM_STPPCI_ICH# AC20
PM_STPCPU_ICH# AE21
GPIO26 A21
BIOS_REC_R B21
FWH_MFG_MODE_R E23
GPIO27
GPIO28
CLKRUN# AG18
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN# AC19
GPIO34/AZ_DOCK_RST# U2
WAKE# F20
SERIRQ AH21
THRM# AF20
VR_PWRGD_CK410 AD22
GPIO6 AC21
GPIO7 AC18
GPIO8 E21

AE19 BOARD_ID1
AH18 BOARD_ID0
AH19 SATA2GP
AE19 SATA3GP
AC1 14M_ICH
B2 CLKUSB_48
C20 T54
B24 R353 100/F
D23 R231 100/F
F22 T55
AA4 ICH_PWROK
AC22 PM_DPRSLPVR_R R376 100/F
C21 PM_BATLOW#
C23 DNBSWON#
R214 *100K
C19 R217 0/F
Y4 PM_RSMRST#_R R409 100/F
E20 SWI#
A20 DASP_ON
F19 MXM_THERM#
F19 WAKE_SCI#_R
R4 T33
E22
R3
D20 R362 100/F
AD21 T31
AD20 T150
AE20 T58
T51
FELICA_CD# 28

14M_ICH 12
CLKUSB_48 12
SUSB# 29
SUSC# 29
DNBSWON# 29
PLTRST# 14,17,27,31,33
RSMRST#
SWI# 29
GBE_CLKREQ# 31
DPRSLPVR 34

RSMRST# R423 10K
34 VR_PWRGD_CK410#
Q26 2N7002E
R241 100K
VR_PWRGD_CK410
VCC3
Consider change to logic IC next version

Note: External pull-up 3V
CKL :100Kohm PD

GPIO25 /Suspend rail is a HW strap , don't pull down .

Board ID	ID:0	ID0:1
ID1:0		
ID1:1		

MXM_ON#: 1 -> No MXM Module
0 -> MXM Module

EC54
SWI# R216 10K RVCC3
MXM_THERM# R365 *10K RVCC3

CLKUSB_48
R402 10/B
C483 10P
14M_ICH
R403 33/B
C492 10P

VCC3
R220 10K/F
R219 0/F
BIOS_REC
BIOS_REC_R
R361 *0/F

RVCC3
R230 10K/F
R233 0/F
FWH_MFG_MODE
FWH_MFG_MODE_R
R227 *0/F

3VSUS
C789 0.1U CC0402-K
U56
NC7SZ08P5X
7,34 DELAY_VR_PWRGOOD
24 NPWROK
ICH_PWROK
R660 10K

RVCC3
C100 .1U
R137 22K
U14A
U14B
7WZ14
7WZ14
RSMRST#
C109 1U

R223 10K
PCLK_SMB
Q25 2N7002E
SCLK0 12,27,29
VCC3
R215 10K
PDATA_SMB
Q22 2N7002E
SDATA0 12,27,29

QUANTA COMPUTER

Title: ICH7-M GPIO (3/4)
Size: Custom
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13,29 VCCRTC → VCCRTC
3,4,5,7,8,9,12,13,35 GMCH_VTT → GMCH_VTT

U33E
ICH7-M

U33F
ICH7-M

Oreginal 270U P/N "CH7270LM885"

Oreginal N1608ZE101T01 "CX8HS800005"

30mils
30mils
200mils

Title	ICH7-M POWER (4/4)
Size	Custom
Document Number	WR1D MAIN BOARD
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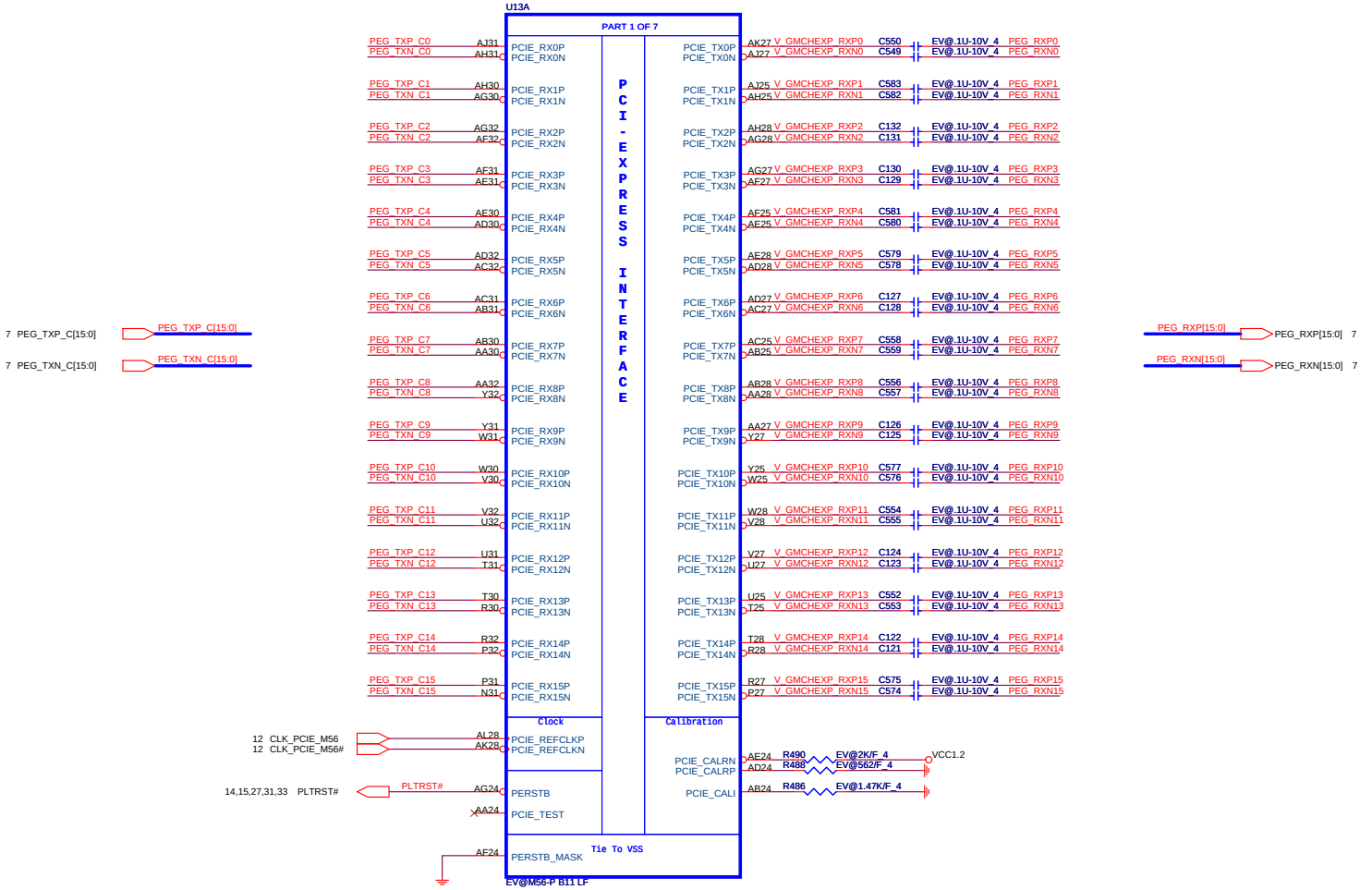
QUANTA COMPUTER

NOTE: some of the PCIE testpoints will be available trought via on traces.



Title	VGA ATi M54P_PCIE_Interface
Size	Custom
Document Number	WR1D MAIN BOARD
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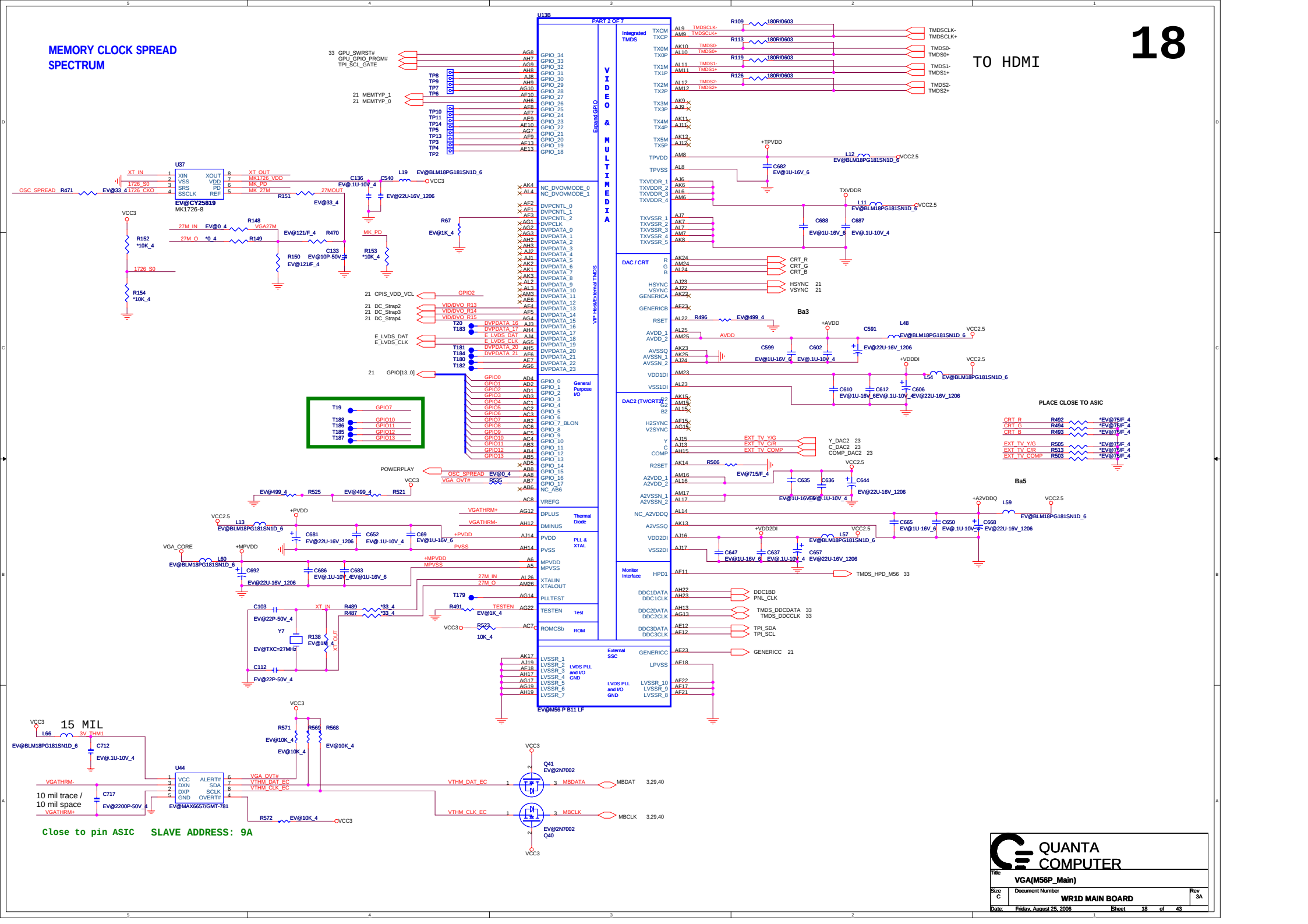
QUANTA COMPUTER


MEMORY CLOCK SPREAD SPECTRUM
TO HDMI
18
U13B
PART 2 OF 7
VIDEO & MULTIMEDIA
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
Expand GPIO
VIP Host/External TMDS
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
External SSC
LVDS PLL and I/O GND
U37
EV@CY25819
MK1726-8
U44
EV@MAX6657/GMT-781
Q41 EV@2N7002
Q40 EV@2N7002
EV@M56-P B11 LF
PLACE CLOSE TO ASIC
Ba3
Ba5
15 MIL
10 mil trace / 10 mil space
Close to pin ASIC
SLAVE ADDRESS: 9A
QUANTA COMPUTER
VGA(M56P_Main)
WR1D MAIN BOARD
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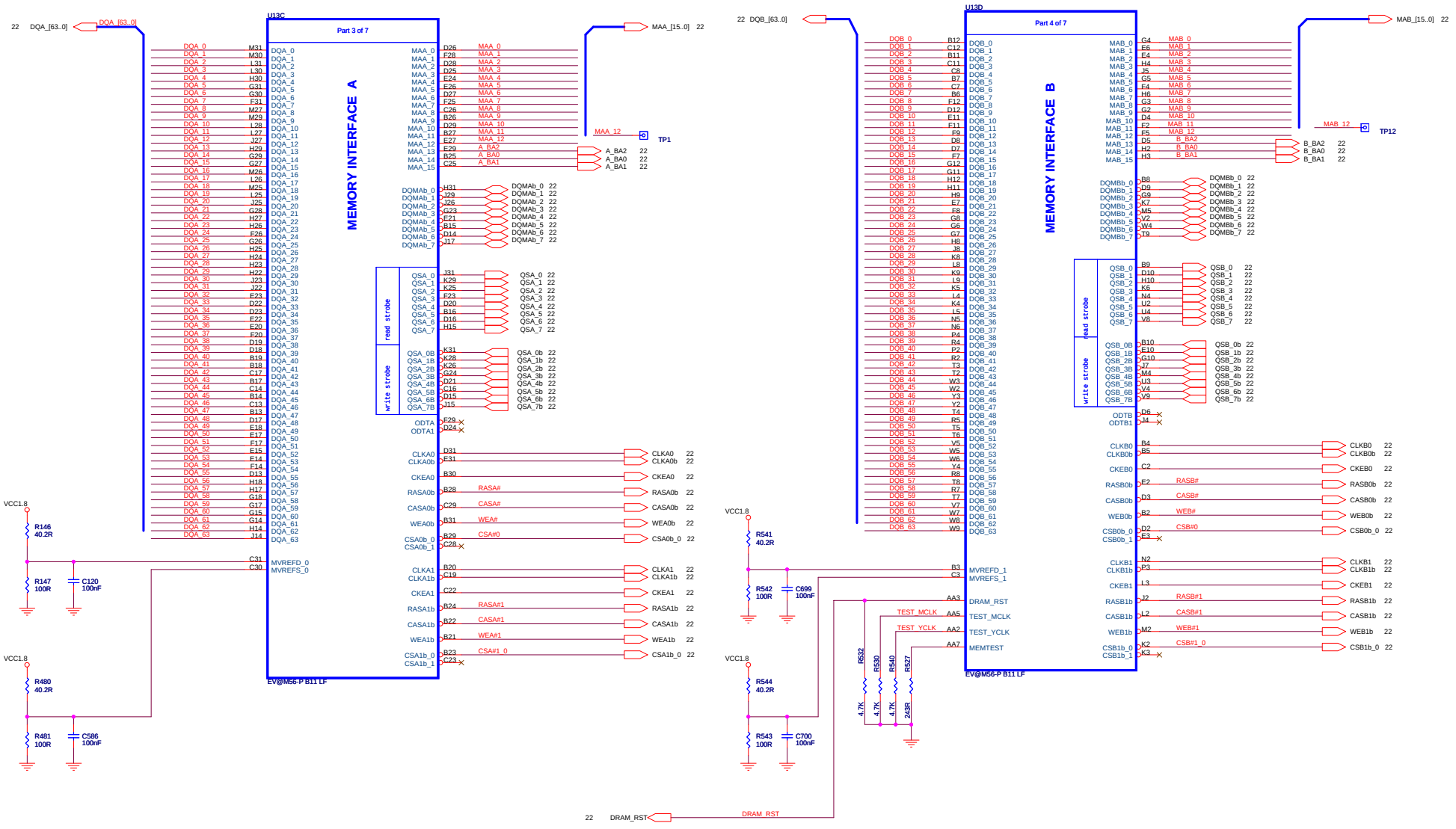
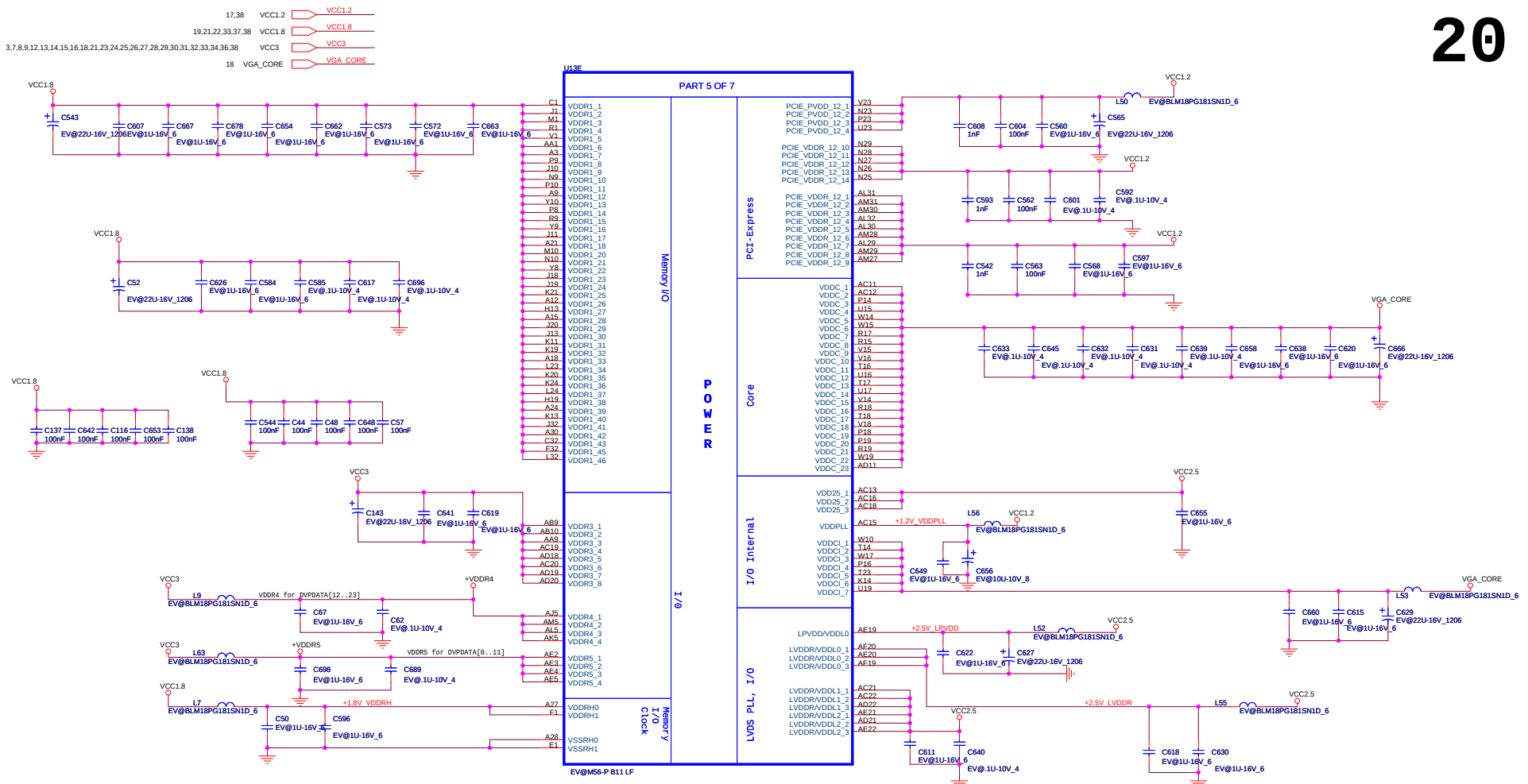


QUANTA COMPUTER

Title	VGA M56P Memory A_B	
Size C	Document Number WR1D MAIN BOARD	Rev 3A
Date: Friday, August 25, 2006	Sheet 19 of 43	



Title	VGA Video Memory
Size	C
Document Number	WR1D MAIN BOARD
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Date:	Friday, August 25, 2006
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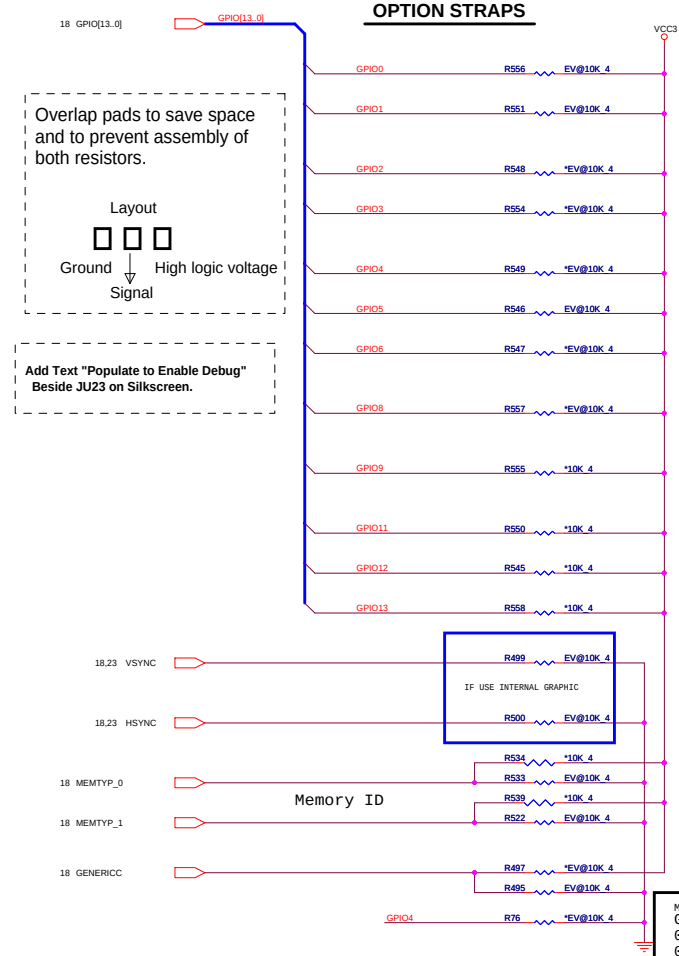
QUANTA COMPUTER

OPTION STRAPS



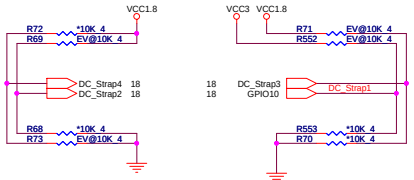
Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground ↓ High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.



Memory Aperture Size Select
When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the memory aperture size.
GPIO[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

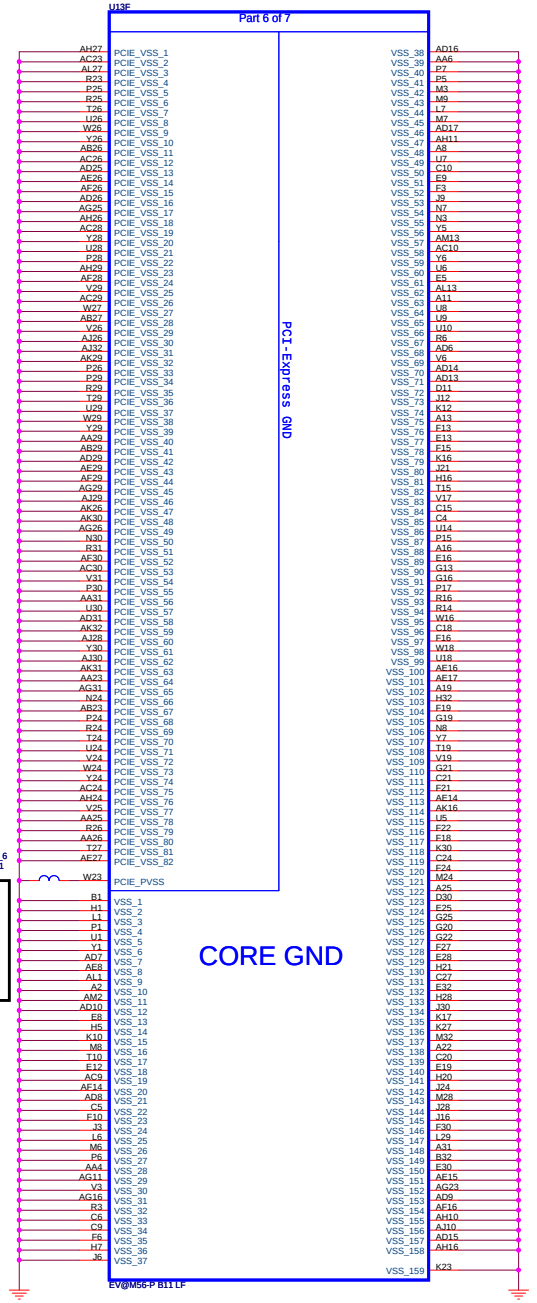
M56-P Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force_Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 001x - No ROM,MEM_AP_SIZE=01 010x - No Rom, MEM_AP_SIZE=10 011x - No ROM,MEM_AP_SIZE=11 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port devices present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

MEMTYP_1	MEMTYP_0	Vendor	Part No	Package organized	Memory Size	
GPIO27	GPIO26					
0	0	Samsung	K4J52324QC-BC14	512M(16Mx32) GDDR3	256MB(dual channel)	R522,R533
0	1	Samsung	K4J55323QG-BC20	256M(8Mx32) GDDR3	128MB(Dual channel)	R522,R534
1	0	Infineon	HYB18H512321AFL20	512M(16Mx32) GDDR3	256MB(dual channel)	R539,R533
1	1	Infineon	HYB18H256321AFL20	256M(8Mx32) GDDR3	128MB(Dual channel)	R539,R534

Board Straps REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO27,26	Memory Type select 00 Samsung 256MB(dual channel) 01 Samsung 128MB(dual channel) 10 Infineon 256MB(dual channel) 11 Infineon 128MB(dual channel)	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1



EV@BLM18PG181SN1D_6
L51

QUANTA COMPUTER

Title	VGA P_Core_GND		
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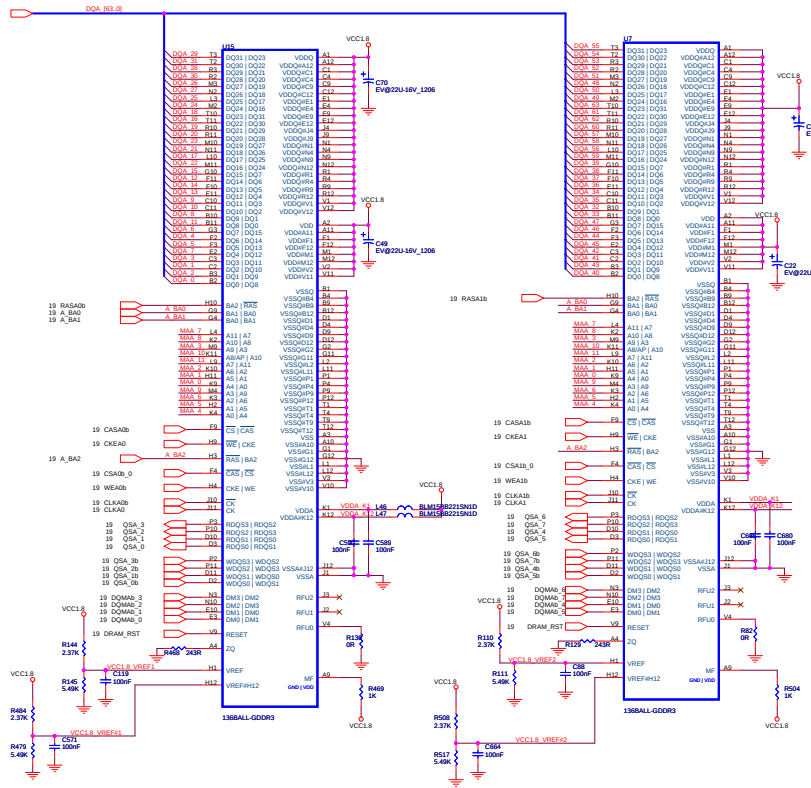
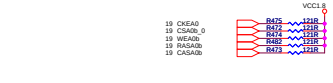
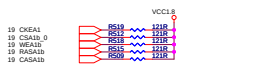
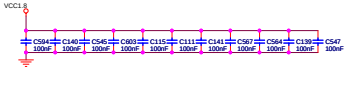
256 Mbit GDDRIII Channels A and B Rank 1

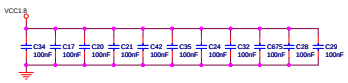
Channel A

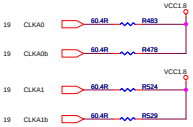


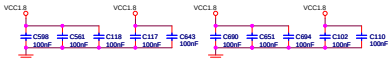




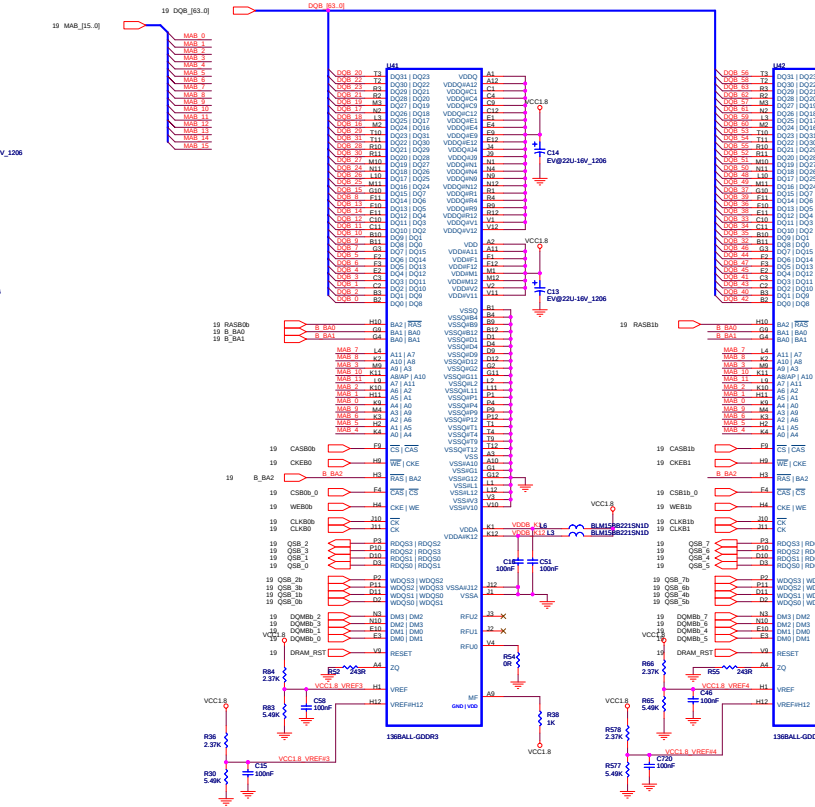


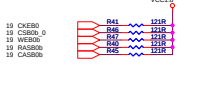


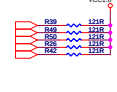


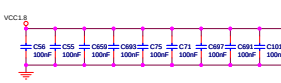


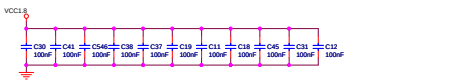
Channel B

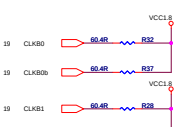












QUANTA COMPUTER			
Title: VGA Video Memory(GDDRIII_A_B_Rank0)			
Size: Custom	Document Number: WR1D MAIN BOARD		Rev: 3A
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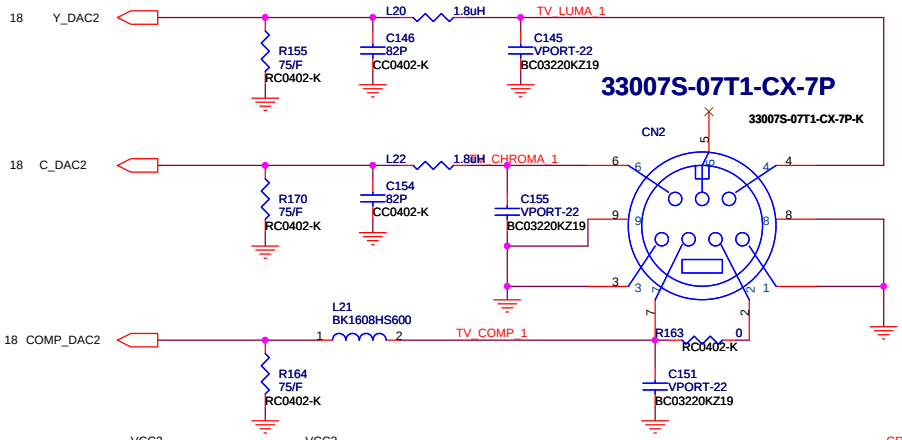
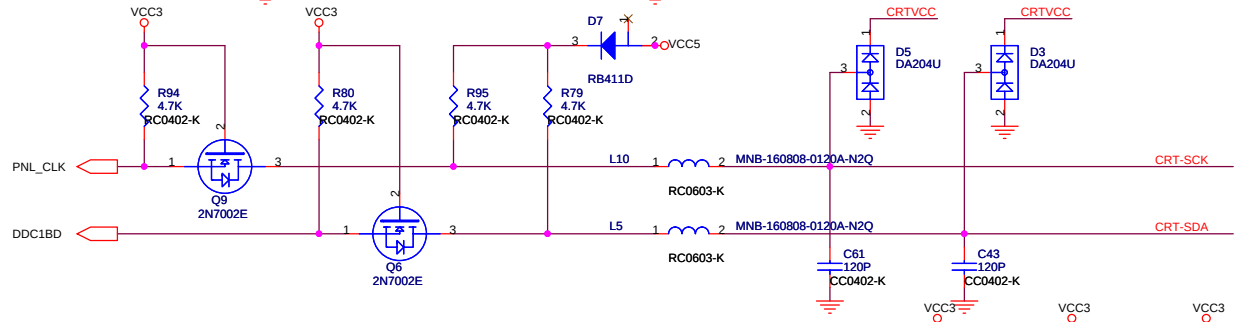
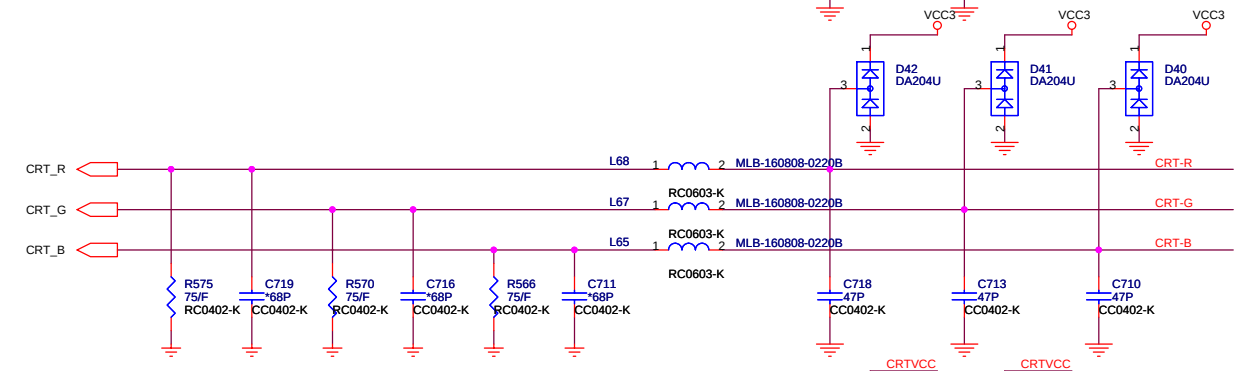
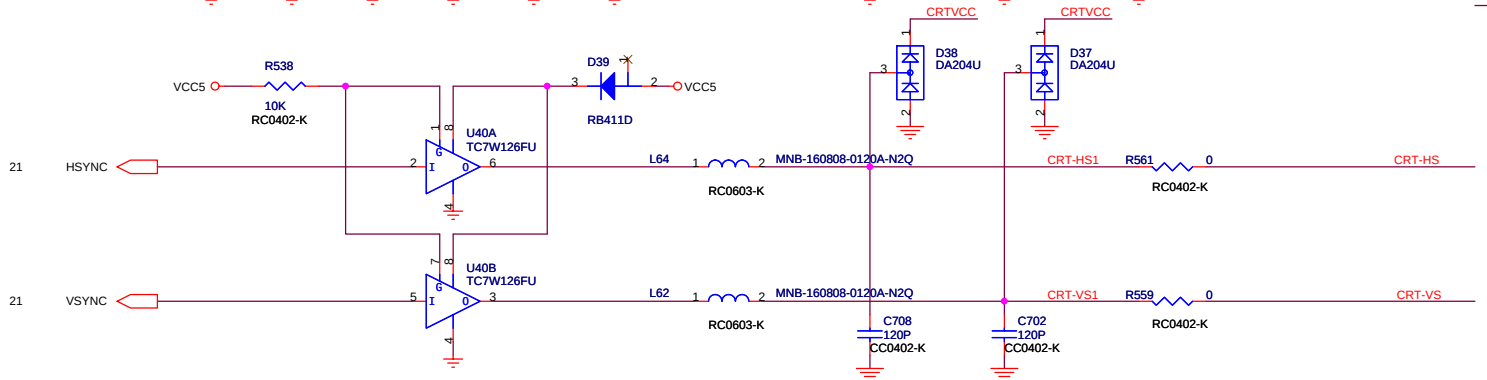
S-VIDEO CONNECTOR

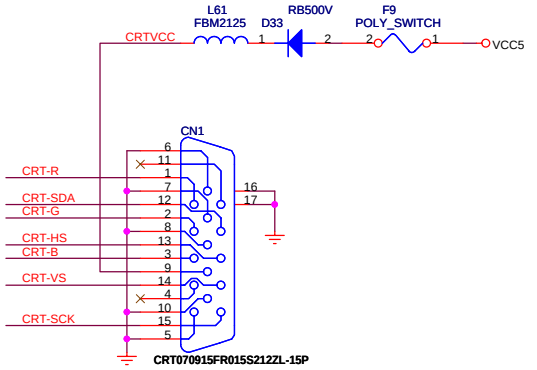








CRT CONNECTOR

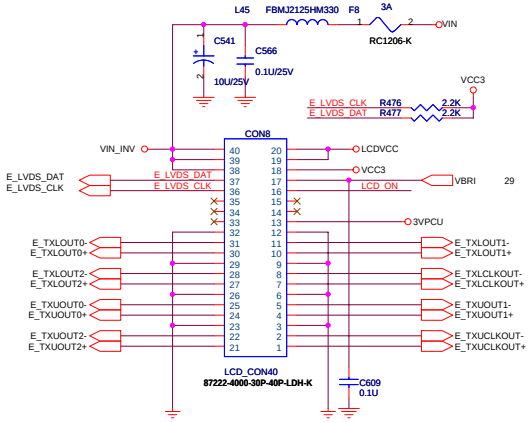


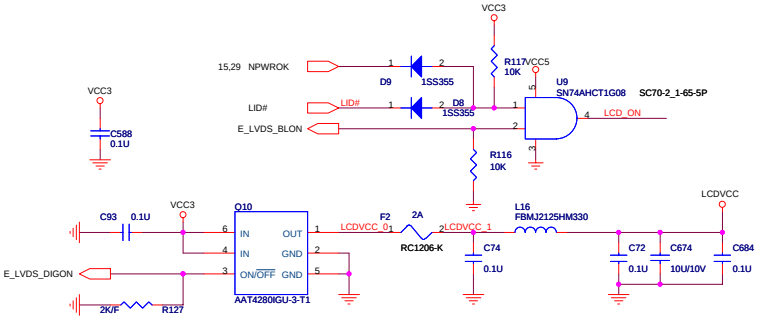
VCC5 VCC5 16,24,25,26,28,29,30,31,32,33,38

VCC3 VCC3 10,11,13,14,15,16,18,20,21,24,25,26,27,28,29,30,31,32,33,34,36,38

QUANTA COMPUTER

Title	CRT/TV OUT PORT	
Size B	Document Number WR1D MAIN BOARD	Rev 3A
Date: Friday, August 25, 2006	Sheet 23 of 43	

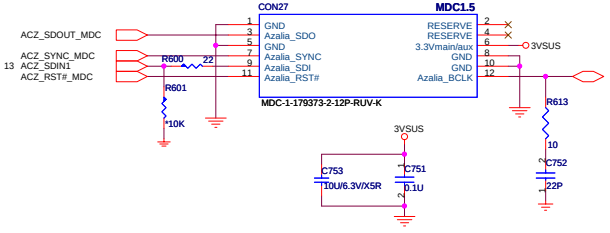


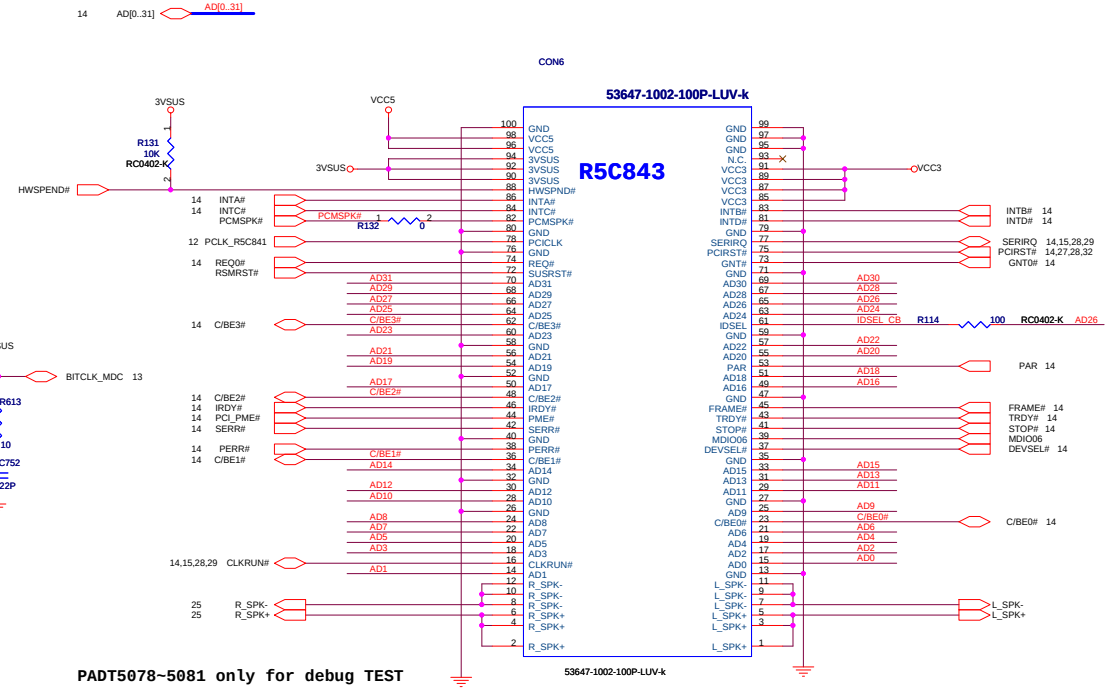


PANEL VCC CONTROL

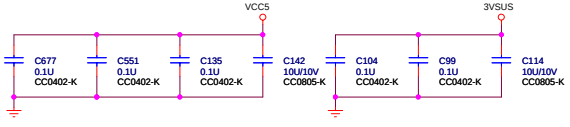
CARD READ	MINIPCI	TV
IDSEL:AD26	IDSEL:AD20	IDSEL:AD28
INTA,B,C	INTA,B	INTC,D
REQ0	REQ2	REQ3
PCICLK2	PCICLK0	PCICLK6

HD_MDC





PADT5078~5081 only for debug TEST



QUANTA COMPUTER

Title: **Daughter board CONN**

Size	Document Number	Rev
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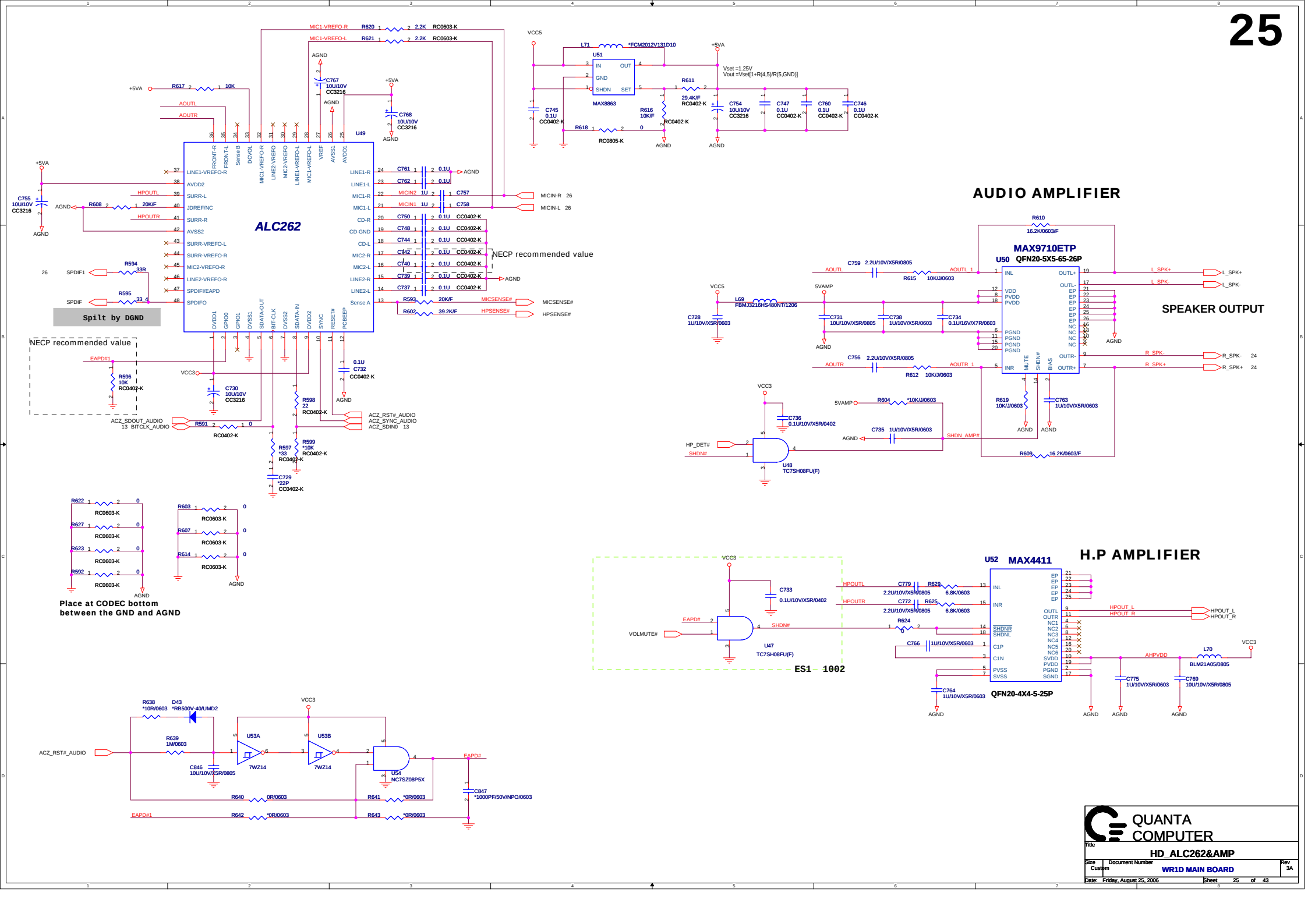
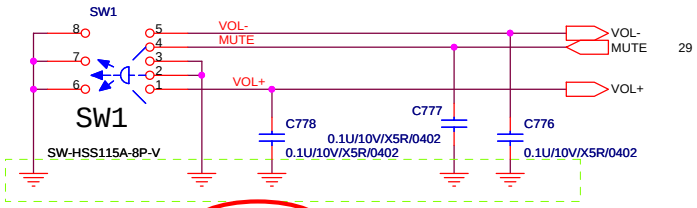
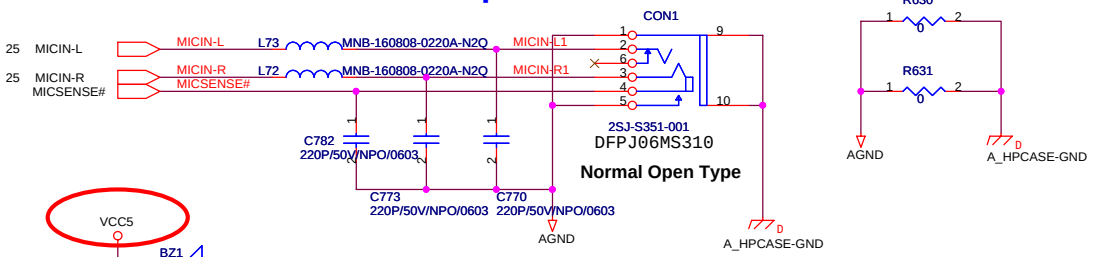

ALC262
Spilt by DGND
NECP recommended value
NECP recommended value
Place at CODEC bottom
between the GND and AGND
AUDIO AMPLIFIER
MAX9710ETP
U50 QFN20-5X5-65-26P
SPEAKER OUTPUT
H.P AMPLIFIER
U52 MAX4411
QFN20-4X4-5-25P
MAX8863
U51
*FCM2012V131D10
Vset =1.25V
Vout =Vset[1+R(4,5)/R(5,GND)]
U49
U47
TC7SH08FU(F)
U48
TC7SH08FU(F)
U53A
U53B
7WZ14
7WZ14
U54
NC7SZ08P5X
ES1 1002
QUANTA COMPUTER
HD_ALC262&AMP
WR1D MAIN BOARD
Friday, August 25, 2006

Multi-SW

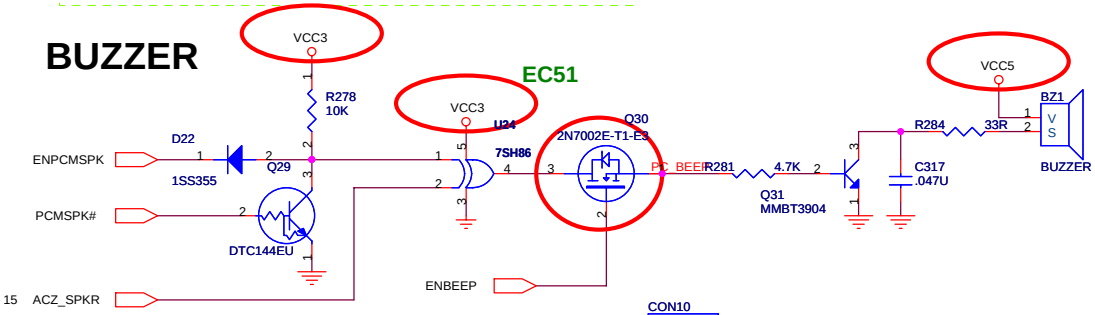


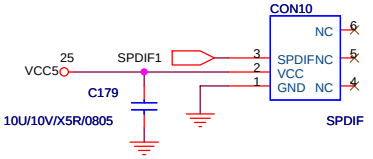
MIC-IN

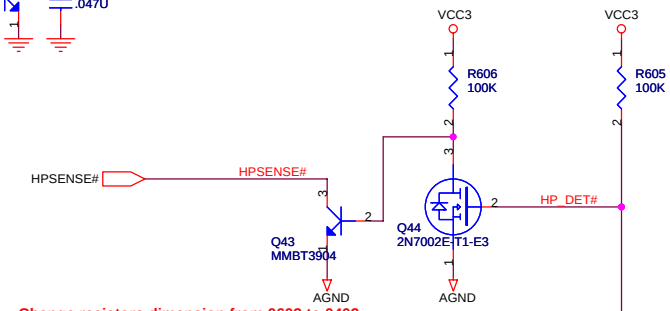
Max. 100mVrms input for Mic-IN



BUZZER

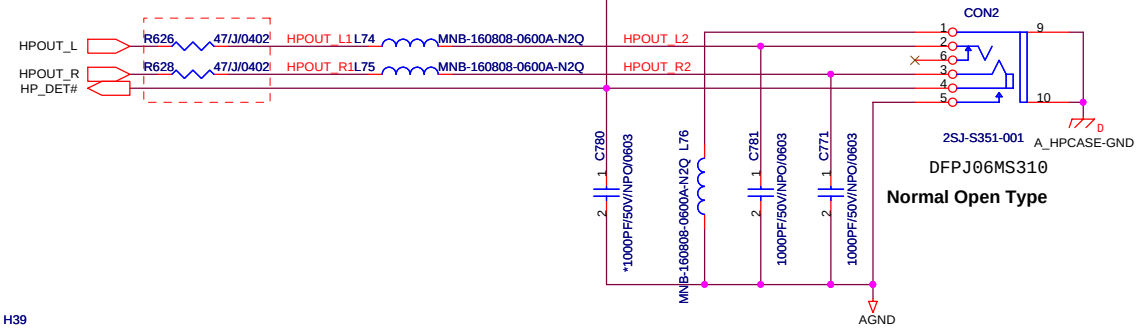


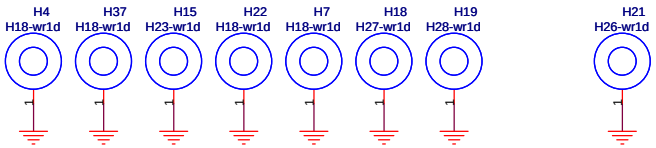


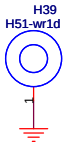


Change resistors dimension from 0603 to 0402
to prevent PCB bending cause solder and components
crack issue!

Headphone-OUT







QUANTA COMPUTER

Title	BUZZER & AUDIO/BOARD	
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Mini PCI-E Card

When system support at wake on wireless
RF_SW# pull-high 3VSUS

keep RP47,RP48,R581 for debug

WLSW:
Low : disable the radio.
High : Enable the radio.

EC50

New Card

EXPRESS CARD SLOT

1. Pin assignments for ExpressCard connector is wrong.
   Please change 7 pin from RSVD#1 to SMBCLK.
   Please change 8 pin from SMBCLK to SMBDATA.
   Please change 9 pin from SMBDATA to 1.5V.
2. Please apply 100K pull-up resistor to CPPE#.
3. Please apply 100K pull-up resistor to CPUSB#.
4. Please apply capacitor (0.1uF and 10uF) to +3.3V_NC1, +3.3VAUX_NC1 and +1.5V_NC1 respectively.

Title	Mini PCI-E / NEW Card	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
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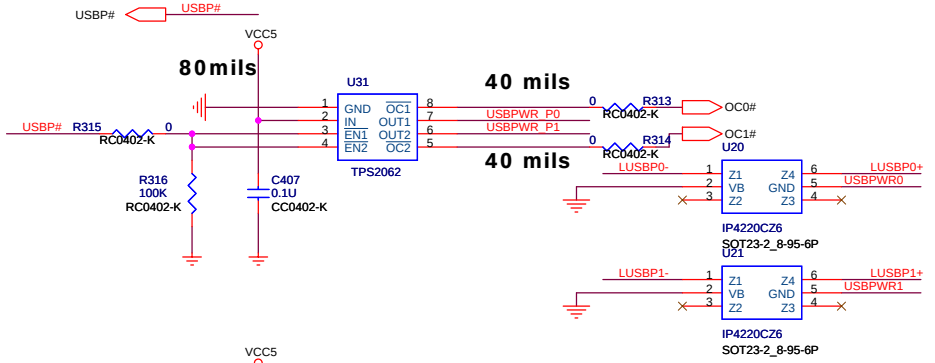
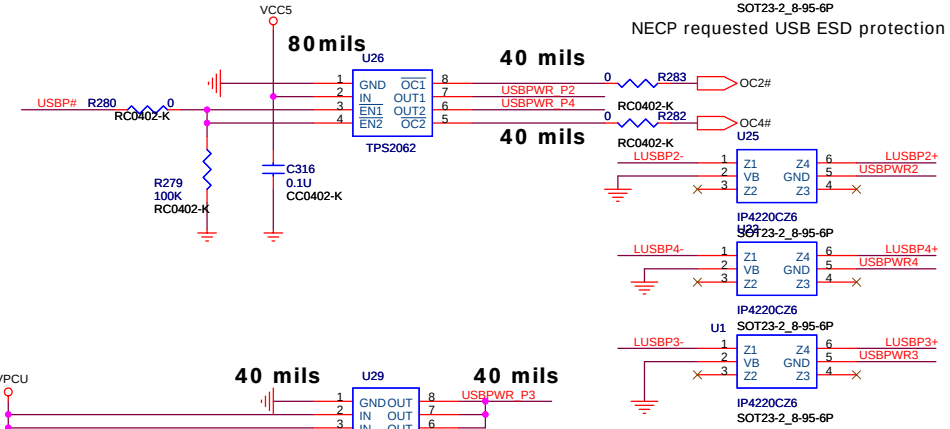
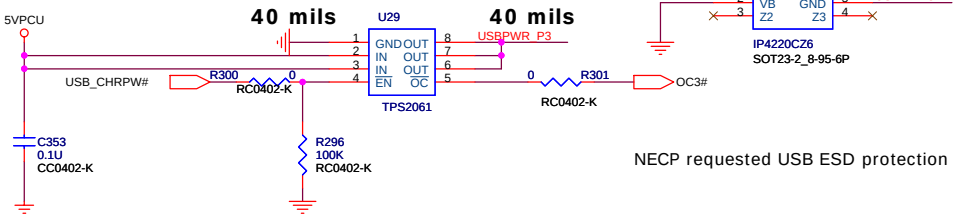
QUANTA COMPUTER

USB Power and Over current



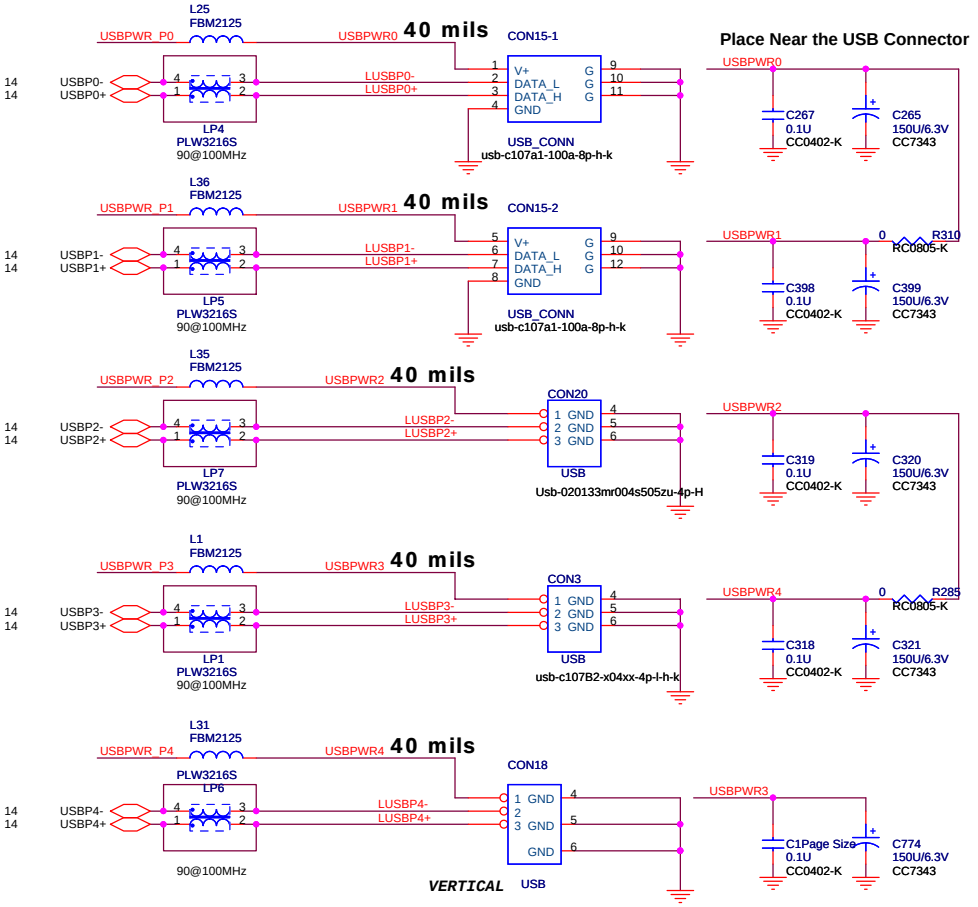
NECP requested USB ESD protection



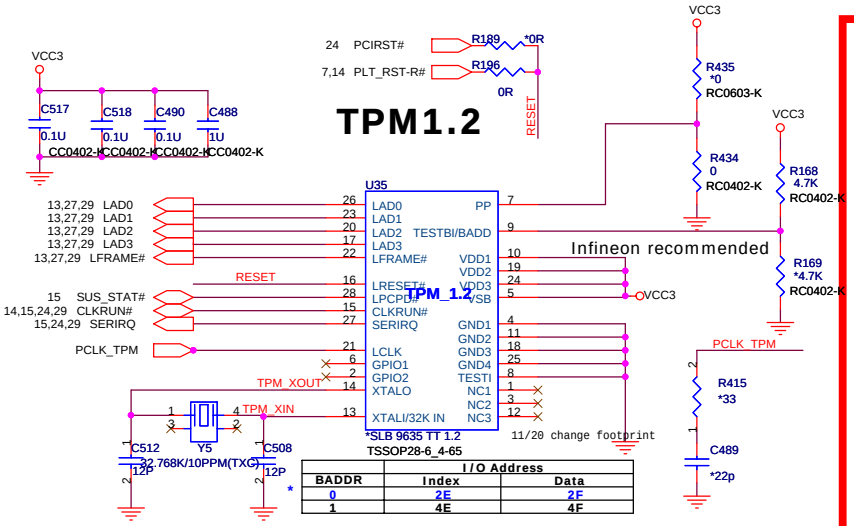


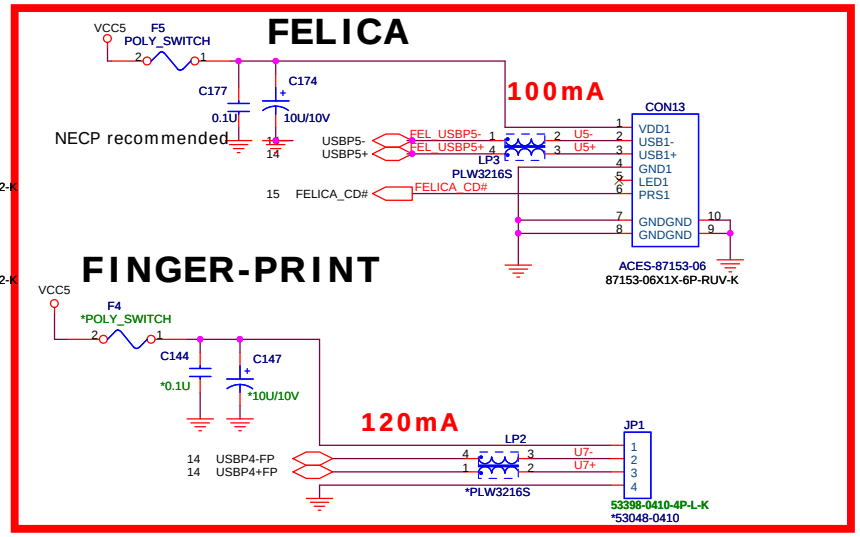
NECP requested USB ESD protection

USB Connector



Place Near the USB Connector





NECP request to add self power protection

QUANTA COMPUTER

Title	USB&TPM&FELICA&FINGER-PRINT	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
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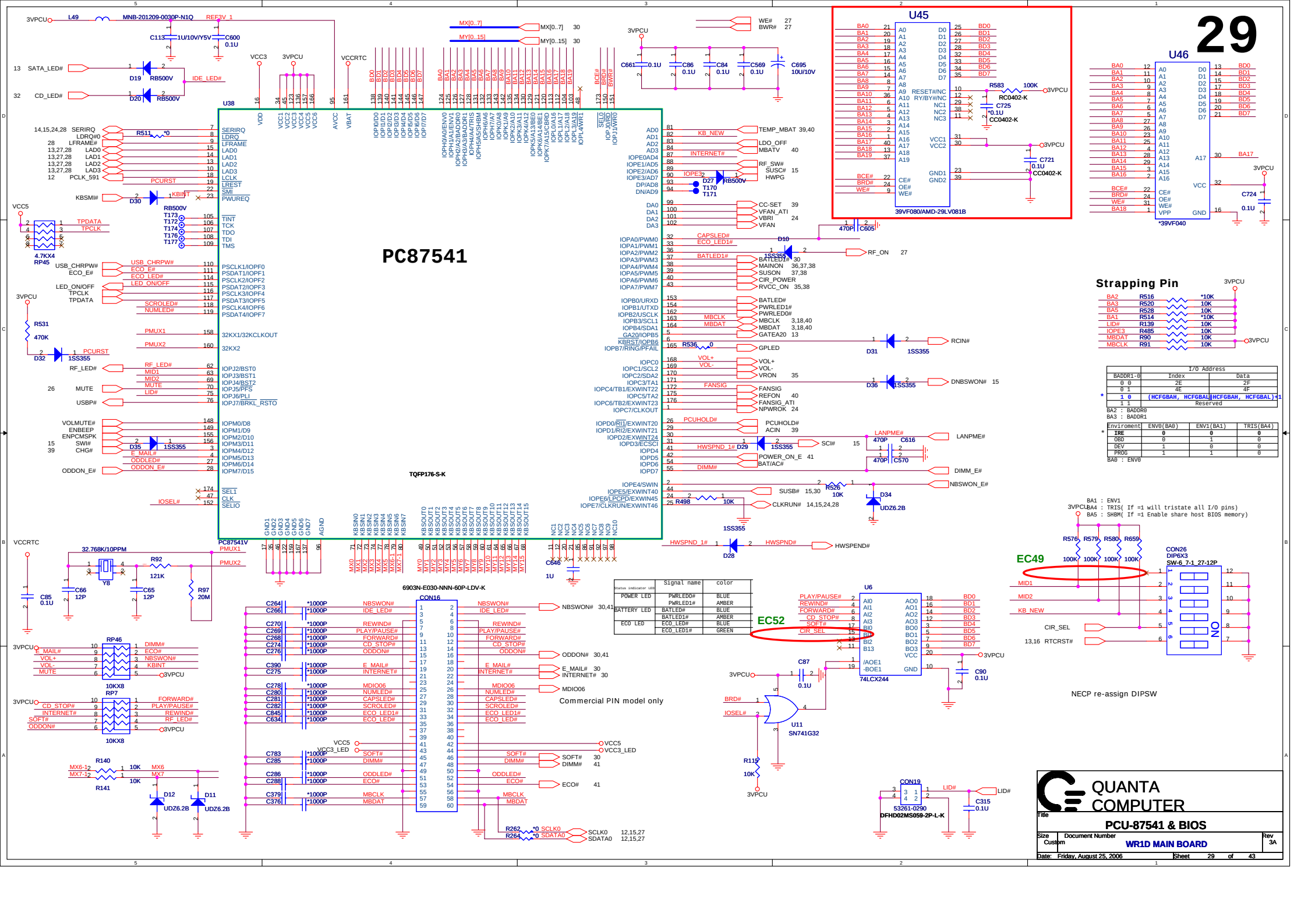
29
PC87541
TQFP176-S-K
U38
U45
39VF080/AMD-29LV081B
U46
*39VF040
Strapping Pin
I/O Address
EC49
EC52
U6
74LCX244
U11
SN741G32
CON16
6903N-E030-NNN-60P-LDV-K
CON26
DIP6X3
SW-6 7-1 27-12P
CON19
53261-0290
DFHD02MS059-2P-L-K
Commercial PIN model only
NECP re-assign DIPSW
QUANTA COMPUTER
PCU-87541 & BIOS
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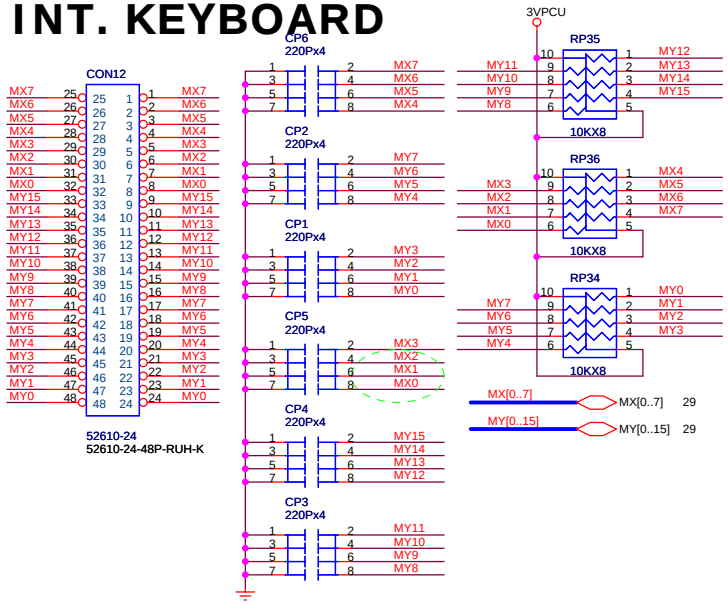
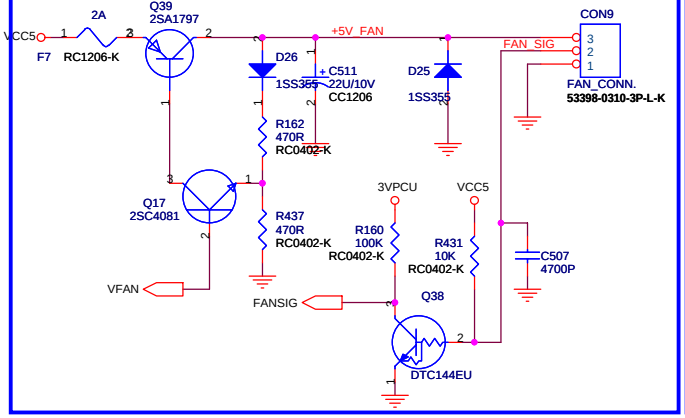
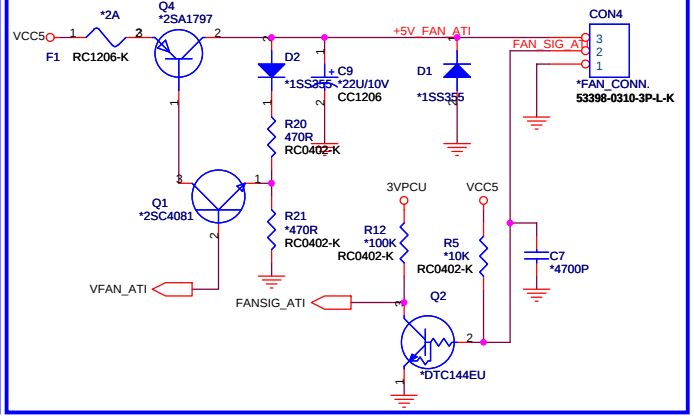
INT. KEYBOARD



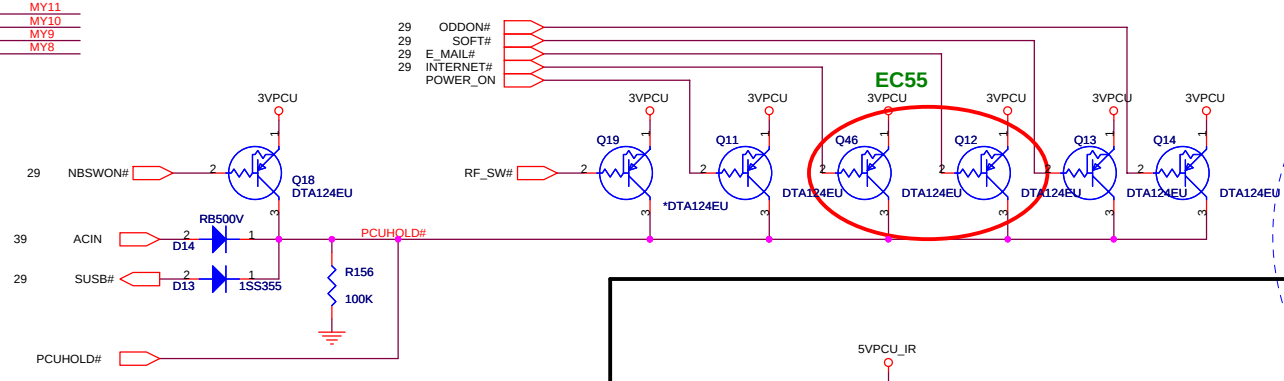
CPU FAN Circuit

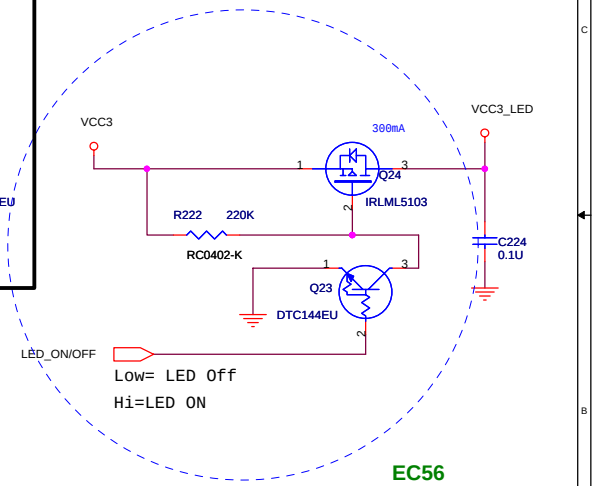


ATI FAN Circuit

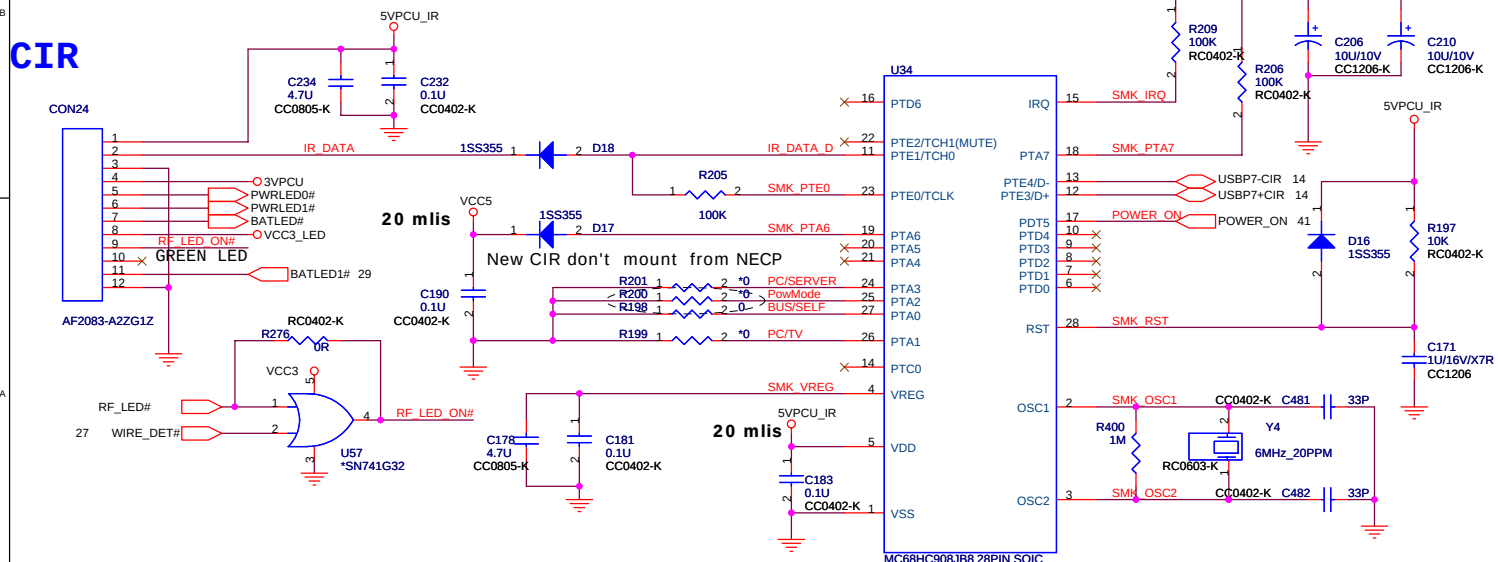


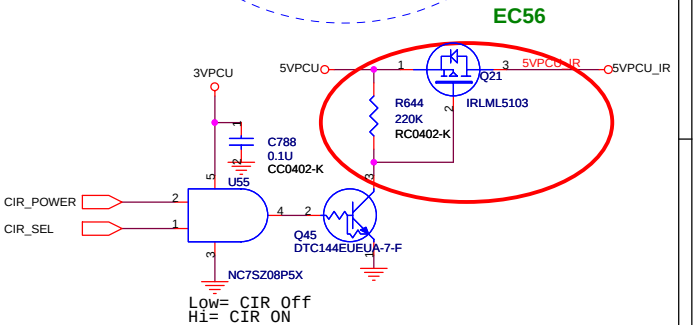
30





CIR





QUANTA COMPUTER

Title	INT.KB & FAN & PS2&CIR	
Size: Custom	Document Number: WR1D MAIN BOARD	Rev: 3A
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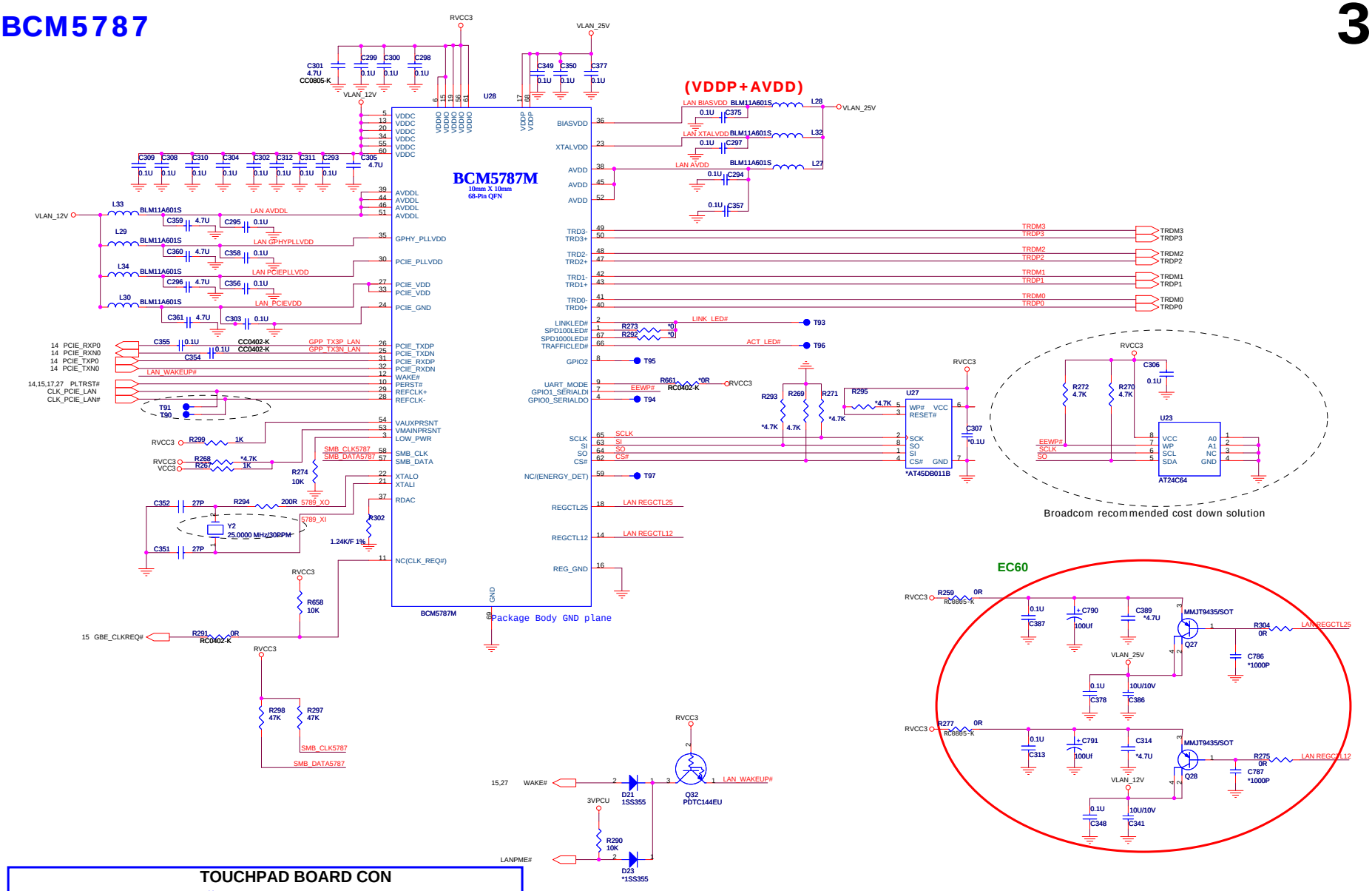
BCM5787



QUANTA COMPUTER			
Title	BCM5787M &TouchPAD CONN		
Size: Custom	Document Number: WR1D MAIN BOARD		Rev: 3A
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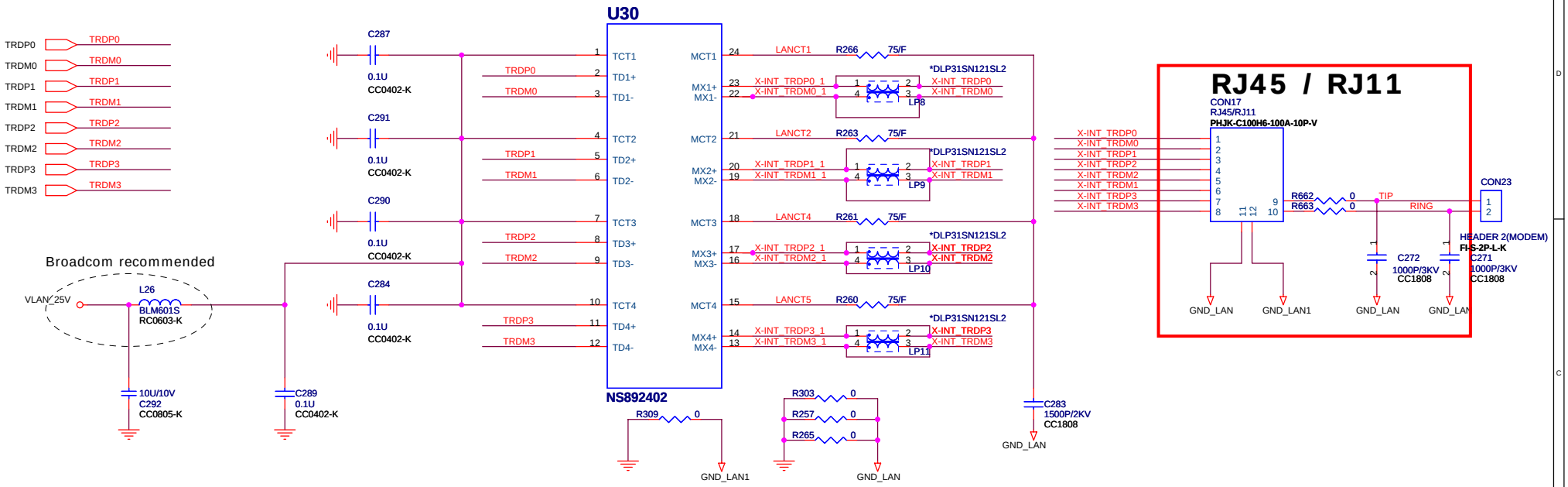
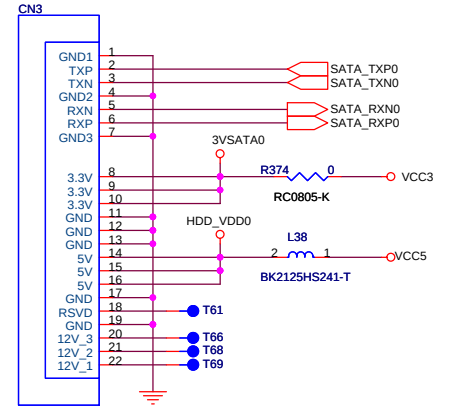
LAN TR & CONNECTOR

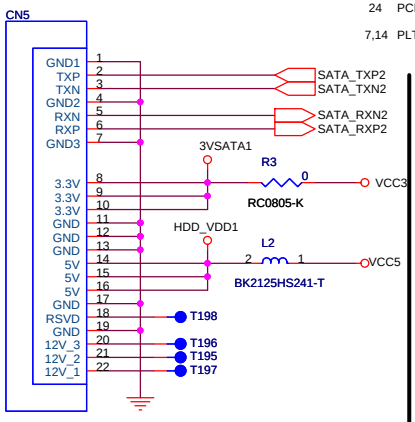
32

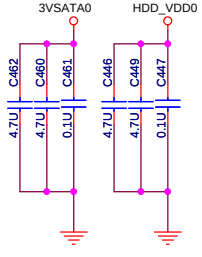


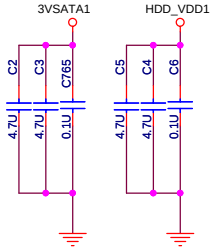
SATA_TOP(MASTER)



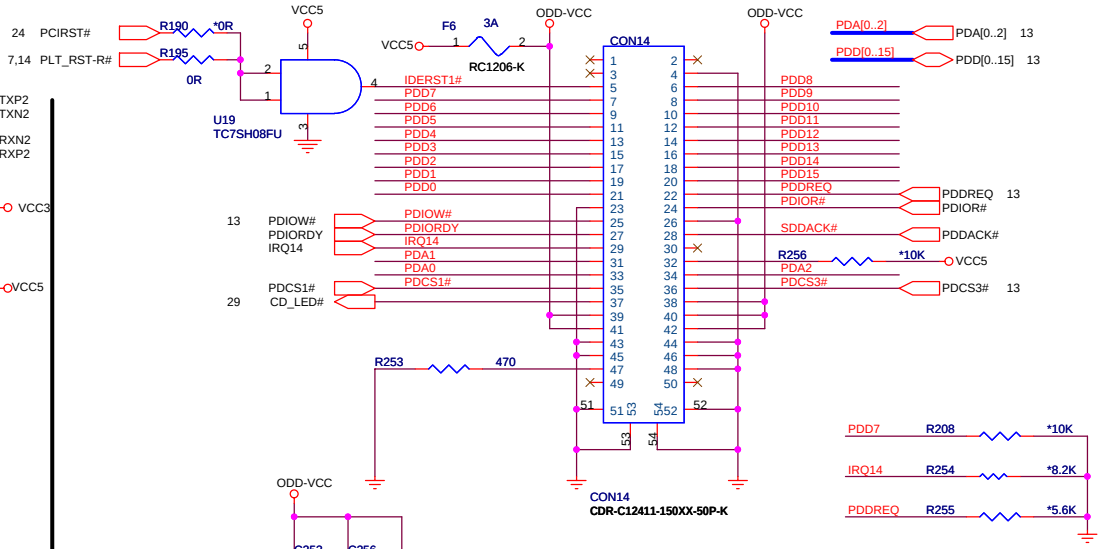
SATA_BOT(SLAVER)







ODD interface



Title	LAN(TR&CONNECTOR) &SATA HDD +ODD		
Size B	Document Number WR1D MAIN BOARD		Rev 3A
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PVCC1 67mA
PVCC2 13.5mA
SPVCC 30mA
SVCC 323mA
VCC 133mA

HDMI PORT

Place close to the connector

Improve signal swing

Please near U12

Please near U7001

Sil1930

Sil1930 TQFN package

For Sil1930,should be openned (default)
For Sil1932,should be connected

I2C ADDRESS = 20h

Mount R63, keep R64 NC at the beginning
Remove R63, mount R64 after VBIOS add PRGM# function.

To U7014#4

Open if use Atmel uC

R7110 For ES1 debug only

P1.2,P1.3 : Software I2C (SST)
P4.1,P4.3 : Hardware I2C (ATMEL)

Silicom request need to add this MOSFET to avoid ATMEL latch up

HDMI_SDA & HDMI_SCL capacitance MUST less than 50PF

Title	HDMI INTERFACE
Size	Custom
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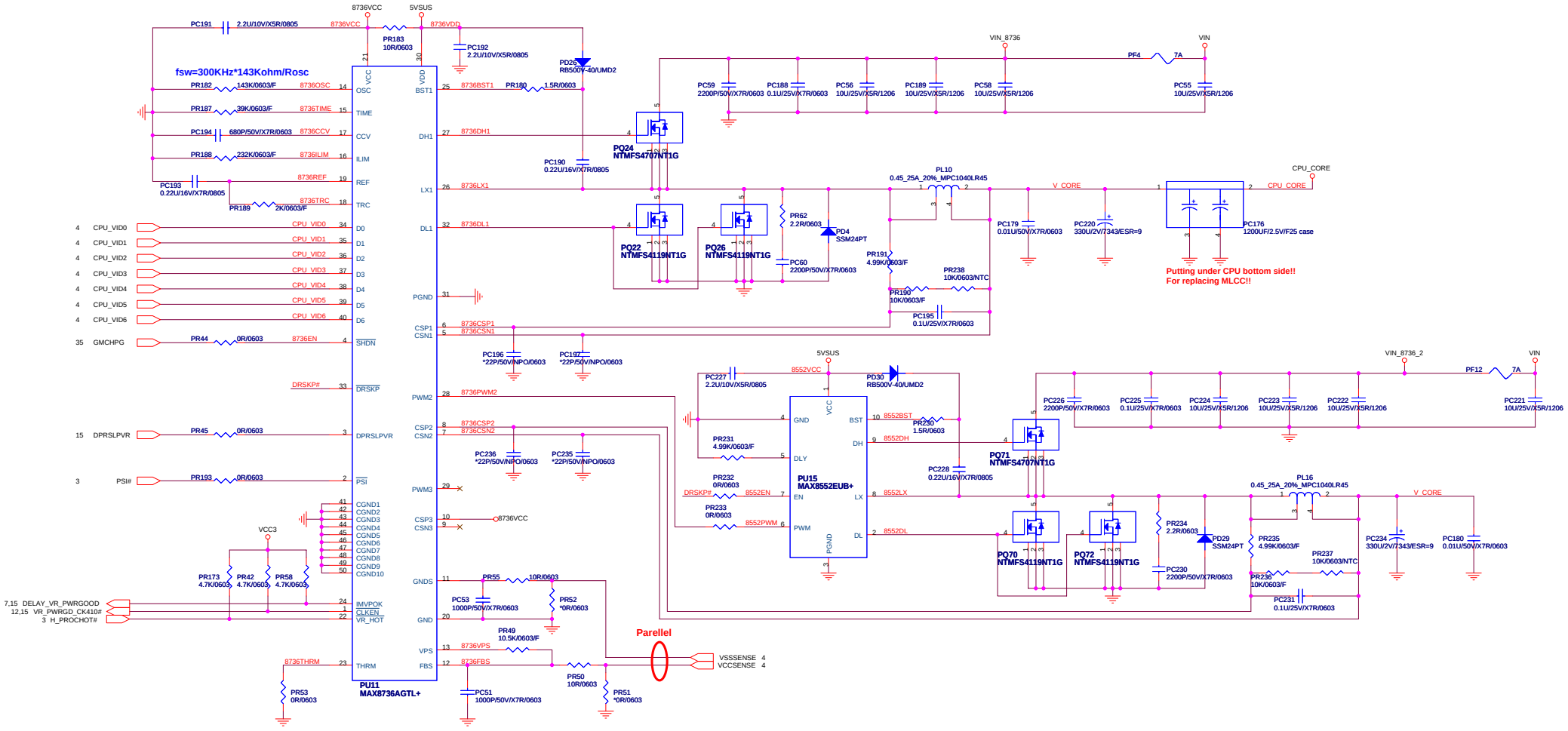
CPU CORE

dV_Target/dt=12.5mV/us*71.5kohm/R_TIME

R_ILIM(PK)=8V*R_TRC/I(PK)LIMIT*Rsense



Title	CPU CORE (MAX8736)
Size	Custom
Document Number	WR1D MAIN BOARD
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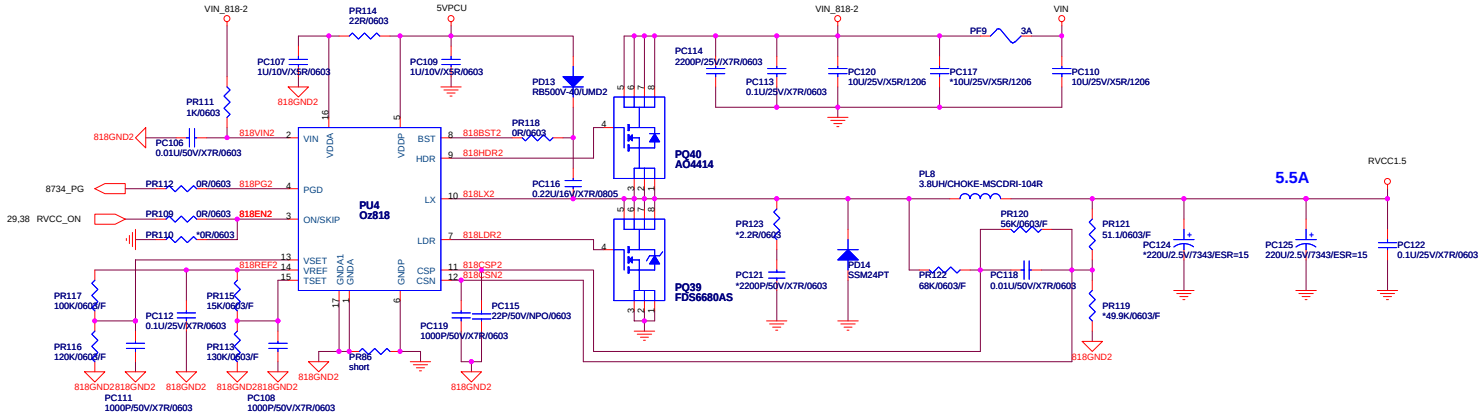
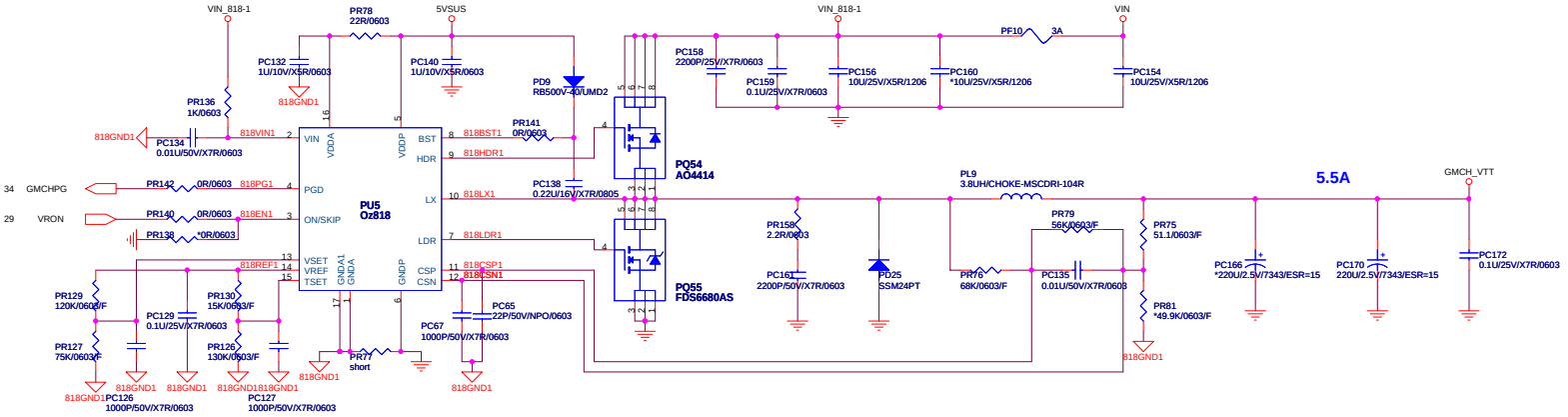
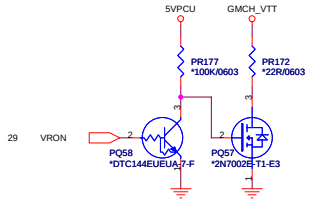
QUANTA COMPUTER

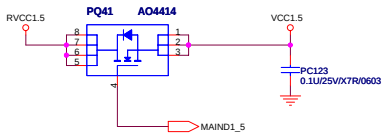
GMCH_VTT(1.05V) / RVCC1.5

38 RVCC1.5 → RVCC1.5
7,8,14,16,27,38 VCC1.5 → VCC1.5
24,34,36,38,39,40 VIN → VIN
7,9,13,16 GMCH_VTT → GMCH_VTT









QUANTA COMPUTER

Title	GMCH_VTT & RVCC1.5	
Size	Document Number: WR1D MAIN BOARD	Rev: 3A
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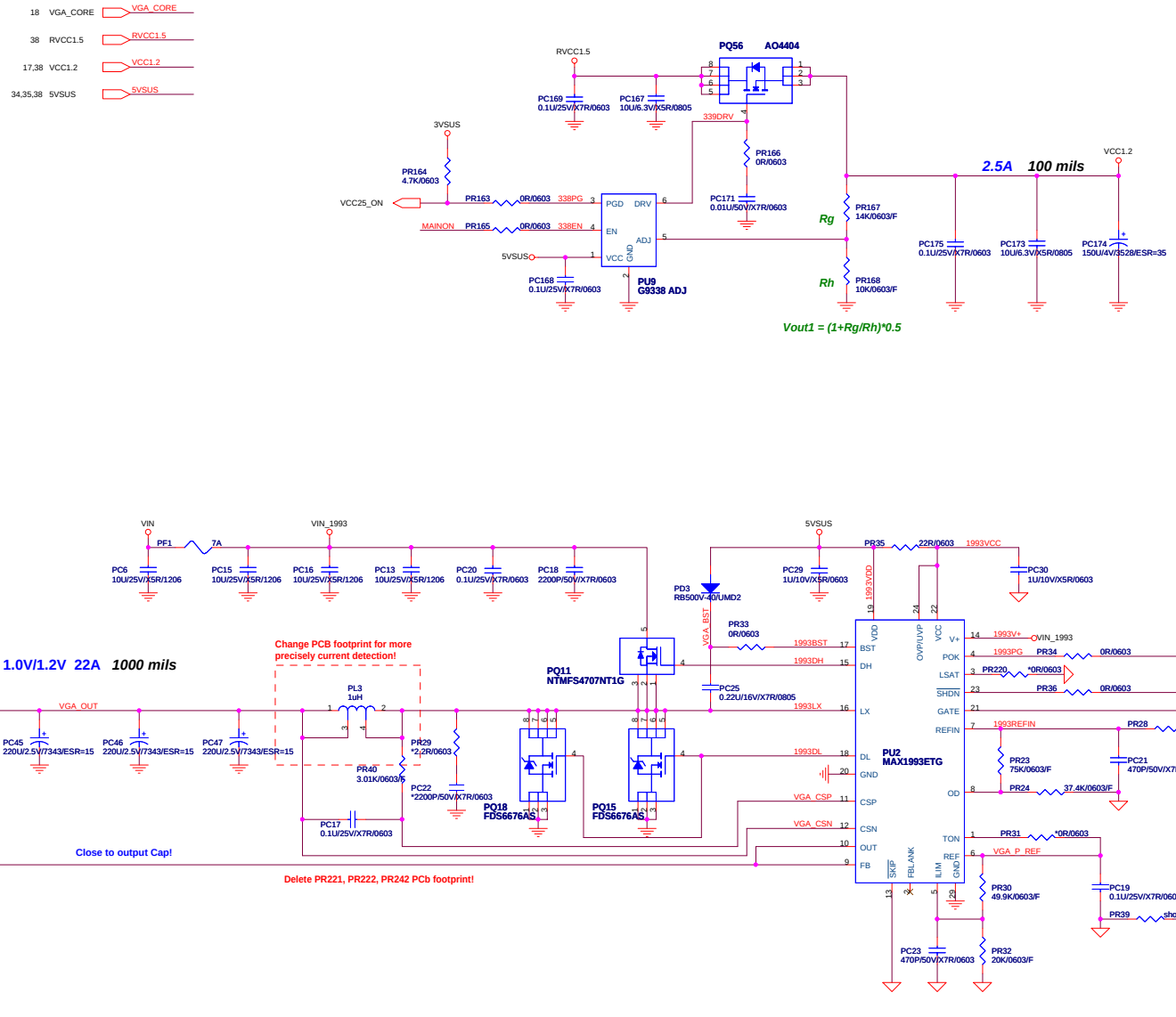
VGA Core & VCC1.2



QUANTA COMPUTER

Title: VGA POWER

Size: Custom | Document Number: WR1D Main Board | Rev: 3A

Date: Friday, August 25, 2006 | Sheet 36 of 43

SMDDR_VREF — SMDDR_VREF 7,10,11

SMDDR_VTERM — SMDDR_VTERM 10

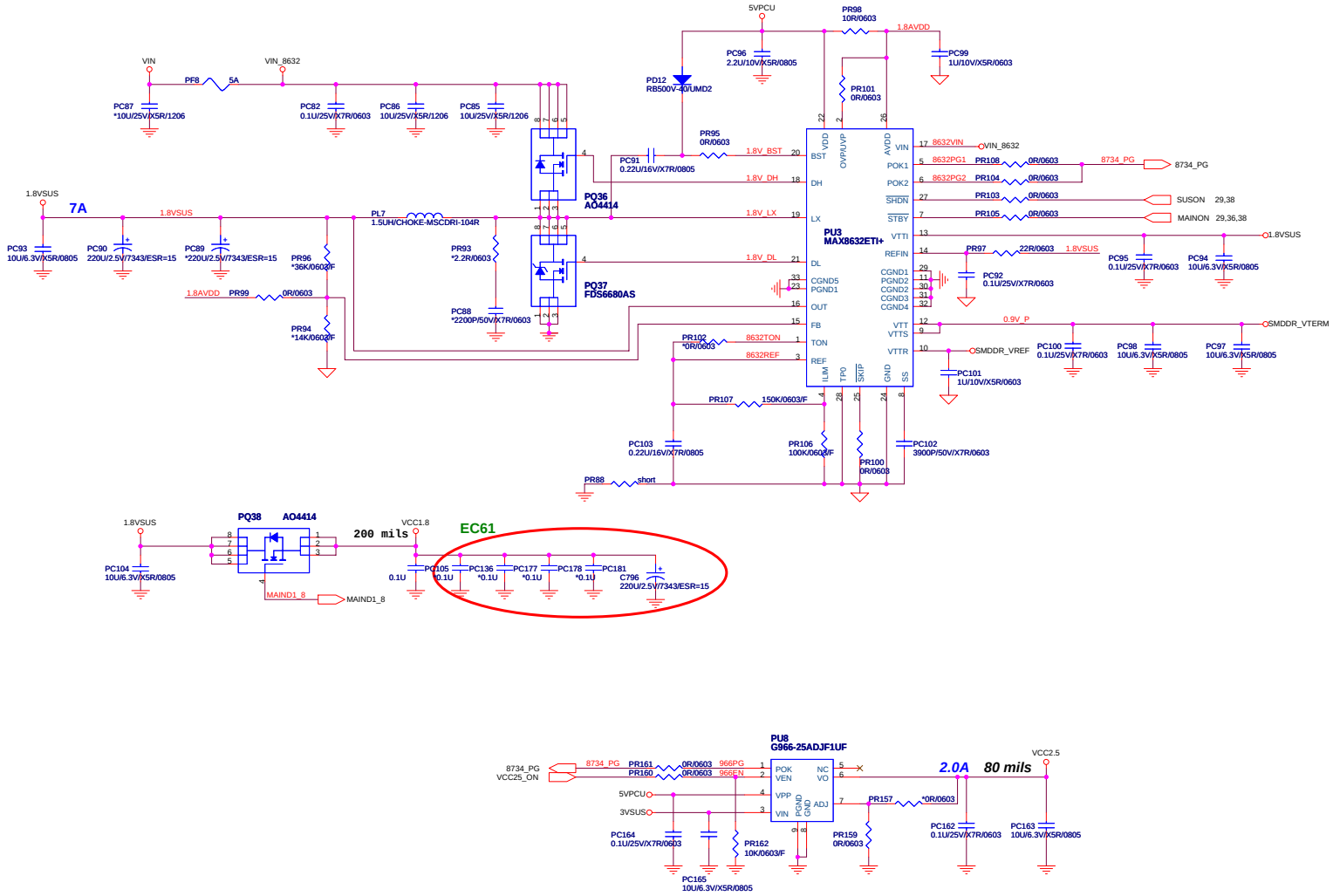
VCC1.8 — VCC1.8 19,20,21,22,33,38

1.8VSUS — 1.8VSUS 10,11,38

VCC2.5 — VCC2.5 18,20,38

VIN — VIN 24,34,36,38,39,40

1.8VSUS & VTT & VCC2.5



Title	1.8VSUS & VTT & VCC2.5		
Size: Custom	Document Number: WR1D Main Board		Rev: 3A
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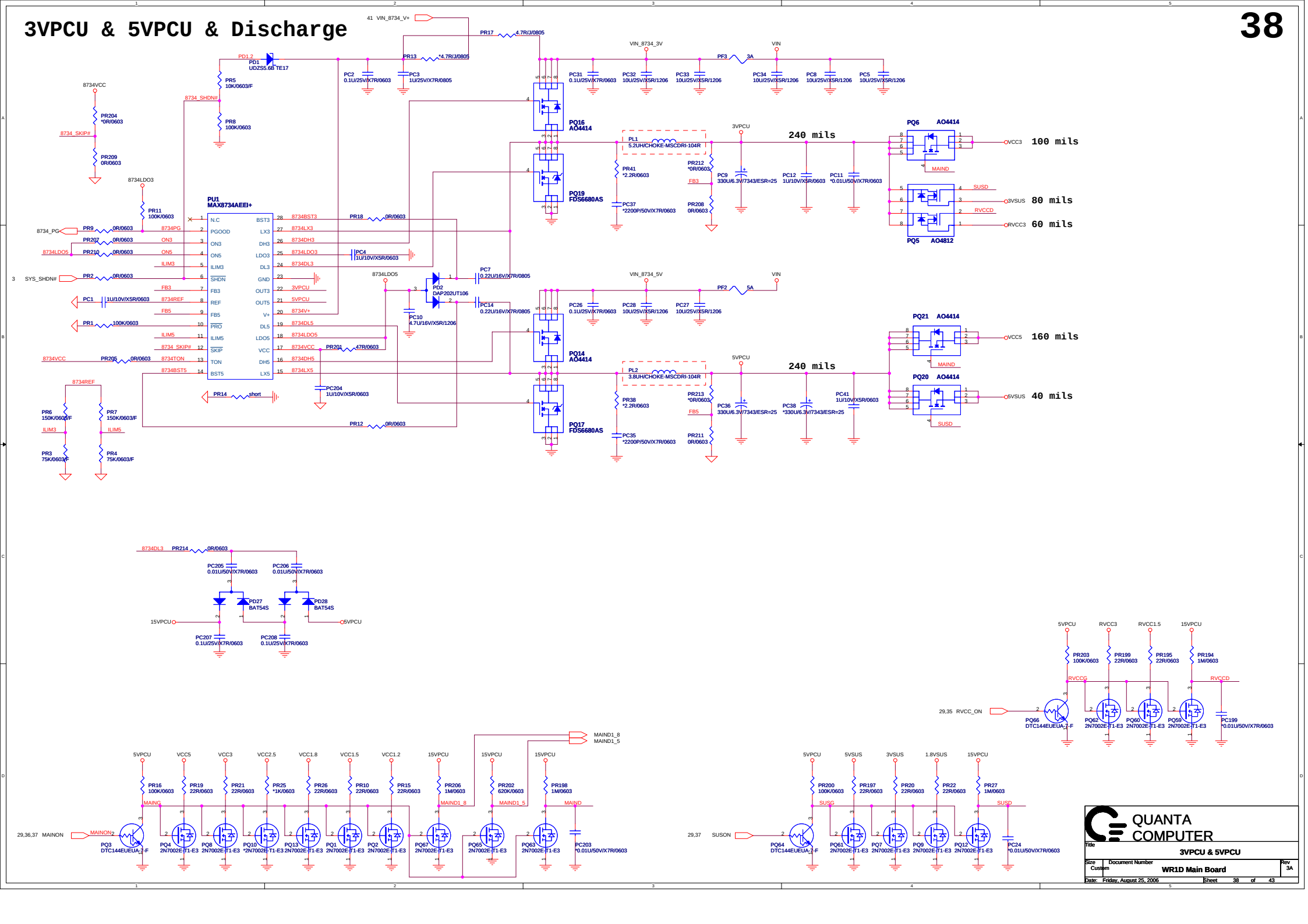
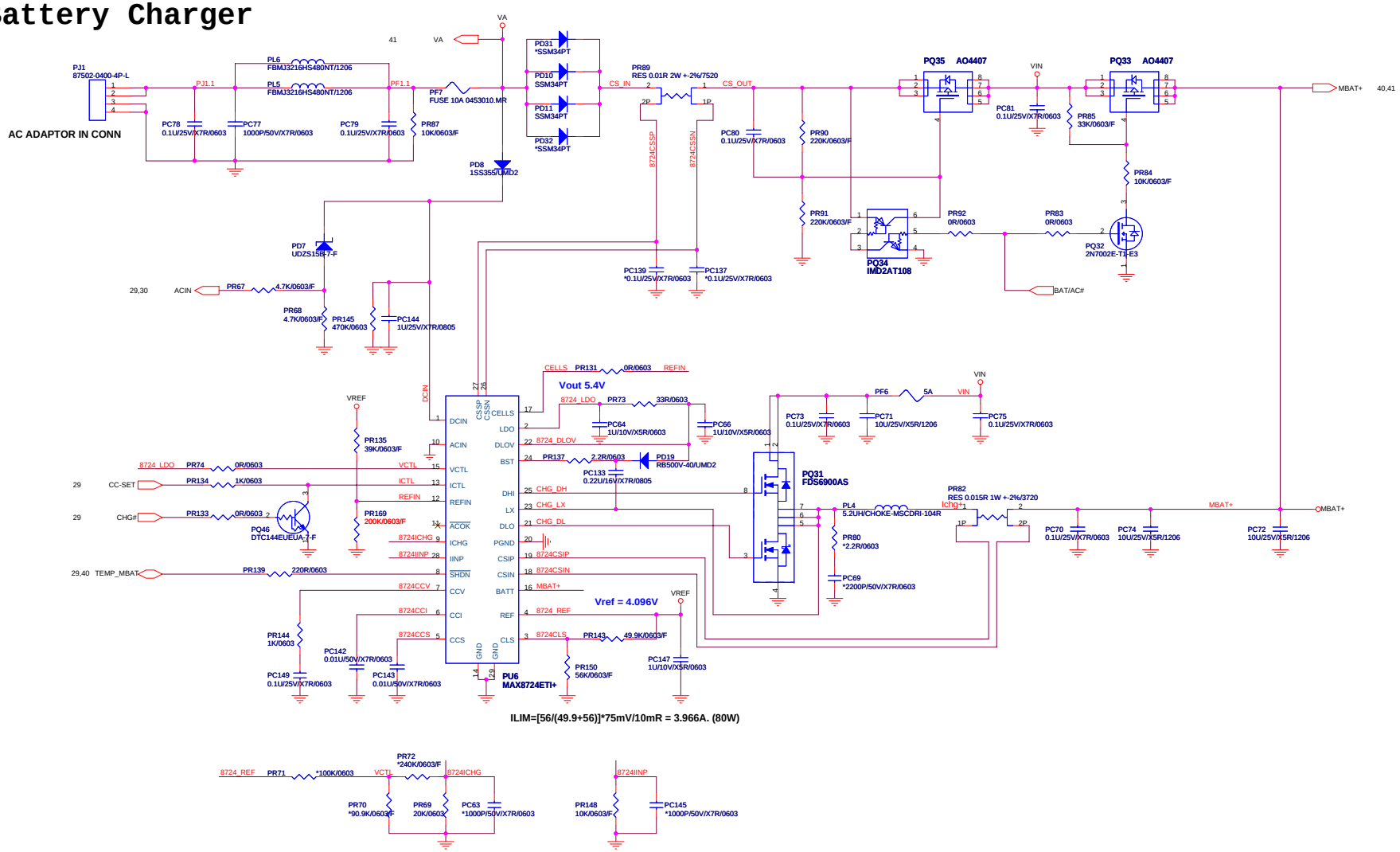
3VPCU & 5VPCU & Discharge



QUANTA COMPUTER

Title	3VPCU & 5VPCU	
Size: Custom	Document Number: WR1D Main Board	Rev: 3A
Date: Friday, August 25, 2006	Sheet 38 of 43	

Battery Charger



QUANTA COMPUTER

Title: BATTERY CHARGER

Size: Custom | Document Number: WR1D Main Board | Rev: 3A

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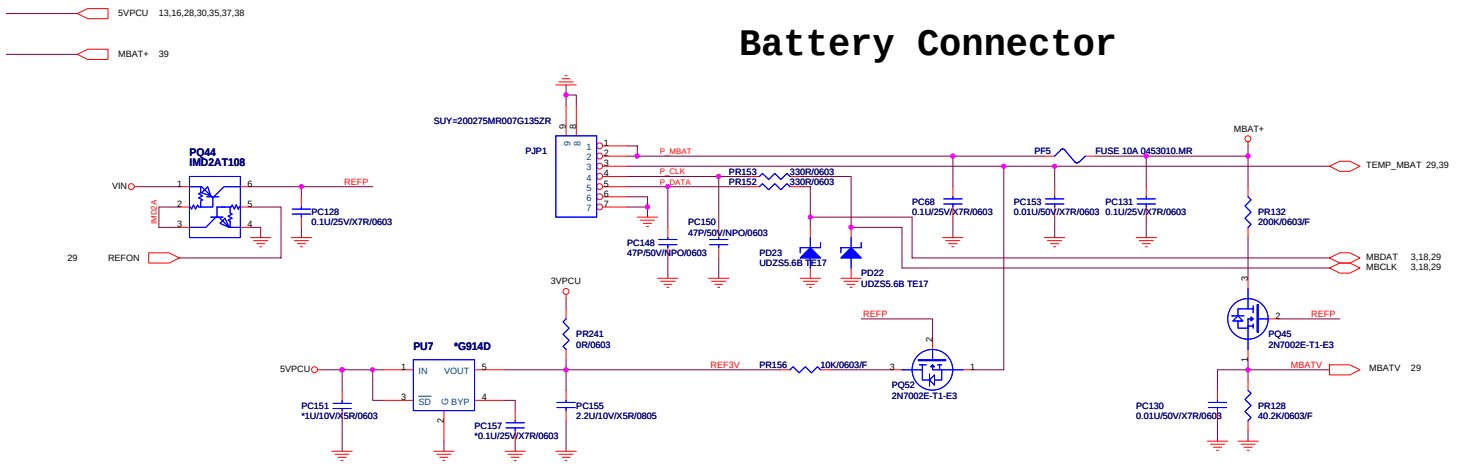
Battery Connector



TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :	
Li-ion 4S*P	16.8V*40.2/(200+40.2)= 2.812V 12.0V*40.2/(200+40.2)= 2.008V
Ni-MH 8S1P	8.0V*40.2/(200+40.2)= 1.34V

QUANTA COMPUTER

Title	BATTERY CONNECTOR	
Size: Custom	Document Number: WR1D Main Board	Rev: 3A
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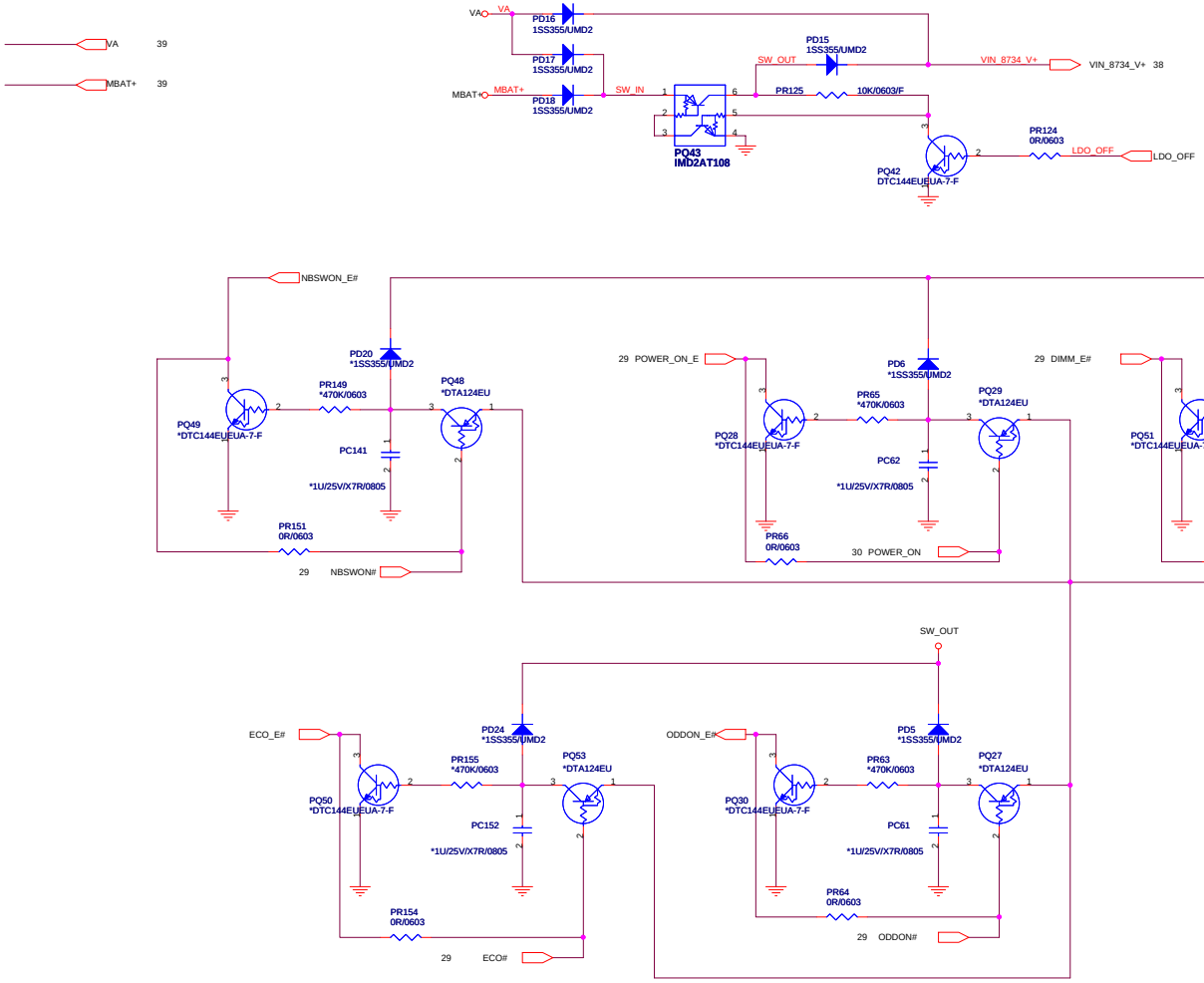
No Power On S5



QUANTA COMPUTER

Title	No Power On S5	
Size: Custom	Document Number: WR1D Main Board	Rev: 3A
Date: Friday, August 25, 2006	Sheet 41 of 43	

ES1 TO ES2 CHANGE LIST

EC0 PAGE ALL--ALL POSITION RENAME AFTER ES1 for less position code.
EC1 PAGE 27--Add C786,C787 for debug.
EC2 PAGE 30--Change CIR power circuit for reduce leakage issue.
EC3 PAGE 16--Add U56,C789,R660 for correct timing.
EC4 PAGE32---Cahnge C271 , C272 connect from GND to LAN_GND for Broadcom request.
EC5 PAGE31---Add L83,L84,C784,C785 on TPDATA ,TPCLK for EMI request.
EC6 PAGE7,12--Reserve R649~R656 and RP49,RP50 for GMCH GM Version.
EC7 PAGE7---ADD PCIEX16 AC Coupling CAP for can't boot issue.C783~C844 0.1uf.
EC8 PAGE8,9---Modify schematic C273,C277,C338,C403,C848 for Intel platform request.
EC9 PAGE9---Reserve L77~L81 and R143,R258,R657 for GM Version debug.
EC10 PAGE11---SWAP M_CLK_DDR2 and M_CLK_DDR3 AND set SA0_B to low SA1_B to Hi to improve second DIMM can't boot issue.
EC11 PAGE13---Change Y3 pin define from #1,#2 to #1,#4 for correct layout.
EC12 PAGE18---SWAP DDC1BD and PNL_CLK for correct layout.
EC13 PAGE25---Add EAPD function for pop noise.
EC14 PAGE26---Change Q44 to MosFET for HP sense function.
EC15 PAGE27---Reserve R632~R636 for customer request.
EC16 PAGE29---Add ECOLED1# and BATLED1 for customer spec.
EC17 PAGE29---Add ext port for net error to improve net link issue.
EC18 PAGE29---D10 Reverse and mount R585 FOR CORRECT circuit.
EC19 PAGE29---Pull-up E-MAIL# and INTERNET# signal for Auto power on issue.
EC20 PAGE30---Change CIR CONN CON24 from 10pin to 12pin for add BATTERY LED1.
EC21 PAGE32---SWAP LAN Signal P0~3 and M0~3 for correct layout.
EC22 PAGE32---SWAP SATA Signal TXP and TXN for correct layout.
EC23 PAGE33---SWAP TMDS0~2+ and TMDS0~2- for correct layout.
EC24 PAGE33---Change U2,U3 pin define pin3 to GND AND pin5 to VCC for correct layout.
EC25 PAGE33---ADD LP12~LP15 for EMI issue.
EC26 PAGE33---Change net CON7#15 to DDCCLK CON7#16 to DDCDATA for 5V level I2C.
EC27 PAGE27---Change SW2 pin 3 to GND for coreect layout.
EC28 PAGE15---Change The GPIO PIN to GPI pin.
EC29 PAGE28--- U29#2,#3 Change from VCC5 to 5VPCU for USB port Charge function when S3,S4 AC mode.
EC30 PAGE29---Add EC0_LED1# and BAT_LED1 CONTROL PIN.
EC31 PAGE31--Change R267 from 4.7K to 1K for customer request.
EC32 PAGE31---DEL R276 because double pull-high resistor.
EC33 PAGE33---SWAP U4#1,U4#44 for correct layout.
EC34 PAGE34---Change from one phase solution to 2 phase solution for Merom supporting.
EC35 PAGE36; PAGE38---For optimize ATI M56 performance and mechanical required high limit changed.
EC36 PAGE38---Change 9VPCU solution to 15VPCU solution for power saving during S4 & S5.
EC37 PAGE39;40---For power saving suring S4 & S5.
EC38 PAGE29,30---Change CIR circuit for customer request.
EC39 PAGE31---Reserve R661 PAD for debug broadcom request.

ES2 TO PP CHANGE LIST

EC40 PAGE36---Due to ES2 wrong schematic, add PR242 for low side Rdson sense.
EC41 PAGE30---Change RF-LED green Color to match spec.
EC42 PAGE36---Delete PL17, and change PL3 to single large inductor, due to mechanical lift maximum 3mm hight!!
EC43 PAGE30---Delete Q29 DIMM signal for DRD spec.
EC44 PAGE14,27---Change Mini_PCIE circuit to other PCIE bus from SB to avoid same with new card PCIE bus for correct design.
EC45 PAGE13---Add CON28 for CMOS BATTERY leakage and deformed issue ,beacause thermal issue.
EC46 PAGE27,30---Add U57 R664,R665 for LED off ,when wireless lan doesn't install , The LED can't be controlled by EC It is always off.
EC47 PAGE13---Delete the internal link for CMOS BATTERY deform issue.

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PP TO IRT CHANGE LIST

EC48 PAGE13---Delete G1 short PAD Because non-using.Change RTCRST# net for SW can't clear CMOS issue.
EC49 PAGE29---Delete FW PROGRAM SW SET.Original for debug using.
EC50 PAGE27---ADD R664,R665 for when the mini pcie haven't device install on it the led will be disable.
EC51 PAGE26---Change BUZZER power to S0 power to improve leakage issue.
EC52 PAGE29---ADD CIR_SET NET TO EC FOR SOFTWARE DETECT DIP SW ON OR OFF.
EC53 PAGE14---Swap MINI CARD PCI-E and EXPRESS CARD (NEW CARD) signal junction to ICH7 for Software request.
EC54 PAGE15---Change SWI# and MXM_THERM# Power rail to RVCC3 for improve leakage when S5.
EC55 PAGE30---Add Q12,Q46 for E-Mail and Internet EC detect signal ,when S4,S5 can power on.
EC56 PAGE30---modify CIR power circuit support battery mode power on.
EC57 PAGE36---reserve PR174 and PQ68 pad for powerplay control.
EC58 PAGE13---Change RTCRST# net to VCCRTC for CMOS clear function "date and time".
EC59 PAGE3---Change THRMTRIP# net for low temperature can't boot issue.
EC60 PAGE31---Add C790,C791 for 3V singnal drop issue when initial boot.
EC61 PAGE37---Reserve PC136,PC177,PC178,PC181 and C796 for keep VCC 1.8 at right level when run 3D mark.

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