FEATURES

- Single 5V to 21V application
- Wide Input Voltage Range from 1.5V to 21V with external Vcc
- Output Voltage Range: 0.6V to 0.86*PVin
- 0.5% accurate Reference Voltage
- Enhanced line/load regulation with Feed-Forward
- Programmable Switching Frequency up to 1.5MHz
- Internal Digital Soft-Start
- Enable input with Voltage Monitoring Capability
- Remote Sense Amplifier with True Differential Voltage Sensing
- Thermally compensated current limit and Hiccup Mode Over Current Protection
- Smart LDO to enhance efficiency
- Vp for tracking applications and sequencing
- Vref is available externally to enable margining
- External synchronization with Smooth Clocking
- Dedicated output voltage sensing for power good indication and overvoltage protection which remains active even when Enable is low.
- Enhanced Pre-Bias Start up
- Body Braking to improve transient
- Integrated MOSFET drivers and Bootstrap diode
- Thermal Shut Down
- Post Package trimmed rising edge dead-time
- Programmable Power Good Output with tracking
- Small Size 5mm x 7mm PQFN
- Operating Junction Temp: -40°C<Tj<125°C
- Lead-free, Halogen-free and RoHS Compliant

DESCRIPTION

The IR3846 SupIRBuck® is an easy-to-use, fully integrated and highly efficient DC/DC regulator. The onboard PWM controller and MOSFETs make IR3846 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications.

IR3846 is a versatile regulator which offers programmability of switching frequency and current limit while operating in wide input and output voltage range.

The switching frequency is programmable from 300 kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Over Voltage Protection (OVP), Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

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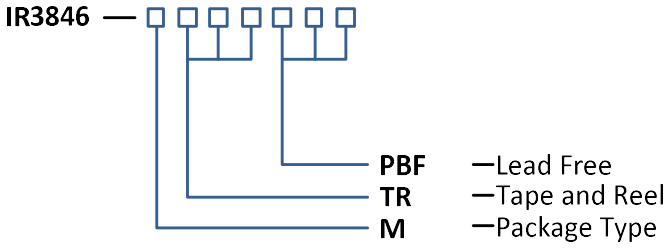
APPLICATIONS

- Netcom Applications
- Embedded Telecom Systems
- Server Application
- Distributed Point of Load Power Architectures
- Storage Applications

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR3846	PQFN 5mm x 7mm	Tape and Reel	4000	IR3846MTRPBF



BASIC APPLICATION

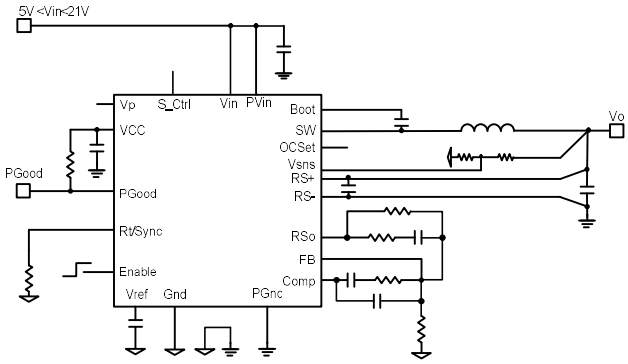


Figure 1: IR3846 Basic Application Circuit

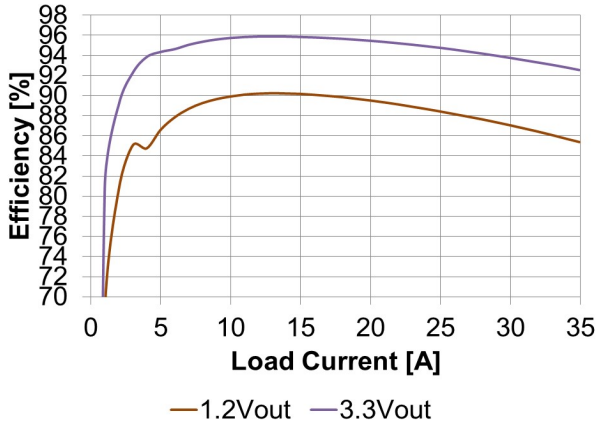
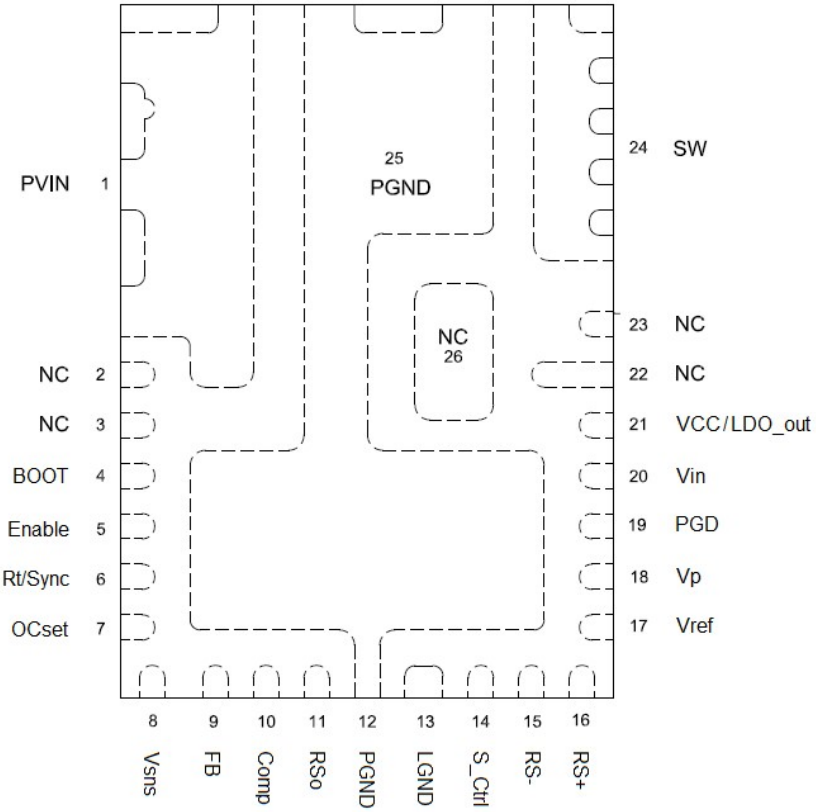


Figure 2: Efficiency [Vin=12V, Fsw=600kHz]

PIN DIAGRAM

5mm X 7mm POWER QFN
Top View



FUNCTIONAL BLOCK DIAGRAM

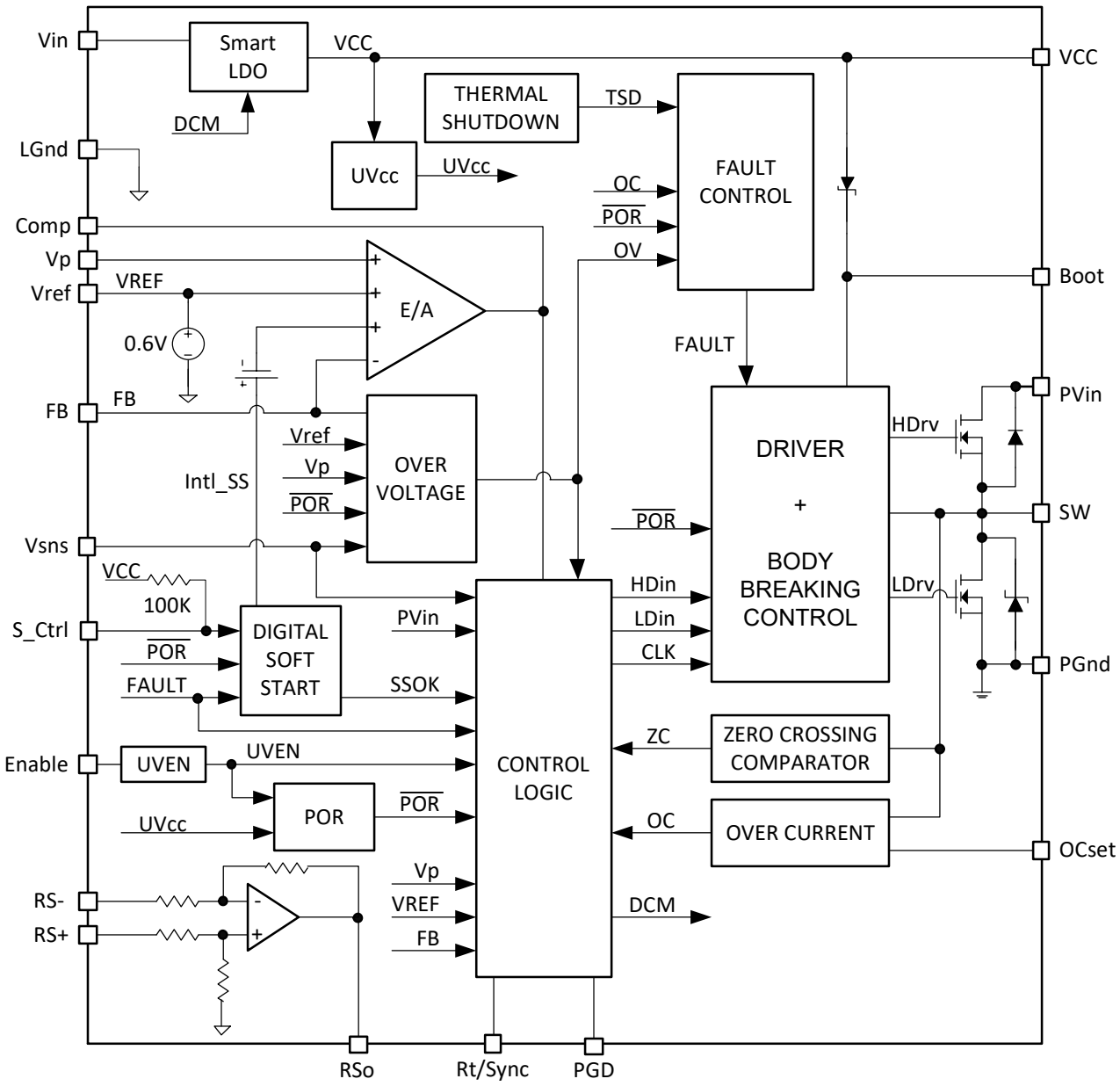


Figure 3: IR3846 Simplified Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	PVin	Input voltage for power stage. Bypass capacitors between PVin and PGND should be connected very close to this pin and PGND; also forms input to feedforward block
2, 3, 22, 23, 26	NC	No Connect
4	Boot	Supply voltage for high side driver
5	Enable	Enable pin to turning on and off the IC.
6	Rt/Sync	Use an external resistor from this pin to LGND to set the switching frequency, very close to the pin. This pin can also be used for external synchronization.
7	OCset	Current limit setpoint. This pin allows the trip point to be set to one of three possible settings by either floating, tying to VCC or tying to PGnd.
8	Vsns	Sense pin for OVP and PGood
9	FB	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator or to the output of the remote sense amplifier, via resistor divider to set the output voltage and provide feedback to the error amplifier.
10	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to FB to provide loop compensation.
11	RSo	Remote Sense Amplifier Output
12, 25	PGND	Power ground. This pin should be connected to the system's power ground plane. Bypass capacitors between PVin and PGND should be connected very close to PVIN pin (pin 1) and this pin.
13	LGND	Signal ground for internal reference and control circuitry.
14	S_Ctrl	Soft start/stop control. A high logic input enables the device to go into the internal soft start; a low logic input enables the output soft discharged. Pin is internally pulled high when this function is not used.
15	RS-	Remote Sense Amplifier input. Connect to ground at the load.
16	RS+	Remote Sense Amplifier input. Connect to output at the load.
17	Vref	External reference voltage can be used for margining operation. A capacitor between 100pF and 180pF should be connected between this pin and LGnd. Tie to LGnd for tracking function.
18	Vp	Used for voltage sequencing and tracking. Leave open if sequencing or tracking is not needed, ensuring that there is no capacitor on the pin.
19	PGD	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to VCC.
20	Vin	Input Voltage for LDO.
21	VCC/LDO_out	Bias Voltage for IC and driver section, output of LDO. Add a minimum of 4.7uF bypass cap from this pin to PGnd.
24	SW	Switch node. This pin is connected to the output inductor.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PVin		-0.3V to 25V
Vin		-0.3V to 25V
VCC, Enable		-0.3V to 8V (Note 1)
SW		-0.3V to 25V (DC), -4V to 25V (AC, 100ns)
BOOT		-0.3V to 33V
BOOT to SW		-0.3V to VCC + 0.3V (Note 2)
Other Input/Output pins		-0.3V to 3.9V
RS+, RS-, RSo, PGD, OCset, S_Ctrl		-0.3V to VCC + 0.3V (Note 2)
PGND to LGND, RS- to LGND		-0.3V to +0.3V
Junction Temperature Range		-40°C to 150°C (Note1)
Storage Temperature Range		-55°C to 150°C
ESD	Machine Model	Class A
	Human Body Model	Class 1C
	Charged Device Model	Class III
Moisture Sensitivity level		JEDEC Level 3 @ 260°C
RoHS Compliant		Yes

Note:

1. VCC must not exceed 7.5V for Junction Temperature between -10°C and -40°C.
2. Must not exceed 8V.

THERMAL INFORMATION	
Thermal Resistance, Junction to Case (θ_{JC_TOP})	30 °C/W
Thermal Resistance, Junction to PCB (θ_{JB})	2.71 °C/W
Thermal Resistance, Junction to Ambient (θ_{JA}) (Note 3)	14.3 °C/W

Note:

3. Thermal resistance (θ_{JA}) is measured with components mounted on a high effective thermal conductivity test board in free air.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

SYMBOL	DEFINITION	MIN	MAX	UNIT
PVin	Input Bus Voltage *	1.5	21	V
Vin	Supply Voltage	5.0	21	
VCC	Supply Voltage **	4.5	7.5	
Boot to SW	Supply Voltage	4.5	7.5	
V_O	Output Voltage	0.6	0.86 PVin	
I_O	Output Current	0	±35	A
Fs	Switching Frequency	300	1500	kHz
T_J	Junction Temperature	-40	125	°C

* SW node must not exceed 25V

** When VCC is connected to an externally regulated supply, also connect Vin.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specification apply over, 1.5V < PVin < 21V, 4.5V< VCC < 7.5V, 0°C < T_J < 125°C.
Typical values are specified at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Loss						
Power Loss	P_{LOSS}	V_{in} = PV_{in} = 12V, V_O = 1.2V, I_O = 35A, Fs = 600kHz, L=0.250uH, T_A = 25°C, Note 4		5.3		W
MOSFET $R_{ds(on)}$						
Top Switch	Rds(on)_Top	V_{Boot} – V_{SW} = 6.8V, I_D = 35A, Without Cu Clip, Tj = 25°C		3.1	4	mΩ
Bottom Switch	Rds(on)_Bot	VCC =6.8V, I_D = 35A, With Cu Clip, Tj = 25°C		1.27	1.64	
Reference Voltage						
Feedback Voltage	V_{FB}			0.6		V
Accuracy		Vref=0.6V, 0°C < Tj < 105°C	-0.5		+0.5	%
		Vref=0.6V, -40°C < Tj < 125°C	-1.0		+1.0	
Sink Current	Isink_Vref	Vref=0.7V	12.7	16.0	19.3	µA
Source Current	Isrc_Vref	Vref=0.5V	12.7	16.0	19.3	
Vref Comparator Threshold	Vref_disable	Vref Pin connected externally			0.15	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
	Vref_enable		0.4			V
Supply Current						
V_{in} Supply Current (Standby)	$I_{in(Standby)}$	Vin=21V, Enable low, No Switching		300	425	µA
V_{in} Supply Current (Dyn)	$I_{in(Dyn)}$	Vin=21V, Enable high, Fs = 600kHz			40	mA
VCC Supply Current (Standby)	$I_{cc(Standby)}$	Enable low, VCC=7V, No Switching		300	425	µA
VCC Supply Current (Dyn)	$I_{cc(Dyn)}$	Enable high, VCC=7V, Fs = 600kHz			40	mA
Under Voltage Lockout						
VCC–Start–Threshold	VCC_UVLO_Start	VCC Rising Trip Level	4.0	4.2	4.4	V
VCC–Stop–Threshold	VCC_UVLO_Stop	VCC Falling Trip Level	3.7	3.9	4.2	
Enable–Start–Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	V
Enable–Stop–Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Enable leakage current	Ien	Enable=3.3V			1	µA
Oscillator						
Rt Voltage				1		V
Frequency Range	F_S	Rt=80.6k	270	300	330	kHz
		Rt=39.2k	540	600	660	
		Rt=15k	1350	1500	1650	
Ramp Amplitude	Vramp	PVin=6.8V, PVin(max) slew rate=1V/us, Note 4		1.02		Vp-p
		PVin=12V, PVin(max) slew rate=1V/us, Note 4		1.8		
		PVin=16V, PVin(max) slew rate=1V/us, Note 4		2.4		
Ramp Offset	Ramp (os)	Note 4		0.16		V
Min Pulse Width	Tmin (ctrl)	Note 4			50	ns
Fixed Off Time		Note 4		200	230	ns
Max Duty Cycle	Dmax	Fs=300kHz, PVin=Vin=12V	86			%
Sync Frequency Range		Note 4	270		1650	kHz
Sync Pulse Duration			100	200		ns
Sync Level Threshold	High		3			V
	Low				0.6	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Error Amplifier						
Input Offset Voltage	Vos_Vref	VFb – Vref, Vref = 0.6V	-1.5		+1.5	% Vref
	Vos_Vp	VFb – Vp, Vp = 0.6V	-1.5		+1.5	%Vp
Input Bias Current	IFb(E/A)		-0.5		+0.5	µA
Input Bias Current	IVp(E/A)		0		4	µA
Sink Current	Isink(E/A)		0.4	0.85	1.2	mA
Source Current	Isource(E/A)		4	7.5	11	mA
Slew Rate	SR	Note 4	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	Note 4	20	30	40	MHz
DC Gain	Gain	Note 4	100	110	120	dB
Maximum Output Voltage	Vmax(E/A)		1.7	2	2.3	V
Minimum Output Voltage	Vmin(E/A)				100	mV
Common Mode Voltage	Vcm_Vp	Note 4	0		1.2	V
Margining Range	Vmarg_Vref	Note 4	0.4		1.2	V
Remote Sense Differential Amplifier						
Unity Gain Bandwidth	BW_RS	Note 4	3	6.4	9	MHz
DC Gain	Gain_RS	Note 4		110		dB
Offset Voltage	Offset_RS	Vref=0.6V, 0°C < Tj < 85°C	-1.5	0	1.5	mV
		Vref=0.6V, -40°C < Tj < 125°C	-2		2	mV
Source Current	Isource_RS		3	13	20	mA
Sink Current	Isink_RS		0.4	1	2	mA
Slew Rate	Slew_RS	Note 4, Cload = 100pF	2	4	8	V/µs
RS+ input impedance	Rin_RS+		45	63	85	kohm
RS- input impedance	Rin_RS-	Note 4		63		kohm
Maximum Voltage	Vmax_RS	V(VCC) – V(RSo)	0.5	1	1.5	V
Minimum Voltage	Min_RS			50		mV
Internal Digital Soft Start						
Soft Start Clock	Clk_SS	Note 4	180	200	220	kHz
Soft Start Ramp Rate	Ramp(SS_Start)	Note 4	0.3	0.4	0.5	mV / µs
S_CTRL Threshold	High		2.4			V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
	Low				0.6	V
Bootstrap Diode						
Forward Voltage		I(Boot) = 30mA	360	520	960	mV
Switch Node						
SW Leakage Current	Isw	SW = 0V, Enable = 0V			1	µA
		SW = 0V, Enable = HIGH, Vp=0 V				
Internal Regulator (VCC/LDO)						
Output Voltage	VCC	Vin(min) = 7.2V, Io=0-30mA, Cload = 2.2uF, DCM=0	6.3	6.8	7.1	V
		Vin(min) = 7.2V, Io=0-30mA, Cload = 2.2uF, DCM=1	4	4.4	4.8	
VCC dropout	VCC_drop	Vin = 7V, Io=70 mA, Cload = 2.2uF			0.7	V
Short Circuit Current	Ishort	Note 4		70		mA
Zero-crossing Comparator Delay	Tdly_zc			256 / Fs		s
Zero-crossing Comparator Offset	Vos_zc	Note 4		0		mV
Body Braking						
BB Threshold	BB_threshold	Fb > Vref, Sw duty cycle, Note 3		0		%
FAULTS						
Power Good						
Power Good Low Upper Threshold	VPG_low(upper)	Vsns Rising, 0.4V < Vref < 1.2V	115	120	125	% Vref
		Vsns Rising, Vref < 0.1V	115	120	125	% Vp
Power Good Low Upper Threshold Falling delay	VPG_low(upper)_Dly	Vsns > VPG_low(upper)	1.5	2.5	3.5	µs
Power Good High Lower Threshold	VPG_high(lower)	Vsns Rising, 0.4V < Vref < 1.2V		95		% Vref
		Vsns Rising, Vref < 0.1V		95		% Vp
Power Good High Lower Threshold Rising Delay	VPG_high(lower)_Dly	Vsns rising		1.28		ms
Power Good Low Lower Threshold	VPG_low(lower)	Vsns falling, 0.4V < Vref < 1.2V		90		% Vref
		Vsns falling,		90		%Vp

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
		0.1V < Vref				
Power Good Low Lower Threshold Falling delay	VPG_low(lower)_Dly	Vsns < VPG_low(lower)	101	150	199	µs
PGood Voltage Low	PG (voltage)	I_{PGood} = -5mA			0.5	V
Tracker Comparator Upper Threshold	VPG(tracker_upper)	Vp Rising, Vref < 0.1V		0.4		V
Tracker Comparator Lower Threshold	VPG(tracker_lower)	Vp Falling, Vref < 0.1V		0.3		V
Tracker Comparator Delay	Tdelay(tracker)	Vp Rising, Vref < 0.1V		1.28		ms
Over Voltage Protection (OVP)						
OVP Trip Threshold	OVP (trip)	Vsns Rising, 0.45V < Vref < 1.2V	115	120	125	% Vref
		Vsns Rising, Vref < 0.1V	115	120	125	% Vp
OVP Fault Prop Delay	OVP (delay)	Vsns rising	1.5	2.5	3.5	µs
Over-Current Protection						
OC Trip Current	I_{TRIP}	OCSet=VCC, VCC = 6.8V, TJ = 25°C	41	44.4	48	A
		OCSet=floating, VCC = 6.8V, TJ = 25°C	32	35	38	A
		OCSet=PGnd, VCC =6.8V, TJ = 25°C	24	26.88	30	A
Hiccup blanking time	Tblk_Hiccup	Note 4		20.48		ms
Thermal Shutdown						
Thermal Shutdown		Note 4		145		°C
Hysteresis		Note 4		20		°C

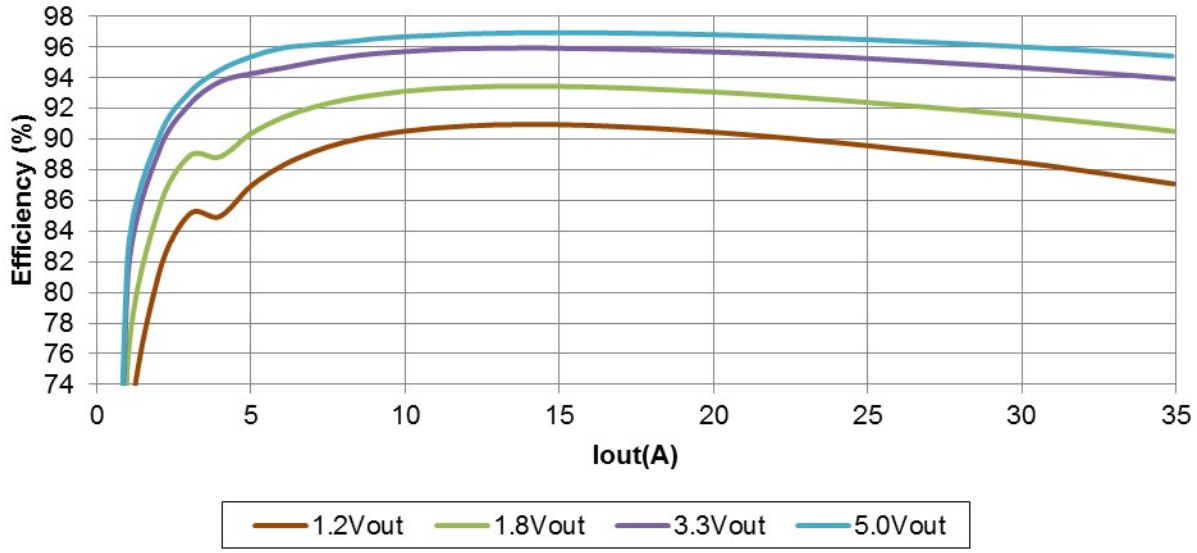
Notes:

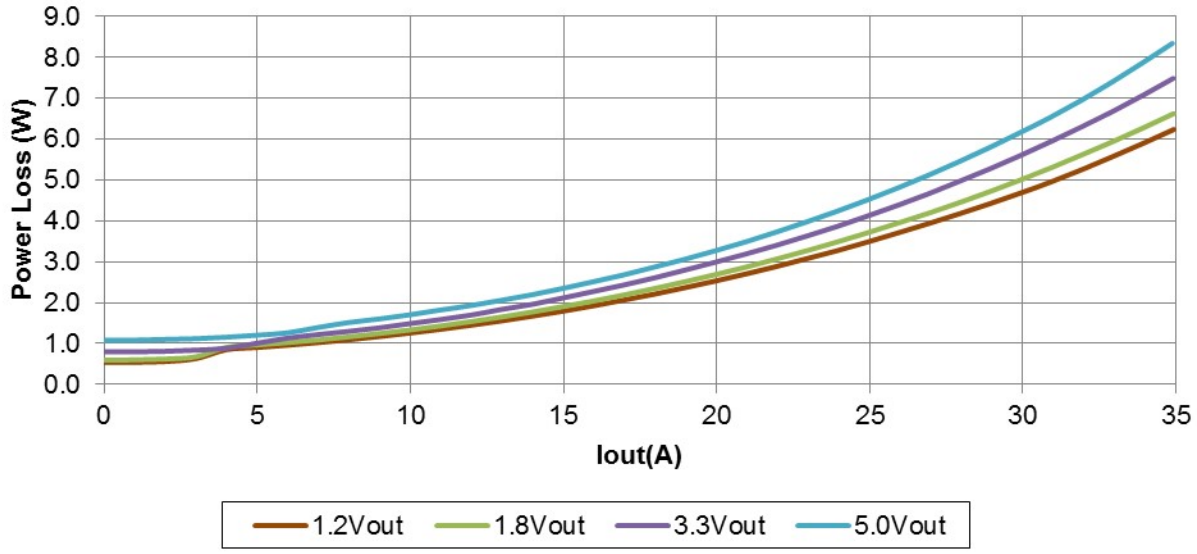
4. Guaranteed by design but not tested in production.

TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = 12V, VCC = Internal LDO, Io=0-35A, Fs= 600kHz, Room Temperature, LFM=200. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.2	0.25	744309025 (Wurth Electronik)	0.165
1.8	0.33	744309033 (Wurth Electronik)	0.165
3.3	0.33	744309033 (Wurth Electronik)	0.165
5.0	0.33	744309033 (Wurth Electronik)	0.165





TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = 12V, Vin = VCC = 5V, Io=0-35A, Fs= 600kHz, Room Temperature, LFM=200. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.2	0.25	744309025 (Wurth Electronik)	0.165
1.8	0.33	744309033 (Wurth Electronik)	0.165
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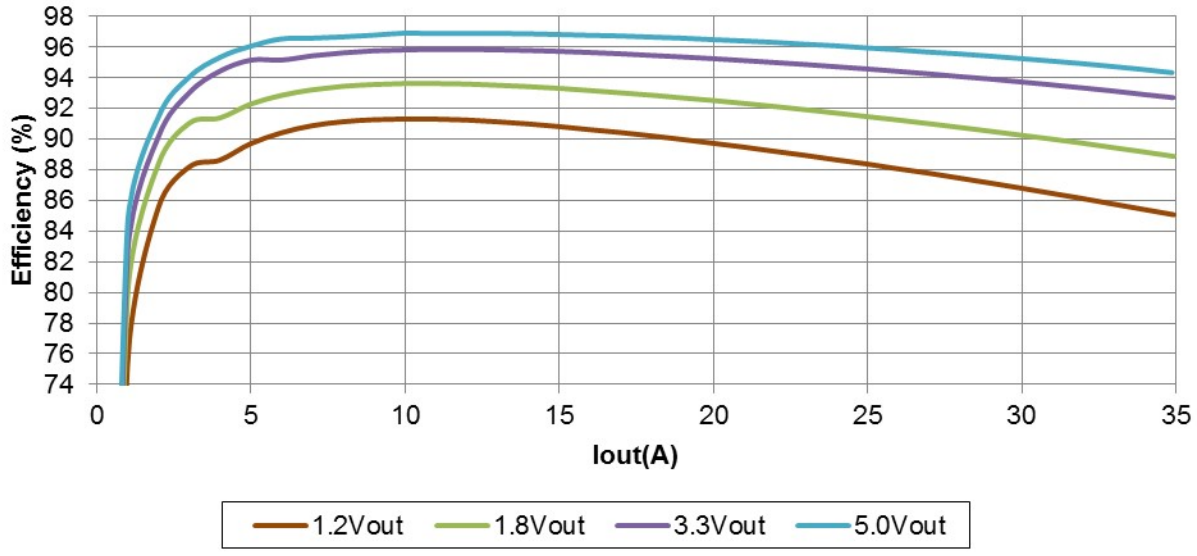
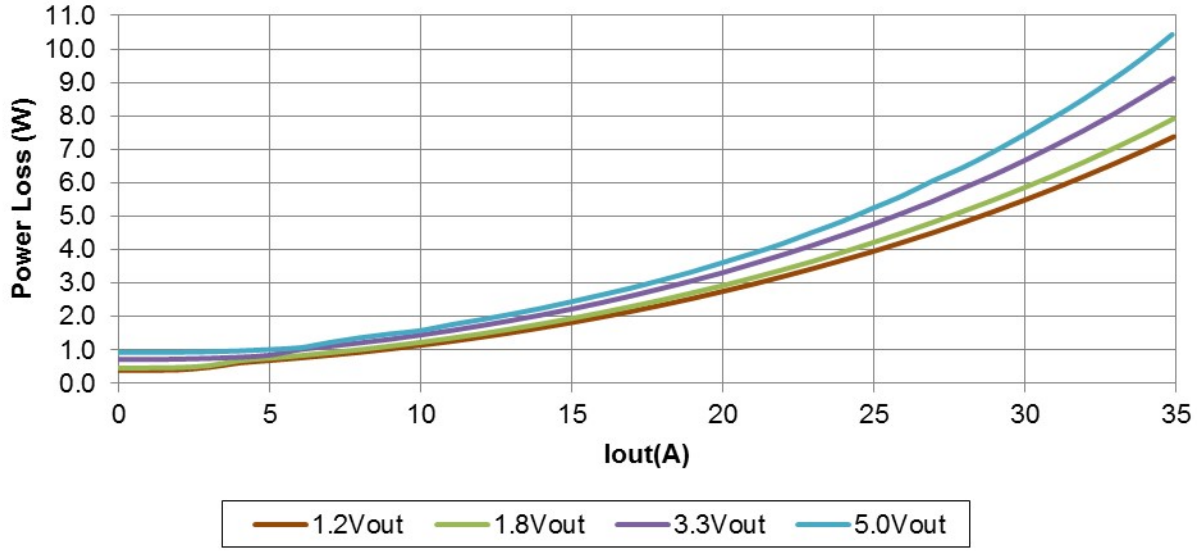
5.0	0.33	744309033 (Wurth Electronik)	0.165

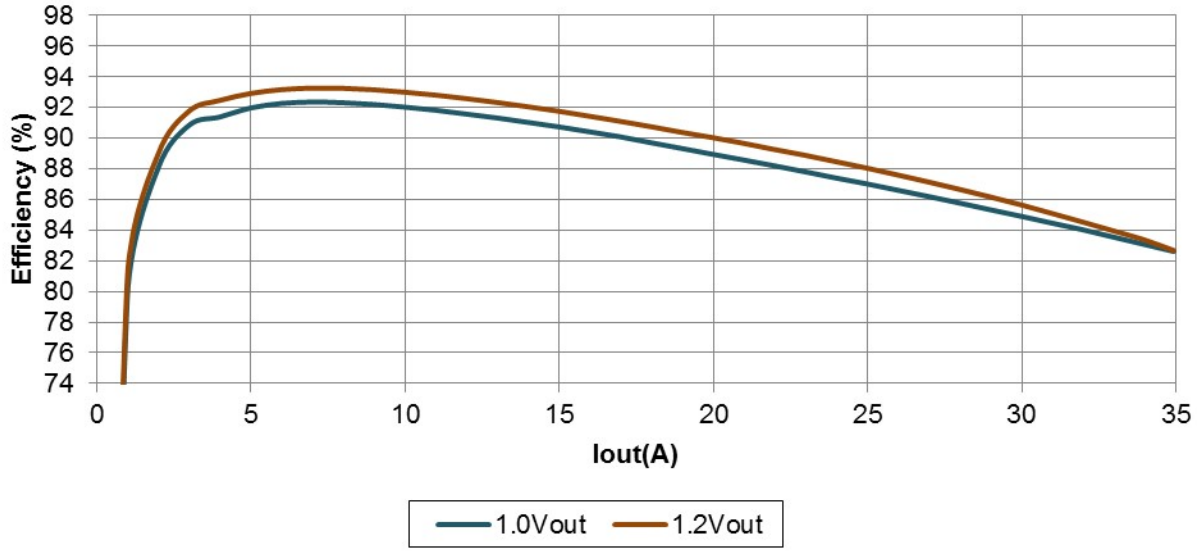


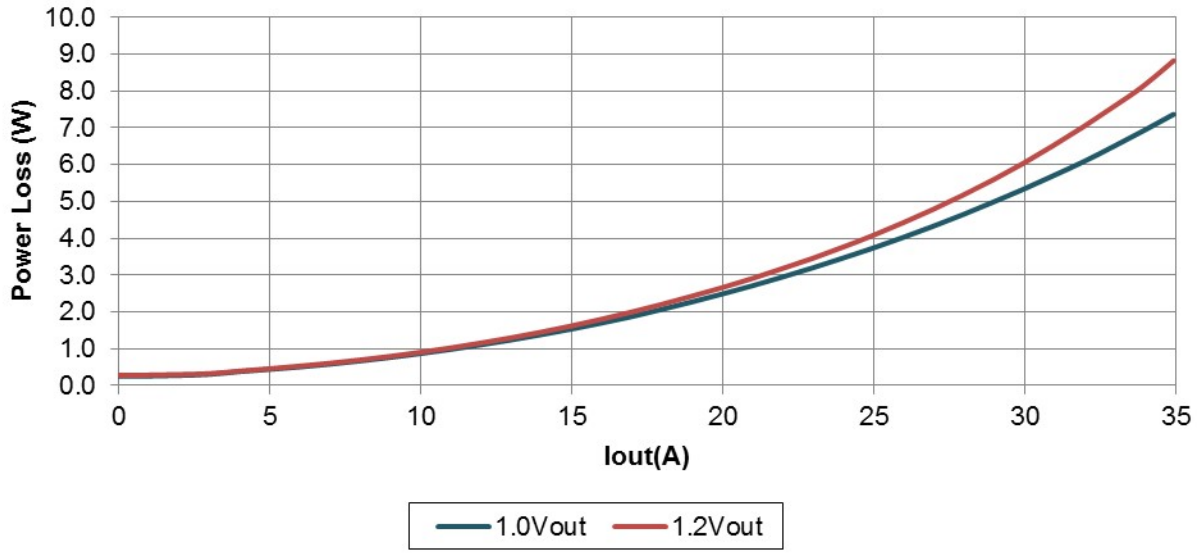


TYPICAL EFFICIENCY AND POWER LOSS CURVES

PVin = Vin = VCC = 5V, Io=0-35A, Fs= 600kHz, Room Temperature, LFM=200. Note that the losses of the inductor, input and output capacitors are also considered in the efficiency and power loss curves. The table below shows the indicator used for each of the output voltages in the efficiency measurement.

VOUT (V)	LOUT (uH)	P/N	DCR (mΩ)
1.0	0.19	SL40307A-R19KHF (ITG)	0.200
1.2	0.19	SL40307A-R19KHF (ITG)	0.200

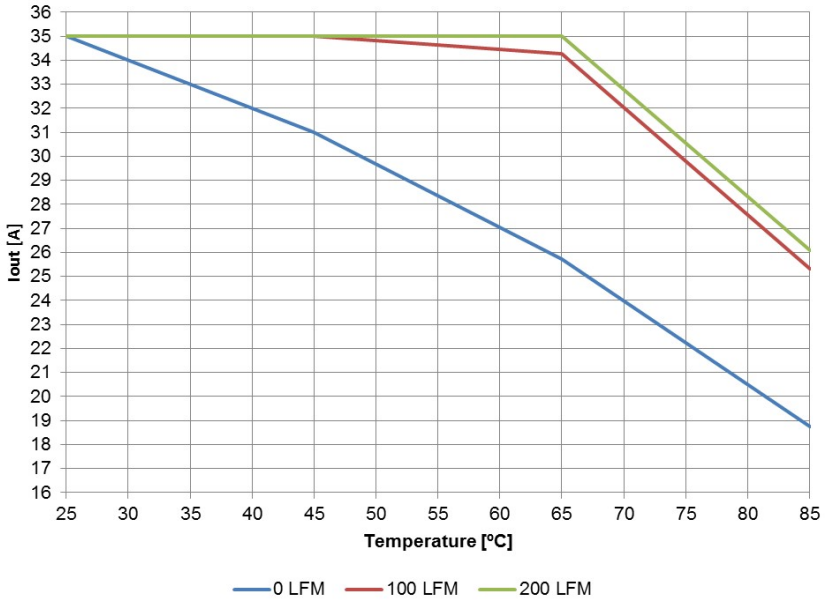




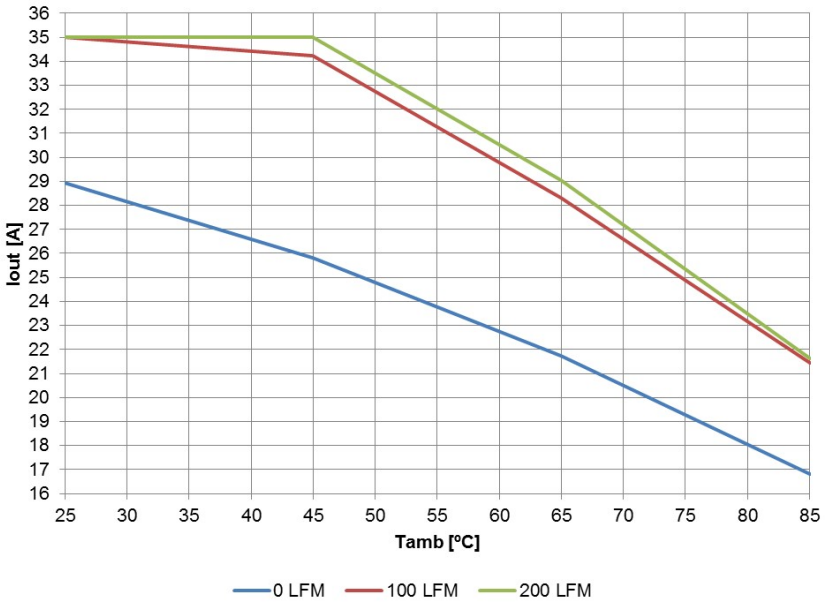
THERMAL DERATING CURVES

Measurements are done on IR3846 Evaluation board. PCB is a 6 layer board with 2 oz copper and FR4 material.

Vin=PVin=12V, Vout =1.2V, VCC=internal LDO (6.8V), Fs = 600kHz

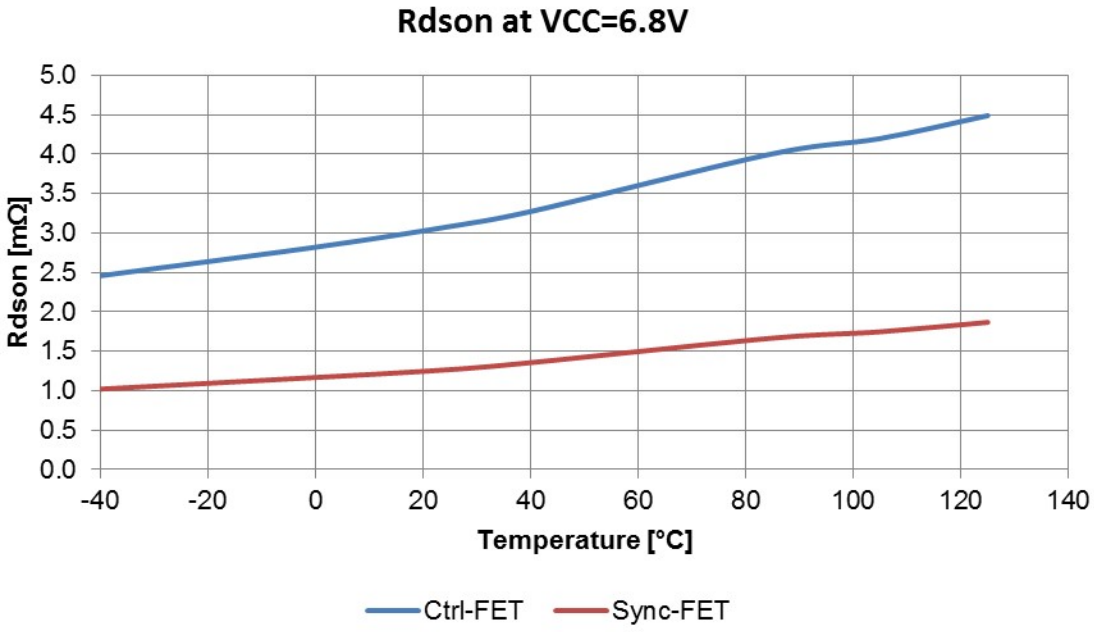


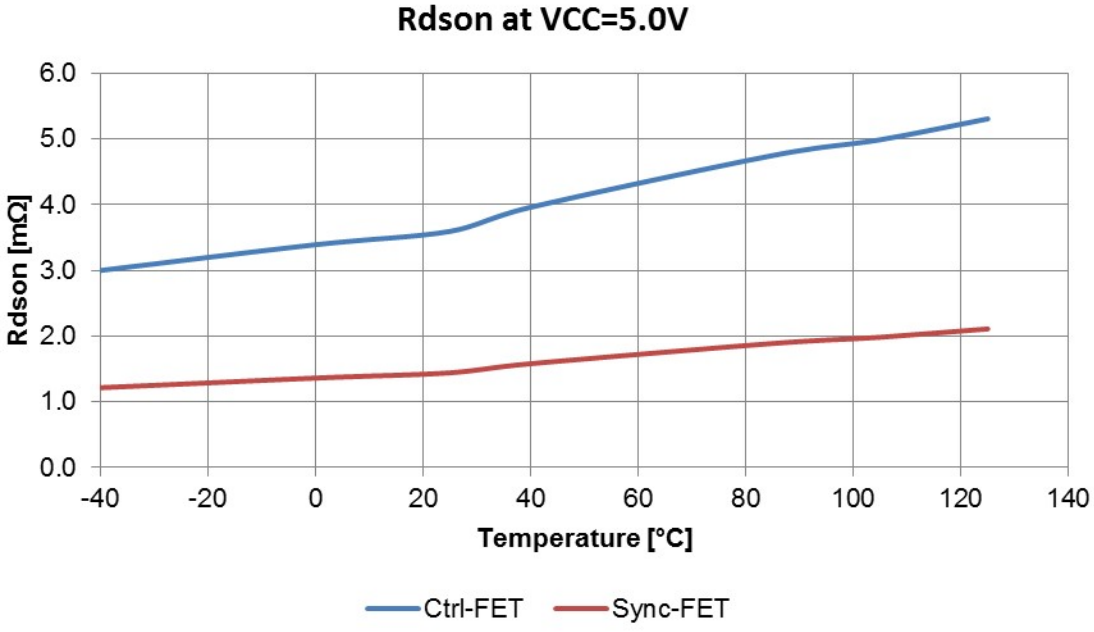
Vin=PVin=12V, Vout =3.3V, VCC=internal LDO (6.8V), Fs = 600kHz



Note: International Rectifier Corporation specifies current rating of SupIRBuck devices conservatively. The continuous current load capability might be higher than the rating of the device if input voltage is 12V typical and switching frequency is below 600kHz. However, the maximum current is limited by the internal current limit and designers need to consider enough guard bands between load current and minimum current limit to guarantee that the device does not trip at steady state condition.

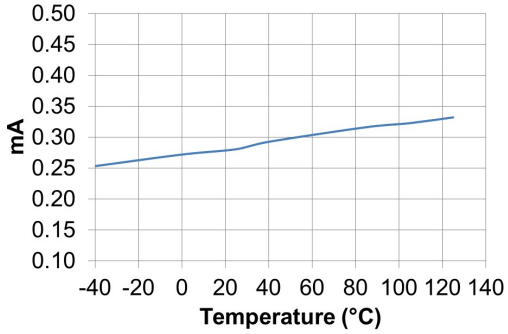
MOSFET RDSON VARIATION OVER TEMPERATURE



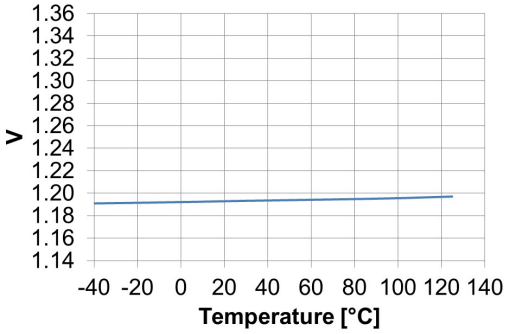


TYPICAL OPERATING CHARACTERISTICS (-40°C to +125°C)

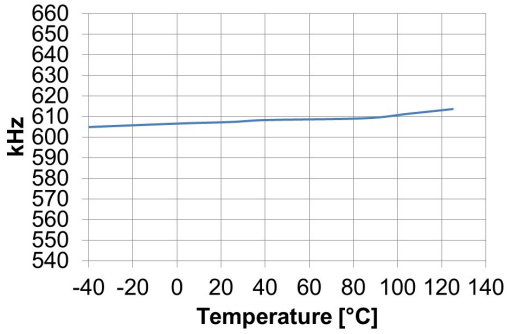
IIN (STANDBY)



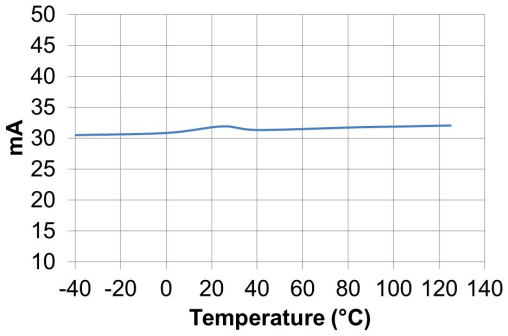
EN_UVLO_START



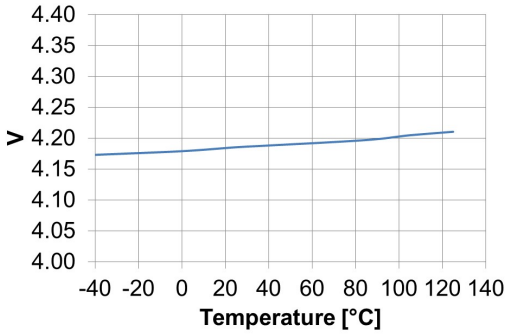
FREQUENCY [RT=39.2KΩ]



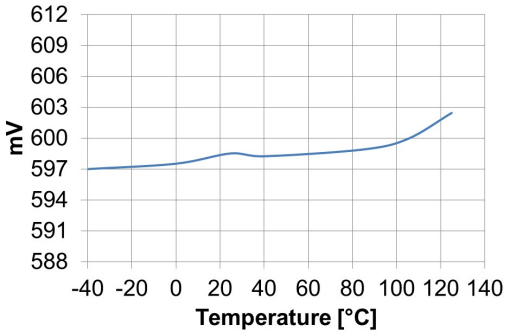
IIN (DYNAMIC) @ Fs=600kHz



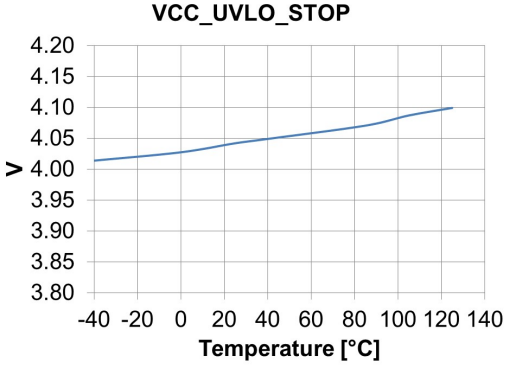
VCC_UVLO_START

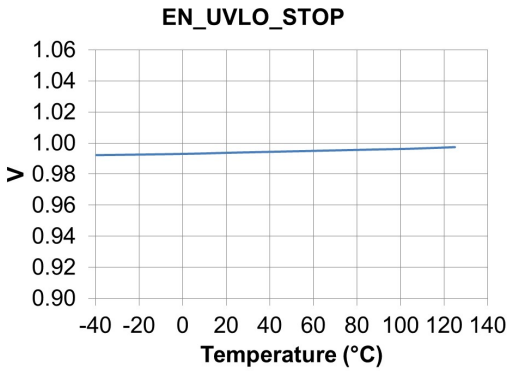


VFB

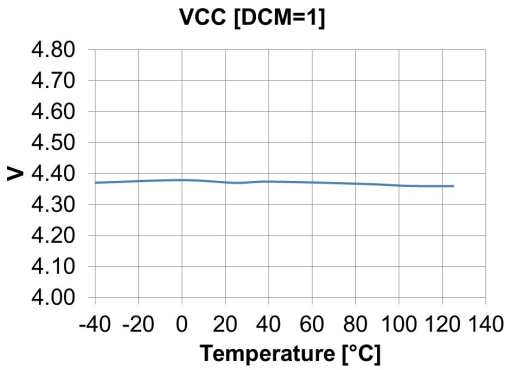


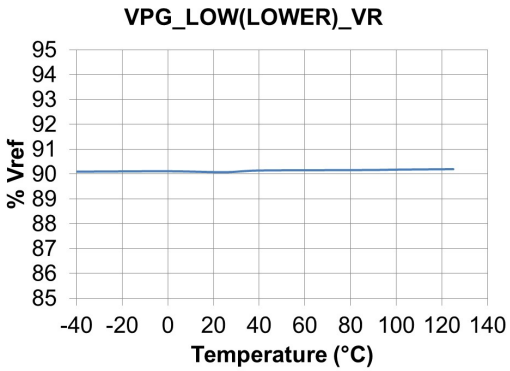
VCC_UVLO_STOP

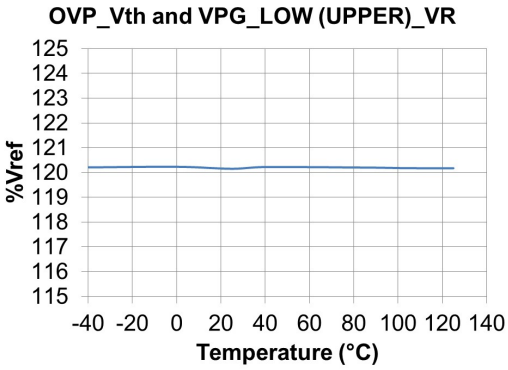


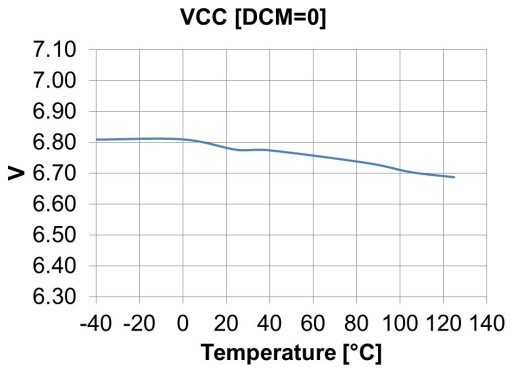


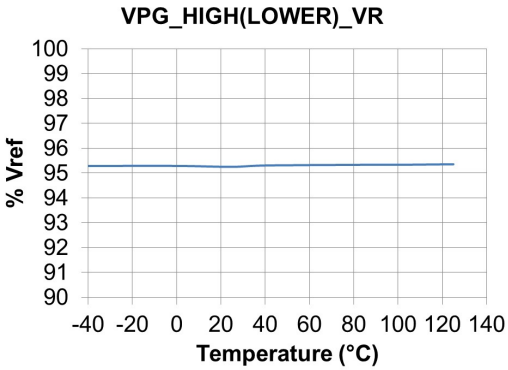
TYPICAL OPERATING CHARACTERISTICS (-40°C to +125°C)

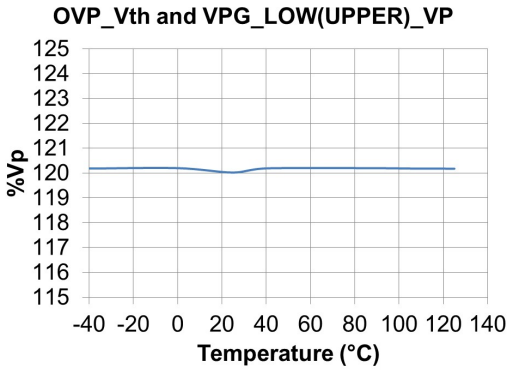


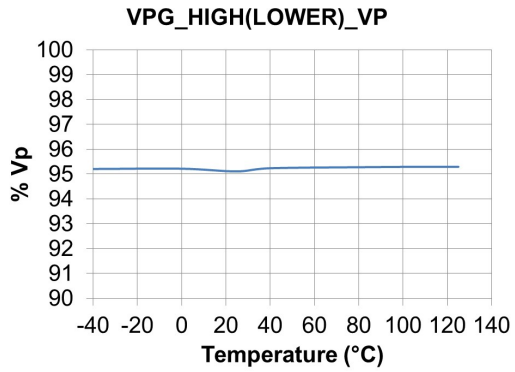


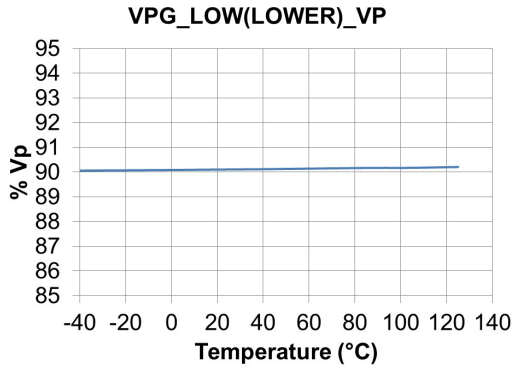




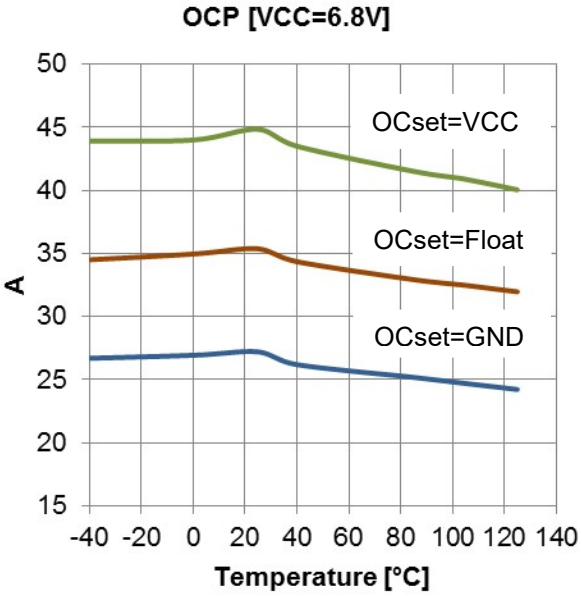


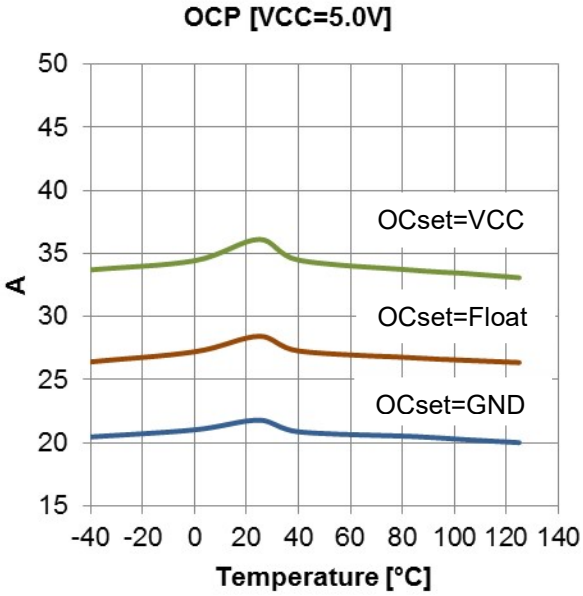


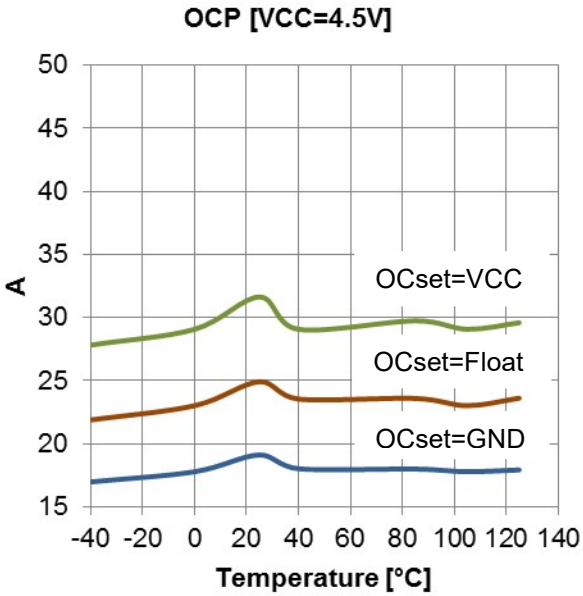

VPG_HIGH(LOWER)_VP
100
99
98
97
96
95
94
93
92
91
90
% Vp
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)


VPG_LOW(LOWER)_VP
95
94
93
92
91
90
89
88
87
86
85
% Vp
-40 -20 0 20 40 60 80 100 120 140
Temperature (°C)

TYPICAL OPERATING CHARACTERISTICS (-40°C to +125°C)







THEORY OF OPERATION

DESCRIPTION

The IR3846 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 300kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3846 provides precisely regulated output voltage programmed via two external resistors from 0.6V to 0.86*PVin.

The IR3846 operates with an internal bias supply (LDO) which is connected to the VCC pin. This allows operation with single supply. The bias voltage is variable according to load condition. If the output load current is less than half of the peak-to-peak inductor current, a lower bias voltage, 4.4V, is used as the internal gate drive voltage; otherwise, a higher voltage, 6.8V, is used.

This feature helps the converter to reduce power losses. The device can also be operated with an external bias from 4.5V to 7.5V, allowing an extended operating input voltage (PVin) range from 1.5V to 21V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external bias is used, it should be connected to VCC pin and the Vin pin should be shorted to VCC pin.

The device utilizes the on-resistance of the low side MOSFET (synchronous Mosfet) as current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3846 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

UNDER-VOLTAGE LOCKOUT AND POR

The under-voltage lockout circuit monitors the voltage of VCC pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drops below the set thresholds. Normal operation resumes once VCC and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

ENABLE

The Enable features another level of flexibility for startup. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3846 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3846 does not turn on until the bus voltage reaches the desired level as shown in Figure 4. Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3846 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3846, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). It can help prevent the IR3846 from regulating at low PVin voltages that can cause excessive input current.

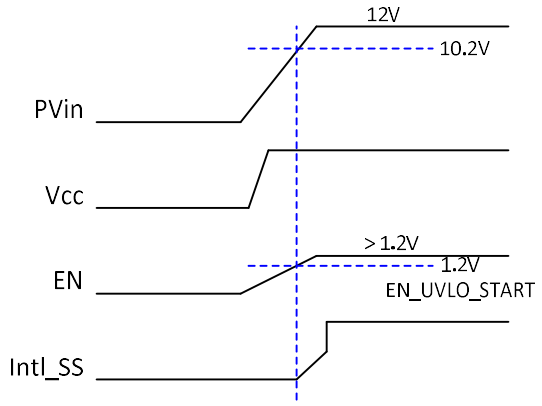


Figure 4: Normal Start up, device turns on when the bus voltage reaches 10.2V

A resistor divider is used at EN pin from PVin to turn on the device at 10.2V.

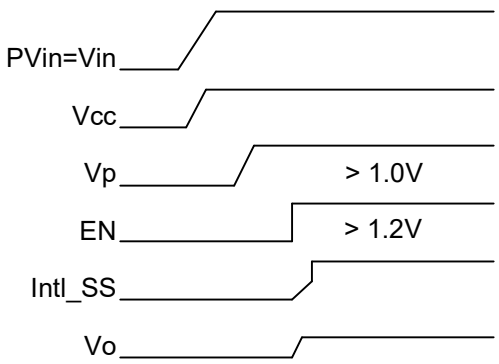


Figure 5: Recommended startup for Normal operation

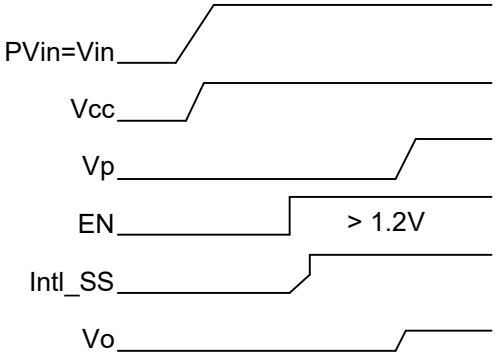


Figure 6: Recommended startup for sequencing operation (ratiometric or simultaneous)

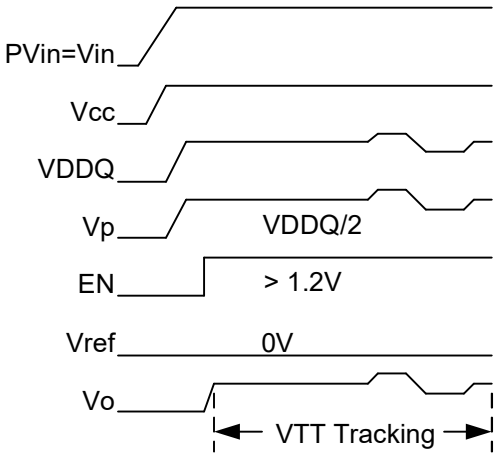


Figure 7: Recommended startup for memory tracking operation (Vtt-DDR)

Figure 5 shows the recommended startup sequence for the normal (non-tracking, non-sequencing) operation of IR3846, when Enable is used as a logic input. In this operating mode Vref is left floating. Figure 6 shows the recommended startup sequence for sequenced operation of IR3846 with Enable used as logic input. Figure 7 shows the recommended startup sequence for tracking operation of IR3846 with Enable used as logic input. For this mode of operation, Vref should be connected to LGND.

PRE-BIAS STARTUP

Pre-bias can restrict the V_boot voltage and prevent the IC from starting up properly. Knowing the Vboot requirement, Vcc voltage (Vcc) and forward diode (Vd) voltage the maximum pre-bias can be determined. The power stage driver requires a minimum of 3V Vboot during startup which translates to a maximum pre-bias voltage of (Vcc – Vd – Vboot)V.

Pre-Bias voltage Limit < Vcc – Vd – Vboot **(1)**

Vcc	Supply Rail (Internal LDO / External Supply)
Vd	Bootstrap diode forward voltage. [0.8V]
Vboot	Required Vboot voltage at start up. [3V]

IR3846 implements asynchronous switching during startup to help prevent oscillation and output disturbance when starting up with a pre-biased output. The regulator starts in an asynchronous fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. Figure 8 shows a typical Pre-Bias condition at start up. The sync FET always starts with a narrow pulse width (12.5% of a switching period) and gradually increases its duty cycle with a step of 12.5% until it reaches the steady state value. The number of these startup pulses for each step is 16 and it's internally programmed. Figure 9 shows the series of 16x8 startup pulses.

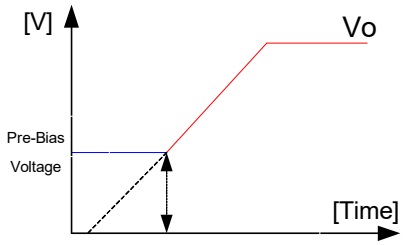


Figure 8: Pre-Bias startup

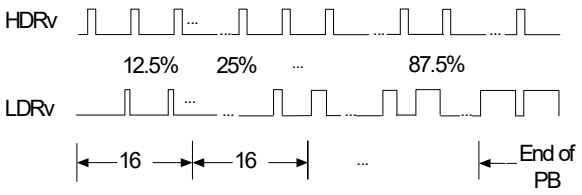


Figure 9: Pre-Bias startup pulses

SOFT-START

IR3846 has an internal digital soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and VCC rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal soft-start (Intl_SS) signal linearly rises with the rate of 0.4mV/µs from 0V to 1.5V. Figure 10 shows the waveforms during soft start. The normal Vout startup time is fixed, and is equal to:

$$Tstart = \frac{(0.75V - 0.15V)}{0.4mV/\mu S} = 1.5mS \qquad \textbf{(2)}$$

During the soft start the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

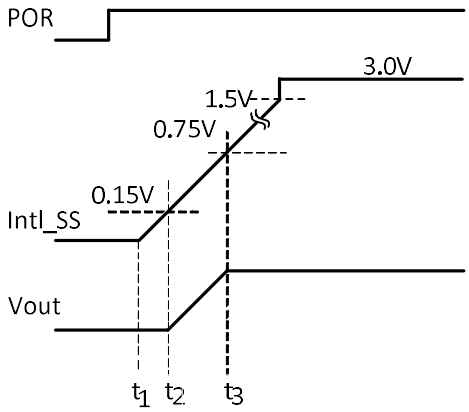


Figure 10: Theoretical operation waveforms during soft-start (non tracking / non sequencing)

OPERATING FREQUENCY

The switching frequency can be programmed between 300kHz – 1500kHz by connecting an external resistor from R_t pin to LGnd. Table 1 tabulates the oscillator frequency versus R_t.

Table 1: Switching Frequency(Fs) vs. External Resistor(*Rt*)

Rt (KΩ)	Freq (KHz)
80.6	300
60.4	400
48.7	500
39.2	600
34	700
29.4	800
26.1	900
23.2	1000
21	1100
19.1	1200
17.4	1300
16.2	1400
15	1500

SHUTDOWN

IR3846 can be shutdown by pulling the Enable pin below its 1.0V threshold. During shutdown the high side and the low side drivers are turned off.

OVER CURRENT PROTECTION

The Over Current (OC) protection is performed by sensing the inductor current through the $R_{DS(on)}$ of the Synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The Over Current (OC) limit can be set to one of three possible settings by floating the OCset pin, by pulling up the OCset pin to VCC, or pulling down the OCset pin to PGnd. The current limit scheme in the

IR3846 uses an internal temperature compensated current source to achieve an almost constant OC limit over temperature.

Over Current Protection circuit senses the inductor current flowing through the Synchronous MOSFET. To help minimize false tripping due to noise and transients, inductor current is sampled for about 30 nS on the downward inductor current slope approximately 12.5% of the switching period before the inductor current valley. However, if the Synchronous MOSFET is on for less than 12.5% of the switching period, the current is sampled approximately 40nS after the start of the downward slope of the inductor current. When the sampled current is higher than the OC Limit, an OC event is detected.

When an Over Current event is detected, the converter enters hiccup mode. Hiccup mode is performed by latching the OC signal and pulling the Intl_SS signal to ground for 20.48 mS (typ.). OC signal clears after the completion of hiccup mode and the converter attempts to return to the nominal output voltage using a soft start sequence. The converter will repeat hiccup mode and attempt to recover until the overload or short circuit condition is removed.

Because the IR3846 uses valley current sensing, the actual DC output current limit will be greater than OC limit. The DC output current is approximately half of peak to peak inductor ripple current above selected OC limit. OC Limit, inductor value, input voltage, output voltage and switching frequency are used to calculate the DC output current limit for the converter. Equation (2) to determine the approximate DC output current limit.

$$I_{OCP} = I_{LIMIT} + \frac{\Delta i}{2} \quad \textbf{(3)}$$

I_{OCP} = DC current limit hiccup point
I_{LIMIT} = Current Limit Valley Point
Δi = Inductor ripple current

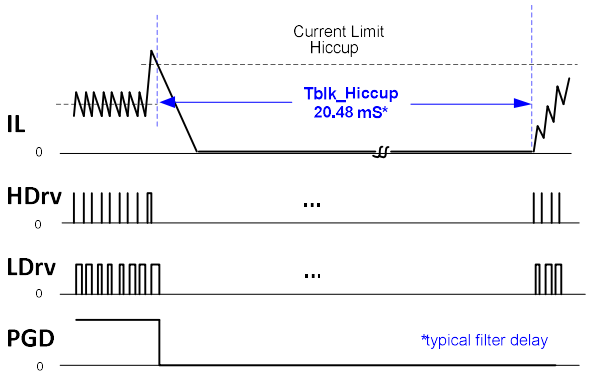


Figure 11: Timing Diagram for Current Limit Hiccup

THERMAL SHUTDOWN

Temperature sensing is provided inside IR3846. The trip threshold is typically 145°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and resets the internal soft start.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

REMOTE VOLTAGE SENSING

True differential remote sensing in the feedback loop is critical to high current applications where the output voltage across the load may differ from the output voltage measured locally across an output capacitor at the output inductor, and to applications that require die voltage sensing.

The RS+ and RS- pins of the IR3846 form the inputs to a remote sense differential amplifier (RSA) with high speed, low input offset and low input bias current which ensure accurate voltage sensing and fast transient response in such applications.

The input range for the differential amplifier is limited to 1.5V below the VCC rail. Note that IR3846 incorporates a smart LDO which switches the VCC rail voltage depending on the loading. When determining the input range assume the part is in light load and using the lower VCC rail voltage.

There are two remote sense configurations that are usually implemented. Figure 12 shows a general remote sense (RS) configuration. This configuration allows the RSA to monitor output voltages above

VCC. A resistor divider is placed in between the output and the RSA to provide a lower input voltage to the RSA inputs. Typically, the resistor divider is calculated to provide VREF (0.6V) across the RSA inputs which is then outputted to RSo. The input impedance of the RSA is 63 KOhms typically and should be accounted for when determining values for the resistor divider. To account for the input impedance, assume a 63 KOhm resistor in parallel to the lower resistor in the divider network. The compensation is then designed for 0.6V to match the RSo value.

Low voltage applications can use the second remote sense configuration. When the output voltage range is within the RSA input specifications, no resistor divider is needed in between the converter output and RSA. The second configuration is shown in Figure 13. The RSA is used as a unity gain buffer and compensation is determined normally.

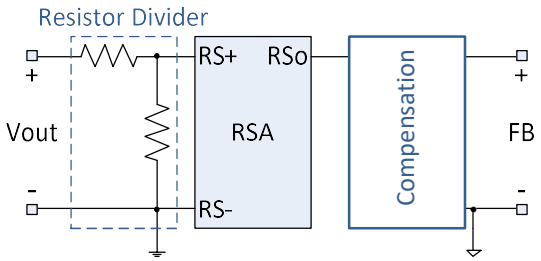


Figure 12: General Remote Sense Configuration

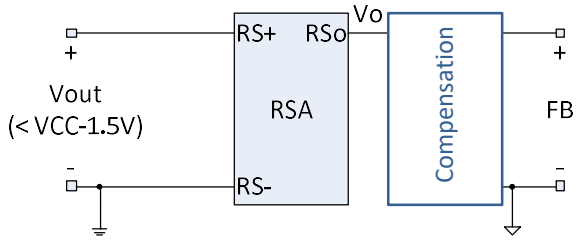


Figure 13: Remote Sense Configuration for Vout less than VCC-1.5V

EXTERNAL SYNCHRONIZATION

IR3846 incorporates an internal phase lock loop (PLL) circuit which enables synchronization of the internal oscillator to an external clock. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple point-of-load (POL) regulators are used. A multi-function pin, Rt/Sync, is used to connect the external clock. If the external clock is present before the converter turns on, Rt/Sync pin can be connected to the external clock signal solely and no other resistor is needed. If the external clock is applied after the converter turns on, or the converter switching frequency needs to toggle between the external clock frequency and the internal free-running frequency, an external resistor from Rt/Sync pin to LGnd is required to set the free-running frequency.

When an external clock is applied to Rt/Sync pin after the converter runs in steady state with its free-running frequency, a transition from the free-running frequency to the external clock frequency will happen. This transition is to gradually make the actual switching frequency equal to the external clock frequency, no matter which one is higher. When the external clock signal is removed from Rt/Sync pin, the switching frequency is also changed to free-running gradually. In order to minimize the impact from these transitions to output voltage, a diode is recommended to add between the external clock and Rt/Sync pin. Figure 14 shows the timing diagram of these transitions.

An internal circuit is used to change the PWM ramp slope according to the clock frequency applied on Rt/Sync pin. Even though the frequency of the external synchronization clock can vary in a wide range, the PLL circuit keeps the ramp amplitude constant, requiring no adjustment of the loop compensation. PVin variation also affects the ramp amplitude, which will be discussed separately in Feed-Forward section.

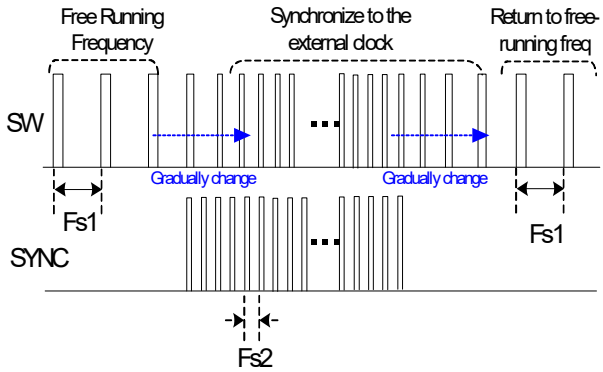


Figure 14: Timing Diagram for Synchronization to the external clock (Fs1>Fs2 or Fs1<Fs2)

FEED-FORWARD

Feed-Forward (F.F.) is an important feature, because it can keep the converter stable and preserve its load transient performance when PVin varies. The PWM ramp amplitude (Vramp) is proportionally changed with PVin to maintain PVin/Vramp almost constant throughout PVin variation range (as shown in Figure 15). The PWM ramp amplitude is adjusted to 0.15 of PVin. Thus, the control loop bandwidth and phase margin can be maintained constant. Feed-forward function can also minimize impact on output voltage from fast PVin change. F.F. is disabled when PVin<6.2V and the PWM ramp is typically 0.9V. For PVin<6.2V, PVin voltage should be accounted for when calculating control loop parameters.

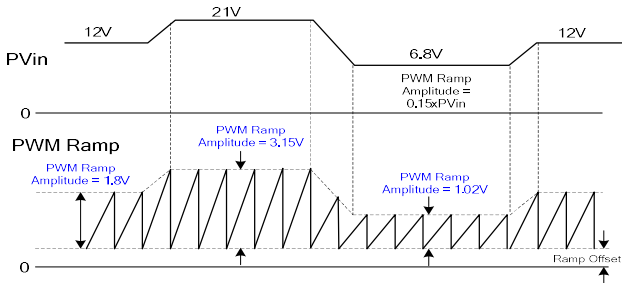


Figure 15: Timing Diagram for Feed-Forward (F.F.) Function

SMART LOW DROPOUT REGULATOR (LDO)

IR3846 has an integrated low dropout (LDO) regulator which can provide gate drive voltage for both drivers. In order to improve overall efficiency over the whole load range, LDO voltage is set to 6.8V (typ.) at mid- or heavy load condition to reduce Rds(on) and thus MOSFET conduction loss; and it is reduced to 4.4V (typ.) at light load condition to reduce gate drive loss.

The smart LDO selects its output voltage according to the load condition by sensing the inductor current (I_L). At light load condition, the inductor current can fall below zero as shown in Figure 16. A zero crossing comparator is used to detect when the inductor current falls below zero at the LDrv Falling Edge. If the comparator detects zero crossing events for 256 consecutive switching cycles, the smart LDO reduces its output to 4.4V. The LDO voltage will remain low until a zero crossing is not detected. Once a zero crossing is not detected, the counter is reset and LDO voltage returns to 6.8V. Figure 16 shows the timing diagram. Whenever the device turns on, LDO always starts with 6.8V, then goes to 4.4V / 6.8V depending upon the load condition. However, if only Vin is applied with Enable low, the LDO output is 4.4V.

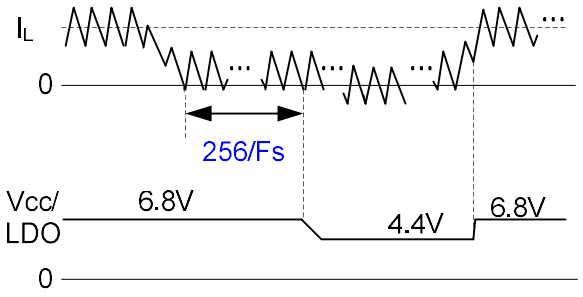


Figure 16: Time Diagram for Smart LDO

Users can configure the IR3846 to use a single supply or dual supplies. Depending on the configuration used the PVin, Vin and VCC pins are connected differently. Below several configurations are shown. In an internally biased configuration, the LDO draws from the Vin pin and provides a gate drive voltage, as shown in Figure 17. By connecting Vin and PVin together as shown in the Figure 18, IR3846 is an internally biased single supply configuration that runs off a single supply.

IR3846 can also use an external bias to provide gate drive voltage for the drivers instead of the internal LDO. To use an external bias, connected Vin and VCC to the external bias. PVin can use a separate rail as shown in Figure 19 or run off the same rail as Vin and VCC.

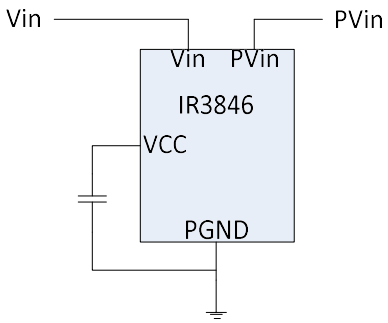


Figure 17: Internally Biased Configuration

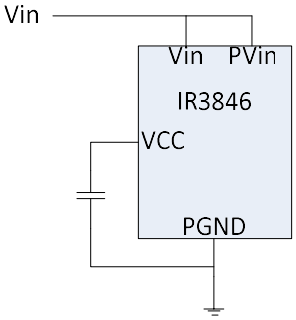


Figure 18: Internally Biased Single Supply Configuration

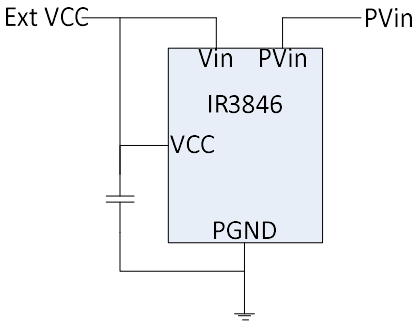


Figure 19: Externally Biased Configuration

When the Vin voltage is below 6.8V, the internal LDO enters the dropout mode at medium and heavy load. The dropout voltage increases with the switching frequency. Figure 20 shows the LDO voltage for 600kHz and 1000kHz switching frequency respectively.

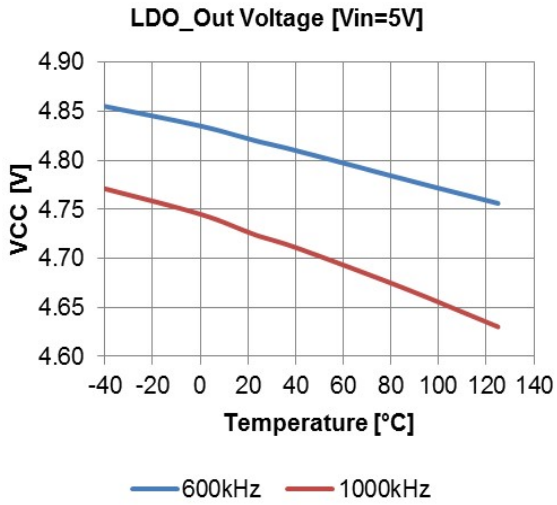


Figure 20: LDO_Out Voltage in dropout mode

OUTPUT VOLTAGE TRACKING AND SEQUENCING

IR3846 can accommodate user programmable tracking and/or sequencing options using Vp, Vref, Enable, and Power Good pins. In the block diagram presented on page 3, the error-amplifier (E/A) has been depicted with three positive inputs. Ideally, the input with the lowest voltage is used for regulating the output voltage and the other two inputs are ignored. In practice the voltage of the other two inputs should be at least 200mV greater than the low-voltage input so that their effects can completely be ignored. Vp is pulled up to an internal rail via a high impedance path. For normal operation, Vp and Vref is left floating (Vref should have a bypass capacitor).

Therefore, in normal operating condition, after Enable goes high, the internal soft-start (Intl_SS) ramps up the output voltage until Vfb (voltage of feedback/Fb pin) reaches about 0.6V. Then Vref takes over and the output voltage is regulated.

Tracking-mode operation is achieved by connecting Vref to LGND. Then, while Vp = 0V, Enable is taken above its threshold so that the soft-start circuit generates Intl_SS signal. After the Intl_SS signal reaches the final value (refer to Figure 7), ramping up the Vp input will ramp up the output voltage. In tracking mode, Vfb always follows Vp which means Vout is always proportional to Vp voltage (typical for DDR/Vtt rail applications). The effective Vp range is 0V~1.2V.

In sequencing mode of operation (simultaneous or ratiometric), Vref is left floating and Vp is kept to ground level until Intl_SS signal reaches the final value. Then Vp is ramped up and Vfb follows Vp. When Vp>0.6V the error-amplifier switches to Vref and the output voltage is regulated with Vref. The final Vp voltage after sequencing startup should between 0.8V ~ 3.0V.

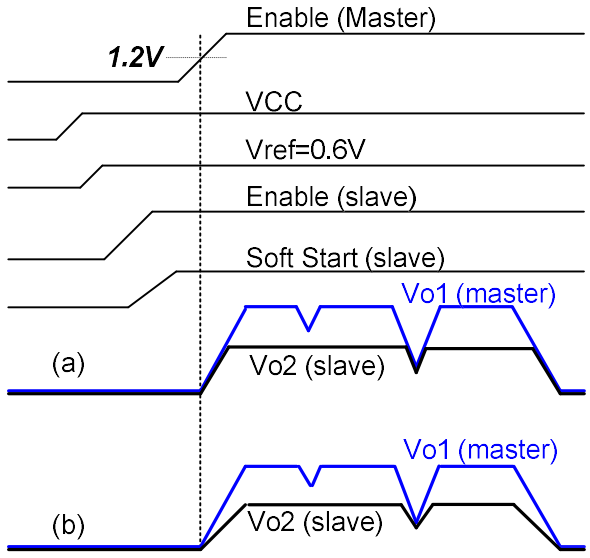


Figure 21: Typical waveforms for sequencing mode of operation: (a) simultaneous, (b) ratiometric

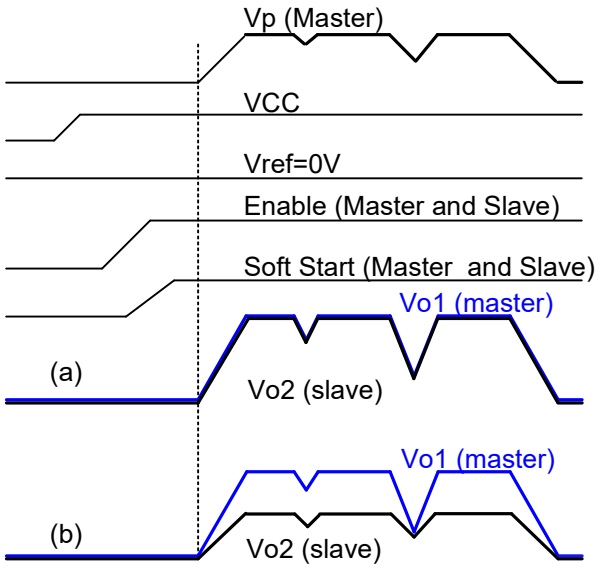


Figure 22: Typical waveforms in tracking mode of operation: (a) simultaneous, (b) ratiometric

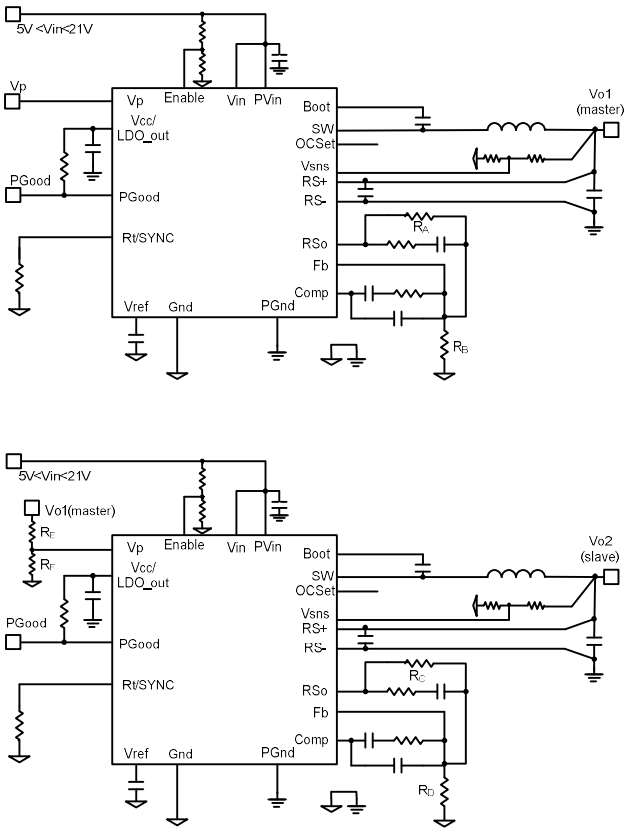


Figure 23: Application Circuit for Simultaneous and Ratiometric Sequencing

Tracking and sequencing operations can be implemented to be simultaneous or ratiometric (refer to Figure 21 and Figure 22). Figure 23 shows typical circuit configuration for sequencing operation. With this power-up configuration, the voltage at the Vp pin of the slave reaches 0.6V before the Fb pin of the master. If $R_E/R_F = R_C/R_D$, simultaneous startup is achieved. That is, the output voltage of the slave follows that of the master until the voltage at the Vp pin of the slave reaches 0.6 V. After the voltage at the Vp pin of the slave exceeds 0.6V, the internal 0.6V reference of the slave dictates its output voltage. In reality the regulation gradually shifts from Vp to internal Vref. The circuit shown in Figure 23 can also be used for simultaneous or ratiometric tracking operation if Vref of the slave is connected to LGND. Table 2 summarizes the required conditions to achieve simultaneous/ratiometric tracking or sequencing operations.

Table 2: Required Conditions for Simultaneous / Ratiometric Tracking and Sequencing (Figure 23)

Operating Mode	Vref (Slave)	Vp	Required Condition
Normal (Non-sequencing, Non-tracking)	0.6 (Floating)	Floating	—
Simultaneous Sequencing	0.6V	Ramp up from 0V	$R_A/R_B > R_E/R_F = R_C/R_D$
Ratiometric Sequencing	0.6V	Ramp up from 0V	$R_A/R_B > R_E/R_F > R_C/R_D$
Simultaneous Tracking	0V	Ramp up from 0V	$R_E/R_F = R_C/R_D$
Ratiometric Tracking	0V	Ramp up from 0V	$R_E/R_F > R_C/R_D$

VREF

This pin reflects the internal reference voltage which is used by the error amplifier to set the output voltage. In most operating conditions this pin is only connected to an external bypass capacitor and it is left floating. A minimum 100pF ceramic capacitor is required from stability point of view. In tracking mode this pin should be pulled to LGND. For margining applications, an external voltage source is connected to Vref pin and overrides the internal reference voltage. The external voltage source should have a low internal resistance (<100Ω) and be able to source and sink more than 25µA.

POWER GOOD OUTPUT (TRACKING, SEQUENCING, VREF MARGINING)

IR3846 continually monitors the output voltage via the sense pin (Vsns) voltage. The Vsns voltage is an input to the window comparator with upper and lower threshold of 1.2*VREF and 0.95*VREF respectively. PGood signal is high whenever Vsns voltage is within the PGood comparator window thresholds. Hysteresis has been applied to the lower threshold, PGood signal goes low when Vsns drops below 0.9*VREF instead of 0.95*VREF. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation.

The threshold is set differently in different operating modes and the results of the comparison sets the PGood signal. Figure 24, Figure 25 and Figure 26 show the timing diagram of the PGood signal at different operating modes. Vsns signal is also used by OVP comparator for detecting output over voltage condition. PGood signal is low when Enable is low.

PGood pin should not exceed Vcc pin voltage. By allowing PGood to exceed the VCC voltage, the internal ESD structure will be back biased and the PGood supply can partially drive the VCC rail. Due to current being drawn through the PGood pull-up resistor, the PGood voltage will reside in at an undefined voltage level which may be translated as a low or high level.

Damage is not expected when PGood is back biased, but back biasing PGood is not recommended.

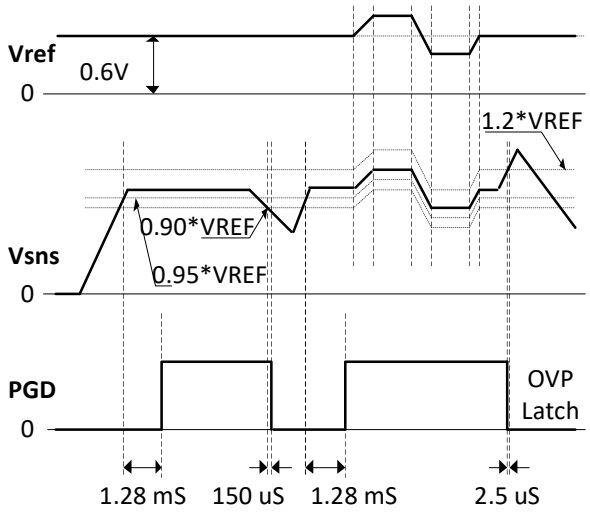


Figure 24: Non-sequence, Non-tracking Startup and Vref Margin (Vp pin floating)

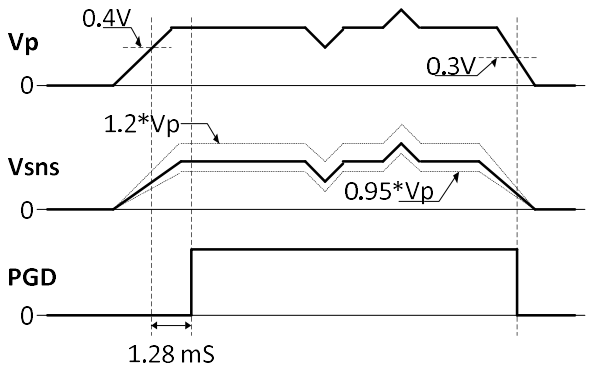


Figure 25: Vp Tracking (Vref = 0V)

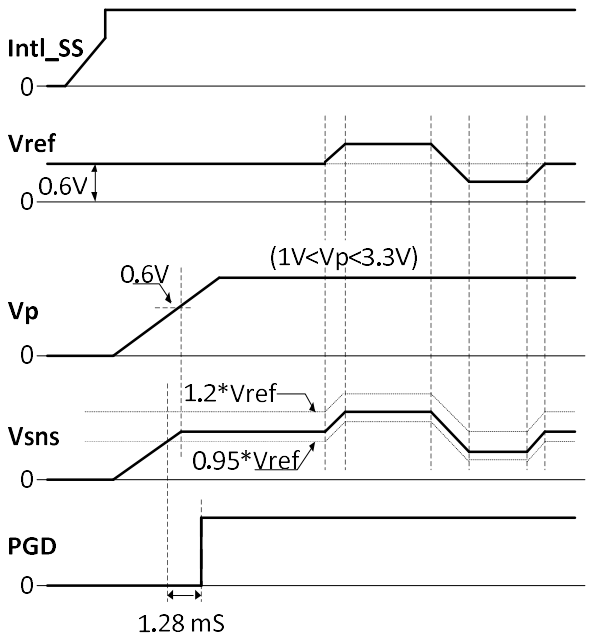


Figure 26: Vp Sequence and Vref Margin

OVER-VOLTAGE PROTECTION (OVP)

Over-voltage protection in IR3846 is achieved by comparing sense pin voltage Vsns to a pre-set threshold. In non-tracking mode, OVP threshold can be set at 1.2*Vref; in tracking mode, it can be at 1.2*Vp. When Vsns exceeds the over voltage threshold, an over voltage trip signal asserts after 2.5 uS (typ.) delay. The high side drive signal HDrv is latched off immediately and PGood flags are set low. The low side drive signal is kept on until the Vsns voltage drops below the threshold. HDrv remains latched off until a reset is performed by cycling VCC. OVP is active when enable is high or low.

Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally. Figure 27 shows the timing diagram for OVP in non-tracking mode.

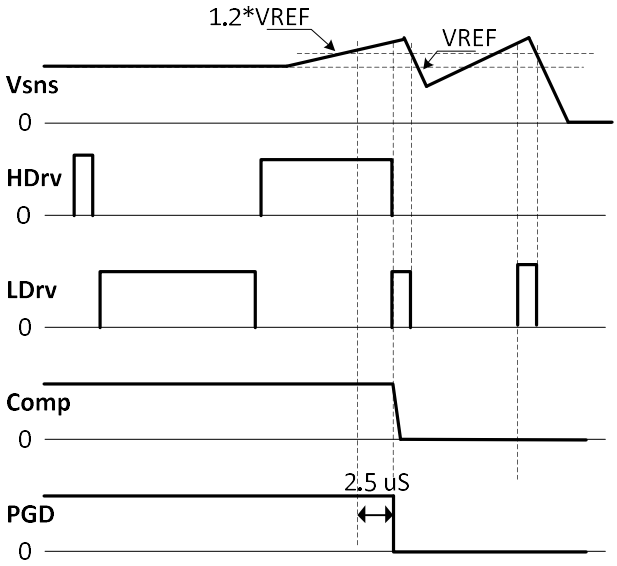


Figure 27: Timing Diagram for OVP in non-tracking mode

SOFT-START / SOFT-STOP (S_CTRL)

S_Ctrl allows for the gradual charging and discharging of Vout to its final value by controlling the Soft-Start and Soft-Stop functions. Soft-Start and Soft-Stop is the gradual charging and discharging of Vout, respectfully. Both functions use the internal Intl_SS ramp to regulate the rate Vout charges and discharges. Soft-Start feature is enabled when S_Ctrl and EN are asserted high. S_Ctrl is internally pulled high, so that EN typically controls the rise of Vout. To delay the charging of Vout, keep S_Ctrl low while setting EN. Then assert S_Ctrl high to initiate the Intl_SS ramp (Soft-Start). Vout follows Intl_SS and ramps up until it reaches its steady state. For Soft-Stop, S_Ctrl needs to be pulled low before EN goes low. When S_Ctrl falls below its lower threshold, Intl_SS becomes a decreasing ramp with the same rate as the Soft-Start ramp. Vout follows this ramp and discharges softly until completely shut down. Figure 28 shows the timing diagram of S_Ctrl controlled soft-start and soft-stop.

If the Enable pin goes low before S_Ctrl, the converter shuts down without Soft-Stop. Both gate drivers are turned off immediately and Vout discharges to zero.

Figure 29 shows the timing diagram of Enable controlled soft-start and soft-stop.

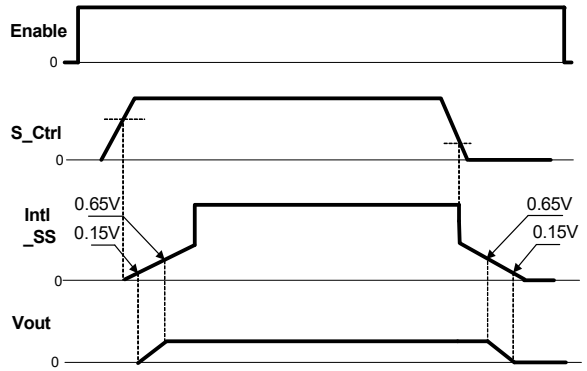


Figure 28: Timing Diagram for S_Ctrl controlled Soft-Start / Soft-Stop

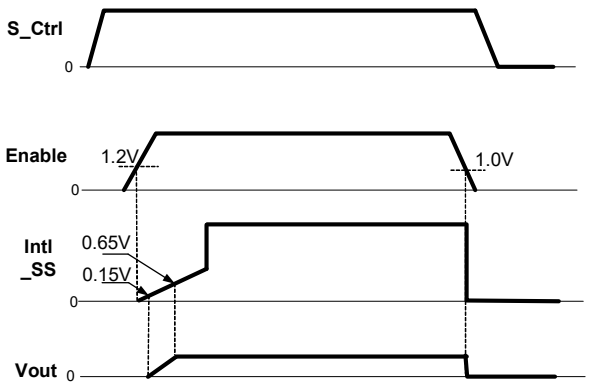


Figure 29: Timing Diagram for Enable controlled Soft-Start / Shutdown

BODY BRAKING™

The Body Braking feature of the IR3846 allows improved transient response for step-down load transients. A severe step-down load transient would cause an overshoot in the output voltage and drive the Comp pin voltage down until control saturation occurs demanding 0% duty cycle and the PWM input to the Control FET driver is kept OFF. When the first such skipped pulse occurs, the IR3846 enters Body Braking mode, wherein the Sync FET also turned OFF. The inductor current then decays by freewheeling through the body diode of the Sync FET. Thus, with Body Braking, the forward voltage drop of the body diode provides and additional voltage to discharge the inductor current faster to the light load value as shown in equation **(4)** and equation **(5)** below:

$$\frac{di_L}{dt} = -\frac{V_o + V_D}{L}, \text{ with body braking} \quad \textbf{(4)}$$

$$\frac{di_L}{dt} = -\frac{V_o}{L}, \text{ without body braking} \quad \textbf{(5)}$$

I_L = Inductor current
V_D = Forward voltage drop of the body diode of the Sync FET.
V_o = output voltage
L = Inductor value

The Body Braking mechanism is kept OFF during pre-bias operation. Also, in the event of an extremely severe load step-down transient causing OVP, the Body Brake is overridden by the OVP latch, which turns on the Sync FET.

MINIMUM ON TIME CONSIDERATIONS

The minimum ON time is the shortest amount of time for Ctrl FET to be reliably turned on. This is very critical parameter for low duty cycle, high frequency applications. Conventional approach limits the pulse width to prevent noise, jitter and pulse skipping. This results to lower closed loop bandwidth.

IR has developed a proprietary scheme to improve and enhance minimum pulse width which utilizes the benefits of voltage mode control scheme with higher switching frequency, wider conversion ratio and higher closed loop bandwidth, the latter results in reduction of output capacitors. Any design or application using IR3846 must ensure operation with a pulse width that is higher than the minimum on-time. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{PV_{in} \times F_s} \quad \textbf{(6)}$$

In any application that uses IR3846, the following condition must be satisfied:

$$t_{on(\min)} \le t_{on} \quad \textbf{(7)}$$

$$t_{on(\min)} \le \frac{V_{out}}{PV_{in} \times F_s} \quad \textbf{(8)}$$

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad \textbf{(9)}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.6V. Therefore, for $V_{out(min)}$ = 0.6V,

$$\therefore PV_{in} \times F_s \le \frac{V_{out}}{t_{on(\min)}} \quad (10)$$

$$\therefore PV_{in} \times F_s \le \frac{0.6V}{50nS} = 12V/\mu S$$

Therefore, at the maximum recommended input voltage 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 571 kHz. Conversely, for operation at the maximum recommended operating frequency (1.5 MHz) and minimum output voltage (0.6V). The input voltage (PVin) should not exceed 8V, otherwise pulse skipping may happen.

MAXIMUM DUTY RATIO

A certain off-time is specified for IR3846. This provides an upper limit on the operating duty ratio at any given switching frequency. The off-time remains at a relatively fixed ratio to switching period in low and mid frequency range, while in high frequency range this ratio increases, thus the lower the maximum duty ratio at which IR3846 can operate. Figure 30 shows a plot of the maximum duty ratio vs. the switching frequency with built in input voltage feed forward mechanism.

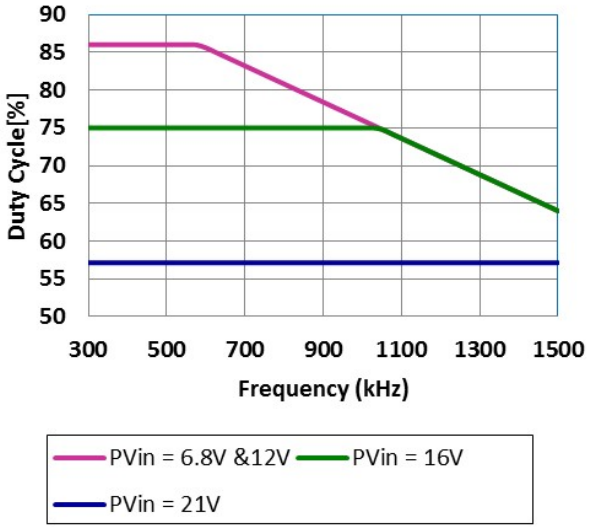


Figure 30: Maximum duty cycle vs. switching frequency

TYPICAL OPERATING WAVEFORM

DESIGN EXAMPLE

The following example is a typical application for IR3846. The application circuit is shown in Figure 37.

V_{in} = PV_{in} = 12V
F_s = 600kHz

V_o = 1.2V
I_o = 35A
Ripple Voltage = ± 1% * V_o
ΔV_o = ± 4% * Vo (for 30% load transient)

Enabling the IR3846

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage as shown in Figure 31.

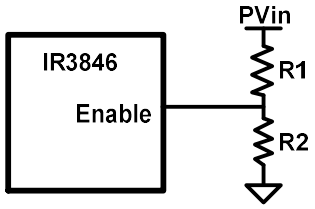


Figure 31: Using Enable pin for UVLO implementation

For a typical Enable threshold of V_{EN} = 1.2 V

$$PV_{in(\min)} \times \frac{R_2}{R_1 + R_2} = V_{EN} = 1.2 \quad (11)$$

$$R_2 = R_1 \frac{V_{EN}}{PV_{in(\min)} - V_{EN}} \quad (12)$$

For $PV_{in\ (min)}$=9.2V, R_1=49.9K and R_2=7.5K ohm is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 39.2 KΩ, using Table 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The FB pin is the inverting input of the error amplifier, which is internally referenced to VREF. The divider ratio is set to equal VREF at the FB pin when the output is at its desired value. When an external resistor divider is connected to the output as shown in Figure 32, the output voltage is defined by using the following equation:

$$V_o = V_{ref} \times \left(1 + \frac{R_5}{R_6}\right) \quad \textbf{(13)}$$

$$R_6 = R_5 \times \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad \textbf{(14)}$$

For the calculated values of R5 and R6, see feedback compensation section.

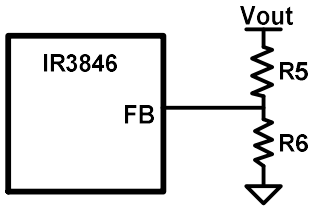


Figure 32: Typical application of the IR3846 for programming the output voltage

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected to the source of the Control FET. This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C1). The operation of the circuit is as follows: When the sync FET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode (Figure 33), which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C1 is approximately given as:

$$V_c \cong V_{cc} - V_D \quad \textbf{(15)}$$

When the control FET turns on in the next cycle, the capacitor node connected to SW rises to the bus

voltage V_{in}. However, if the value of C1 is appropriately chosen, the voltage V_c across C1 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong PV_{in} + V_{cc} - V_D \quad \textbf{(16)}$$

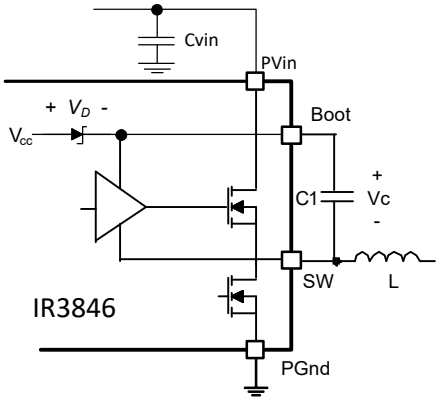


Figure 33: Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple currents generated during the on time of the control FETs should be provided by the input capacitor. The RMS value of this ripple for each channel is expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)} \quad \textbf{(17)}$$

$$D = \frac{V_o}{V_{in}} \quad \textbf{(18)}$$

Where:

D = Duty Cycle
I_{RMS} = RMS value of the input capacitor current
I_o = output current.
V_{in} = Power Stage input voltage

I_o=35A and D = 0.1, the I_{RMS} = 10.5A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 7x22uF, 25V ceramic capacitors, GRM31CR61E226KE15L from Murata. In addition to these, although not mandatory, a 1x330uF, 25V SMD capacitor EEV-FK1E331P from Panasonic may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

Inductors are selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but may also result in reduced efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current. For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L \times \frac{\Delta i}{\Delta t}; \Delta t = D \times \frac{1}{F_s}$$

$$L = (V_{in} - V_o) \times \frac{V_o}{V_{in} \times \Delta i \times F_s} \quad \textbf{(19)}$$

Where:

V_{in} = Maximum input voltage
V_0 = Output Voltage
Δi = Inductor Ripple Current
F_s = Switching Frequency
Δ_t = On time for Control FET
D = Duty Cycle

If $\Delta i \approx 30\% * I_o$, then the inductor is calculated to be 0.24µH. Select L=0.25µH, 744309025, from Wurth Electronik which provides an inductor suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criterion is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{0(ESR)} = \Delta I_L \times ESR$$

$$\Delta V_{0(ESL)} = \left(\frac{V_{in} - V_o}{L}\right) \times ESL$$

$$\Delta V_{0(C)} = \frac{\Delta I_L}{8 \times C_o \times F_s} \quad \textbf{(20)}$$

Where:

ΔV_0 = Output Voltage Ripple

ΔI_L = Inductor Ripple Current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3846 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Six of Murata GRM31CR60J107ME39L (100uF/1206/X5R/ 6.3V) capacitors is a good choice.

It is also recommended to use a 0.1µF ceramic capacitor at the output for high frequency filtering.

Feedback Compensation

The IR3846 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, -40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180°. The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_o \times C_o}} \quad \textbf{(21)}$$

Figure 34 shows gain and phase of the LC filter. Since we already have 180° phase shift from the output filter alone, the system runs the risk of being unstable.

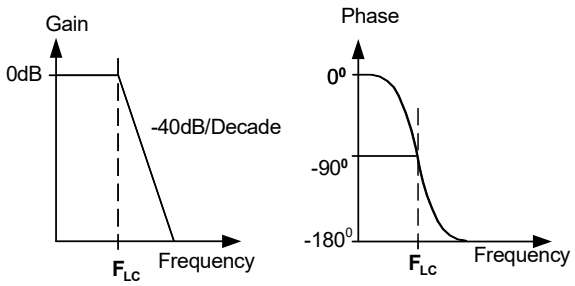


Figure 34: Gain and Phase of LC filter

The IR3846 uses a voltage-type error amplifier with high-gain and high-bandwidth. The output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in type II or type III compensation. Local feedback with Type II compensation is shown in Figure 35.

This method requires that the output capacitor have enough ESR to satisfy stability requirements. If the output capacitor's ESR generates a zero at 5kHz to 50kHz, the zero generates acceptable phase margin and the Type II compensator can be used.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_o} \quad \textbf{(22)}$$

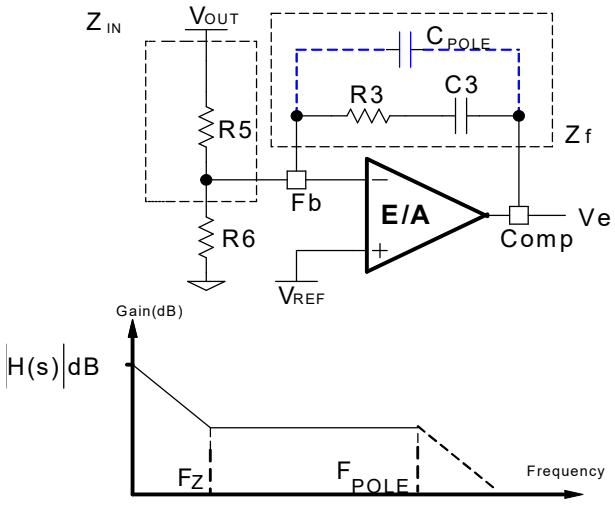


Figure 35: Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_{out}) is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_3}{sR_5C_3} \quad \textbf{(23)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = \frac{R_3}{R_5} \quad \textbf{(24)}$$

$$F_z = \frac{1}{2\times\pi\times R_3\times C_3} \quad \textbf{(25)}$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10)\times F_s \quad \textbf{(26)}$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{ramp}\times F_o \times F_{ESR}\times R_5}{V_{in}\times\beta\times F_{LC}^2} \quad \textbf{(27)}$$

Where:

V_{ramp} = Amplitude of the oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
R_5 = Feedback Resistor
V_{in} = Maximum Input Voltage
β = (RS+ - RS-) / Vo
F_{LC} = Resonant Frequency of the Output Filter

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_Z = 75\%\times F_{LC}$$

$$F_Z = 0.75\times\frac{1}{2\times\pi\sqrt{L_o\times C_o}} \quad \textbf{(28)}$$

Use equation (24), (25) and (26) to calculate C3.

One more capacitor is sometimes added in parallel with C3 and R3. This introduces one more pole which is mainly used to suppress the switching noise.

The additional pole is given by:

$$F_p = \frac{1}{2\times\pi\times\frac{C_3\times C_{POLE}}{C_3+C_{POLE}}} \quad \textbf{(29)}$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi\times R_3\times F_S - \frac{1}{C_3}} \cong \frac{1}{\pi\times R_3\times F_S} \quad \textbf{(30)}$$

For a general unconditional stable solution for any type of output capacitors with a wide range of ESR values, we use a local feedback with a type III compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 36.

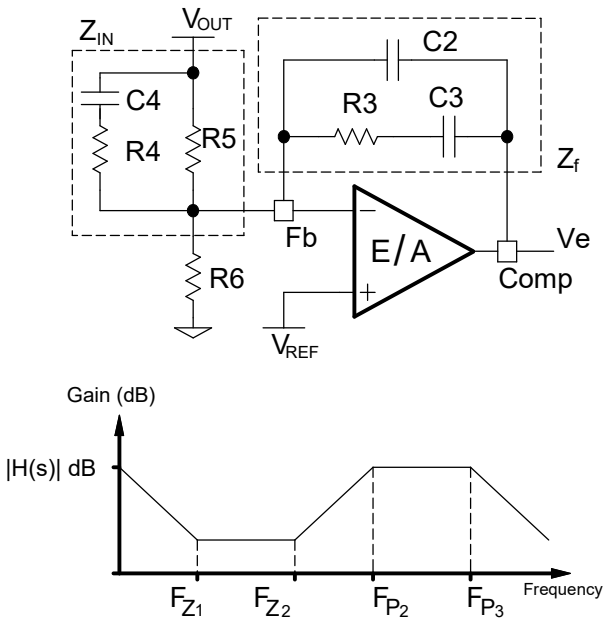


Figure 36: Type III Compensation network and its asymptotic gain plot

Again, the transfer function is given by:

$$\frac{V_e}{V_{out}} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f, according to Figure 36, the transfer function can be expressed as:

$$H(s) = -\frac{(1+sR_3C_3)[1+sC_4(R_4+R_5)]}{sR_5(C_2+C_3)\left[1+sR_3\left(\frac{C_2\times C_3}{C_2+C_3}\right)\right](1+sR_4C_4)} \quad \textbf{(31)}$$

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad \textbf{(32)}$$

$$F_{P2} = \frac{1}{2\pi\times R_4\times C_4} \quad \textbf{(33)}$$

$$F_{P3} = \frac{1}{2\pi\times R_3\left(\frac{C_2\times C_3}{C_2+C_3}\right)} \cong \frac{1}{2\pi\times R_3\times C_2} \quad \textbf{(34)}$$

$$F_{Z1} = \frac{1}{2\pi\times R_3\times C_3} \quad \textbf{(35)}$$

$$F_{Z2} = \frac{1}{2\pi\times C_4\times(R_4\times R_5)} \cong \frac{1}{2\pi\times C_4\times R_5} \quad \textbf{(36)}$$

Cross over frequency is expressed as:

$$F_o = R_3\times C_4\times\beta\times\frac{V_{in}}{V_{ramp}}\times\frac{1}{2\pi\times L_o\times C_o} \quad \textbf{(37)}$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to the crossover frequency, the compensation type can be different. Table 3 shows the compensation types for relative locations of the crossover frequency.

Table 3: Different types of compensators

Compensator Type	F_{ESR} vs F_O	Typical Output Capacitor
Type II	$F_{LC} < F_{ESR} < F_O < F_S/2$	Electrolytic
Type III	$F_{LC} < F_O < F_{ESR}$	SP Cap, Ceramic

The higher the crossover frequency is, the potentially faster the load transient response will be. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency (F_o) is selected such that:

$$F_o \le (1/5 \sim 1/10)^* F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45° for overall stability.

The specifications for designing channel 1:

V_{in} = 12V

V_o = 1.2V

V_{ramp}= 1.8V (This is a function of Vin, pls. see Feed-Forward section)

V_{ref} = 0.6V

β = (RS+ - RS-) / Vo (This assumes the resistor divider placed between Vout and the RSA scales down the output voltage to Vref. If the RSA is not used or Vout is connected directly

to the RSA, β = 1. Please refer to the Remote Sensing Amplifier section)

L_o = 0.250 µH

C_o = 6 x 100µF, ESR≈3mΩ each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 100µF capacitor used in this design is 56µF at 1.2 V DC bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency F_{LC} and using equation **(21)** to compute the small signal C_o.

These result to:

F_{LC} = 17.4 kHz

F_{ESR} = 947 kHz

$F_s/2$ = 300 kHz

Select crossover frequency F_0=100 kHz

Since $F_{LC}<F_0<Fs/2<F_{ESR}$, Type III is selected to place the pole and zeros.

Detailed calculation of compensation Type III:

Desired Phase Margin Θ = 70°

$$F_{Z2} = F_o\sqrt{\frac{1-\sin\Theta}{1+\sin\Theta}} = 14.1 \text{ kHz}$$

$$F_{P2} = F_o\sqrt{\frac{1+\sin\Theta}{1-\sin\Theta}} = 567.1 \text{ kHz}$$

Select:

$$F_{Z1} = 0.5 \times F_{Z2} = 7.05 \text{ kHz and}$$

$$F_{P3} = 0.5 \times F_s = 300 \text{ kHz}$$

Select C_4 = 2.2nF.

Calculate R_3, C_3 and C_2:

$$R_3 = \frac{2 \times \pi \times F_o \times L_o \times C_o \times V_{ramp}}{C_4 \times V_{in} \times \beta}$$; R_3 = 3.60 kΩ,

Select: R_3 = 2.7 kΩ

$$C_3 = \frac{1}{2 \times \pi \times F_{Z1} \times R_3}$$; C_3 = 8.49 nF,

Select: C_3 = 8.2 nF

$$C_2 = \frac{1}{2 \times \pi \times F_{P3} \times R_3}$$; C_2 = 196 pF,

Select: C_2 = 160 pF

Calculate R_4, R_5 and R_6:

$$R_4 = \frac{1}{2 \times \pi \times C_4 \times F_{P2}}$$; R_4 = 127.6 Ω,

Select R_4 = 127 Ω

$$R_5 = \frac{1}{2 \times \pi \times C_4 \times F_{Z2}}$$; R_5 = 5.13 kΩ,

Select R_5 = 4.02 kΩ

$$R_6 = \frac{V_{ref}}{(\beta \times V_o) - V_{ref}} \times R_5$$; R_6 = 4.02 kΩ,

Select R_6 = 4.02 kΩ

If (β x V_o) equals Vref, R6 is not used.

Setting the Power Good Threshold

In this design IR3846, the PGood outer limits are set at 95% and 120% of VREF. PGood signal is asserted 1.3ms after Vsns voltage reaches 0.95*0.6V=0.57V (Figure 37). As long as the Vsns voltage is between the threshold ranges, Enable is high, and no fault happens, the PGood remains high.

The following formula can be used to set the PGood threshold. $V_{out\ (PGood_TH)}$ can be taken as 95% of Vout. Choose Rsns1=4.02 KΩ.

$$Rsns2 = \left(\frac{V_{out(PGood_TH)}}{0.95 \times VREF} - 1 \right) \times Rsns1 \quad \textbf{(38)}$$

Rsns2 = 4.02 kΩ, Select 4.02 kΩ.

OVP comparator also uses Vsns signal for Over-Voltage detection. With above values for Rsns2 and Rsns1, OVP trip point ($Vout_{_OVP}$) is

$$Vout_{_OVP} = VREF \times 1.2 \times \frac{(Rsns1 + Rsns2)}{Rsns1} \quad \textbf{(39)}$$

$Vout_{_OVP}$ = 1.44 V

Selecting Power Good Pull-Up Resistor

The PGood is an open drain output and require pull up resistors to VCC. The value of the pull-up resistors should limit the current flowing into the PGood pin to less than 5mA. A typical value used is 10kΩ.

TYPICAL APPLICATION
INTERNALLY BIASED SINGLE SUPPLY

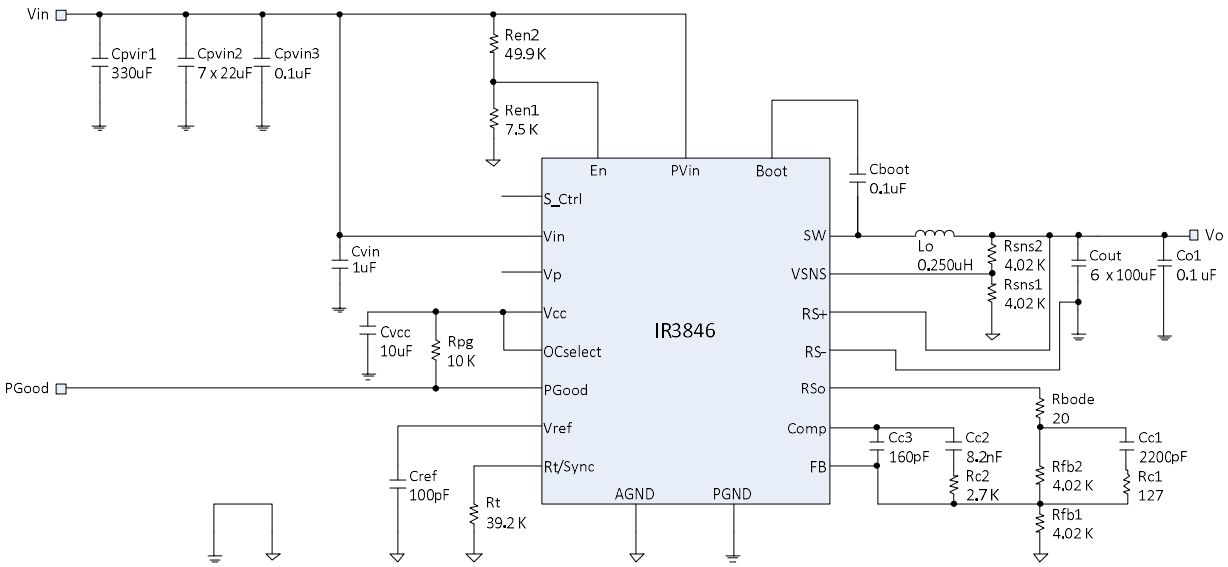


Figure 37: Application circuit for a 12V to 1.2V, 35A Point of Load Converter Using the Internal LDO

Suggested Bill of Material for application circuit 12V to 1.2V

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cpvin1	1	330uF	SMD, electrolytic, 25V, 20%	Panasonic	EEV-FK1E331P
Cpvin2	7	22uF	1206, 25V, X5R, 10%	Murata	GRM31CR61E226KE15L
Cref	1	100pF	0603, 50V, C0G, 5%	Murata	GRM1885C1H101JA01D
Cvin	1	1.0uF	0603, 25V, X5R, 20%	Murata	GRM188R61E105KA12D
Cvcc	1	10uF	0603, 10V, X5R, 20%	TDK	C1608X5R1A106M
Cpvin3 Cboot Co1	3	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01D
Cc1	1	2200pF	0603, 50V, X7R, 10%	Murata	GRM188R71H222KA01D
Cc2	1	8.2nF	0603, 50V, X7R, 10%	Murata	GRM188R71H822KA01D
Cc3	1	160pF	0603, 50V, NPO, 5%	Murata	GRM1885C1H161JA01D
Cout1	6	100uF	1206, 6.3V, X5R, 20%	Murata	GRM31CR60J107ME39L
L0	1	0.250uH	250nH,14x13x9mm DCR=0.165ohm	Wurth Electronik Inc.	744309025
Rbd	1	20	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF20R0V
Rc1	1	127	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF1270V
Rc2	1	2.7K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF2701V
Ren1	1	7.5K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF7501V
Ren2	1	49.9K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF4992V
Rfb1 Rfb2 Rsns1Rsns1	4	4.02K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF4021V
Rt	1	39.2K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF3922V
Rpg	1	10K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF1002V
U1	1	IR3846	PQFN 5x7mm	International Rectifier	IR3846MPBF

EXTERNALLY BIASED DUAL SUPPLIES

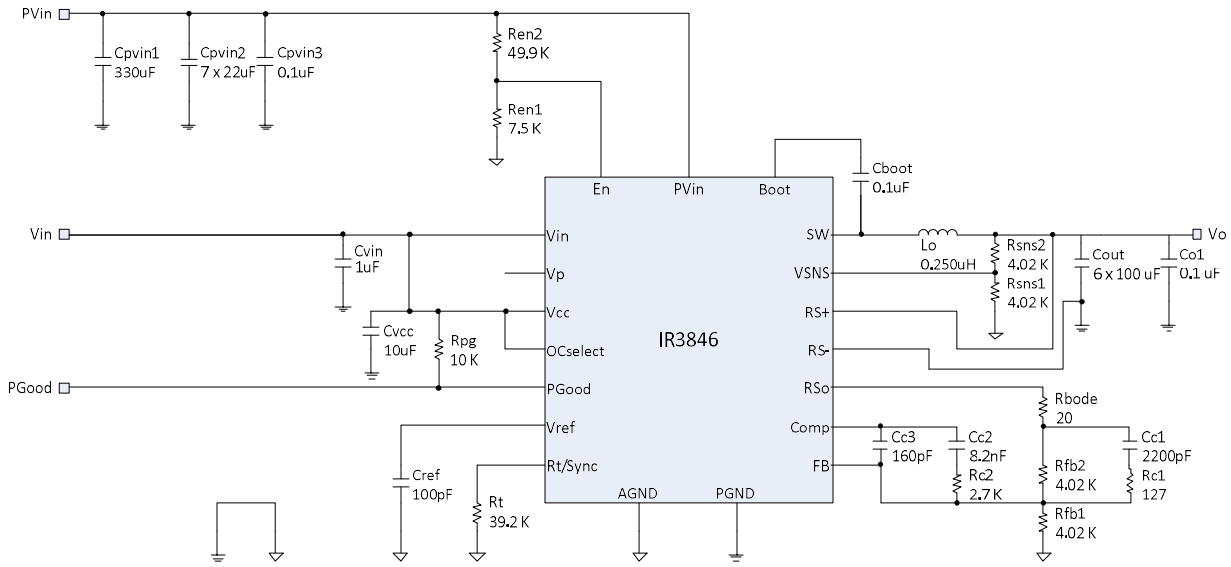


Figure 38: Application circuit for a 12V to 1.2V, 25A Point of Load Converter using external 5V VCC

Suggested Bill of Material for application circuit 12V to 1.2V using external 5V VCC

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cpvin1	1	330uF	SMD, electrolytic, 25V, 20%	Panasonic	EEV-FK1E331P
Cpvin2	7	22uF	1206, 25V, X5R, 10%	Murata	GRM31CR61E226KE15L
Cref	1	100pF	0603, 50V, C0G, 5%	Murata	GRM1885C1H101JA01D
Cvin	1	1.0uF	0603, 25V, X5R, 20%	Murata	GRM188R61E105KA12D
Cvcc	1	10uF	0603, 10V, X5R, 20%	TDK	C1608X5R1A106M
Cpvin3 Cboot Co1	3	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01D
Cc1	1	2200pF	0603, 50V, X7R, 10%	Murata	GRM188R71H222KA01D
Cc2	1	8.2nF	0603, 50V, X7R, 10%	Murata	GRM188R71H822KA01D
Cc3	1	160pF	0603, 50V, NPO, 5%	Murata	GRM1885C1H161JA01D
Cout1	6	100uF	1206, 6.3V, X5R, 20%	Murata	GRM31CR60J107ME39L
L0	1	0.250uH	250nH,14x13x9mm DCR=0.165ohm	Wurth Electronik Inc.	744309025
Rbd	1	20	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF20R0V
Rc1	1	127	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF1270V
Rc2	1	2.7K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF2701V
Ren1	1	7.5K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF7501V
Ren2	1	49.9K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF4992V
Rfb1 Rfb2 Rsns1Rsns1	4	4.02K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF4021V
Rt	1	39.2K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF3922V
Rpg	1	10K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF1002V
U1	1	IR3846	PQFN 5x7mm	International Rectifier	IR3846MPBF

EXTERNALLY BIASED SINGLE SUPPLY

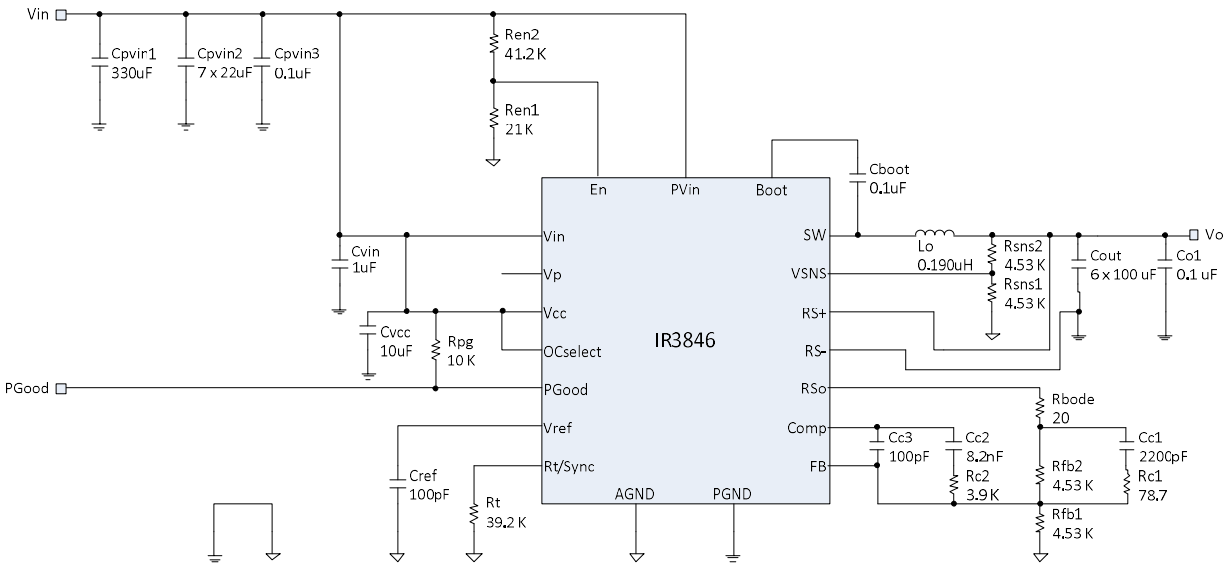


Figure 39: Application circuit for a 5V to 1.2V, 25A Point of Load Converter

Suggested bill of material for application circuit 5V to 1.2V

Part Reference	Qty	Value	Description	Manufacturer	Part Number
Cpvin1	1	330uF	SMD, electrolytic, 25V, 20%	Panasonic	EEV-FK1E331P
Cpvin2	7	22uF	1206, 25V, X5R, 10%	Murata	GRM31CR61E226KE15L
Cref	1	100pF	0603, 50V, C0G, 5%	Murata	GRM1885C1H101JA01D
Cvin	1	1.0uF	0603, 25V, X5R, 20%	Murata	GRM188R61E105KA12D
Cvcc	1	10uF	0603, 10V, X5R, 20%	TDK	C1608X5R1A106M
Cpvin3 Cboot Co1	3	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01D
Cc1	1	2200pF	0603, 50V, X7R, 10%	Murata	GRM188R71H222KA01D
Cc2	1	8.2nF	0603, 50V, X7R, 10%	Murata	GRM188R71H822KA01D
Cc3	1	100pF	0603, 50V, NPO, 5%	Murata	GRM1885C1H101JA01D
Cout1	6	100uF	1206, 6.3V, X5R, 20%	Murata	GRM31CR60J107ME39L
L0	1	0.190uH	10x6.8x7.3mm, DCR=0.20mΩ	Inter-Technical,LLC	SL40307A-R19KHF
Rbd	1	20	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF20R0V
Rc1	1	78.7	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF78R7V
Rc2	1	3.9K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF3901V
Ren1	1	21K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF2102V
Ren2	1	41.2K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF4122V
Rfb1 Rfb2 Rsns1Rsns1	4	4.53K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF4531V
Rt	1	39.2K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF3922V
Rpg	1	10K	Thick Film, 0603, 1/10W, 1%	Panasonic	ERJ-3EKF1002V
U1	1	IR3846	PQFN 5x7mm	International Rectifier	IR3846MPBF

TYPICAL OPERATING WAVEFORMS

Vin=PVin=12V, Vout=1.2V, Iout=0-35A, Fs=600kHz, Room Temperature, No Air Flow

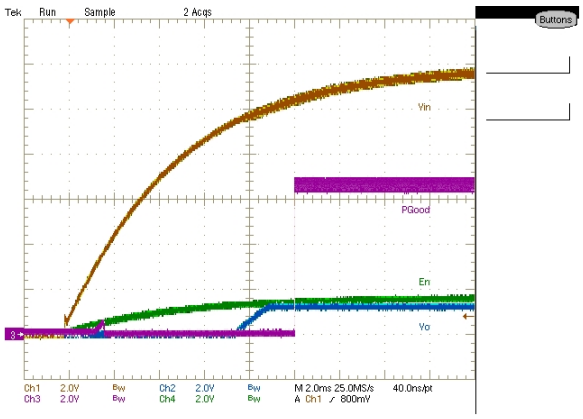


Figure 40: Startup with full load, Enable Signal
CH1:Vin, CH2:Vout, CH3:PGood, CH4:Enable

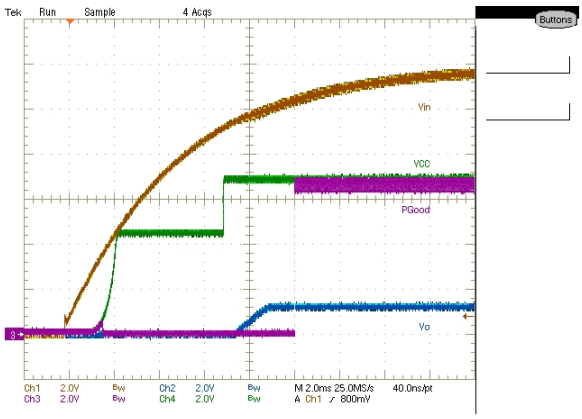


Figure 41: Startup with full load, VCC signal
CH1:Vin, CH2:Vout, CH3:PGood, CH4:VCC

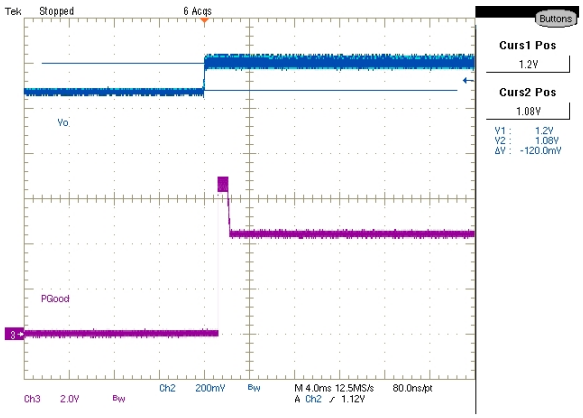


Figure 42: Vout Startup with Pre-Bias, 1.08V
Ch2:Vout, CH3:PGood

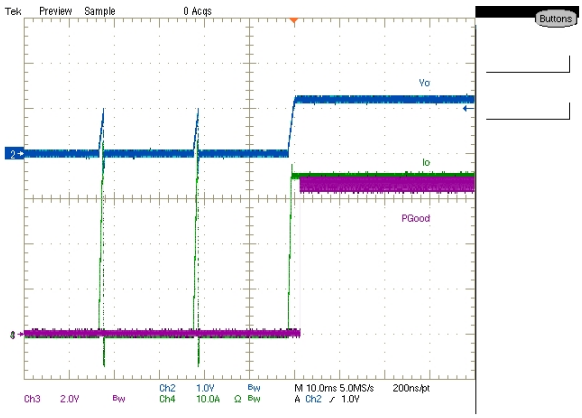


Figure 43: Recovery from Hiccup
CH2:Vout, CH3:PGood, CH4:Iout

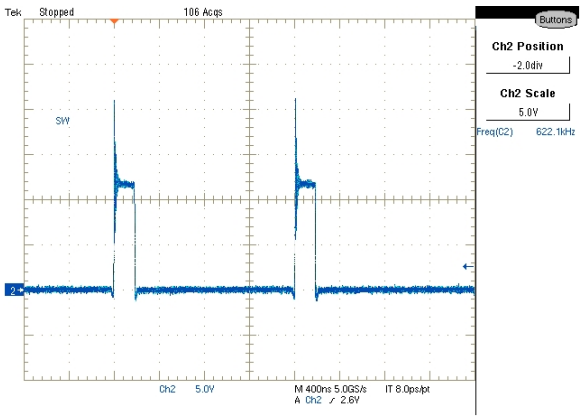


Figure 44: Inductor Switch Node at full load
CH2:SW

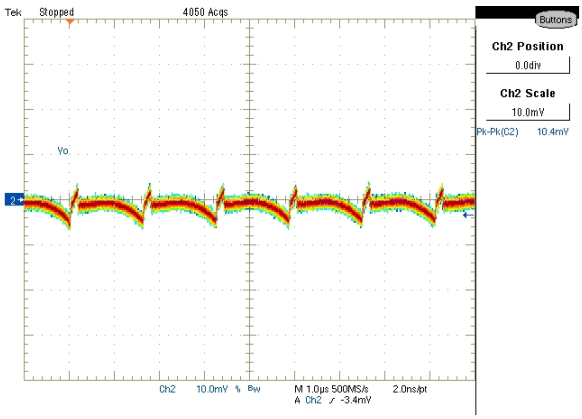


Figure 45: Output Voltage Ripple at full load
CH2:Vout

TYPICAL OPERATING WAVEFORMS

Vin=PVin=12V, Vout=1.2V, Iout=3.5-14A, Fs=600kHz, Room Temperature, No air flow

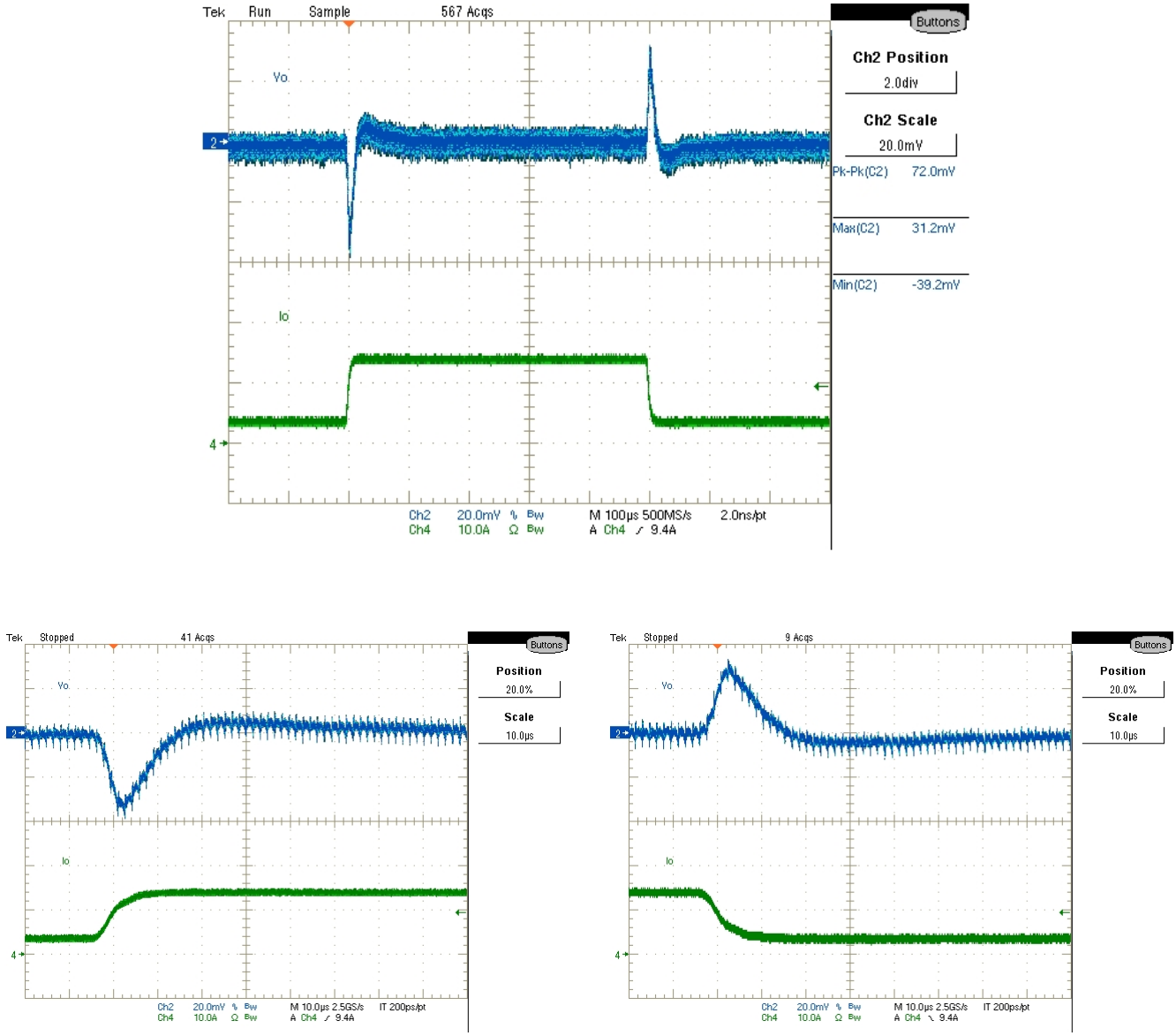


Figure 46: Vout Transient Response, 3.5A to 14.0A step at 2.5A/uSec
CH2:Vout, CH4:Iout

TYPICAL OPERATING WAVEFORMS

Vin=PVin=12V, Vout=1.2V, Iout=24.5-35A, Fs=600kHz, Room Temperature, No air flow

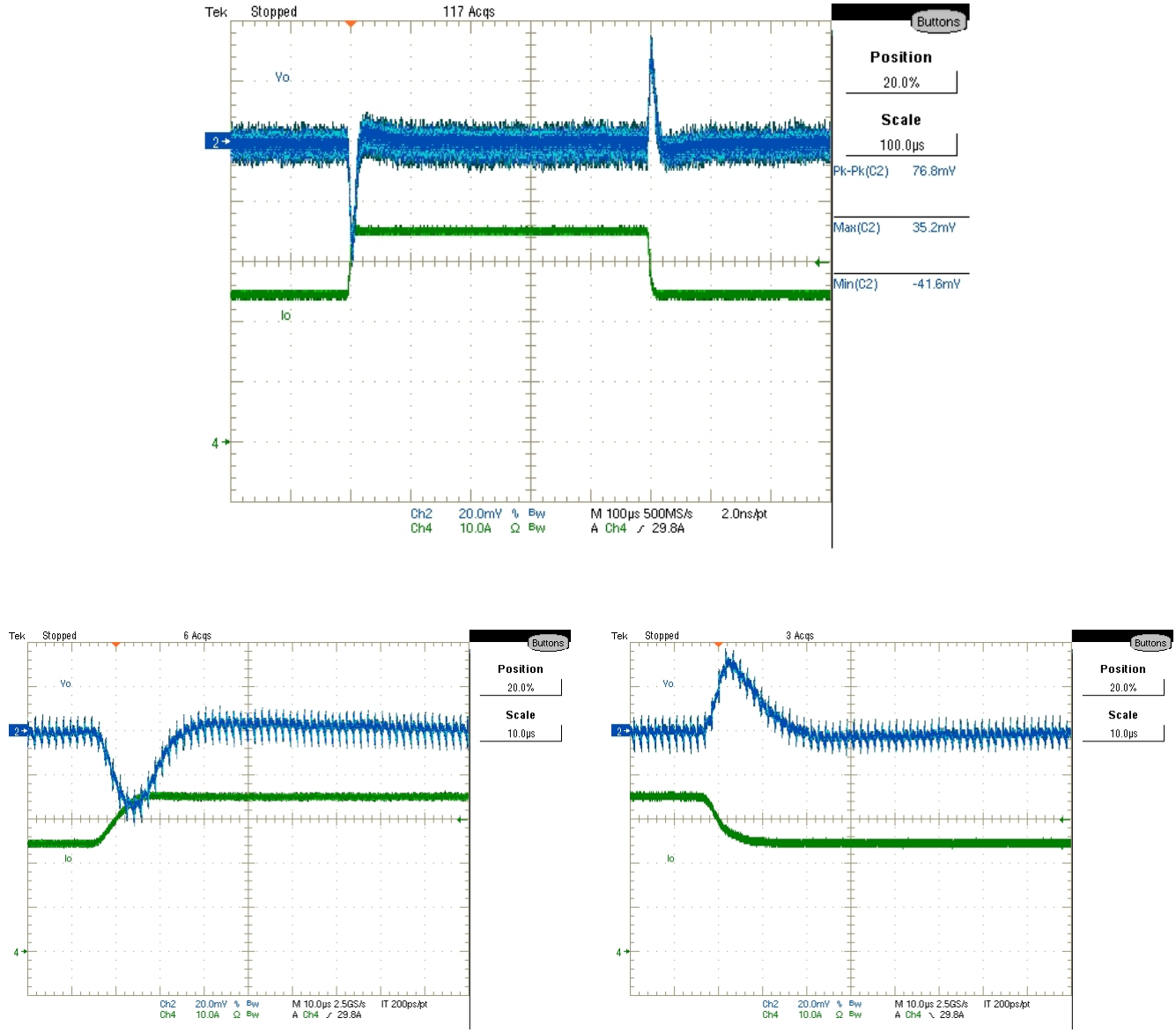
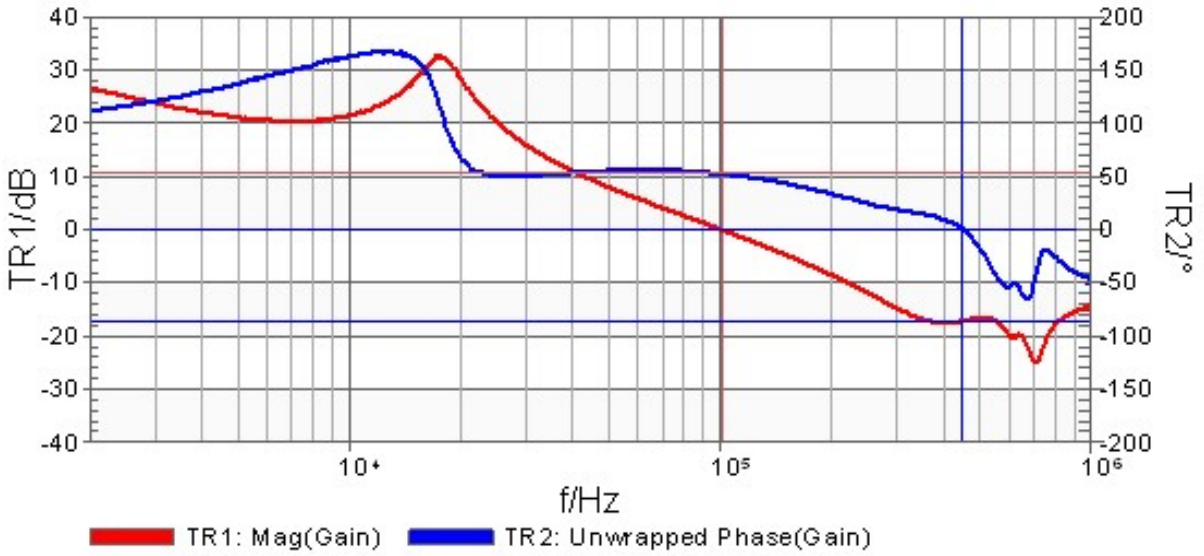


Figure 47: Vout Transient Response, 24.5A to 35A step at 2.5A/uSec
CH2:Vout, CH4:Iout

TYPICAL OPERATING WAVEFORMS

Vin=PVin=12V, Vout=1.2V, Iout=35A, Fs=600kHz, Room Temperature, No air flow



	Frequency	Trace1	Trace2
Cursor 1	100.624 kHz	0.000 dB	52.477 °
Cursor 2	451.686 kHz	-17.230 dB	0.000 °
Delta C2-C1	351.062 kHz	-17.230 dB	-52.477 °

Figure 48: Bode Plot with 35A load: Fo = 100.6 kHz, Phase Margin = 52.5 Degrees

TYPICAL OPERATING WAVEFORMS

Vin=PVin=12V, Vout=1.2V, Iout=0-35A, Fs=600kHz, Room Temperature, No air flow

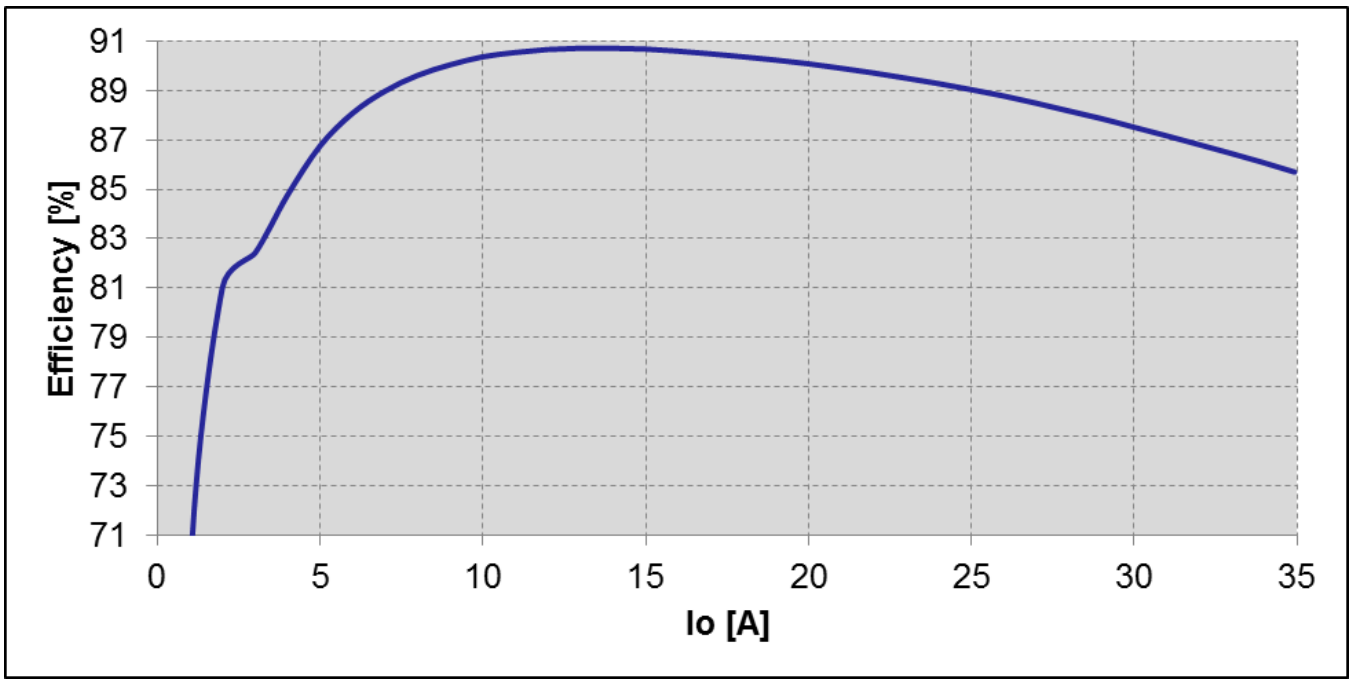


Figure 49: Efficiency versus load current

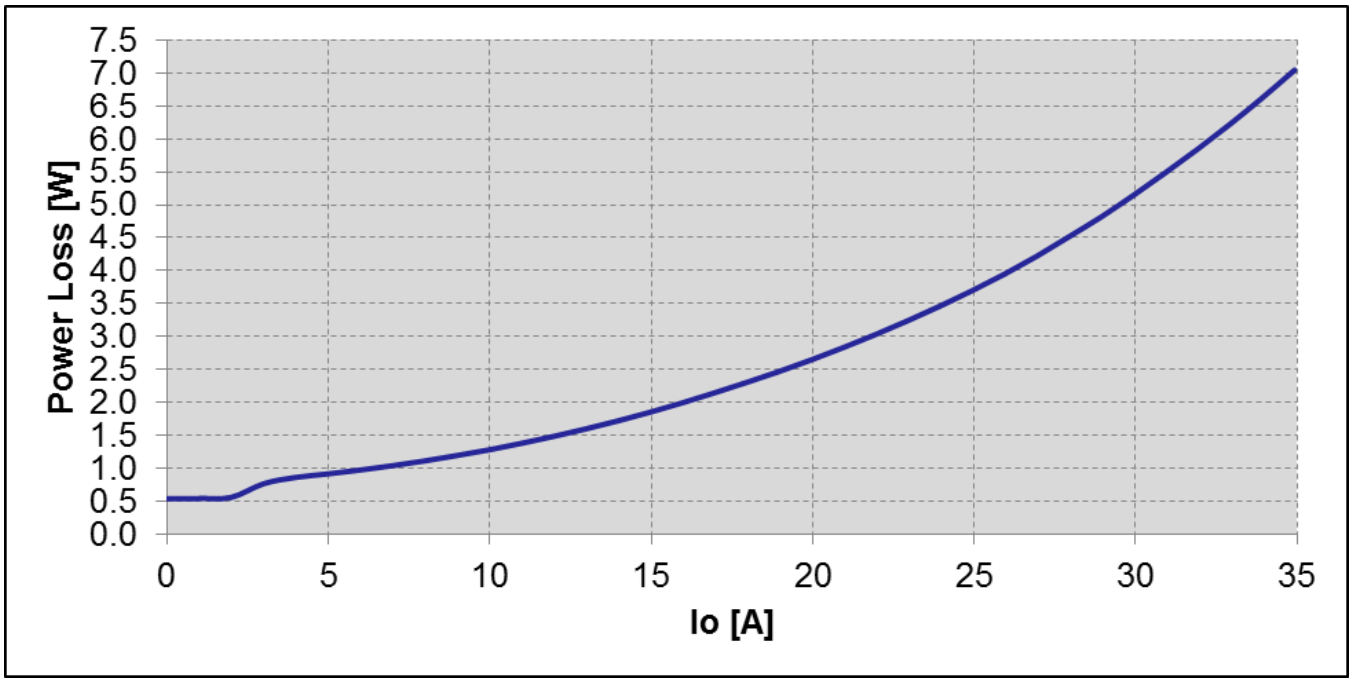


Figure 50: Power Loss versus load current

LAYOUT RECOMMENDATIONS

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, input capacitors, output capacitors and the IR3846 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR3846.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for PVin, Vin and VCC should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use at least one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 6-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. Figure 51a-f illustrates the implementation of the layout guidelines outlined above, on the IRDC3846 6-layer demo board.

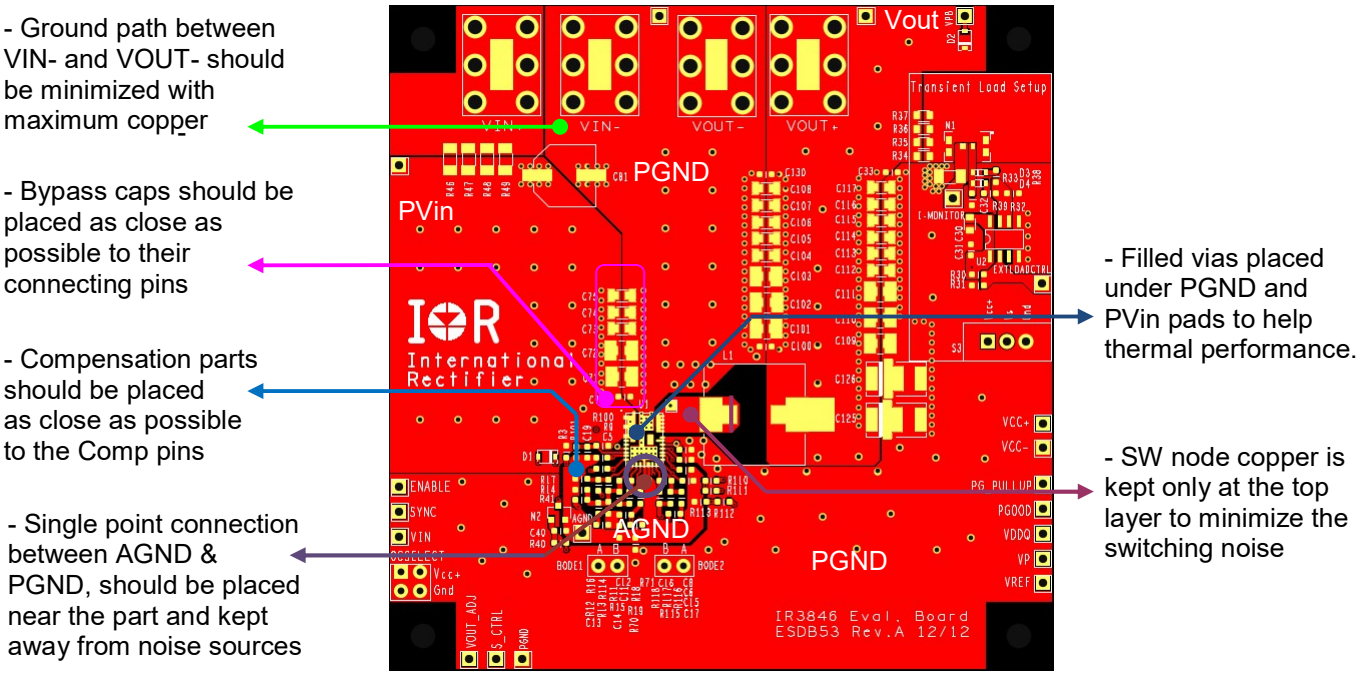


Figure 51a: IRDC3846 Demo board Layout Considerations – Top Layer

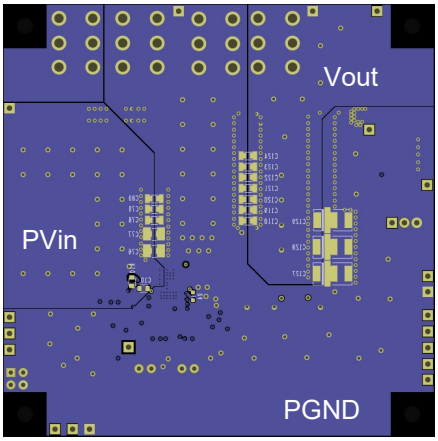


Figure 51b: IRDC3846 Demo board Layout Considerations – Bottom Layer

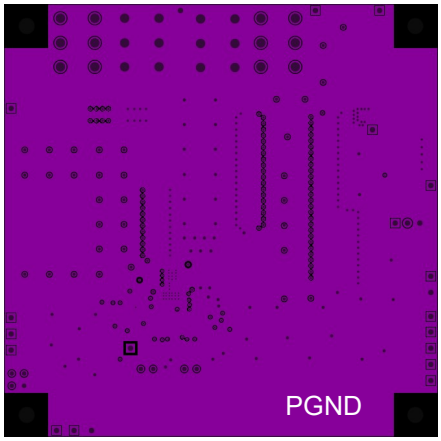


Figure 51c: IRDC3846 Demo board Layout Considerations – Mid Layer 1

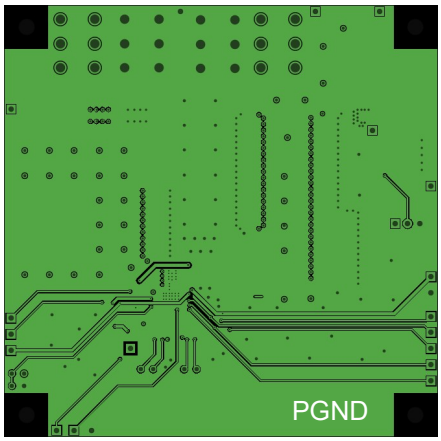


Figure 51d: IRDC3846 Demo board Layout Considerations – Mid Layer 2

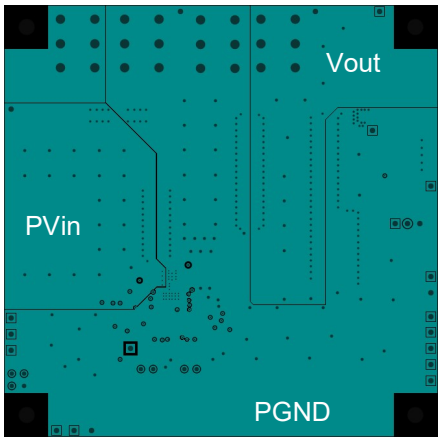


Figure 51e: IRDC3846 Demo board Layout Considerations – Mid Layer 3

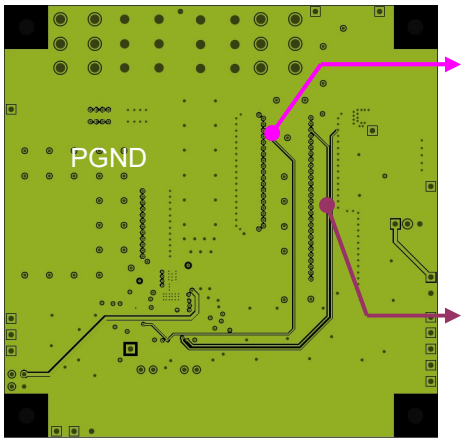
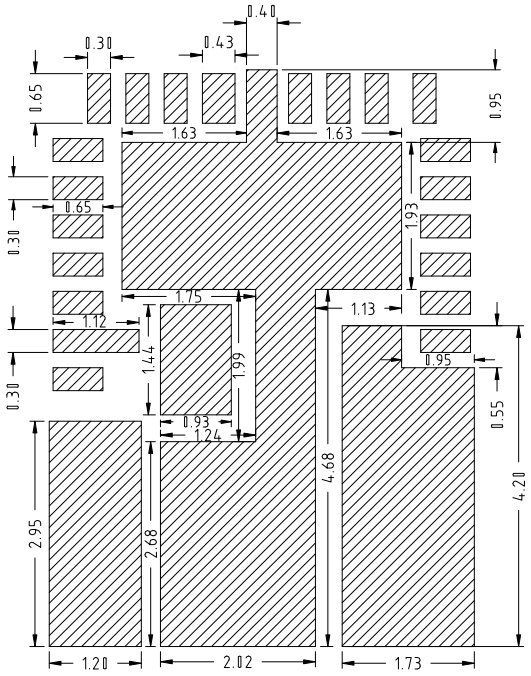


Figure 51f: IRDC3846 Demo board Layout Considerations – Mid Layer 4

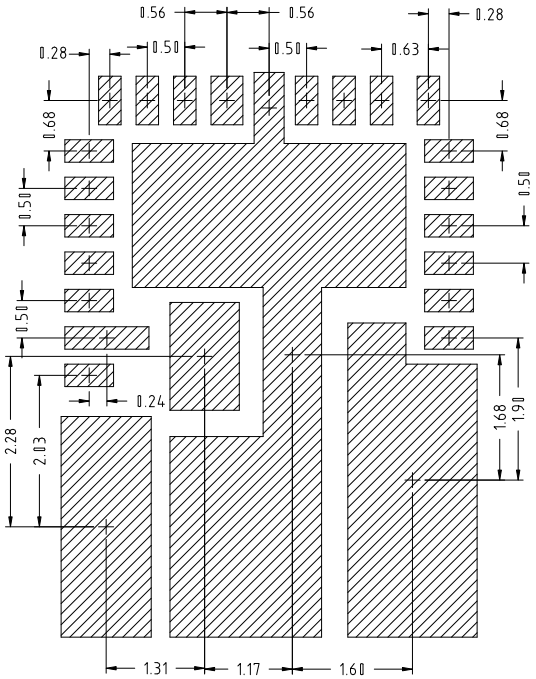
PCB METAL AND COMPONENT PLACEMENT

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes. For further information, please refer to “SupIRBuck® Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note.” **(AN1132)**

PAD SIZES



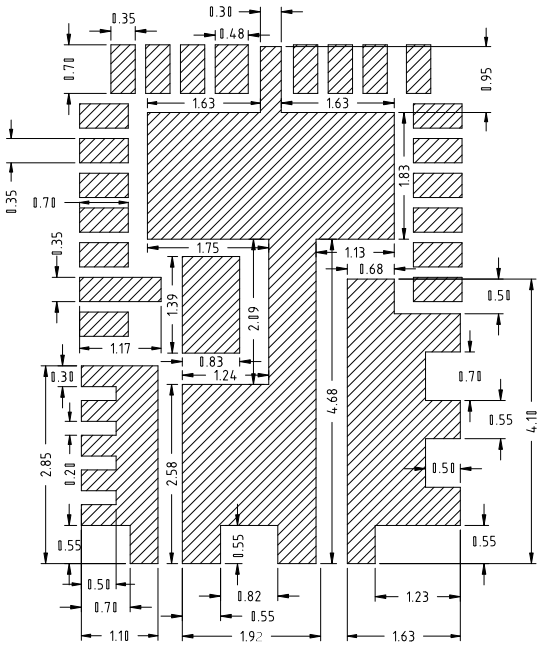
PCB SPACING



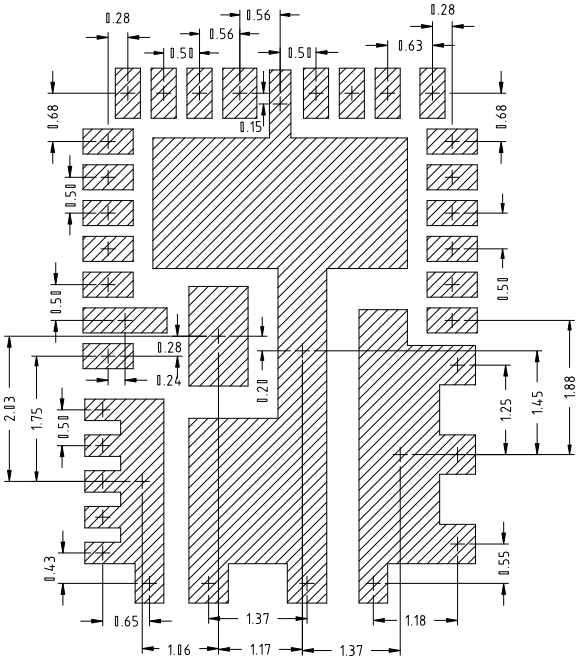
SOLDER RESIST

- IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD). This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.
- When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y).
- However, for the smaller Signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined or Copper Defined.
- When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X & Y), in order to accommodate any layer to layer misalignment.
- Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.

PAD SIZES



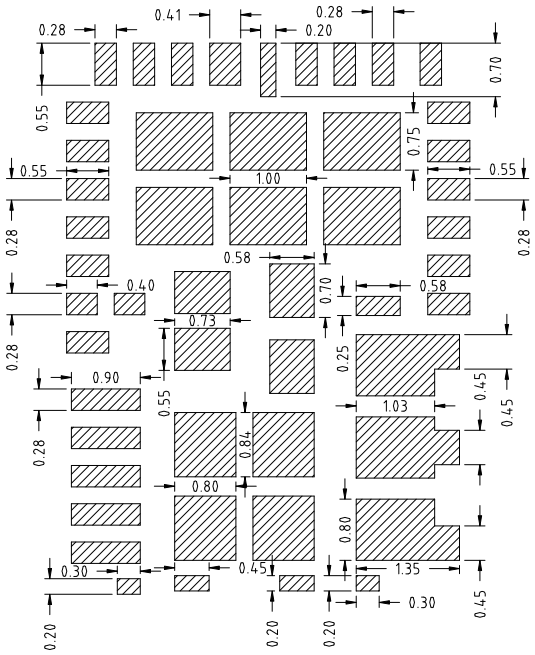
PAD SPACING



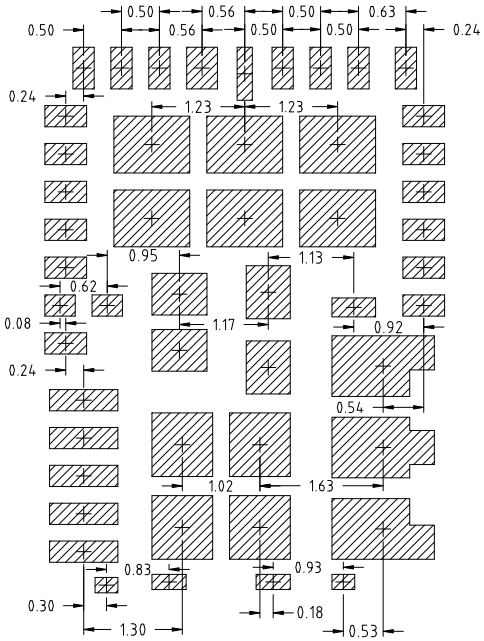
STENCIL DESIGN

- Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.
- Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

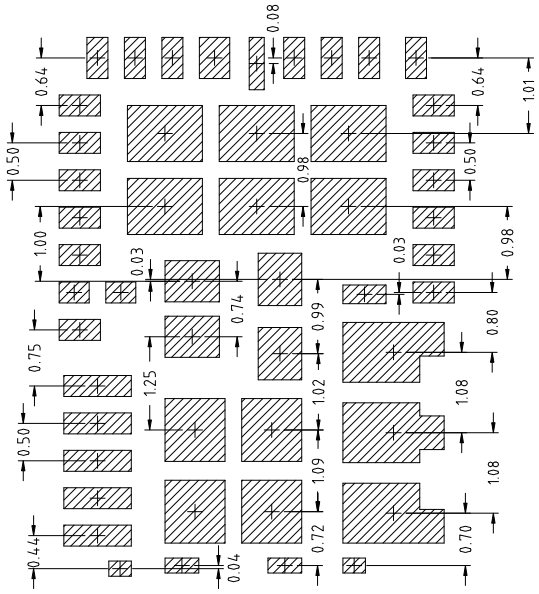
SOLDER PASTE STENCIL PAD SIZES



SOLDER PASTE STENCIL PAD SPACING (DETAIL 1)



SOLDER PASTE STENCIL PAD SPACING (DETAIL 2)



MARKING INFORMATION

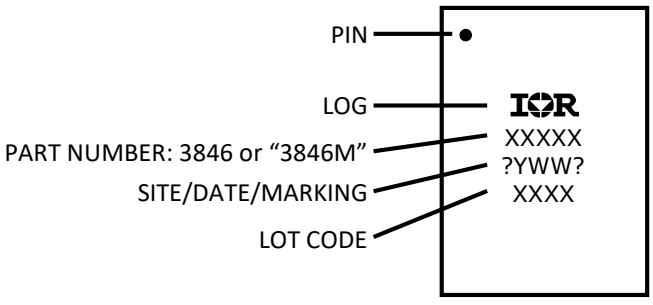
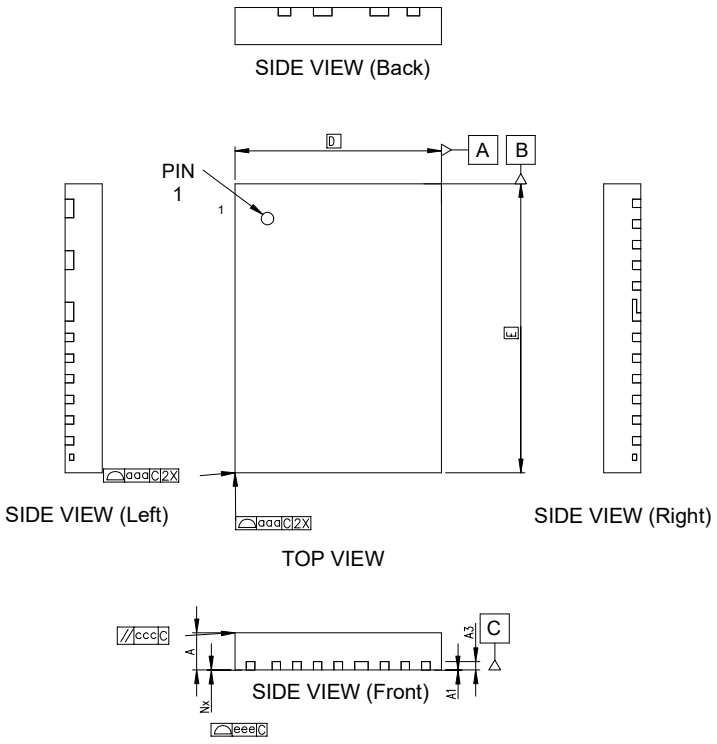
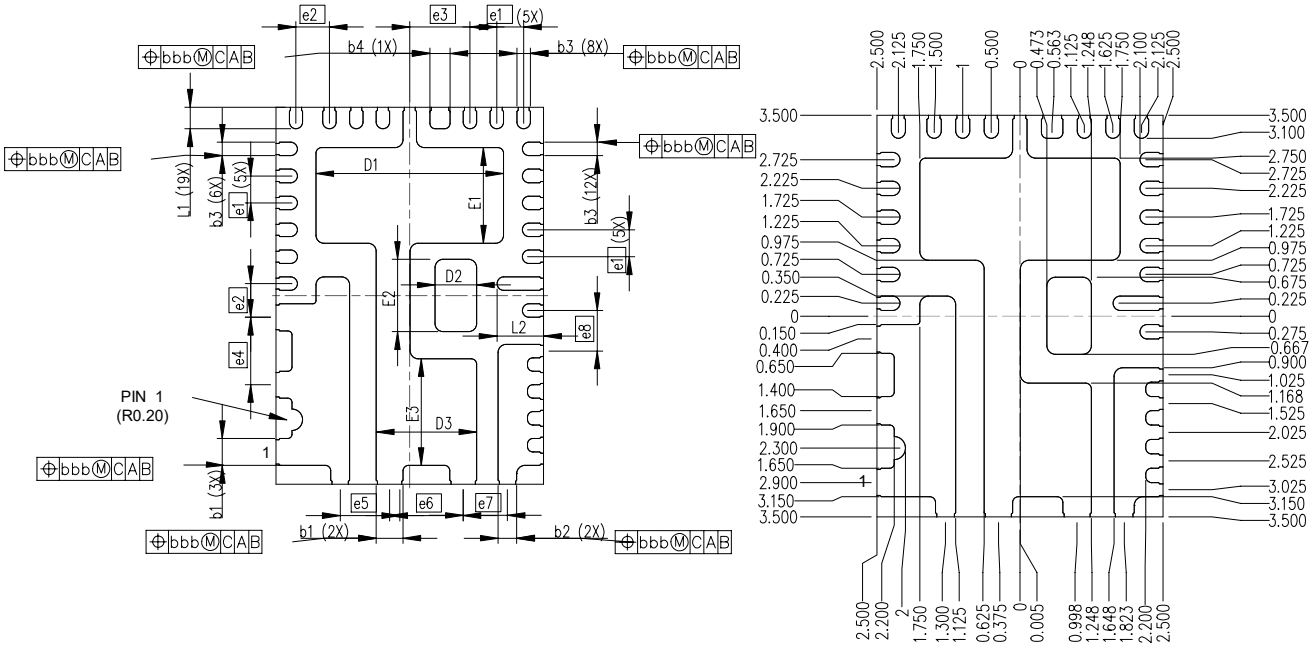


Figure 52: Marking Information

PACKAGING INFORMATION



DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.203 Ref	
b1	0.45	0.50	0.55
b2	0.30	0.35	0.40
b3	0.20	0.25	0.30
b4	0.325	0.375	0.425
D		5.00 BSC	
E		7.00 BSC	
D1	3.450	3.500	3.550
E1	1.725	1.775	1.825
D2	0.725	0.775	0.825
E2	1.292	1.342	1.392
D3	1.823	1.873	1.923
E3	1.932	1.982	2.032
L1	0.35	0.40	0.45
L2	0.822	0.872	0.922
e1		0.500 BSC	
e2		0.625 BSC	
e3		1.125 BSC	
e4		1.250 BSC	
e5		0.925 BSC	
e6		1.373 BSC	
e7		0.825 BSC	
e8		0.750 BSC	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		34	



ENVIRONMENTAL QUALIFICATIONS

Qualification Level		Industrial	
Moisture Sensitivity Level		5mm x 7mm PQFN	MSL3
ESD	Machine Model (JESD22-A115A)	Class A	
		<200V	
	Human Body Model (JESD22-A114F)	Class 1C	
		≥1000V to <2000V	
	Charged Device Model (JESD22-C101D)	Class III	
		≥500V to ≤1000V	
RoHS Compliant		Yes	

REVISION HISTORY

Rev.	Date	Description
3.0	8/1/2013	Initial DR3 Release
3.1	10/3/2013	Correct typos and equation Added thermal derating data
3.2	4/16/2014	Update ordering options Correct typos
3.3	11/19/2014	Change MSL Correct packaging information Correct block diagram Correct typos
3.4	11/6/2015	Correct package marking Correct package drawings
3.5	2/5/2016	Update POD, converted to Infineon format
3.6	9/30/2016	Update ABS Max Ratings
3.7	3/3/2017	Add Pre-bias limit information in Pre-Bias startup section Add PGood Back-Bias information into PGood section
3.8	3/5/2020	Update package marking Update MSL to Level 3 from Level 2

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