

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-205AF)

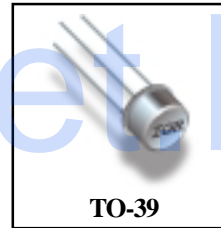
IRFF110
JANTX2N6782
JANTXV2N6782
REF:MIL-PRF-19500/556
100V, N-CHANNEL

Product Summary

| Part Number | BVDSS | RDS(on) | ID |
|-------------|-------|---------|------|
| IRFF110 | 100V | .60Ω | 3.5A |

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.



TO-39

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

| | Parameter | | Units |
|----------------------------|---------------------------------|-------------------------------------------|-------|
| ID @ VGS = 10V, TC = 25°C | Continuous Drain Current | 3.5 | A |
| ID @ VGS = 10V, TC = 100°C | Continuous Drain Current | 2.25 | |
| IDM | Pulsed Drain Current ① | 14 | |
| PD @ TC = 25°C | Max. Power Dissipation | 15 | W |
| | Linear Derating Factor | 0.12 | W/°C |
| VGS | Gate-to-Source Voltage | ±20 | V |
| EAS | Single Pulse Avalanche Energy ② | 68 | mJ |
| IAR | Avalanche Current ① | — | A |
| EAR | Repetitive Avalanche Energy ① | — | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.5 | V/ns |
| TJ | Operating Junction | -55 to 150 | °C |
| TSTG | Storage Temperature Range | | |
| | Lead Temperature | 300 (0.063 in. (1.6mm) from case for 10s) | |
| | Weight | 0.98(typical) | g |

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------------------------|----------------------------------------------|-----|------|------|-------|-----------------------------------------------------------------------------------------------|
| BV _{DSS} | Drain-to-Source Breakdown Voltage | 100 | — | — | V | V _{GS} = 0V, I _D = 1.0mA |
| ΔBV _{DSS} /ΔT _J | Temperature Coefficient of Breakdown Voltage | — | 0.10 | — | V/°C | Reference to 25°C, I _D = 1.0mA |
| R _{DS(on)} | Static Drain-to-Source On-State Resistance | — | — | 0.60 | Ω | V _{GS} = 10V, I _D = 2.25A ④ |
| | | — | — | 0.69 | | V _{GS} = 10V, I _D = 3.5A ④ |
| V _{GS(th)} | Gate Threshold Voltage | 2.0 | — | 4.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Transconductance | 0.8 | — | — | S (Ω) | V _{DS} > 15V, I _{DS} = 2.25A ④ |
| I _{DSS} | Zero Gate Voltage Drain Current | — | — | 25 | μA | V _{DS} = 80V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 80V V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Leakage Forward | — | — | 100 | nA | V _{GS} = 20V |
| I _{GSS} | Gate-to-Source Leakage Reverse | — | — | -100 | | V _{GS} = -20V |
| Q _g | Total Gate Charge | 4.1 | — | 6.5 | nC | V _{GS} = 10V, I _D = 3.5A |
| Q _{gs} | Gate-to-Source Charge | 0.4 | — | 1.6 | | V _{DS} = 50V |
| Q _{gd} | Gate-to-Drain ('Miller') Charge | 1.4 | — | 3.5 | | |
| t _{d(on)} | Turn-On Delay Time | — | — | 15 | | |
| t _r | Rise Time | — | — | 25 | ns | V _{DD} = 50V, I _D = 3.5A, R _G = 7.5Ω |
| t _{d(off)} | Turn-Off Delay Time | — | — | 25 | | |
| t _f | Fall Time | — | — | 20 | | |
| L _S + L _D | Total Inductance | — | 7.0 | — | nH | Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package) |
| C _{iss} | Input Capacitance | — | 180 | — | pF | V _{GS} = 0V, V _{DS} = 25V |
| C _{oss} | Output Capacitance | — | 82 | — | | f = 1.0MHz |
| C _{rss} | Reverse Transfer Capacitance | — | 15 | — | | |

Source-Drain Diode Ratings and Characteristics

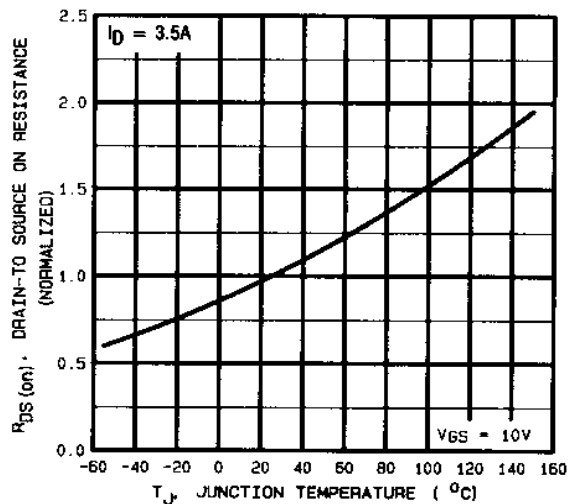
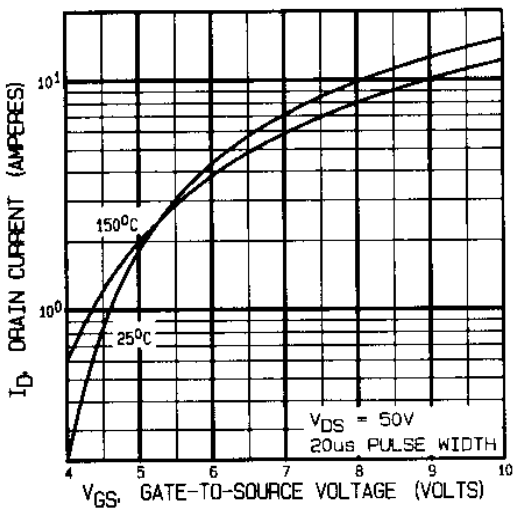
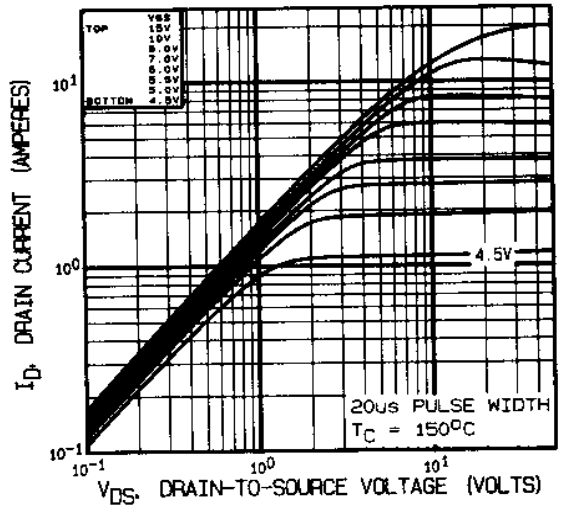
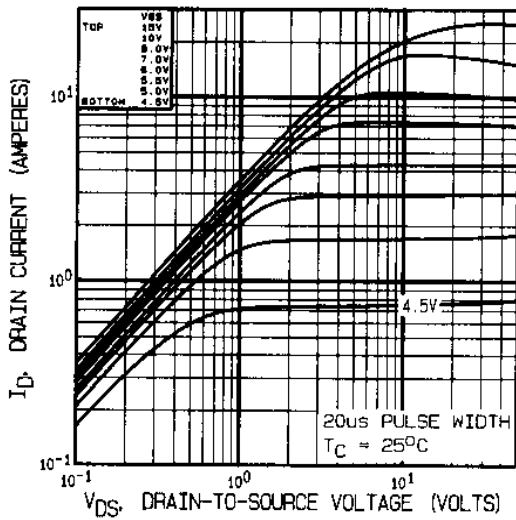
| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-----------------|----------------------------------------|----------------------------------------------------------------------------------------------------------------------|-----|-----|-------|----------------------------------------------------------------------|
| I _S | Continuous Source Current (Body Diode) | — | — | 3.5 | A | |
| I _{SM} | Pulse Source Current (Body Diode) ① | — | — | 14 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.5 | V | T _j = 25°C, I _S = 3.5A, V _{GS} = 0V ④ |
| t _{rr} | Reverse Recovery Time | — | — | 180 | nS | T _j = 25°C, I _F = 3.5A, di/dt ≤ 100A/μs |
| Q _{RR} | Reverse Recovery Charge | — | — | 2.0 | μC | V _{DD} ≤ 50V ④ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D . | | | | |

Thermal Resistance

| | Parameter | Min | Typ | Max | Units | Test Conditions |
|-------------------|---------------------|-----|-----|-----|-------|-----------------------|
| R _{thJC} | Junction-to-Case | — | — | 8.3 | °C/W | |
| R _{thJA} | Junction-to-Ambient | — | — | 175 | | Typical socket mount. |

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page



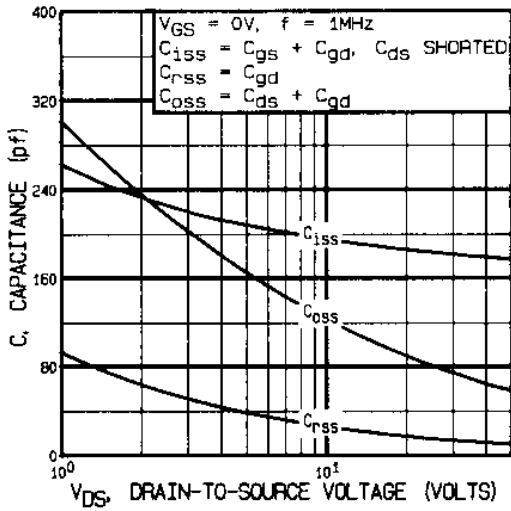


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

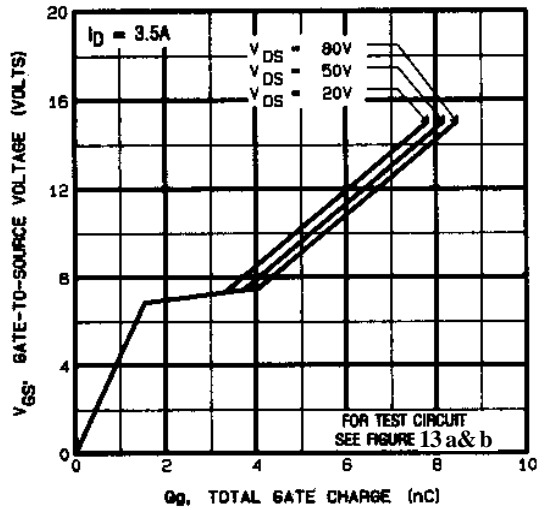


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

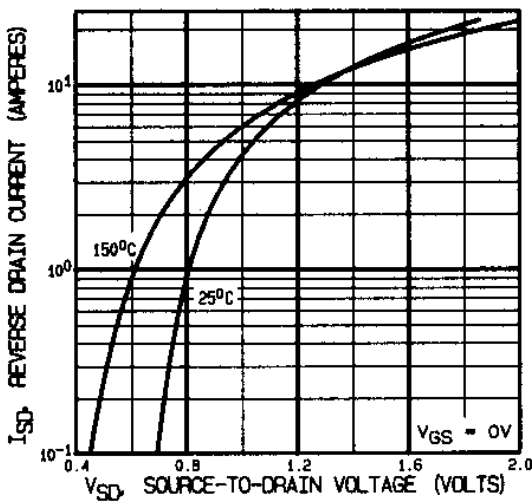


Fig 7. Typical Source-Drain Diode Forward Voltage

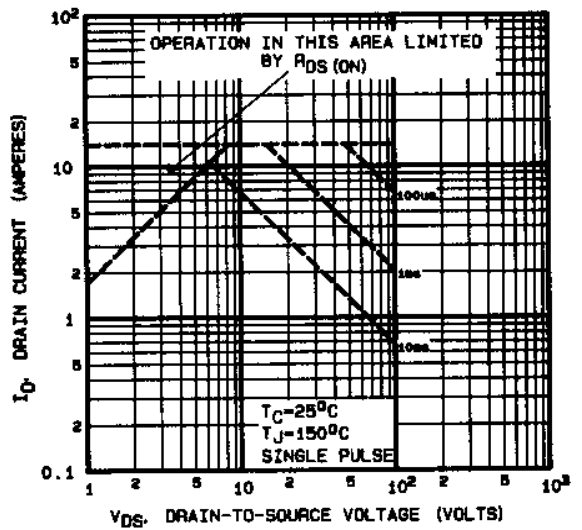


Fig 8. Maximum Safe Operating Area

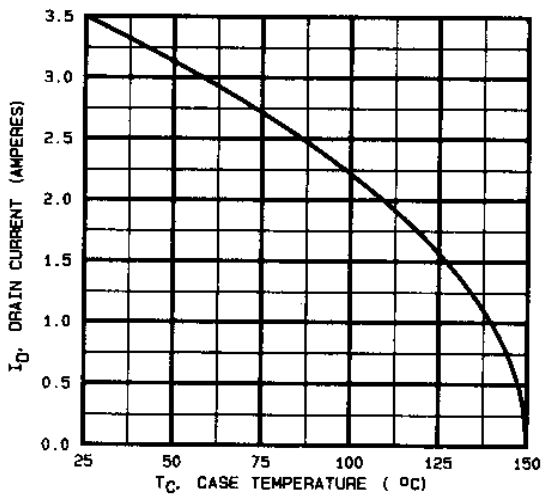


Fig9. Maximum Drain Current Vs. Case Temperature

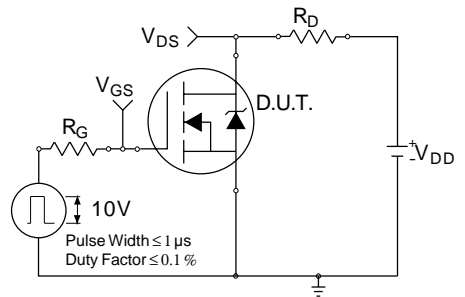


Fig 10a. Switching Time Test Circuit

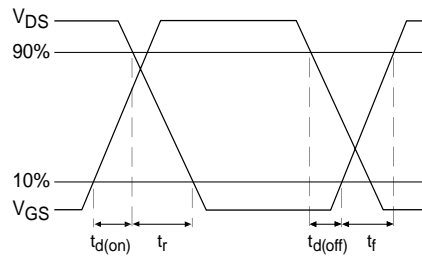


Fig 10b. Switching Time Waveforms

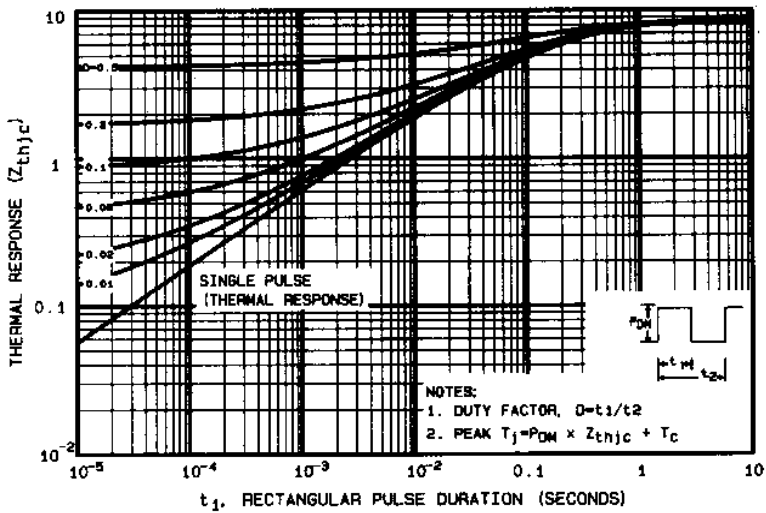


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

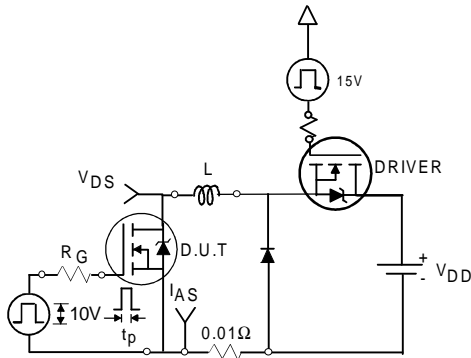


Fig 12a. Unclamped Inductive Test Circuit

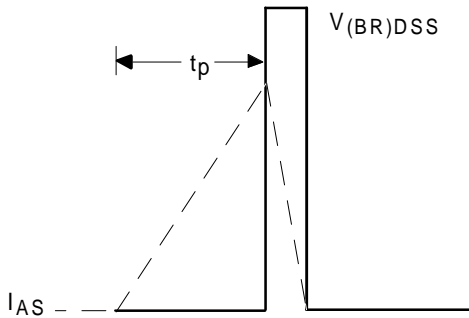


Fig 12b. Unclamped Inductive Waveforms

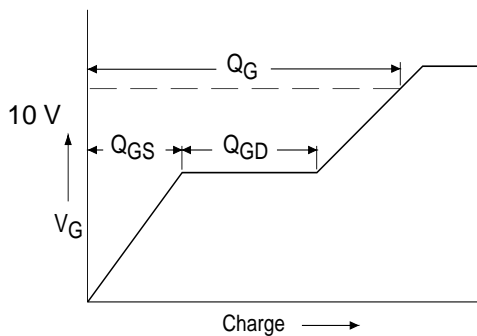


Fig 13a. Basic Gate Charge Waveform

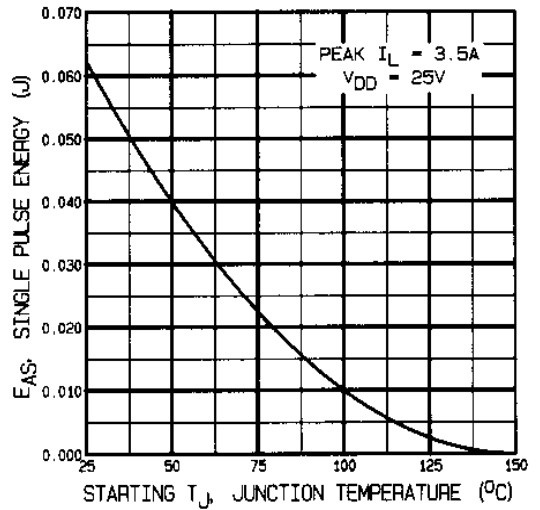


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

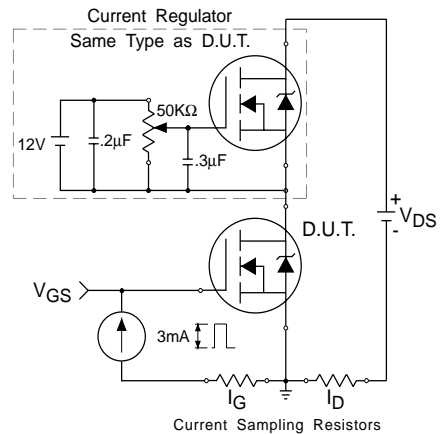
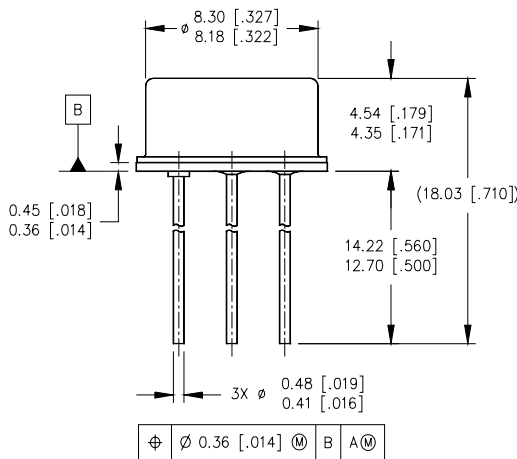


Fig 13b. Gate Charge Test Circuit

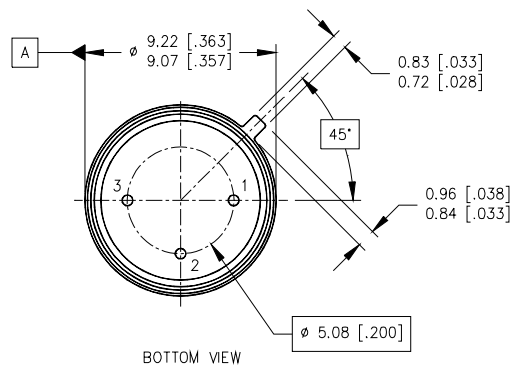
Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^{\circ}C$,
 Peak $I_L = 3.5A$,
- ③ $I_{SD} \leq 3.5A$, $di/dt \leq 75A/\mu s$,
 $V_{DD} \leq 100V$, $T_J \leq 150^{\circ}C$
 Suggested $R_G = 7.5 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-205AF



SIDE VIEW



BOTTOM VIEW

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. CONTROLLING DIMENSION: INCH.
- 4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN