

**High Speed CMOS Logic
8-Input NAND Gate**
Features

- Buffered Inputs
- Typical Propagation Delay: 10ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC30 and 'HCT30 each contain an 8-input NAND gate in one package. They provide the system designer with the direct implementation of the positive logic 8-input NAND function. Logic gates utilize silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The HCT logic family is functionally pin compatible with the standard LS logic family.

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|--------------|------------------|--------------|
| CD54HC30F3A | -55 to 125 | 14 Ld CERDIP |
| CD54HCT30F3A | -55 to 125 | 14 Ld CERDIP |
| CD74HC30E | -55 to 125 | 14 Ld PDIP |
| CD74HC30M | -55 to 125 | 14 Ld SOIC |
| CD74HC30MT | -55 to 125 | 14 Ld SOIC |
| CD74HC30M96 | -55 to 125 | 14 Ld SOIC |
| CD74HC30NSR | -55 to 125 | 14 Ld SOP |
| CD74HC30PW | -55 to 125 | 14 Ld TSSOP |
| CD74HC30PWR | -55 to 125 | 14 Ld TSSOP |
| CD74HC30PWT | -55 to 125 | 14 Ld TSSOP |
| CD74HCT30E | -55 to 125 | 14 Ld PDIP |
| CD74HCT30M | -55 to 125 | 14 Ld SOIC |
| CD74HCT30MT | -55 to 125 | 14 Ld SOIC |
| CD74HCT30M96 | -55 to 125 | 14 Ld SOIC |

Pinout

CD54HC30, CD54HCT30 (CERDIP)
 CD74HC30 (PDIP, SOIC, SOP, TSSOP)
 CD74HCT30 (PDIP, SOIC)
 TOP VIEW



NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

| INPUTS | | | | | | | | OUTPUT |
|--------|---|---|---|---|---|---|---|--------|
| A | B | C | D | E | F | G | H | |
| L | X | X | X | X | X | X | X | H |
| X | L | X | X | X | X | X | X | H |
| X | X | L | X | X | X | X | X | H |
| X | X | X | L | X | X | X | X | H |
| X | X | X | X | L | X | X | X | H |
| X | X | X | X | X | L | X | X | H |
| X | X | X | X | X | X | L | X | H |
| X | X | X | X | X | X | X | L | H |
| H | H | H | H | H | H | H | H | L |

NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Irrelevant

Logic Symbol



CD54/74HC30, CD54/74HCT30

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Operating Conditions

| | |
|--|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

Thermal Information

| | |
|--|----------------|
| Package Thermal Impedance, θ_{JA} (see Note 1) | |
| E (PDIP) Package | 80°C/W |
| M (SOIC) Package | 86°C/W |
| NS (SOP) Package | 76°C/W |
| PW (TSSOP) Package | 113°C/W |
| Maximum Junction Temperature (Hermetic Package or Die) . . . | 175°C |
| Maximum Junction Temperature (Plastic Package) | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |
| (SOIC - Lead Tips Only) | |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|----------|-------------------------|------------|--------------|------|-----|-----------|----------------|---------|----------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |

CD54/74HC30, CD54/74HCT30

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|------------------------------------|---------------------|---------------------|------|-----|------|----------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 6 | - | - | 2 | - | 20 | - | 40 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | -0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | - | 5.5 | - | | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 2 | - | 20 | - | 40 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 2) | ΔI _{CC} | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|-------|------------|
| All | 0.6 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay, Input to Output (Figure 1) | t _{pLH} , t _{pHL} | C _L = 50pF | 2 | - | - | 130 | - | 165 | - | 195 | ns |
| | | | 4.5 | - | - | 26 | - | 33 | - | 39 | ns |
| | | | 6 | - | - | 22 | - | 28 | - | 33 | ns |
| Propagation Delay, Data Input to Output Y | t _{pLH} , t _{pHL} | C _L = 15pF | 5 | - | 10 | - | - | - | - | ns | |

CD54/74HC30, CD54/74HCT30

Switching Specifications Input $t_r, t_f = 6\text{ ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|--------------------|----------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Transition Times (Figure 1) | t_{TLH}, t_{THL} | $C_L = 50\text{ pF}$ | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Input Capacitance | C_I | - | - | - | 10 | - | 10 | - | 10 | pF | |
| Power Dissipation Capacitance (Notes 3, 4) | C_{PD} | - | 5 | - | 25 | - | - | - | - | pF | |
| HCT TYPES | | | | | | | | | | | |
| Propagation Delay, Input to Output (Figure 2) | t_{RHL}, t_{PHL} | $C_L = 50\text{ pF}$ | 4.5 | - | - | 28 | - | 35 | - | 42 | ns |
| Propagation Delay, Data Input to Output Y | t_{PLH}, t_{PHL} | $C_L = 15\text{ pF}$ | 5 | - | 11 | - | - | - | - | - | ns |
| Transition Times (Figure 2) | t_{TLH}, t_{THL} | $C_L = 50\text{ pF}$ | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Input Capacitance | C_I | - | - | - | 10 | - | 10 | - | 10 | pF | |
| Power Dissipation Capacitance (Notes 3, 4) | C_{PD} | - | 5 | - | 26 | - | - | - | - | pF | |

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per gate.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-8974601CA | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type |
| 8404001CA | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type |
| CD54HC30F | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type |
| CD54HC30F3A | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type |
| CD54HCT30F3A | ACTIVE | CDIP | J | 14 | 1 | TBD | Call TI | N / A for Pkg Type |
| CD74HC30E | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC30EE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HC30M | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30M96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30M96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30ME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30MT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30MTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30NSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30PW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30PWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30PWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30PWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30PWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HC30PWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT30E | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT30EE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| CD74HCT30M | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT30M96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT30M96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT30ME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CD74HCT30MT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CD74HCT30MTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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