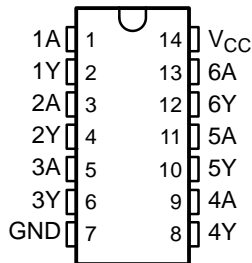


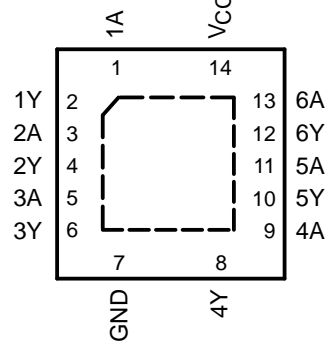
FEATURES

- Operate From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max t_{pd} of 2.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

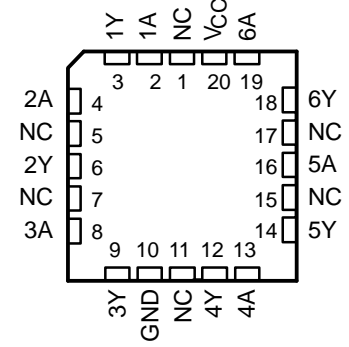
SN54LVC07A . . . J OR W PACKAGE
SN74LVC07A . . . D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC07A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC07A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

These hex buffers/drivers are designed for 1.65-V to 5.5-V V_{CC} operation.

The outputs of the 'LVC07A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of these devices as translators in a mixed-system environment.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC07ARGYR	LC07A
		Tube of 50	SN74LVC07AD	LVC07A
	SOIC – D	Reel of 2500	SN74LVC07ADR	
		Reel of 250	SN74LVC07ADT	
	SOP – NS	Reel of 2000	SN74LVC07ANSR	LVC07A
	SSOP – DB	Reel of 2000	SN74LVC07ADBR	LC07A
	TSSOP – PW	Tube of 90	SN74LVC07APW	LC07A
		Reel of 2000	SN74LVC07APWR	
Reel of 250		SN74LVC07APWT		
TVSOP – DGV	Reel of 2000	SN74LVC07ADGVR	LC07A	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC07AJ	SNJ54LVC07AJ
	CFP – W	Tube of 150	SNJ54LVC07AW	SNJ54LVC07AW
	LCCC – FK	Tube of 55	SNJ54LVC07AFK	SNJ54LVC07AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

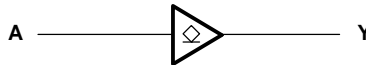


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLE
 (EACH BUFFER/DRIVER)**

INPUT A	OUTPUT Y
H	H
L	L

LOGIC DIAGRAM, EACH BUFFER/DRIVER (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	6.5	V
V_I	Input voltage range ⁽²⁾	-0.5	6.5	V
V_O	Output voltage range	-0.5	6.5	V
I_{IK}	Input clamp current		-50	mA
I_{OK}	Output clamp current		-50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance	D package ⁽³⁾	86	°C/W
		DB package ⁽³⁾	96	
		DGV package ⁽³⁾	127	
		NS package ⁽³⁾	76	
		PW package ⁽³⁾	113	
		RGY package ⁽⁴⁾	47	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾

		SN54LVC07A ⁽²⁾		SN74LVC07A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.65	5.5	1.65	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V		1.7		
		V _{CC} = 2.7 V to 3.6 V		2		
		V _{CC} = 4.5 V to 5.5 V		0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V		0.7		
		V _{CC} = 2.7 V to 3.6 V		0.8		
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	5.5	0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4		mA
		V _{CC} = 2.3 V		12		
		V _{CC} = 2.7 V		12		
		V _{CC} = 3 V		24		
		V _{CC} = 4.5 V		24		
T _A	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product preview

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC07A ⁽¹⁾		SN74LVC07A		UNIT
			MIN	TYP ⁽²⁾	MAX	MIN	
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V	0.2		0.2		V
	I _{OL} = 4 mA	1.65 V	0.45		0.45		
	I _{OL} = 12 mA	2.3 V	0.7		0.7		
		2.7 V	0.4		0.4		
	I _{OL} = 24 mA	3 V	0.55		0.55		
4.5 V							
I _I	V _I = 5.5 V or GND	3.6 V	±5		±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	10		10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V	500		500		μA
C _i	V _I = V _{CC} or GND	3.3 V	5		5		pF

(1) Product preview

(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN54LVC07A, SN74LVC07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCAS5950–OCTOBER 1997–REVISED JULY 2005

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#) through [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC07A ⁽¹⁾										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

(1) Product preview

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#) through [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC07A										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	3.5	1	2.8	3		1	2.9	1	2.6	ns

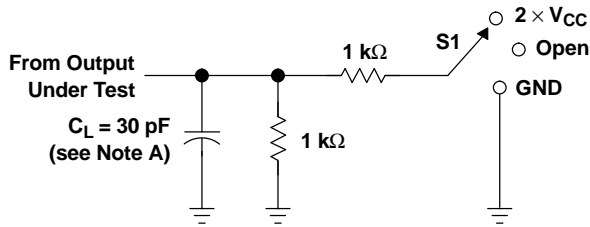
Operating Characteristics

T_A = 25°C

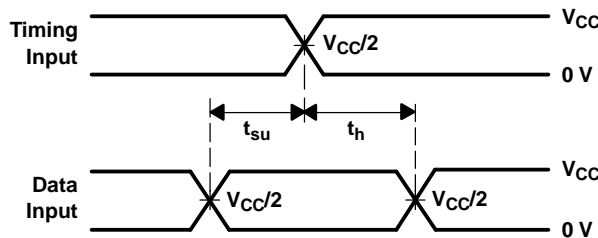
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver f = 10 MHz	1.8	2	2.5	3.78	pF

PARAMETER MEASUREMENT INFORMATION

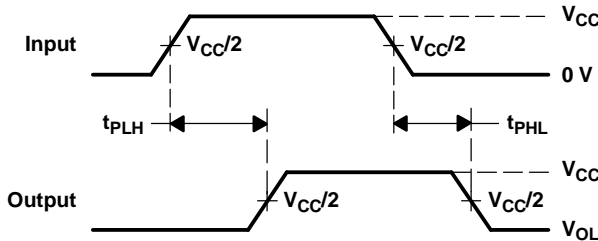
$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$



LOAD CIRCUIT

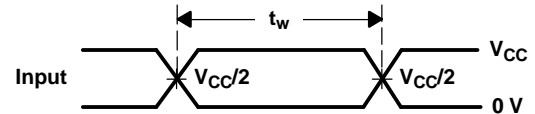


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

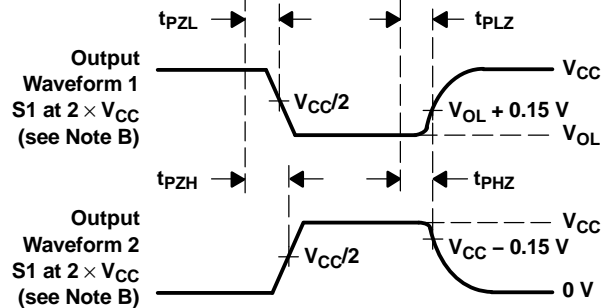
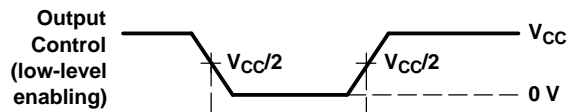


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{PZL} (see Note F)	$2 \times V_{CC}$
t_{PLZ} (see Note G)	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	$2 \times V_{CC}$



VOLTAGE WAVEFORMS
PULSE DURATION

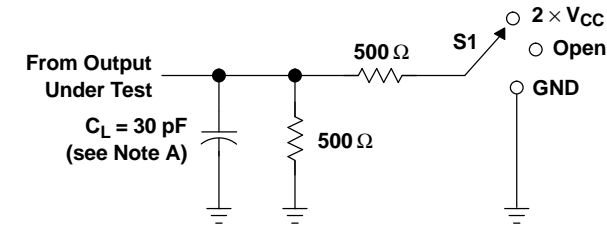


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

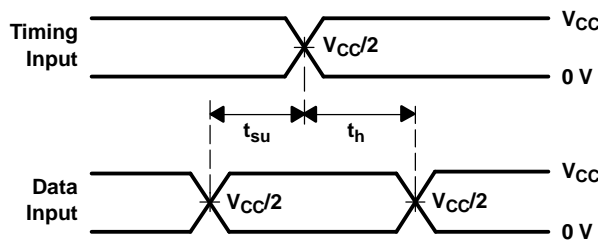
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 F. t_{PZL} is measured at $V_{CC}/2$.
 G. t_{PLZ} is measured at $V_{OL} + 0.15\text{ V}$.
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

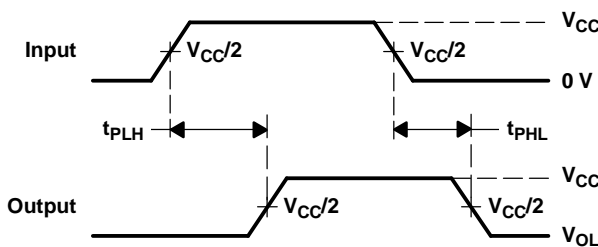
PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



LOAD CIRCUIT

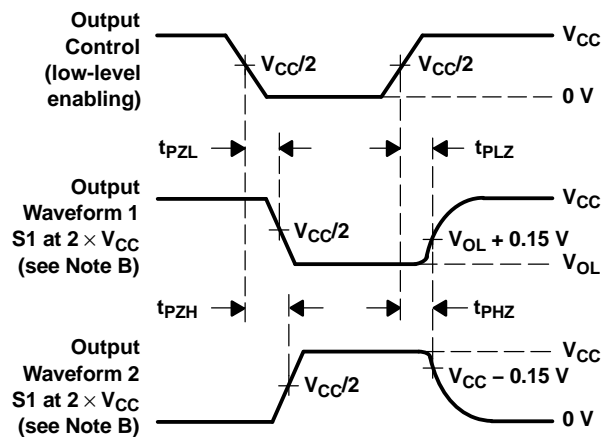
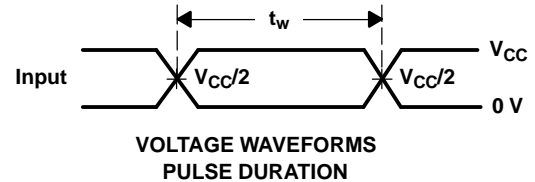


VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES

TEST	S1
t_{PZL} (see Note F)	2 $\times V_{CC}$
t_{PLZ} (see Note G)	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	2 $\times V_{CC}$



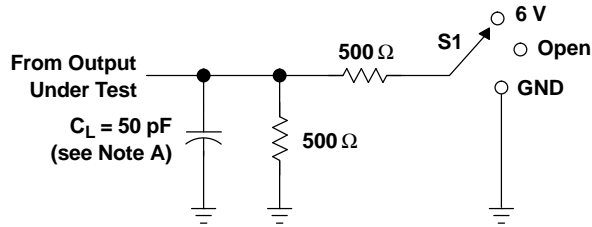
VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 F. t_{PZL} is measured at $V_{CC}/2$.
 G. t_{PLZ} is measured at $V_{OL} + 0.15 \text{ V}$.
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

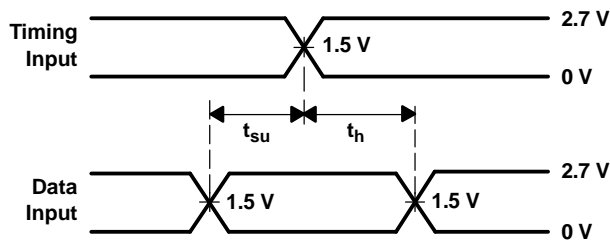
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7 \text{ and } 3.3 \text{ V} \pm 0.3 \text{ V}$

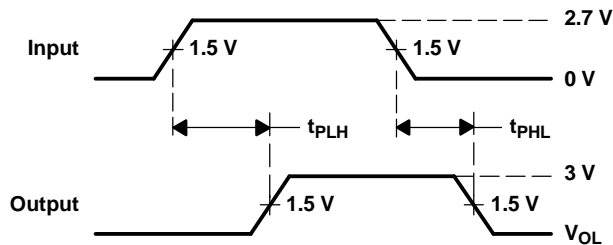


LOAD CIRCUIT

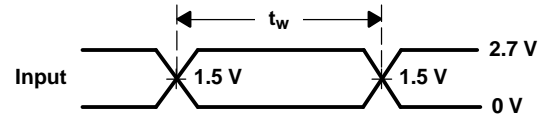
TEST	S1
t_{PZL} (see Note F)	6 V
t_{PLZ} (see Note G)	6 V
t_{PHZ}/t_{PZH}	6 V



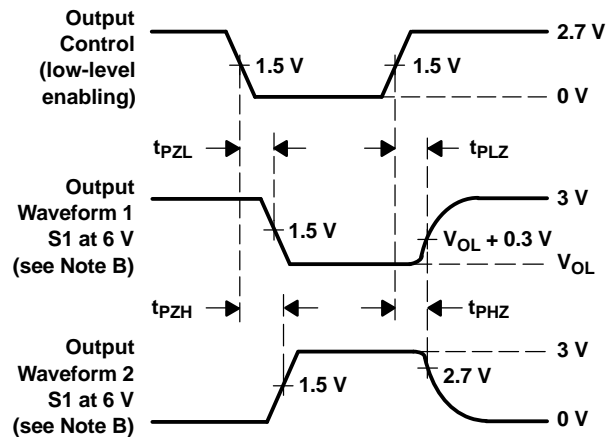
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

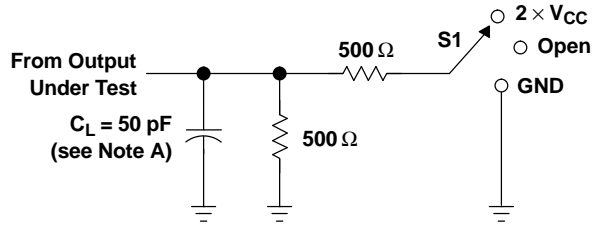


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 F. t_{PZL} is measured at 1.5 V.
 G. t_{PLZ} is measured at $V_{OL} + 0.3 \text{ V}$.
 H. All parameters and waveforms are not applicable to all devices.

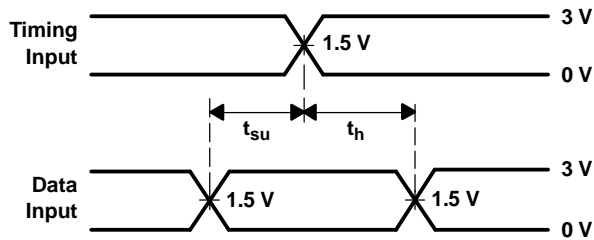
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

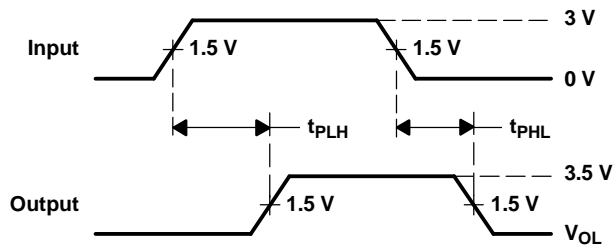


LOAD CIRCUIT

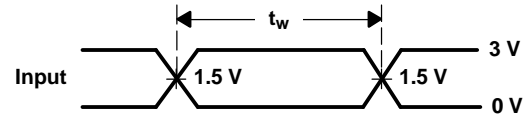
TEST	S1
t_{PZL} (see Note F)	2 \times V_{CC}
t_{PLZ} (see Note G)	2 \times V_{CC}
t_{PHZ}/t_{PHL}	7 V



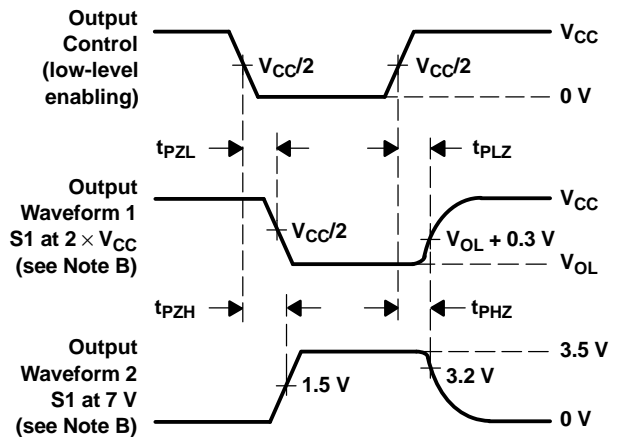
VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 F. t_{PZL} is measured at $V_{CC}/2$.
 G. t_{PLZ} is measured at $V_{OL} + 0.3\text{ V}$.
 H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC07AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ADTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74LVC07APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC07ARGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC07ARGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

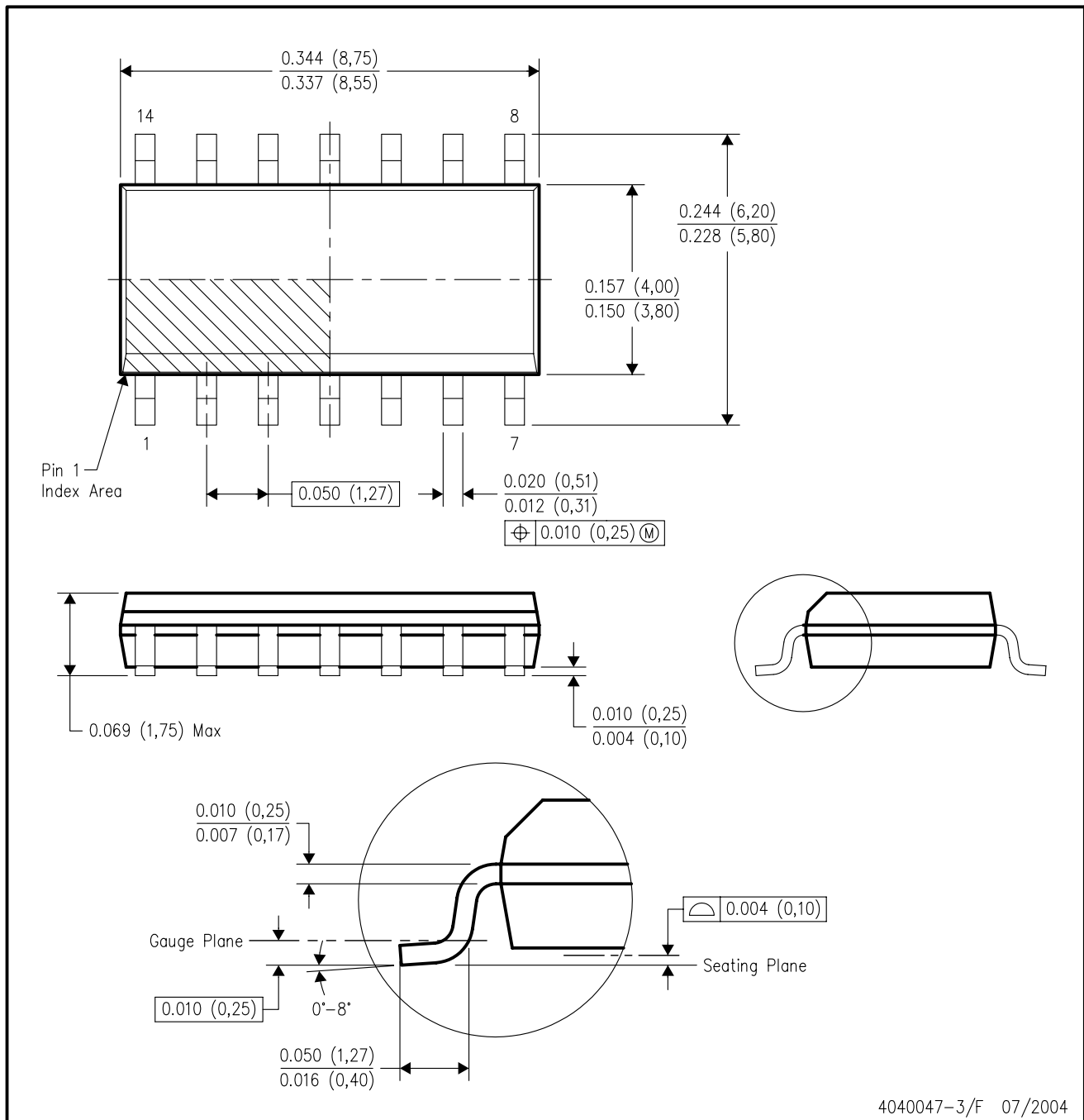
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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TI Home > Semiconductors > Logic > Buffers, Drivers and Transceivers > Non-Inverting Buffers and Drivers >

View ROHS Compliant Devices

clear gif

SN74LVC07A, Status: ACTIVE

View RoHS Compliant Devices

Hex Buffers/Drivers With Open-Drain Outputs



clear gif

<input type="checkbox"/> Features	<input type="checkbox"/> Samples	<input type="checkbox"/> Technical Documents
<input type="checkbox"/> Quality & Pb-Free Data	<input type="checkbox"/> Pricing/Packaging	<input type="checkbox"/> Applications Notes
<input type="checkbox"/> Related Products	<input type="checkbox"/> Inventory	<input type="checkbox"/> Simulation Models
<input type="checkbox"/> Tools & Software	<input type="checkbox"/> Symbols/Footprints	<input type="checkbox"/> Reference Designs



Refine Your Selection

- Logic: Non-Inverting Buffers and Drivers

Support

- KnowledgeBase
- Contact Technical Support
- TI Cross Reference
- Training
- Part Marking Lookup
- Part Number Nomenclature

Datasheet



Download Datasheet

SN54LVC07A, SN74LVC07A (Rev. O) (sn74lvc07a.pdf, 402 KB)
26 Jul 2005 [Download](#)

	SN74LVC07A
Voltage Nodes(V)	5, 3.3, 2.7, 2.5, 1.8
Vcc range(V)	1.65 to 5.5
Logic	True
Input Level	TTL/CMOS
Output Level	LVTTL
Output Drive(mA)	24
No. of Outputs	6
tpd max(ns)	2.6
Static Current	0.01
	Samples
	Inventory

Product Information

<input type="checkbox"/> Features	<input type="checkbox"/> Save this to your personal library
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Operate From 1.65 V to 5 V
 Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
 Max t_{pd} of 2.6 ns at 5 V
 Latch-Up Performance Exceeds 250 mA Per JESD 17

DESCRIPTION/ORDERING INFORMATION

These hex buffers/drivers are designed for 1.65-V to 5.5-V V_{CC} operation.

The outputs of the 'LVC07A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of these devices as translators in a mixed-system environment.


Pricing/Packaging/CAD Design Tools/Samples

			Price	Packaging			CAD Design Tools	Samples
Device	Status	Temp (°C)	Budget Price (\$US) QTY	Industry Standard (TI Pkg) Pins	Top Side Marking	Standard Pack Quantity	Footprints	Samples
SN74LVC07AD	ACTIVE	-40 to 85	0.17 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADBR	ACTIVE	-40 to 85	0.17 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC07ADBRG4	ACTIVE	-40 to 85	0.18 1KU	SSOP (DB) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADE4	ACTIVE	-40 to 85	0.17 1KU	SOIC (D) 14	View	50	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADGVR	ACTIVE	-40 to 85	0.31 1KU	TVSOP (DGV) 14		2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC07ADGVRE4	ACTIVE	-40 to 85	0.31 1KU	TVSOP (DGV) 14		2000	<input type="checkbox"/>	Request Free Samples
SN74LVC07ADGVRG4	ACTIVE	-40 to 85	0.29 1KU	TVSOP (DGV) 14		2000	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADR	ACTIVE	-40 to 85	0.17 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC07ADRE4	ACTIVE	-40 to 85	0.18 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADRG4	ACTIVE	-40 to 85	0.18 1KU	SOIC (D) 14	View	2500	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADT	ACTIVE	-40 to 85	0.29 1KU	SOIC (D) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC07ADTE4	ACTIVE	-40 to 85	0.29 1KU	SOIC (D) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC07ANSR	ACTIVE	-40 to 85	0.18 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC07ANSRE4	ACTIVE	-40 to 85	0.18 1KU	SO (NS) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC07APW	ACTIVE	-40 to 85	0.17 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWE4	ACTIVE	-40 to 85	0.18 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWG4	ACTIVE	-40 to 85	0.19 1KU	TSSOP (PW) 14	View	90	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWLE	OBSOLETE	-40 to 85		TSSOP (PW) 14	View		<input type="checkbox"/>	Not Available
SN74LVC07APWR	ACTIVE	-40 to 85	0.17 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Contact TI Distributor or Sales Office
SN74LVC07APWRE4	ACTIVE	-40 to 85	0.18 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWRG4	ACTIVE	-40 to 85	0.35 1KU	TSSOP (PW) 14	View	2000	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWT	ACTIVE	-40 to 85	0.29 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWTE4	ACTIVE	-40 to 85	0.48 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC07APWTG4	ACTIVE	-40 to 85	0.50 1KU	TSSOP (PW) 14	View	250	<input type="checkbox"/>	Purchase Samples
SN74LVC07ARGYR	ACTIVE	-40 to 85	0.33 1KU	QFN (RGY) 14	View	1000		Request Free Samples
SN74LVC07ARGYRG4	ACTIVE	-40 to 85	0.24 1KU	QFN (RGY) 14	View	1000		Request Free Samples

Inventory							
TI Inventory Status				Reported Distributor Inventory			
As of 9:08 AM GMT, 29 Nov 2005				As of 9:08 AM GMT, 29 Nov 2005			
SN74LVC07AD	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase

View all Distributors

Choose a Region



	0*	>10k 6 Mar	14 Weeks	Americas	Arrow	>1k	<input type="text"/>
					Avnet	>1k	<input type="text"/>
					DigiKey	991	<input type="text"/>
					Newark InOne	>1k	<input type="text"/>
				Europe	Arrow Northern Europe	>1k	<input type="text"/>
					Arrow Southern Europe	624	<input type="text"/>
					Avnet-SILICA	>1k	<input type="text"/>
					EBV Elektronik	44	<input type="text"/>

SN74LVC07ADBR As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1 12 Dec	10 Weeks	Americas	DigiKey	>1k	<input type="text"/>
		562 5 Jan		Europe	Arrow Southern Europe	>1k	<input type="text"/>
		700 12 Jan					
		847 9 Feb					
		>10k 16 Feb					

SN74LVC07ADBRG4 As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	2699 5 Dec	8 Weeks	None Reported View Distributors			
		537 3 Jan					
		668 10 Jan					
		810 7 Feb					
		>10k 14 Feb					

SN74LVC07ADE4 As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Mar	14 Weeks	None Reported View Distributors			

SN74LVC07ADGVR As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	8000*	>10k 12 Dec	10 Weeks	Americas	DigiKey	132	<input type="text"/>

SN74LVC07ADGVRE4 As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	8000*	>10k 12 Dec	10 Weeks	None Reported View Distributors			

SN74LVC07ADGVRG4 As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	695 5 Jan	10 Weeks	None Reported View Distributors			
		648 26 Jan					
		>10k 9 Feb					

SN74LVC07ADR As of 9:08 AM GMT, 29 Nov 2005 As of 9:08 AM GMT, 29 Nov 2005

	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Mar	14 Weeks	Americas	DigiKey	>1k	<input type="text"/>
					Newark InOne	>1k	<input type="text"/>
SN74LVC07ADRE4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Mar	14 Weeks	None Reported View Distributors			
SN74LVC07ADRG4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	2500*	1297 30 Nov	10 Weeks	None Reported View Distributors			
		>10k 30 Dec					
SN74LVC07ADT	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Mar	14 Weeks	None Reported View Distributors			
SN74LVC07ADTE4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 6 Mar	14 Weeks	None Reported View Distributors			
SN74LVC07ANSR	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1465 30 Nov	10 Weeks	Americas	Arrow	>1k	<input type="text"/>
		535 10 Jan					
		267 27 Jan					
		1973 17 Feb					
		611 24 Feb					
SN74LVC07ANSRE4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	1465 30 Nov	10 Weeks	None Reported View Distributors			
		535 10 Jan					
		267 27 Jan					
		1973 17 Feb					
		611 24 Feb					
SN74LVC07APW	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	Europe	Arrow Northern Europe	>1k	<input type="text"/>
					EBV Elektronik	1	<input type="text"/>
SN74LVC07APWE4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			

SN74LVC07APWG4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
SN74LVC07APWR	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 31 Mar	16 Weeks	Americas	Newark InOne	117	<input type="text"/>
				Europe	Avnet-SILICA	>1k	<input type="text"/>
SN74LVC07APWRE4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	29 12 Dec	16 Weeks	None Reported View Distributors			
SN74LVC07APWRG4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	3999 20 Mar	16 Weeks	None Reported View Distributors			
		>10k 3 Apr					
SN74LVC07APWT	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*		16 Weeks	None Reported View Distributors			
SN74LVC07APWTE4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC07APWTG4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 3 Apr	16 Weeks	None Reported View Distributors			
SN74LVC07ARGYR	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 9 Jan	8 Weeks	Europe	Avnet-SILICA	1k	<input type="text"/>
SN74LVC07ARGYRG4	As of 9:08 AM GMT, 29 Nov 2005			As of 9:08 AM GMT, 29 Nov 2005			
	In Stock	In Progress QTY Date	Lead Time	Region	Company	In Stock	Purchase
	0*	>10k 9 Jan	8 Weeks	None Reported View Distributors			

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Quality & Lead (Pb)-Free Data

Device	Product Content			MTBF/FIT Rate	
	Eco Plan*	Lead/Ball Finish	MSL Rating/Peak Reflow	Details	Details
SN74LVC07AD <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADBR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADBRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADGVR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADGVRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADGVRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ADTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ANSR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ANSRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APW <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWRE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWT <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWTE4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07APWTG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	View	View
SN74LVC07ARGYR <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View
SN74LVC07ARGYRG4 <input type="checkbox"/>	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR	View	View

* The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please click on the Product Content Details "View" link in the table above for the latest availability information and additional product content details.

If the information you are requesting is not available online at this time, contact one of our [Product Information Centers](#) regarding the availability of this information.

Technical Documents
 Datasheets

Keep track of what's new

SN54LVC07A, SN74LVC07A (Rev. O) (sn74lvc07a.pdf, 402 KB)

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 Application Notes

Semiconductor Packing Material Electrostatic Discharge (ESD) Protection (szza047.htm, 9 KB)

08 Jul 2004 [Abstract](#)

Selecting the Right Level Translation Solution (Rev. A) (scea035a.htm, 9 KB)

22 Jun 2004 [Abstract](#)

Shelf-Life Evaluation of Lead-Free Component Finishes (szza046.htm, 9 KB)

24 May 2004 [Abstract](#)

Use of the CMOS Unbuffered Inverter in Oscillator Circuits (szza043.htm, 9 KB)

06 Nov 2003 [Abstract](#)

Understanding and Interpreting Standard-Logic Data Sheets (Rev. B) (szza036b.htm, 8 KB)

28 May 2003 [Abstract](#)

Texas Instruments Little Logic Application Report (scea029.htm, 9 KB)

01 Nov 2002 [Abstract](#)

TI IBIS File Creation, Validation, and Distribution Processes (szza034.htm, 9 KB)

29 Aug 2002 [Abstract](#)

16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) (szza029b.htm, 9 KB)

22 May 2002 [Abstract](#)

Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (szza033.htm, 9 KB)

10 May 2002 [Abstract](#)

Selecting the Right Texas Instruments Signal Switch (szza030.htm, 9 KB)

07 Sep 2001 [Abstract](#)

LVC07A: Applications Of An Open-Drain Hex Buffer And Discussion Of Char Results (scea012.htm, 9 KB)

08 Apr 1999 [Abstract](#)

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