

# SN54S260, SN74S260 DUAL 5-INPUT POSITIVE-NOR GATES

SDLS208

DECEMBER 1983 — REVISED MARCH 1988

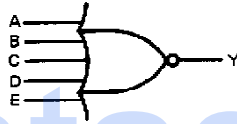
- Package Options Include Ceramic Chip Carriers and Flat Packages in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

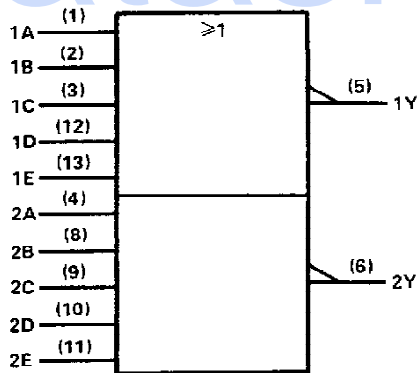
These devices contain two independent 5-input positive -NOR gates. They perform the Boolean function  $Y = A + B + C + D + E$  in positive logic.

The SN54S260 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74S260 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

## logic diagram (each gate)



## logic symbol†

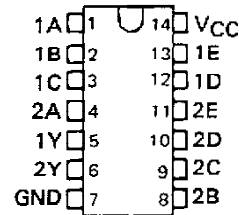


†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

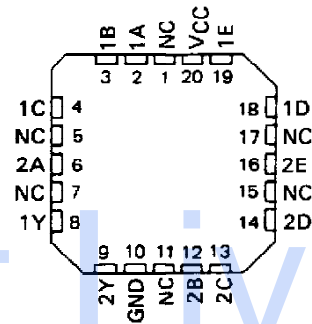
SN54S260 . . . J OR W PACKAGE  
SN74S260 . . . D OR N PACKAGE

(TOP VIEW)



SN54S260 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

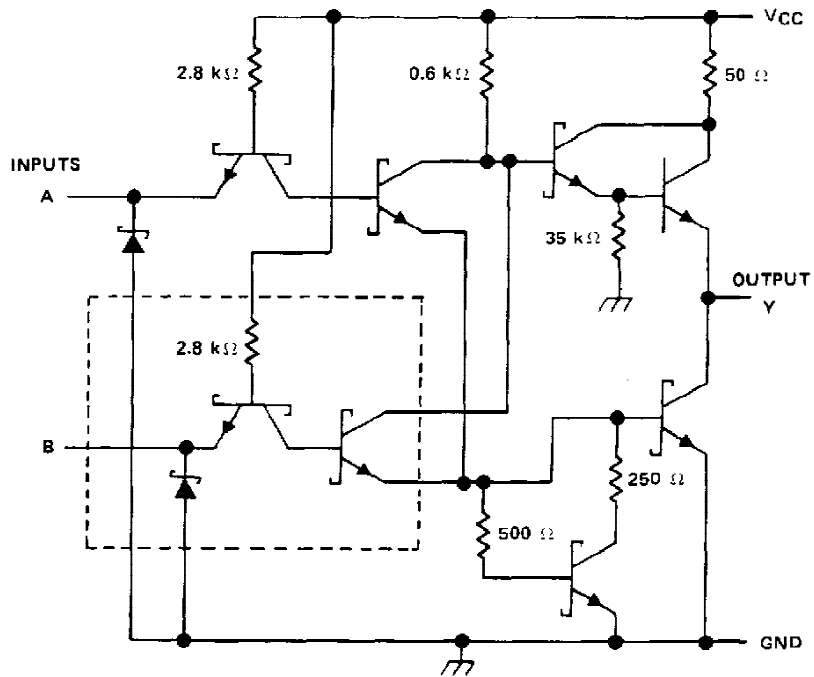
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# SN54S260, SN74S260 DUAL 5-INPUT POSITIVE-NOR GATES

schematic (each gate)



Resistor values shown are nominal.  
The portion of the schematic within the dashed-line is repeated for each additional input.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	5.5 V
Operating free-air temperature range: SN54' .....	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74' .....	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range .....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to network ground terminal.

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# SN54S260, SN74S260 DUAL 5-INPUT POSITIVE-NOR GATES

## recommended operating conditions

	SN54S260			SN74S260			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage	0.8			0.8			V
I <sub>OH</sub> High-level output current	-1			-1			mA
I <sub>OL</sub> Low-level output current	20			20			mA
T <sub>A</sub> Operating free-air temperature	-55			125			°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S260			SN74S260			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.2			-1.2			V	
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4	V		
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 20 mA	0.5			0.5			V	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA	
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2.7 V	50			50			µA	
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>IL</sub> = 0.8 V	-2			-2			mA	
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-40		-100	-40		-100	mA	
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V	17			17			29	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, See Note 2	26			26			45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: One input at 4.5 V, all others at GND.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Y	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF		4	5.5	ns
t <sub>PHL</sub>				4	6	ns	

NOTE 3: See General Information Section for load circuits and voltage waveforms.

  
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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN54S260J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SN74S260D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S260N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S260N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S260NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54S260FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54S260J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54S260W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

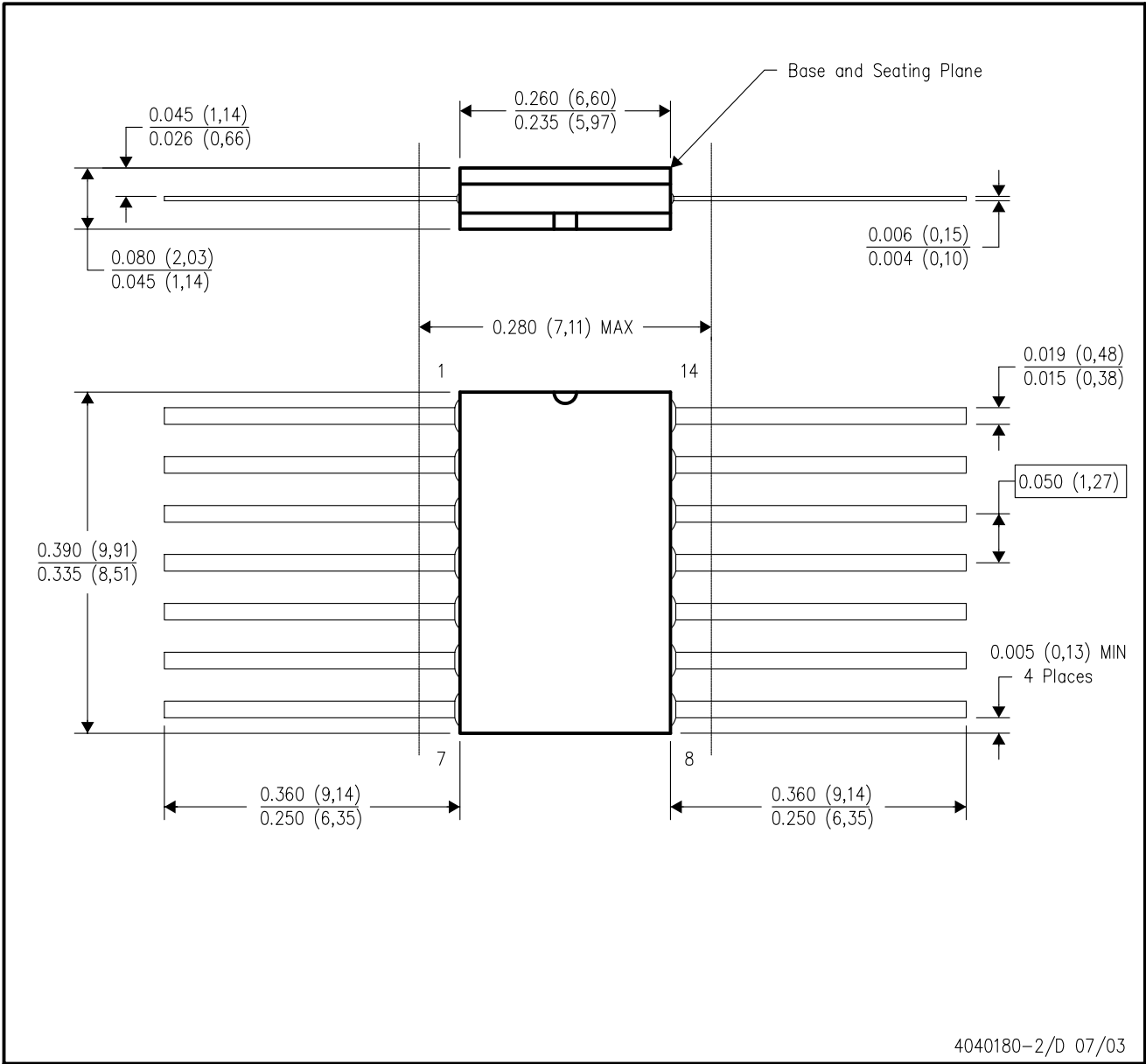


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

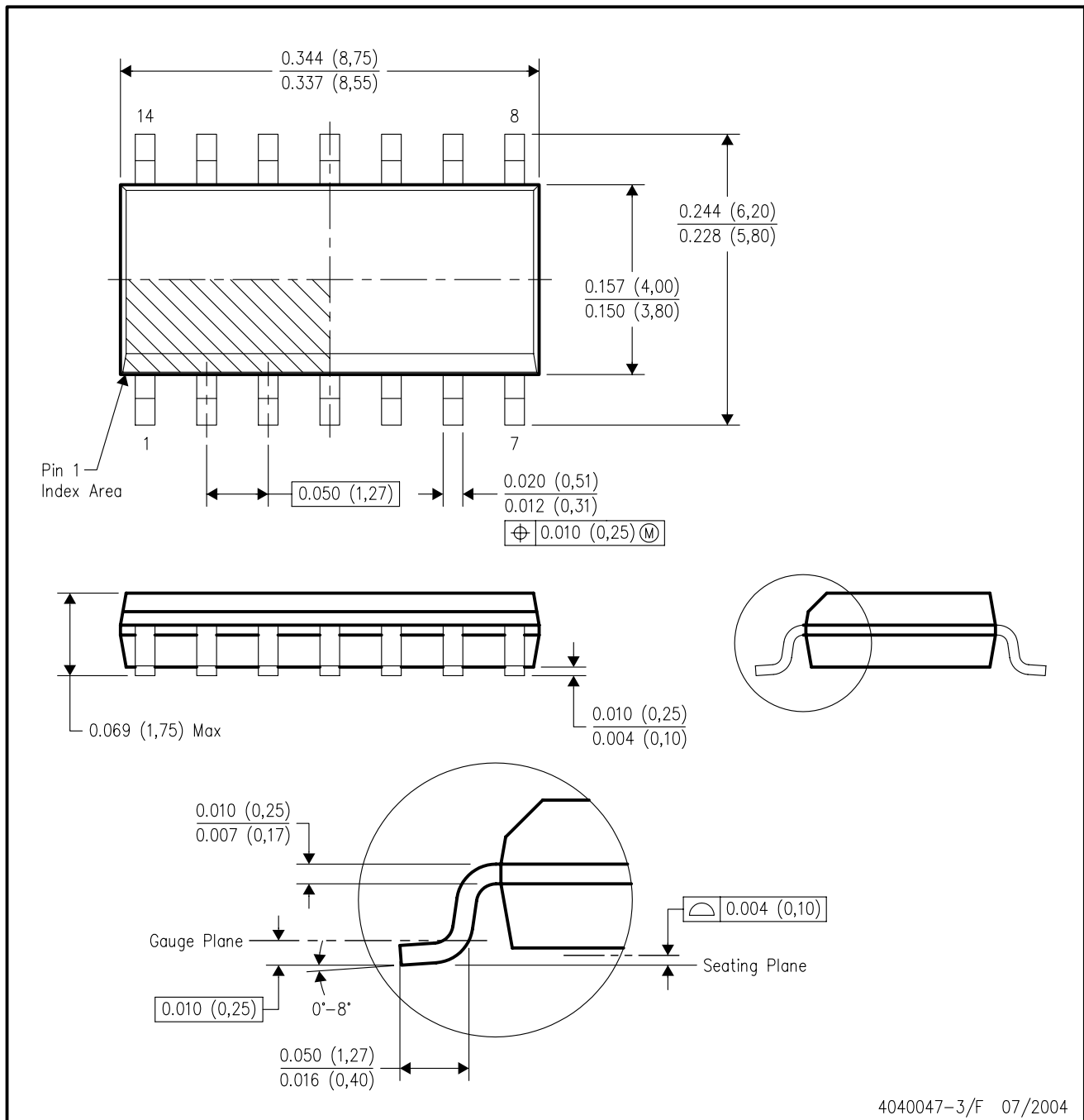


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

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