

SN65LBC180A, SN75LBC180A LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

SLLS378C – MAY 2000 – REVISED JUNE 2002

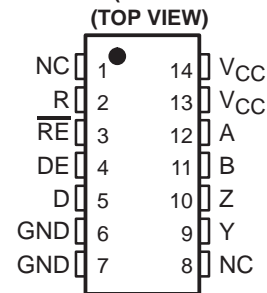
- High-Speed Low-Power LinBICMOS™ Circuitry Designed for Signaling Rates† of up to 30 Mbps
- Bus-Pin ESD Protection Exceeds 12 kV HBM
- Very Low Disabled Supply-Current Requirements . . . 700 μ A Maximum
- Designed for High-Speed Multipoint Data Transmission Over Long Cables
- Common-Mode Voltage Range of –7 V to 12 V
- Low Supply Current . . . 15 mA Max
- Compatible With ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)
- Positive and Negative Output Current Limiting
- Driver Thermal Shutdown Protection

description

The SN65LBC180A and SN75LBC180A differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that are compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E). The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

These devices combine a differential line driver and differential input line receiver and operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off ($V_{CC} = 0$). These parts feature wide positive and negative common-mode voltage ranges, making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive and negative current limiting for protection from line fault conditions. The SN65LBC180A is characterized for operation from –40°C to 85°C, and the SN75LBC180A is characterized for operation from 0°C to 70°C.

SN65LBC180AD (Marked as BL180A)
SN65LBC180AN (Marked as 65LBC180A)
SN75LBC180AD (Marked as LB180A)
SN75LBC180AN (Marked as 75LBC180A)



NC – No internal connection

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < $V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open circuit	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved without this requirement as displayed in the *TYPICAL CHARACTERISTICS* of this device.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



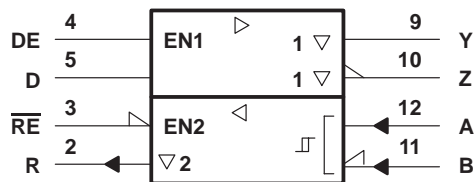
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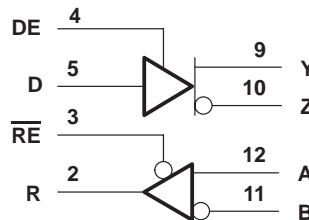
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

AVAILABLE OPTIONS

T _A	PACKAGE	
	SMALL OUTLINE† (D)	PLASTIC DUAL-IN-LINE (N)
0°C to 70°C	SN75LBC180AD	SN75LBC180AN
-40°C to 85°C	SN65LBC180AD	SN65LBC180AN

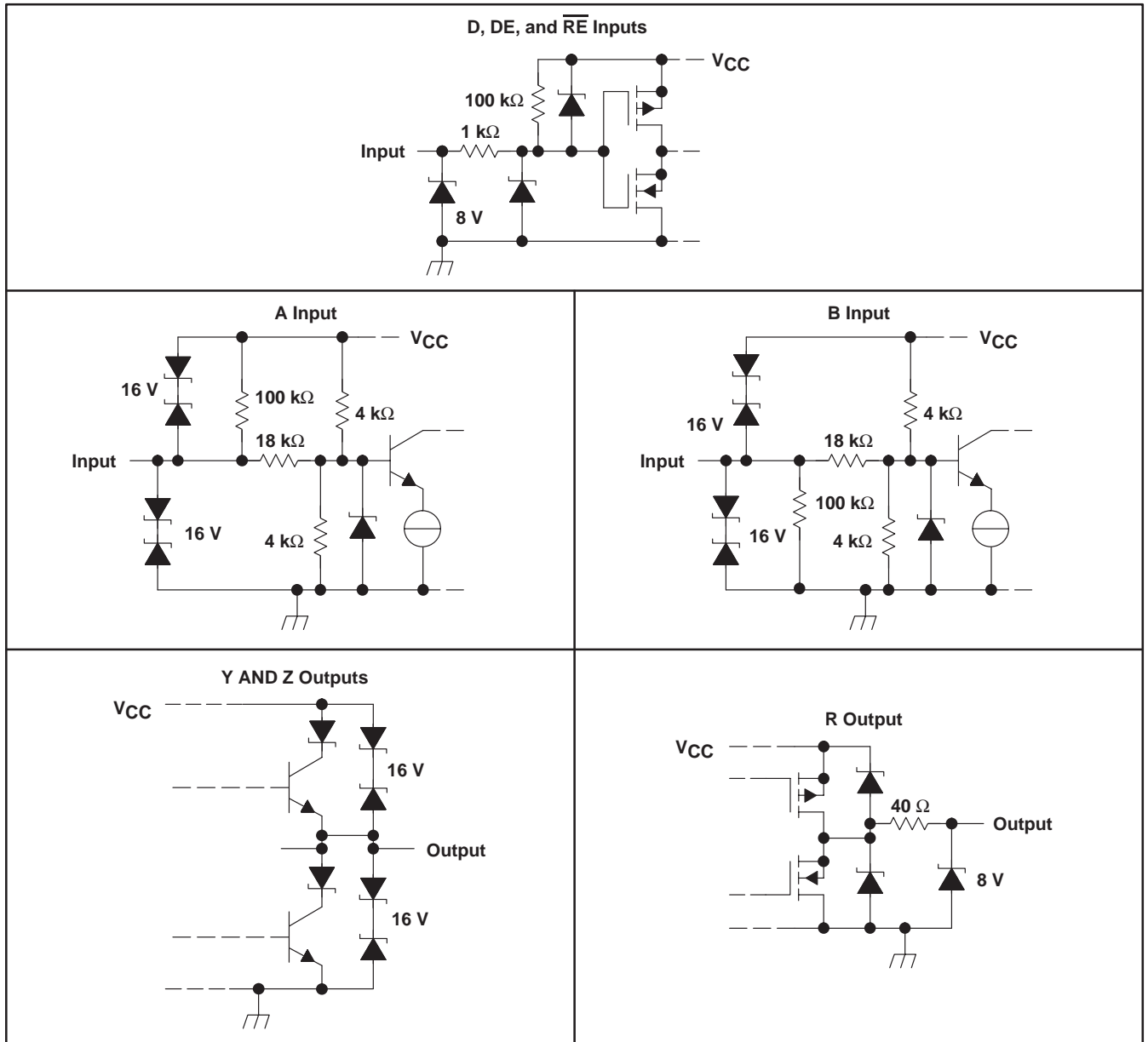
† The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN65LBC180ADR).

SN65LBC180A, SN75LBC180A

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schematics of inputs and outputs



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absolute maximum ratings†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Input voltage range, V_I (A, B)	–10 V to 15 V
Voltage range at D, R, DE, \overline{RE}	–0.3 V to $V_{CC} + 0.5$ V
Continuous total power dissipation (see Note 2)	Internally limited
Total power dissipation	See Dissipation Rating Table
Electrostatic discharge: Bus terminals and GND, Class 3, A: (see Note 3)	12 kV
Bus terminals and GND, Class 3, B: (see Note 3)	400 V
All terminals, Class 3, A:	3 kV
All terminals, Class 3, B:	400 V
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND except for differential input or output voltages.
 2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
 3. Tested in accordance with MIL–STD–883C, Method 3015.7

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR‡	$T_A = 70^\circ\text{C}$	$T_A = 85^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2		V_{CC}	V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}	0		0.8	V
Differential input voltage, V_{ID} (see Note 4)		–12§		12	V
Voltage at any bus terminal (separately or common mode), V_O , V_I , or V_{IC}	A, B, Y, or Z	–7		12	V
High-level output current, I_{OH}	Y or Z	–60			mA
	R	–8			
Low-level output current, I_{OL}	Y or Z			60	mA
	R			8	
Operating free-air temperature, T_A	SN65LBC180A	–40		85	°C
	SN75LBC180A	0		70	

§ The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet.

NOTE 4: Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.



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driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$		-1.5	-0.8		V
$ V_{OD} $	Differential output voltage magnitude	$R_L = 54 \Omega$, See Figure 1	SN65LBC180A	1	1.5	3	V
			SN75LBC180A	1.1	1.5	3	
		$R_L = 60 \Omega$, See Figure 2	SN65LBC180A	1	1.5	3	
			SN75LBC180A	1.1	1.5	3	
$\Delta V_{OD} $	Change in magnitude of differential output voltage (see Note 5)	See Figures 1 and 2		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage			1.8	2.4	2.8	V
ΔV_{OC}	Change in steady-state common-mode output voltage (see Note 5)	See Figure 1		-0.1		0.1	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7 \text{ V to } 12 \text{ V}$	-10		10	μA
I_{IH}	High-level input current	$V_I = 2 \text{ V}$		-100			μA
I_{IL}	Low-level input current	$V_I = 0.8 \text{ V}$		-100			μA
I_{OS}	Short-circuit output current	$-7 \text{ V} \leq V_O \leq 12 \text{ V}$		-250	± 70	250	mA
I_{CC}	Supply current	$V_I = 0$ or V_{CC} , No load	Receiver disabled and driver enabled		5.5	9	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

NOTE 5: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$	Pulse skew ($ t_{PLH} - t_{PHL} $)		0.3		1	ns
t_r	Differential output signal rise time		4	7.5	11	ns
t_f	Differential output signal fall time		4	7.5	11	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	$R_L = 110 \Omega$, See Figure 4		12	22	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	$R_L = 110 \Omega$, See Figure 5		12	22	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	$R_L = 110 \Omega$, See Figure 4		12	22	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	$R_L = 110 \Omega$, See Figure 5		12	22	ns



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receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
V_{IT+}	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$			0.2	V	
V_{IT-}	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-0.2			V	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV	
V_{IK}	Enable-input clamp voltage	$I_I = -18 \text{ mA}$	-1.5	-0.8		V	
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -8 \text{ mA}$	4	4.9		V	
V_{OL}	Low-level output voltage	$V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$		0.1	0.8	V	
I_{OZ}	High-impedance-state output current	$V_O = 0 \text{ V to } V_{CC}$	-1		1	μA	
I_{IH}	High-level enable-input current	$V_{IH} = 2.4 \text{ V}$	-100			μA	
I_{IL}	Low-level enable-input current	$V_{IL} = 0.4 \text{ V}$	-100			μA	
I_I	Bus input current	$V_I = 12 \text{ V}$, $V_{CC} = 5 \text{ V}$	Other input at 0 V		0.4	1	mA
		$V_I = 12 \text{ V}$, $V_{CC} = 0 \text{ V}$			0.5	1	
		$V_I = -7 \text{ V}$, $V_{CC} = 5 \text{ V}$		-0.8	-0.4		
		$V_I = -7 \text{ V}$, $V_{CC} = 0 \text{ V}$		-0.8	-0.3		
I_{CC}	Supply current	$V_I = 0 \text{ or } V_{CC}$, No load	Receiver enabled and driver disabled	4.5	7.5	mA	
			Receiver disabled and driver disabled	0.5	1		
			Receiver enabled and driver enabled	8.5	15		

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$, See Figure 7	7	13	20	ns
t_{PHL}	Propagation delay time, high- to low-level output		7	13	20	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)		0.5	1.5		ns
t_r	Output signal rise time	See Figure 7		2.1	3.3	ns
t_f	Output signal fall time			2.1	3.3	
t_{PZH}	Output enable time to high level	$C_L = 10 \text{ pF}$, See Figure 8		30	45	ns
t_{PZL}	Output enable time to low level			30	45	
t_{PHZ}	Output disable time from high level			20	40	
t_{PLZ}	Output disable time from low level			20	40	



PARAMETER MEASUREMENT INFORMATION

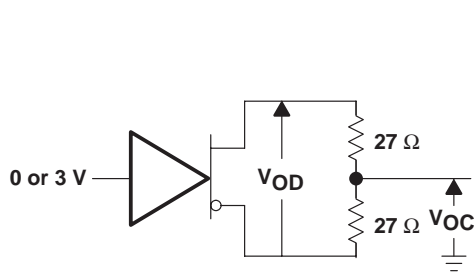


Figure 1. Driver V_{OD} and V_{OC}

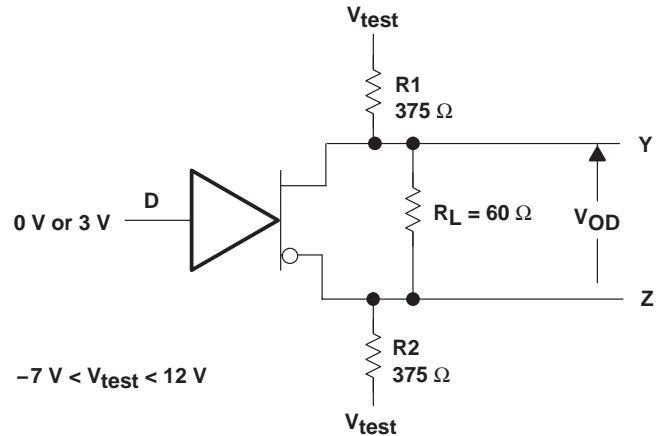
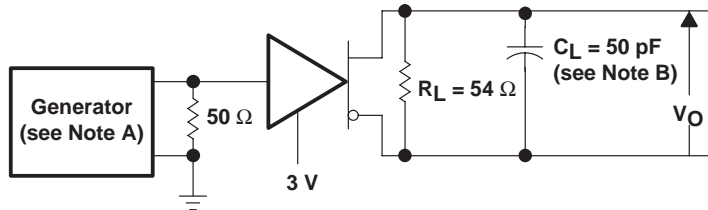
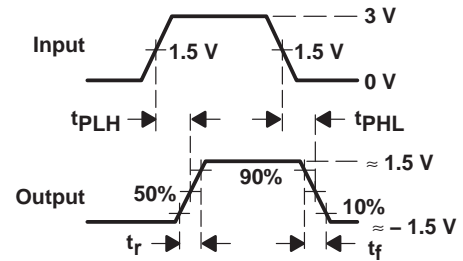


Figure 2. Driver V_{OD}



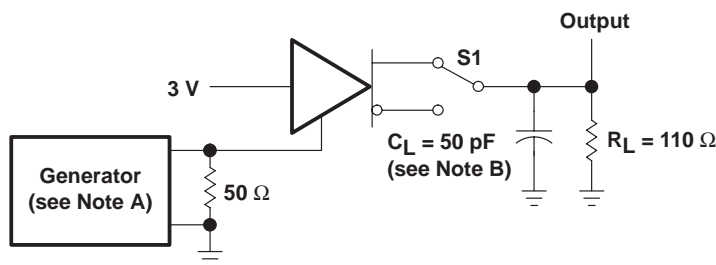
TEST CIRCUIT



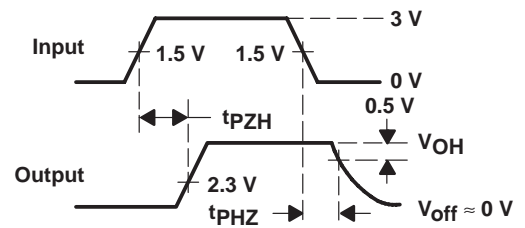
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

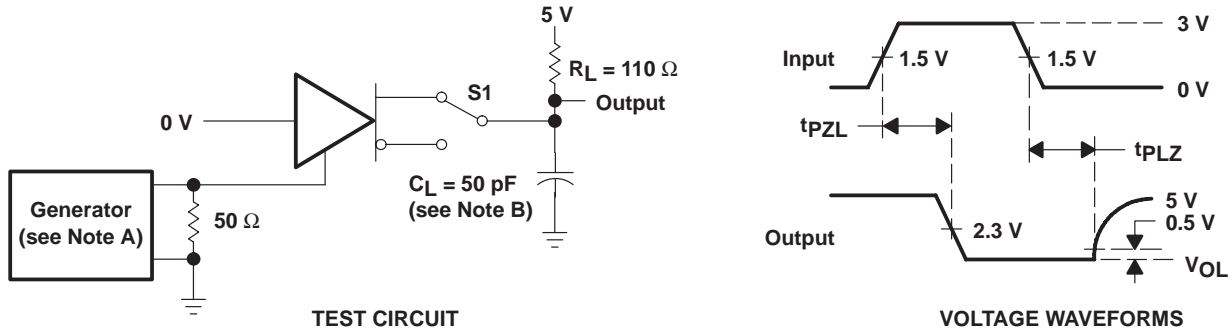
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

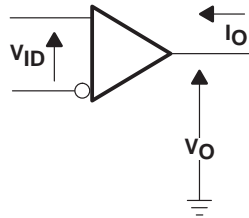
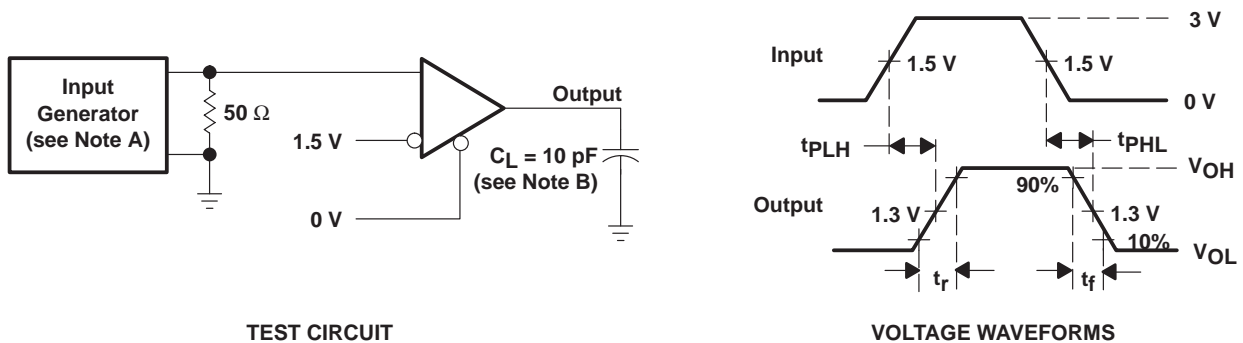


Figure 6. Receiver V_{OH} and V_{OL}



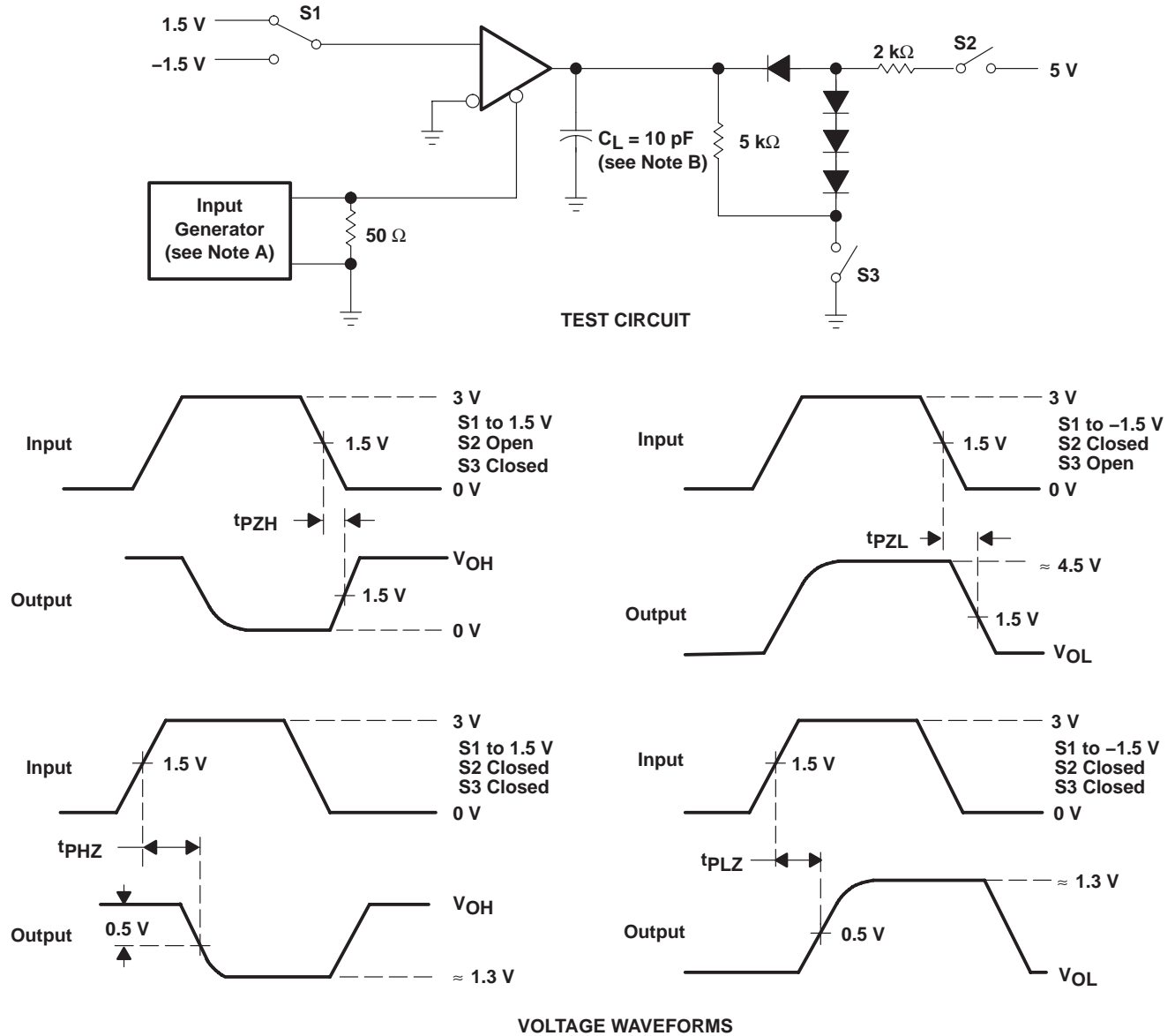
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 8. Receiver Output Enable and Disable Times

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TYPICAL CHARACTERISTICS

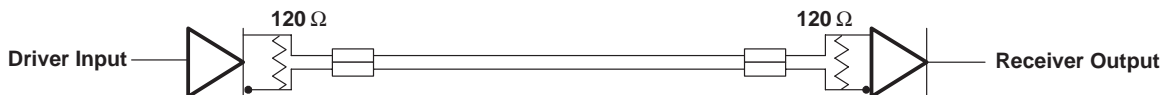
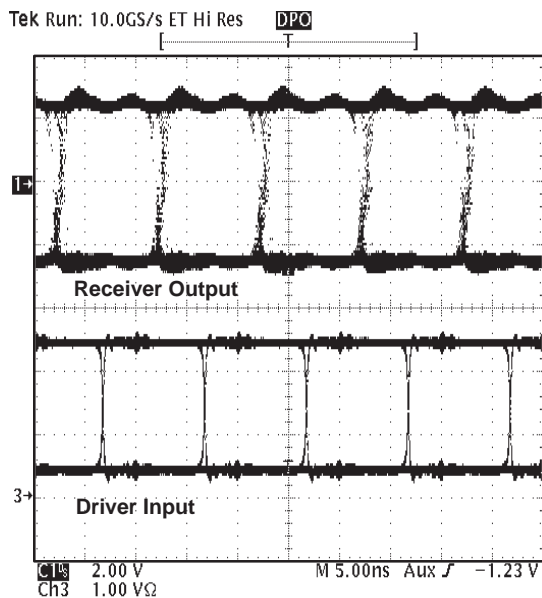


Figure 9. Typical Waveform of Nonreturn-to-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

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TYPICAL CHARACTERISTICS

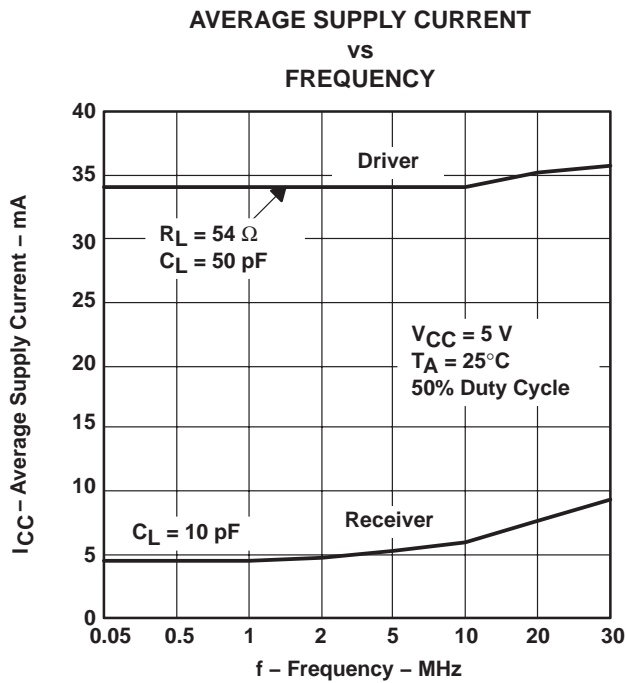


Figure 10

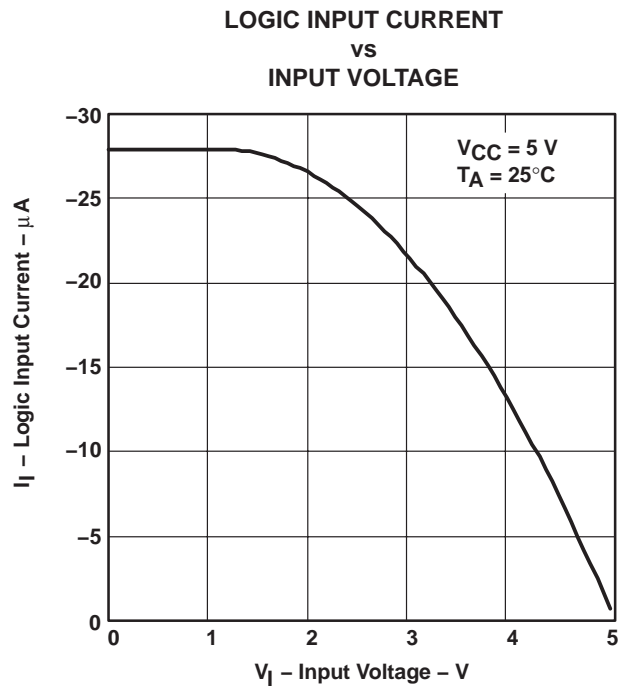


Figure 11

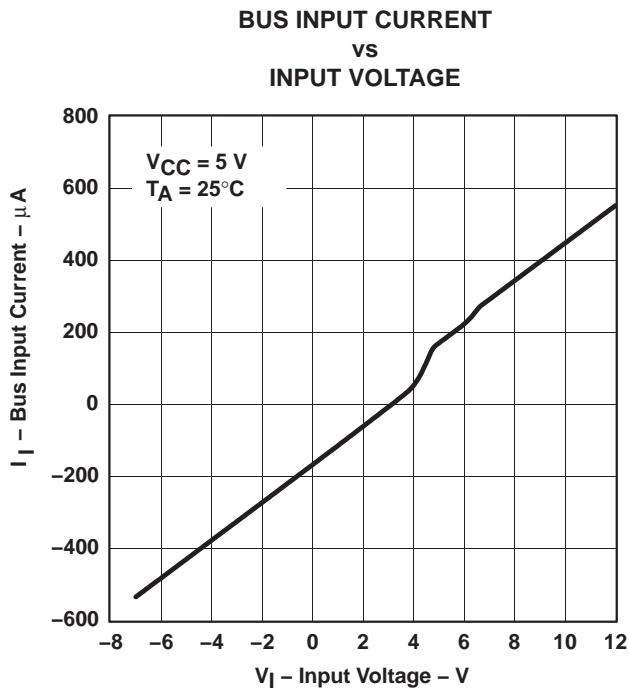


Figure 12

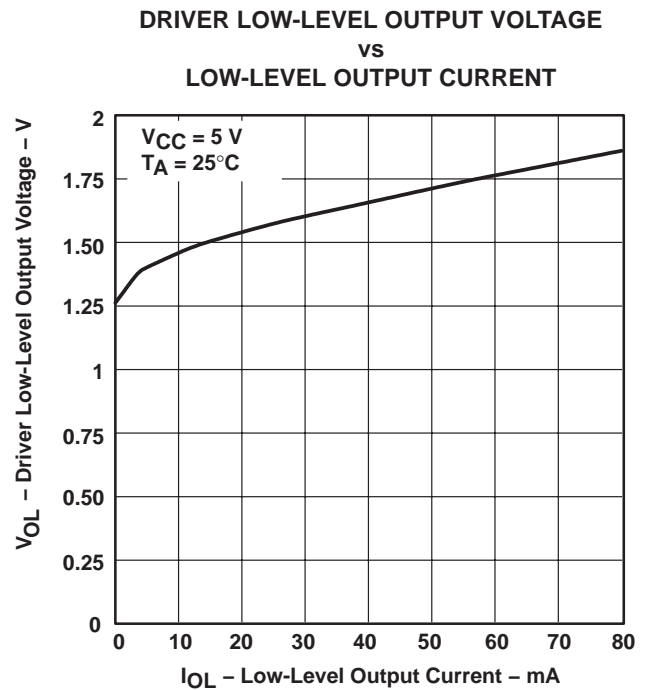
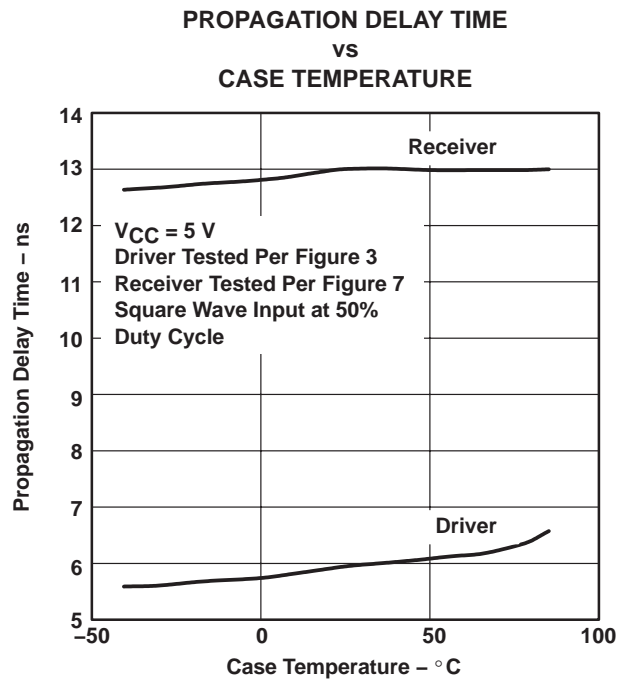
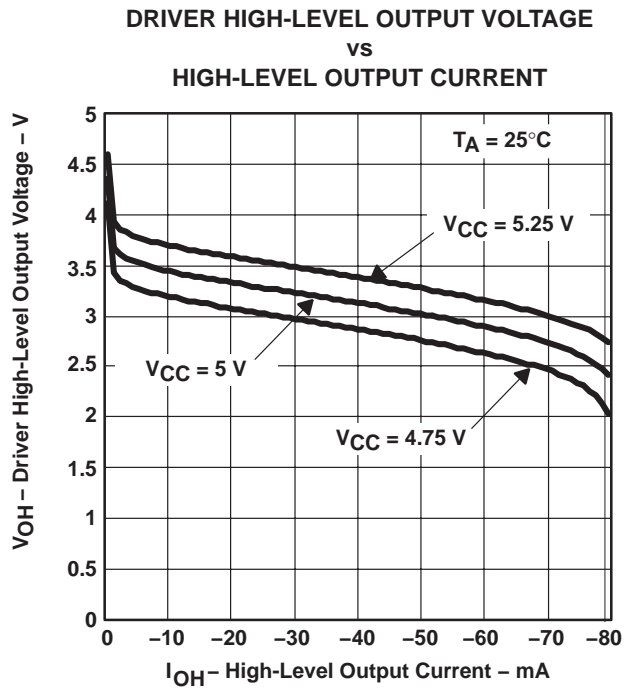


Figure 13

SN65LBC180A, SN75LBC180A LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

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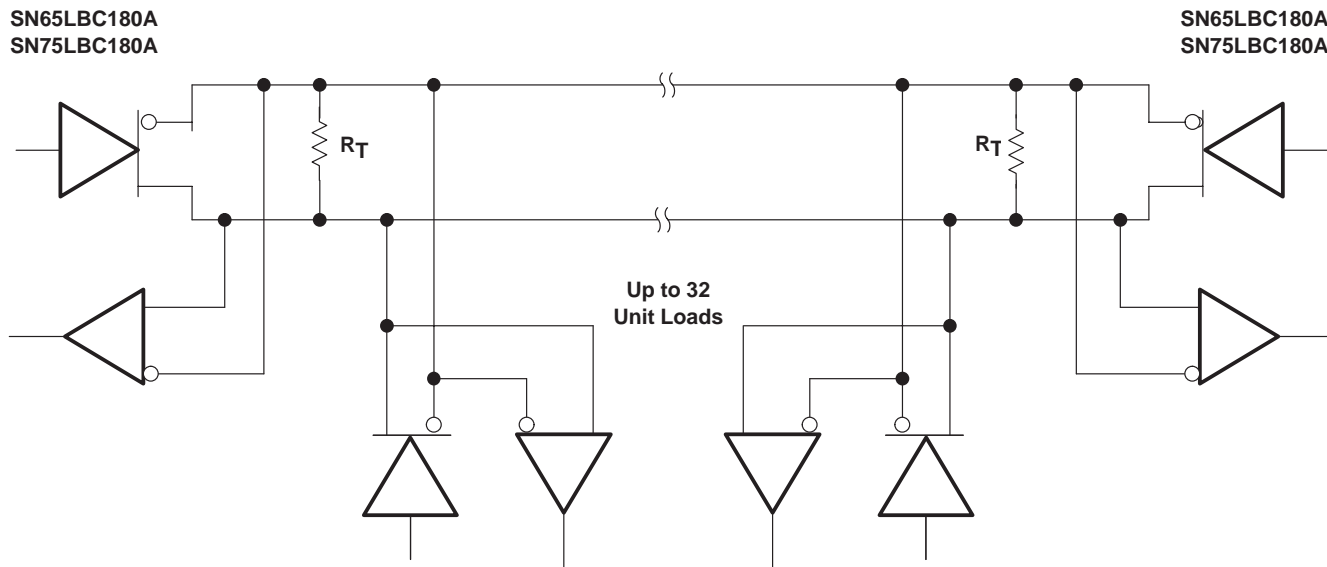
TYPICAL CHARACTERISTICS



SN65LBC180A, SN75LBC180A LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

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APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible. One SN65LBC180A typically represents less than one unit load.

Figure 16. Typical Application Circuit

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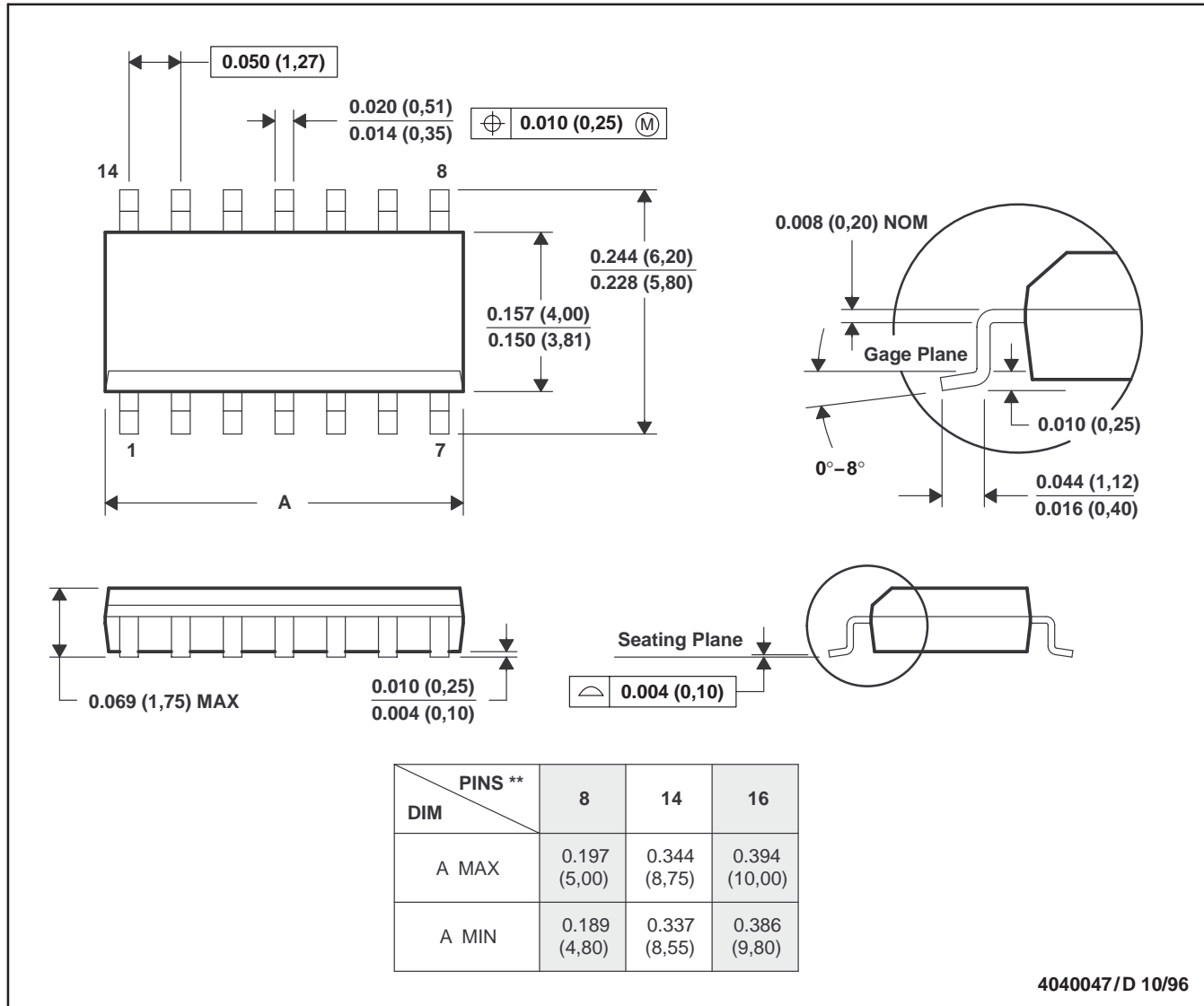
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MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

SN65LBC180A, SN75LBC180A LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

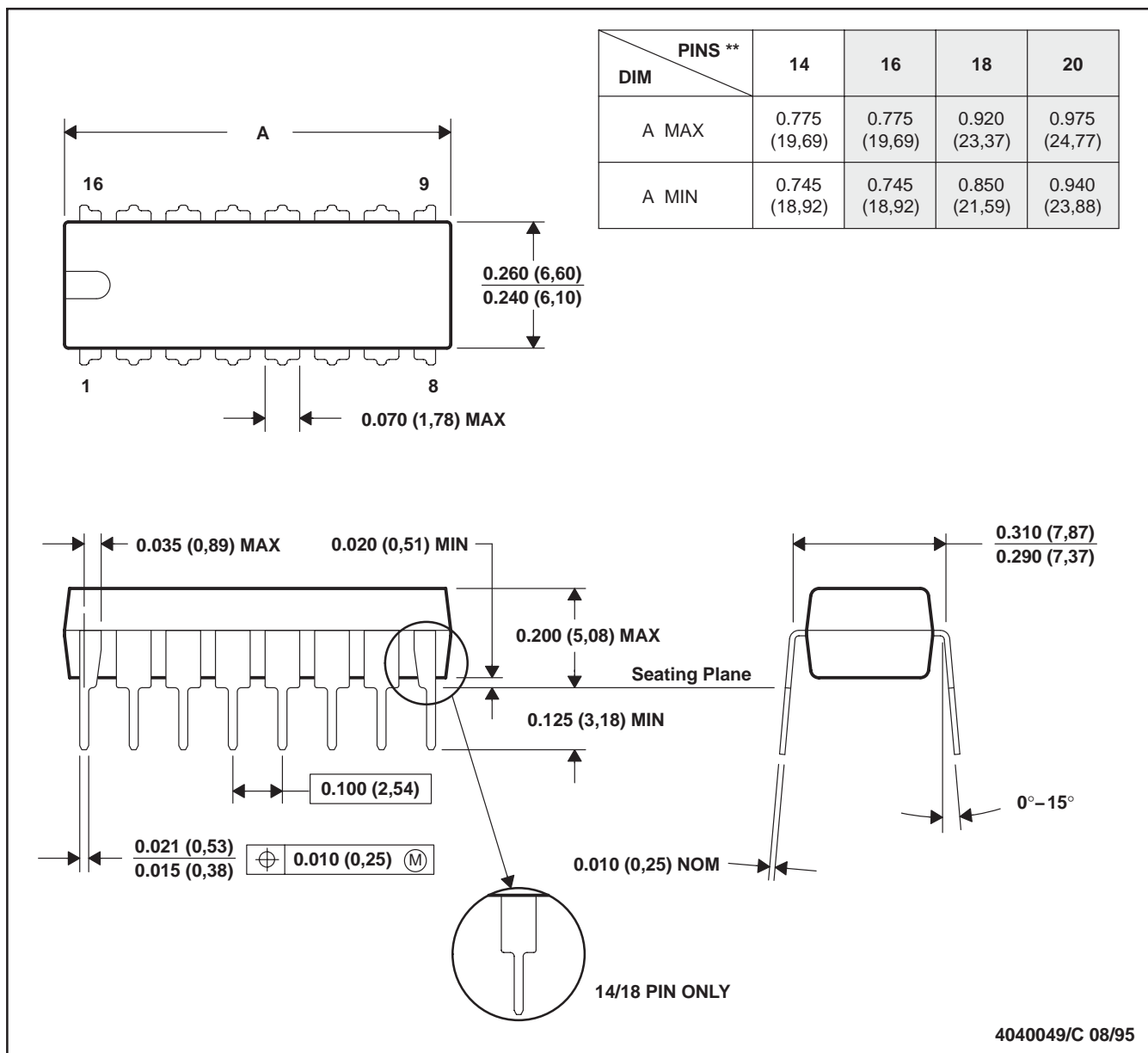
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MECHANICAL DATA

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LBC180AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC180AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN65LBC180ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC180AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC180AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75LBC180ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

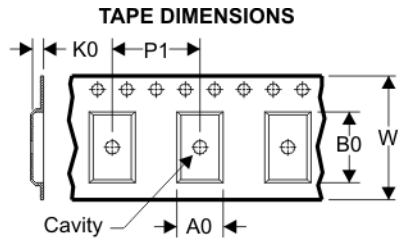
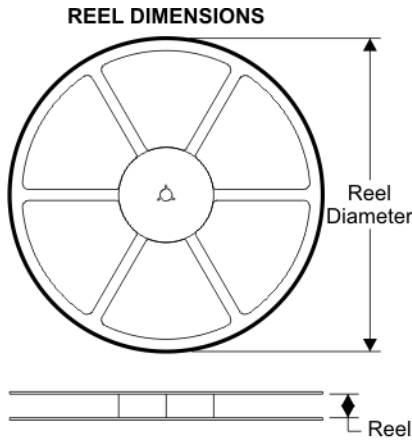
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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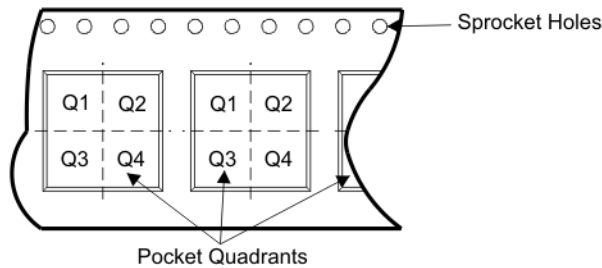
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TAPE AND REEL BOX INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC180ADR	D	14	SITE 27	330	16	6.5	9.0	2.1	8	16	Q1
SN65LBC180ADR	D	14	SITE 60	330	16	6.5	9.0	2.1	8	16	Q1
SN75LBC180ADR	D	14	SITE 27	330	16	6.5	9.0	2.1	8	16	Q1
SN75LBC180ADR	D	14	SITE 60	330	16	6.5	9.0	2.1	8	16	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65LBC180ADR	D	14	SITE 27	342.9	336.6	28.58
SN65LBC180ADR	D	14	SITE 60	346.0	346.0	33.0
SN75LBC180ADR	D	14	SITE 27	342.9	336.6	28.58
SN75LBC180ADR	D	14	SITE 60	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

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