

74LVT125; 74LVTH125

3.3 V quad buffer; 3-state

Rev. 06 — 6 March 2006

Product data sheet

1. General description

The 74LVT125; 74LVTH125 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT125; 74LVTH125 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs ($1OE$, $2OE$, $3OE$ and $4OE$), each controlling one of the 3-state outputs.

2. Features

- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
 - ◆ JESD78: exceeds 500 mA
- ESD protection:
 - ◆ MIL STD 883 method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

3. Quick reference data

Table 1. Quick reference data

$GND = 0 V$; $T_{amb} = 25^{\circ}C$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|--|--|-----|-----|-----|------|
| t_{PLH} | LOW-to-HIGH propagation delay nA to nY | $C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$ | - | 2.7 | - | ns |
| t_{PHL} | HIGH-to-LOW propagation delay nA to nY | $C_L = 50 \text{ pF}$; $V_{CC} = 3.3 \text{ V}$ | - | 2.9 | - | ns |

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Table 1. Quick reference data ...continued

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

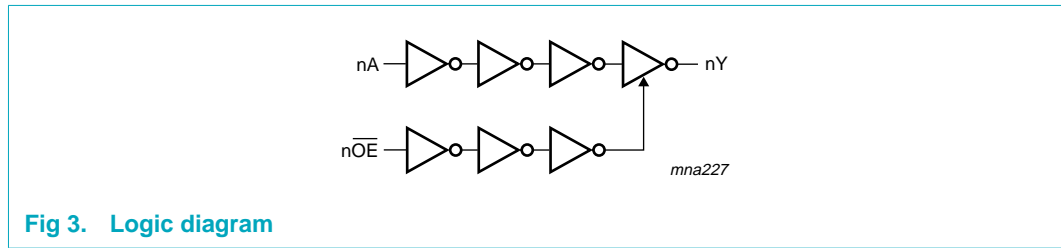
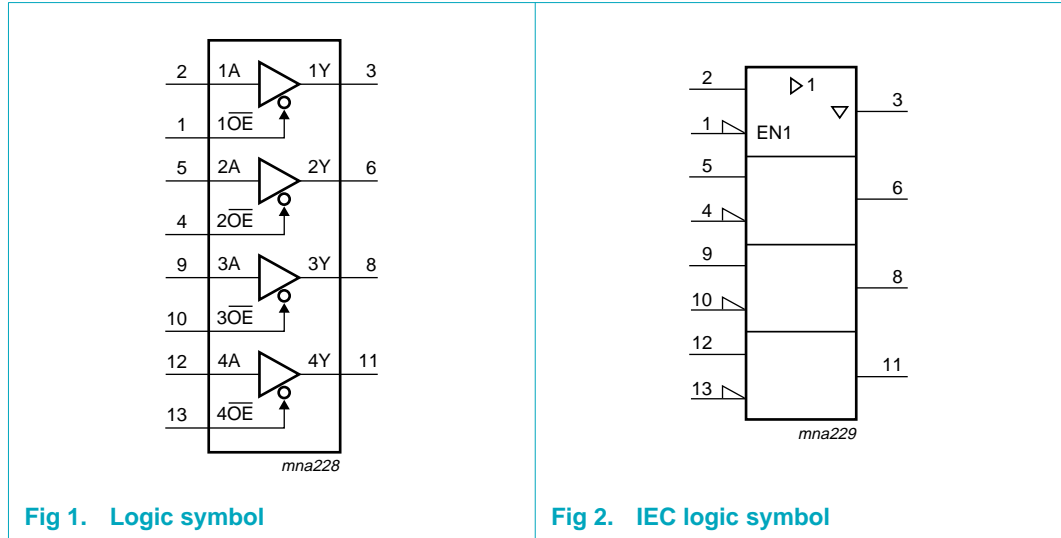
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|---|-----|------|-----|------|
| C_i | input capacitance | $V_I = 0\text{ V or }3.0\text{ V}$ | - | 4 | - | pF |
| C_o | output capacitance | outputs disabled; $V_O = 0\text{ V or }3.0\text{ V}$ | - | 8 | - | pF |
| I_{CC} | quiescent supply current | outputs disabled; $V_{CC} = 3.6\text{ V}$ | - | 0.13 | - | mA |

4. Ordering information

Table 2. Ordering information

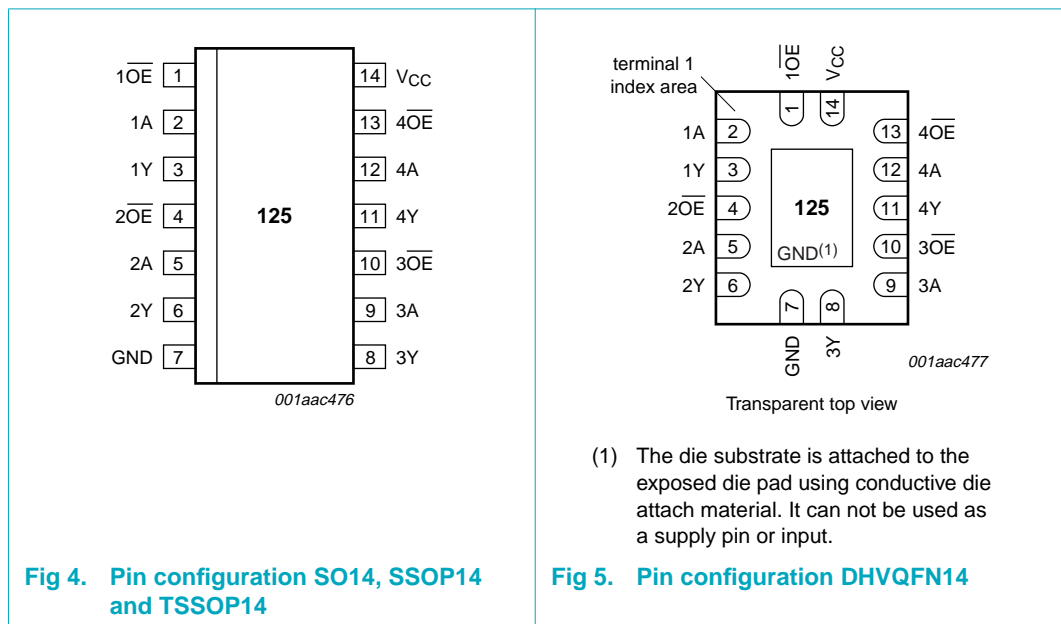
| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVT125D | -40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVT125DB | -40 °C to +85 °C | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74LVT125PW | -40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74LVT125BQ | -40 °C to +85 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74LVTH125D | -40 °C to +85 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
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| 74LVTH125PW | -40 °C to +85 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74LVTH125BQ | -40 °C to +85 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

5. Functional diagram



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|------------------|-----|------------------------------------|
| $1\overline{OE}$ | 1 | 1 output enable input (active LOW) |
| 1A | 2 | 1 data input |
| 1Y | 3 | 1 data output |
| $2\overline{OE}$ | 4 | 2 output enable input (active LOW) |
| 2A | 5 | 2 data input |
| 2Y | 6 | 2 data output |
| GND | 7 | ground (0 V) |
| 3Y | 8 | 3 data output |
| 3A | 9 | 3 data input |
| $3\overline{OE}$ | 10 | 3 output enable input (active LOW) |
| 4Y | 11 | 4 data output |
| 4A | 12 | 4 data input |
| $4\overline{OE}$ | 13 | 4 output enable input (active LOW) |
| V_{CC} | 14 | supply voltage |

7. Functional description

7.1 Function table

Table 4. Function table^[1]

| Control | Input | Output |
|------------------|-------|--------|
| $n\overline{OE}$ | nA | nY |
| L | L | L |
| | H | H |
| H | X | Z |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-----------------------------------|----------|------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | | [1] -0.5 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | - | -50 | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | - | -50 | mA |
| I_O | output current | output in LOW-state | - | 128 | mA |
| | | output in HIGH-state | - | -64 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_j | junction temperature | | [2] - | 150 | °C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|--|-----|-----|-----|------|
| V_{CC} | supply voltage | | 2.7 | - | 3.6 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_{IH} | HIGH-state input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-state input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-state output current | | - | - | -32 | mA |
| I_{OL} | LOW-state output current | none | - | - | 32 | mA |
| | | current duty cycle $\leq 50\%$; $f \geq 1$ kHz | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | 0 | - | 10 | ns/V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---|------------------------------------|---|--|-----------------------|------|------|----|
| T_{amb} = -40 °C to +85 °C^[1] | | | | | | | |
| V _{IK} | input clamping voltage | I _{IK} = -18 mA; V _{CC} = 2.7 V | - | -0.9 | -1.2 | V | |
| V _{OH} | HIGH-state output voltage | I _{OH} = -100 μA; V _{CC} = 2.7 V to 3.6 V | V _{CC} - 0.2 | V _{CC} - 0.1 | - | V | |
| | | I _{OH} = -8 mA; V _{CC} = 2.7 V | 2.4 | 2.5 | - | V | |
| | | I _{OH} = -32 mA; V _{CC} = 3.0 V | 2.0 | 2.2 | - | V | |
| V _{OL} | LOW-state output voltage | V _{CC} = 2.7 V | | | | | |
| | | I _{OL} = 100 μA | - | 0.1 | 0.2 | V | |
| | | I _{OL} = 24 mA | - | 0.3 | 0.5 | V | |
| | | V _{CC} = 3.0 V | | | | | |
| | | I _{OL} = 16 mA | - | 0.25 | 0.4 | V | |
| | | I _{OL} = 32 mA | - | 0.3 | 0.5 | V | |
| I _{LI} | input leakage current | | | | | | |
| | | all input pins | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | 1 | 10 | μA |
| | | control pins | V _{CC} = 3.6 V; V _I = V _{CC} or GND | - | ±0.1 | ±1 | μA |
| | | data pins | V _{CC} = 3.6 V | ^[2] | | | |
| | | V _I = V _{CC} | - | 0.1 | 1 | μA | |
| | | V _I = 0 V | - | -1 | -5 | μA | |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 1 | ±100 | μA | |
| I _{HOLD} | bus hold current data input | V _{CC} = 3 V | ^[3] | | | | |
| | | V _I = 0.8 V | 75 | 150 | - | μA | |
| | | V _I = 2.0 V | -75 | -150 | - | μA | |
| | | V _{CC} = 0 V to 3.6 V | | | | | |
| | | V _I = 3.6 V | ±500 | - | - | μA | |
| I _{EX} | external current into output | output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V and V _{CC} = 3.0 V | - | 60 | 125 | μA | |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care | ^[4] - | ±1 | ±100 | μA | |
| I _{OZ} | OFF-state output current | V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} | | | | | |
| | | output HIGH: V _O = 3.0 V | - | 1 | 5 | μA | |
| | | output LOW: V _O = 0.5 V | - | -1 | -5 | μA | |
| I _{CC} | quiescent supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | | |
| | | outputs HIGH | - | 0.13 | 0.19 | mA | |
| | | outputs LOW | - | 2 | 7 | mA | |
| | | outputs disabled | ^[5] - | 0.13 | 0.19 | mA | |

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|---|-----|-----|-----|------|
| ΔI_{CC} | additional quiescent supply current | per input pin; $V_{CC} = 3.3 \text{ V to } 3.6 \text{ V}$; [6] - one input at $V_{CC} - 0.6 \text{ V}$ and other inputs at V_{CC} or GND | - | 0.1 | 0.2 | mA |
| C_i | input capacitance | $V_I = 0 \text{ V or } 3.0 \text{ V}$ | - | 4 | - | pF |
| C_o | output capacitance | outputs disabled; $V_O = 0 \text{ V or } 3.0 \text{ V}$ | - | 8 | - | pF |

[1] Typical values are measured at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ }^\circ\text{C}$.[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2 \text{ V}$ to $V_{CC} = 3.0 \text{ V}$ to 3.6 V a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25 \text{ }^\circ\text{C}$ only.[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

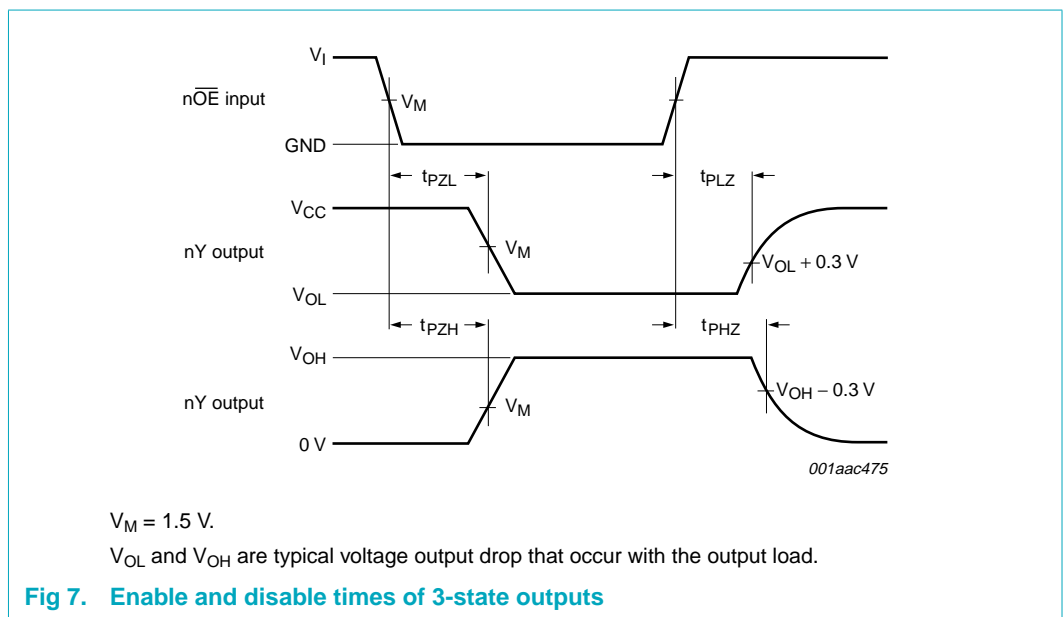
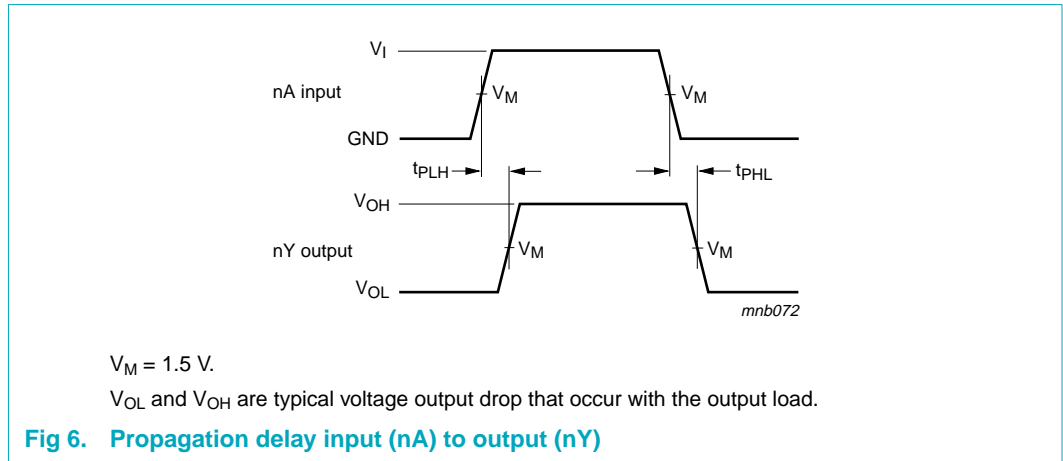
11. Dynamic characteristics

Table 8. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|--|-----|-----|-----|------|
| $T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ [1] | | | | | | |
| t_{PLH} | LOW-to-HIGH propagation delay nAn to nY | see Figure 6 | | | | |
| | | $V_{CC} = 2.7 \text{ V}$ | - | - | 4.5 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.7 | 4.0 | ns |
| t_{PHL} | HIGH-to-LOW propagation delay nAn to nY | see Figure 6 | | | | |
| | | $V_{CC} = 2.7 \text{ V}$ | - | - | 4.9 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 2.9 | 3.9 | ns |
| t_{PZH} | output enable time \overline{nOE} to nY | see Figure 7 | | | | |
| | | $V_{CC} = 2.7 \text{ V}$ | - | - | 6.0 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.0 | 3.4 | 4.7 | ns |
| t_{PZL} | output enable time \overline{nOE} to nY | see Figure 7 | | | | |
| | | $V_{CC} = 2.7 \text{ V}$ | - | - | 6.5 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.1 | 3.4 | 4.7 | ns |
| t_{PHZ} | output disable time \overline{nOE} to nY | see Figure 7 | | | | |
| | | $V_{CC} = 2.7 \text{ V}$ | - | - | 5.7 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.8 | 3.7 | 5.1 | ns |
| t_{PLZ} | output disable time \overline{nOE} to nY | see Figure 7 | | | | |
| | | $V_{CC} = 2.7 \text{ V}$ | - | - | 4.0 | ns |
| | | $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ | 1.3 | 2.6 | 4.5 | ns |

[1] Typical values are at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ }^\circ\text{C}$.

12. Waveforms



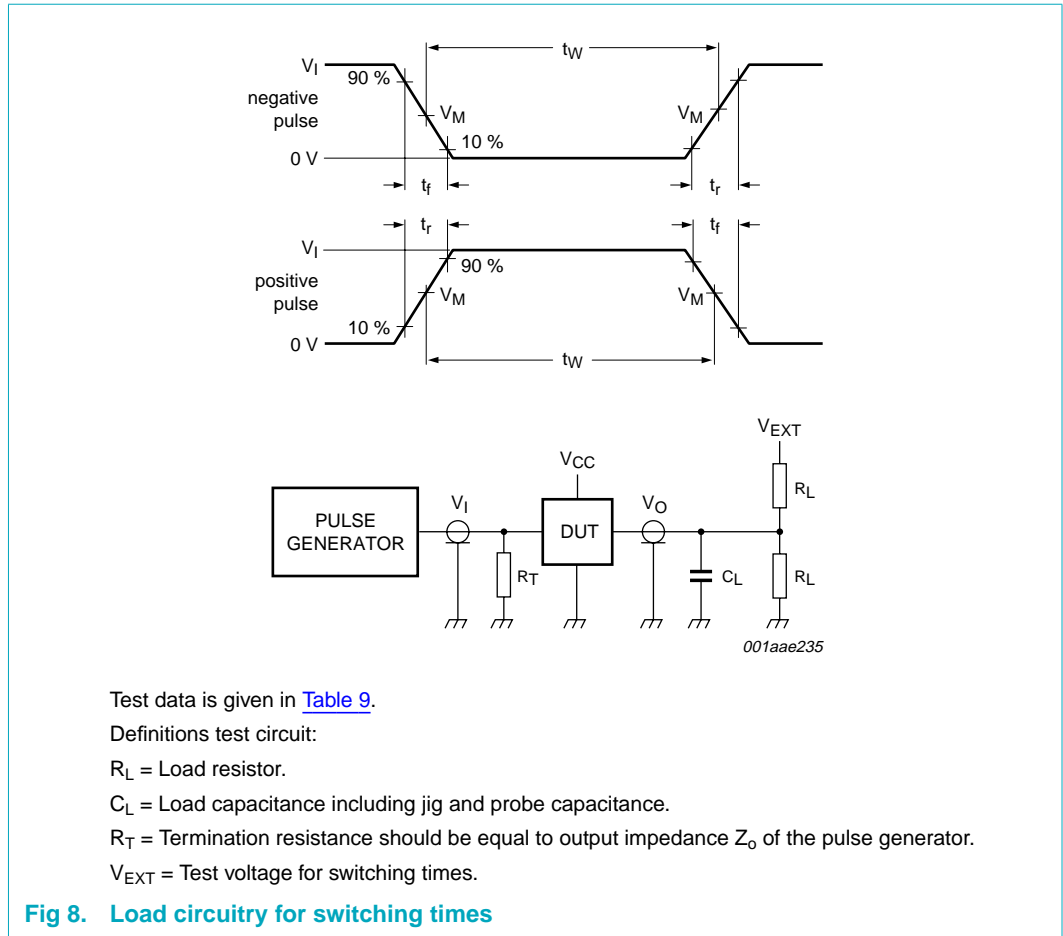


Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|---------------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 2.7 V | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V | open |

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

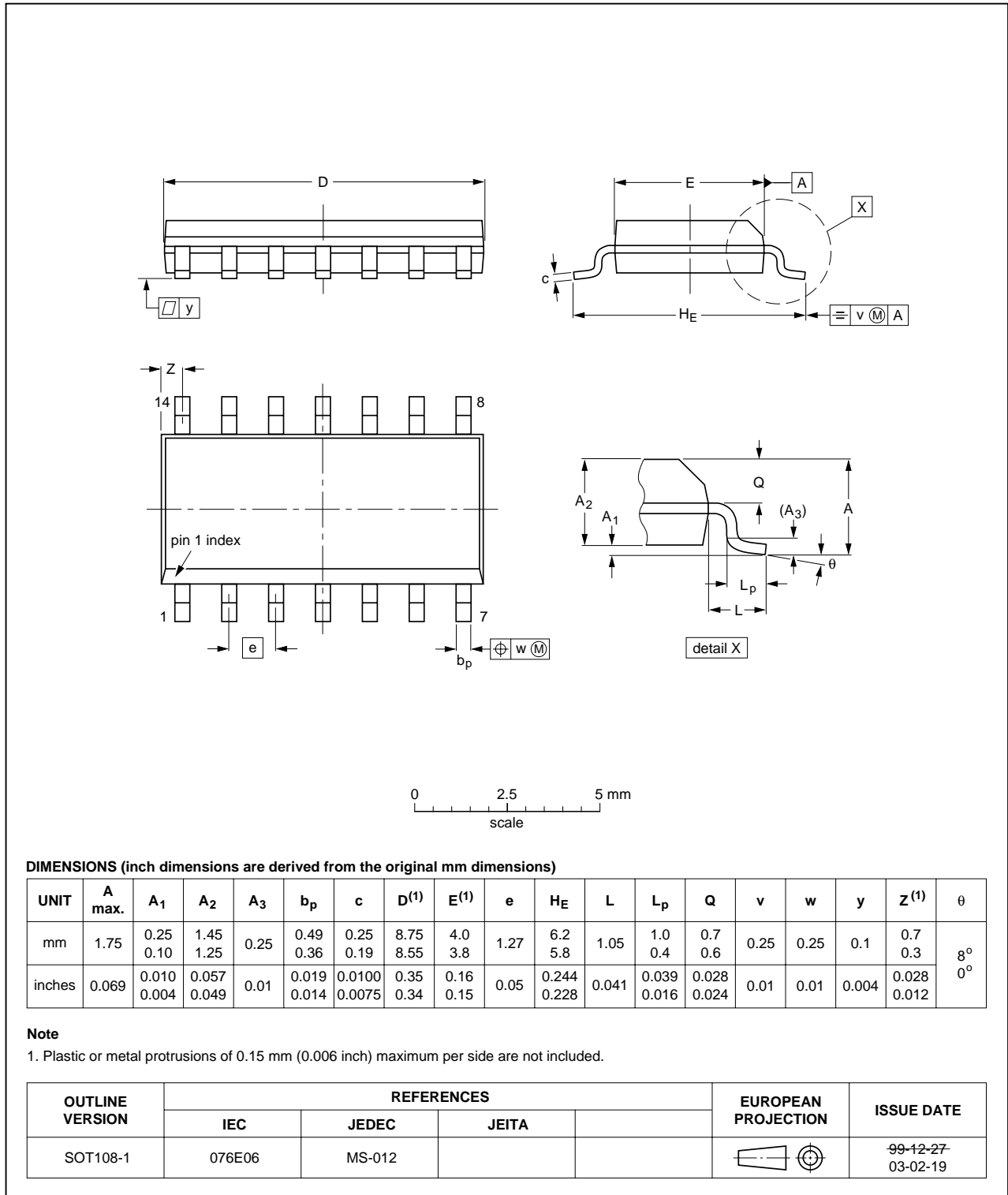


Fig 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

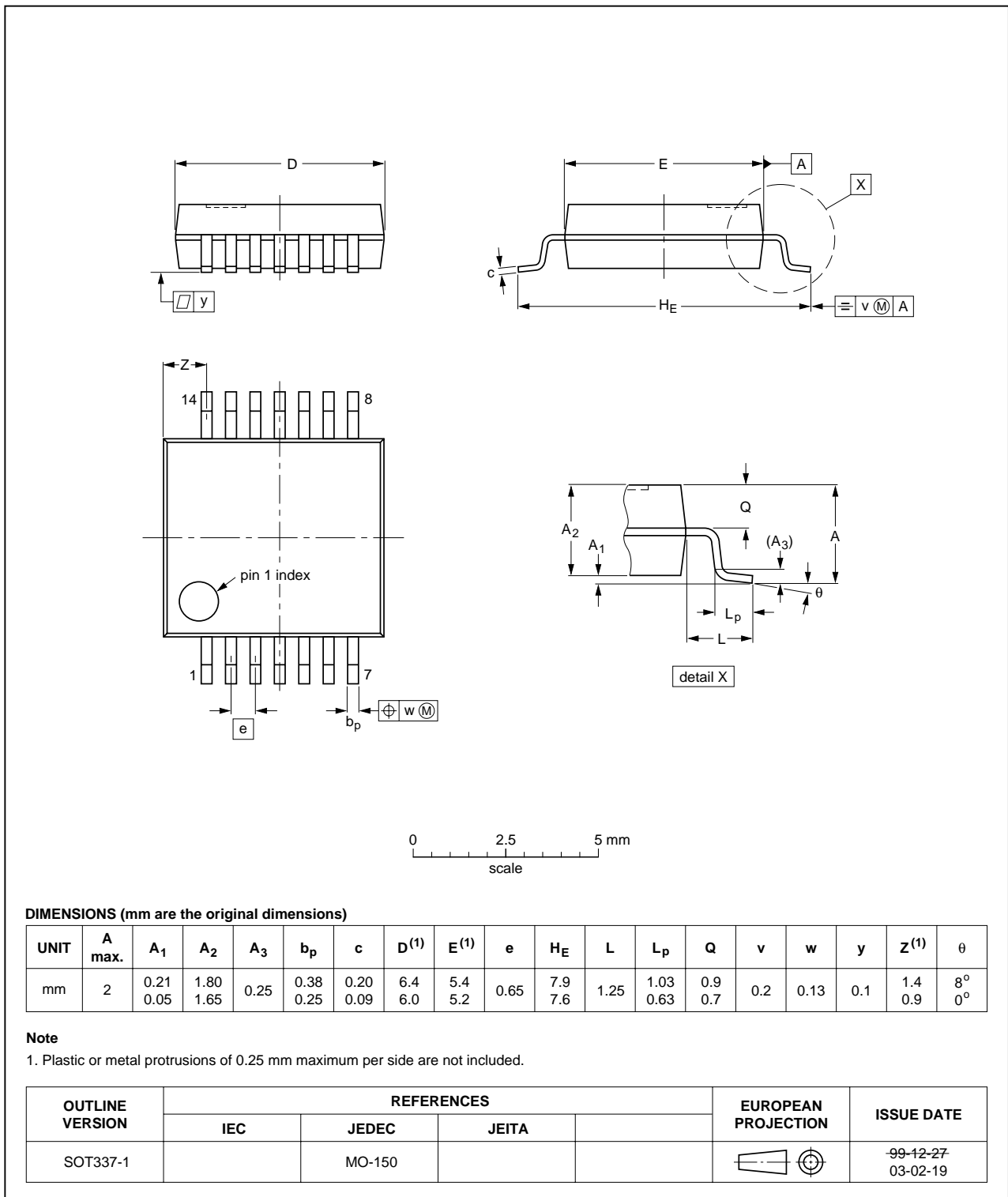


Fig 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

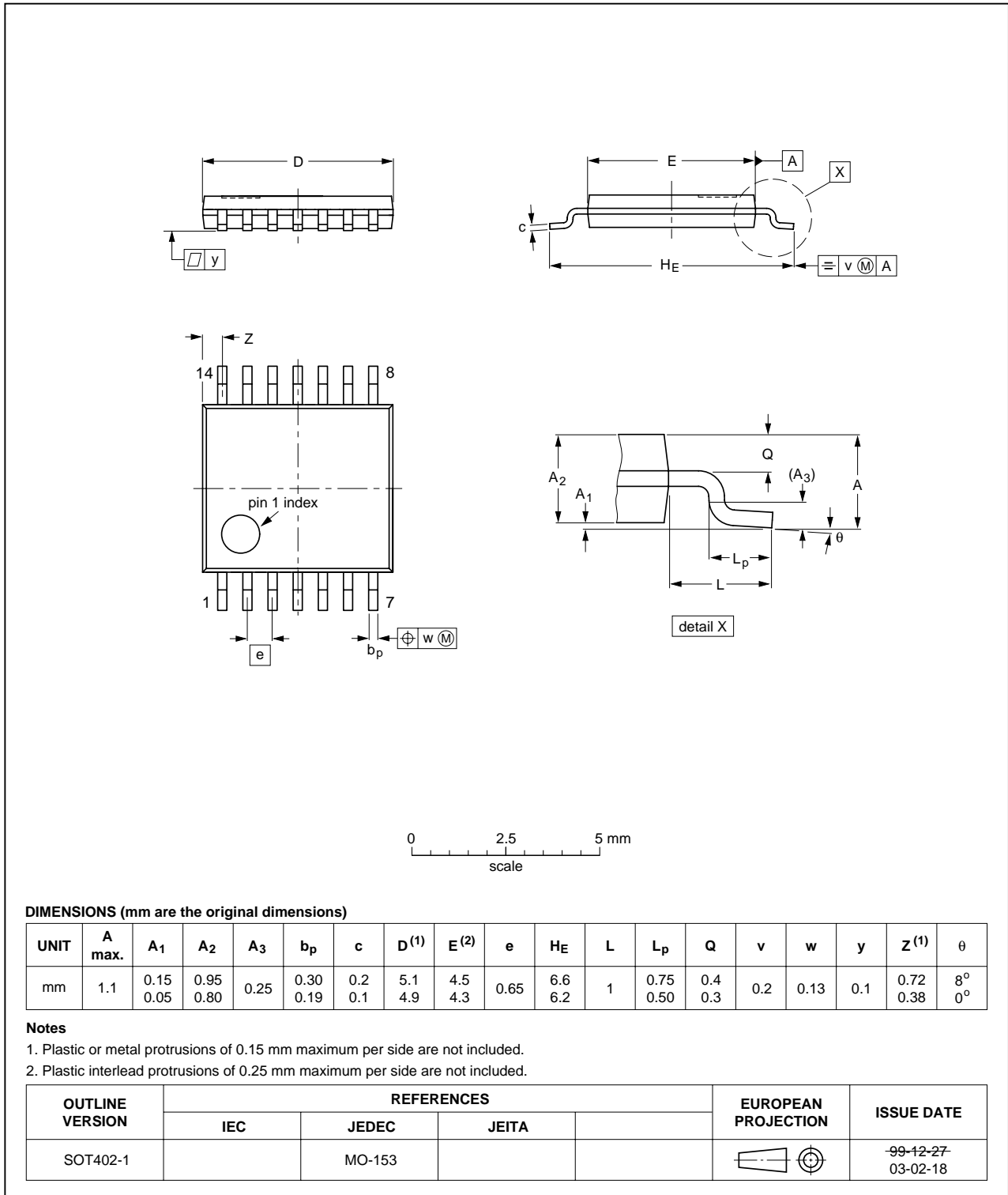


Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

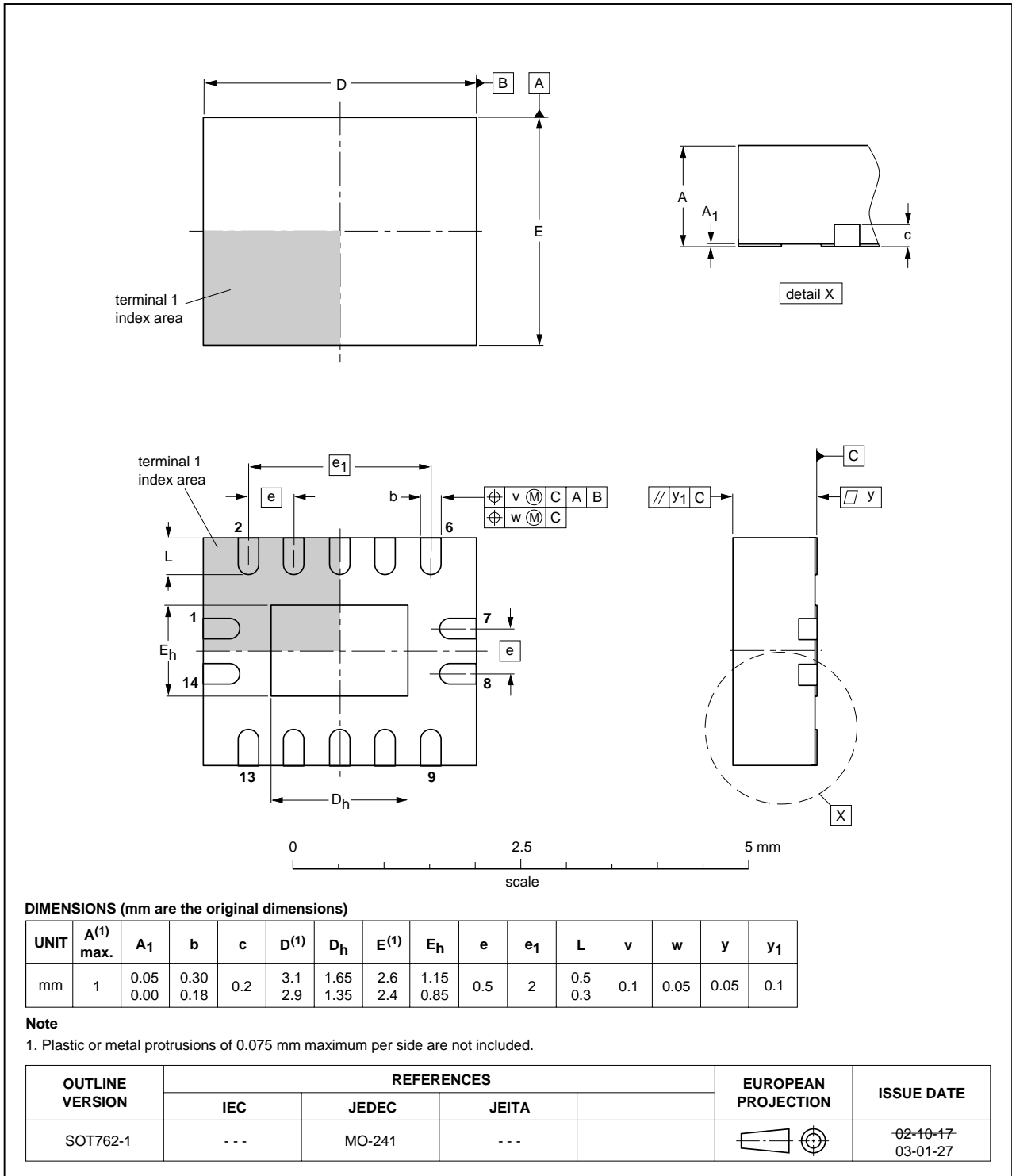


Fig 12. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| TTL | Transistor-Transistor Logic |

15. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|---|-----------------------|---------------|-----------------------------|
| 74LVT_LVTH125_6 | 20060306 | Product data sheet | - | 74LVT125_5 (9397 750 14703) |
| Modifications: | <ul style="list-style-type: none"> Section 4: Added type numbers 74LVTH125D, 74LVTH125DB, 74LVTH125PW and 74LVTH125BQ. | | | |
| 74LVT125_5 | 20050210 | Product data sheet | - | 74LVT125_4 (9397 750 14552) |
| 74LVT125_4 | 20050207 | Product data sheet | - | 74LVT125_3 (9397 750 13535) |
| 74LVT125_3 | 20040624 | Product data sheet | - | 74LVT125_2 (9397 750 03514) |
| 74LVT125_2 | 19980219 | Product specification | - | 74LVT125_1 |
| 74LVT125_1 | - | - | - | - |

16. Legal information

16.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
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| Product [short] data sheet | Production | This document contains the product specification. |

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