Integrated Device Technology, Inc.

79S440
Evaluation Board

Hardware User's Manual

Version 1.1
March 1997

This revised manual provides a product description, updated installation instructions, theory of operation, design notes, and six schematic drawings for the 79S440 evaluation board.

Summary of Contents

Chapter 1, "79S440 Description and Installation Instructions," provides an overview on the 79S440 evaluation board features and includes a physical layout diagram, specification summary, and 64- or 32-bit system interface installation instructions. This chapter includes a section on getting started quickly.

Chapter 2, "Theory of Operation and Design Notes," discusses the functional operation of the 79S440 evaluation board. This chapter includes the jumper or switch settings for R4640 or R4650 CPU selection as well as a section that provides information on R4700, R4640, and R4650 clock structure differences.

Chapter 3, "Schematics," includes six schematic drawings on the 79S440 evaluation board.

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List of Tables and Figures

Integrated Device Technology, Inc.

Introduction

The IDT79S440 is an evaluation board. It is a small module that supports the R4650 and the R4640 on a single printed circuit board (PCB). The S440 allows the system designer to evaluate the performance of either CPU without modification to the existing design. The S440 plugs directly into the PGA socket of the R4700 in any board, including the 79S465 evaluation board. Figure 1.1 shows a block diagram of the 79S440. The board's physical layout is shown in Figure 1.2 on page 1-2.

Overview Of Features

Major features of the 79S440 include:
- R4650/R4640 highly integrated RISController CPU support
- R4640/R4650 clock generation circuitry
- 3.3V and 5V operation
- 32-bit system interface support for R4640 and R4650
- 64-bit system interface support for R4650
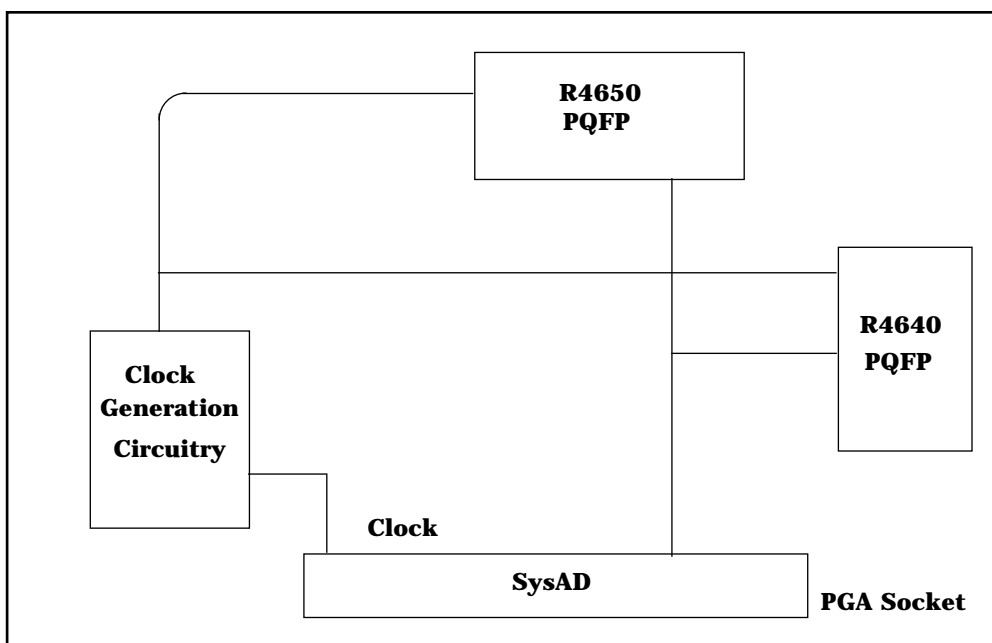
Figure 1.1 79S440 Block Diagram

Explanation of Features

The 79S440 is configured to plug directly into the 79S465 evaluation board. It supports the R4650 PQFP footprint as well as the PQPF footprint of the R4640. Selection between the two CPU options is accomplished through hardware jumpers that are not readable by software.

The 79S440 can be used to evaluate system performance of either the R4650 or the R4640. The S440 supports 32-bit system interface for the R4640 and R4650 as well as 64-bit system interface for the R4650. The 79S440 draws power from the 79S465 evaluation board through the PGA socket it is plugged into and supports 5V operations.
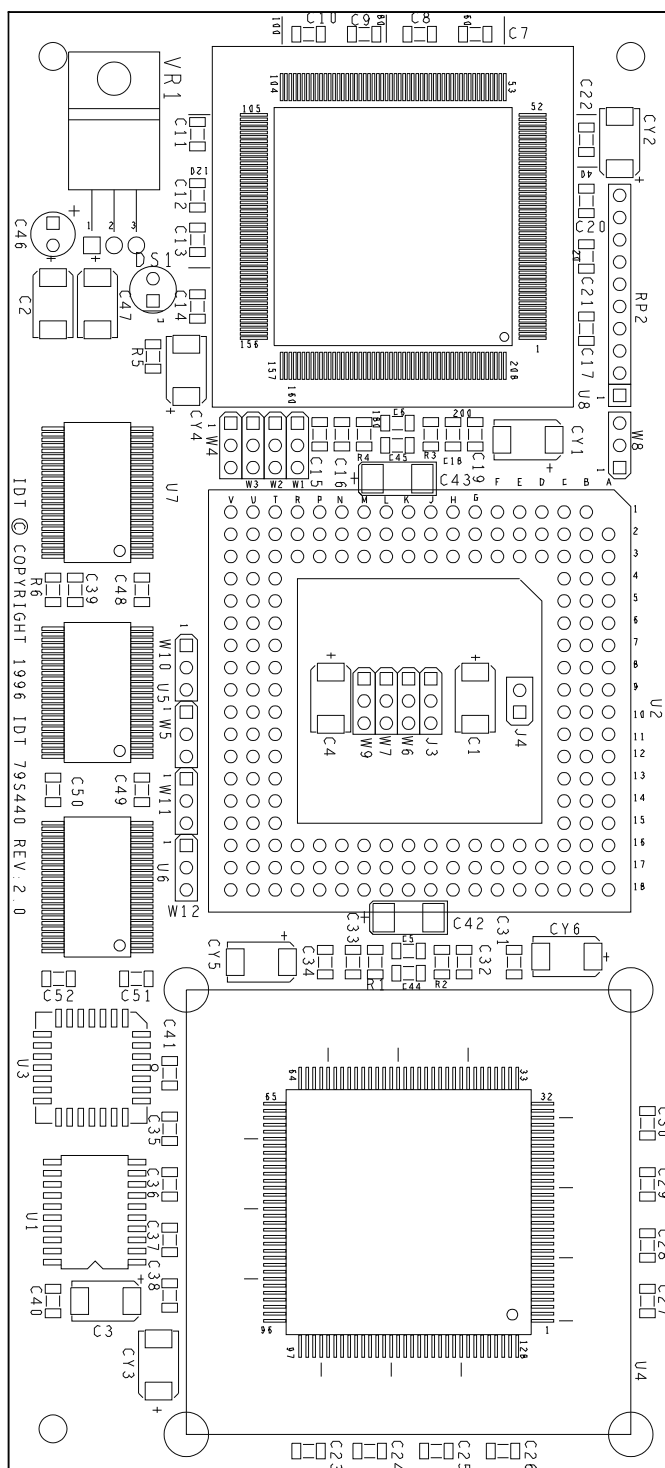
Figure 1.2 Physical Layout of 79S440

Specification Summary

Part Number
- IDT79S440

RISController
- IDT79R4640-133
- IDT79R4650-133

Physical Dimensions
- Rectangular form factor: 6.5" x 3.0"

Operating Temperature
- 0-50°C

Relative Humidity
- 5% - 95%

Power Supply
- 5.0V ± 5%, 10 Amps typical

79S440 Installation_64-bit System Interface*

Note: When using the R4650 in 64-bit mode, the 64-bit system interface must be used.

The S440 attachment board uses a 133 MHz R4640/R4650 CPU while the bus interface runs at 44 MHz. These settings are different from the default settings of the S465 evaluation board, which executes at 100/50 MHz.

The primary installation steps for the 64-bit system interface are as follows:

1. a. Plug the S440 attachment card into the PGA socket provided, replace the S465's crystal (U9) with a 44.33 MHz crystal, and change the default clock multiplier switch settings to x3 as follows:

Switch	Description
S2.3	On
S1.2	On
S1.3	Off

b. For the 64-bit system interface, memory size jumpers must be set to the 64-bit SRAM and DRAM size configurations that are listed in Table 1.1 and Table 1.2.

SRAM SIZE	
0 Mbytes	**4 Mbytes in 64 bit-mode**
S1.5 = OFF	S1.5 = OFF
S1.6 = OFF	S1.6 = OFF
S1.7 = OFF	S1.7 = ON
S1.8 = don't care	S1.8 = OFF
J1 = don't care	J1 = 2-3
J2 = don't care	J2 = 2-3
J3 = don't care	J3 = 2-3
J4 = don't care	J4 = 2-3
J5 = don't care	J5 = 2-3
J6 = don't care	J6 = 2-3

Table 1.1 SRAM Size Selections

DRAM SIZE	
0 Mbytes	**4 Mbytes in 64 bit-mode**
S1.5 = OFF	S1.5 = ON
S1.6 = OFF	S1.6 = ON
S1.7 = OFF	S1.7 = OFF
J9 = don't care	J9 = 1-2
J10 = don't care	J10 = 1-2
J11 = don't care	J11 = 1-2
J12 = don't care	J12 = 1-2
W1 = don't care	W1 = 1-2
W2 = don't care	W2 = 1-2
S1.8 = don't care	S1.8 = ON

Table 1.2 DRAM Size Selections

2. Power for the S440 is drawn from the S465 board through the connectors it is plugged into. For instructions on connecting the S465 board to a power source, see Chapter 2 of the *79S465 Evaluation Board Hardware User's Manual*.

3. The S440 board is shipped with the jumpers set—as shown in Table 1.6—to select the R4650 CPU as the default configuration.

 * The 79S465 board is initially configured for 64-bit system interface.

79S440 Installation_32-bit System Interface*

Note: When using the R4640 or the R4650 in 32-bit mode, the 79S465 board's 32-bit system interface must be used.

The S440 attachment board uses a 133 MHz R4640/R4650 CPU while the bus interface runs at 44 MHz. These settings are different from the default settings of the S465 evaluation board, which executes at 100/50 MHz.

The primary installation steps for 32-bit system interface are as follows:

1. a. Plug the S440 attachment card into the PGA socket provided, replace the S465's xtal (U9) with a 44.33 MHz crystal, and change the default clock multiplier switch settings to x3 as follows:

Switch	Description
S2.3	On
S1.2	On
S1.3	Off

b. For the 32-bit system interface option, modifications to the S465 evaluation board are required as follows:

- Memory size jumpers must be changed according to the 32-bit SRAM and DRAM size configurations, as listed in Table 1.3 and Table 1.4.

SRAM SIZE	
0 Mbytes	**2 Mbytes in 32 bit-mode**
S1.5 = OFF	S1.5 = OFF
S1.6 = OFF	S1.6 = OFF
S1.7 = OFF	S1.7 = ON
S1.8 = don't care	S1.8 = OFF
J1 = don't care	J1 = 2-3
J2 = don't care	J2 = 2-3
J3 = don't care	J3 = 1-2
J4 = don't care	J4 = 2-3
J5 = don't care	J5 = 2-3
J6 = don't care	J6 = 1-2

Table 1.3 SRAM Size Selections

DRAM SIZE	
0 Mbytes	**2 Mbytes in 32 bit-mode**
S1.5 = OFF	S1.5 = ON
S1.6 = OFF	S1.6 = ON
S1.7 = OFF	S1.7 = OFF
J9 = don't care	J9 = 2-3
J10 = don't care	J10- = 2-3
J11 = don't care	J11 = 2-3
J12 = don't care	J12 = 2-3
W1 = don't care	W1 = 2-3
W2 = don't care	W2 = 2-3
S1.8 = don't care	S1.8 = ON

Table 1.4 DRAM Size Selections

- Switch S2.6 must be changed to the ON position as listed in Table 3.12.
- Existing controllers must be replaced with the 79S467 kit (EPLDs for 32-bit system support).

2. Power to the S440 is drawn from the S465 board through the connectors it is plugged into. For instructions on connecting the S465 board to a power source, see Chapter 2 of the *79S465 Evaluation Board Hardware User's Manual.*

3. The S440 board is shipped with the jumpers set to select the R4650 CPU as the default configuration. To select the R4640 CPU, set the jumpers as shown in Table 1.5.

Jumper	**R4640**
W5	2-3
W7	2-3
W8	1-2
W9	1-2
W10	2-3
W11	2-3
W12	2-3

Table 1.5 Switch Configurations for R4640 CPU Selection

* The 79S465 board is initially configured for 64-bit system interface.

Getting Started Quickly

The 79S440 board is shipped ready to run with the R4650 CPU selected. Prior to shipment, the jumpers are configured to the default settings listed in Table 1.6 and do not require further modification or setup.

Two basic requirements for the board to run are:
- A power supply of +5V with at least 10 Amp of current
- A 79S465 evaluation board

Table 1.6 lists the default jumper settings on the 79S440 attachment board.

Jumper or Switch	Default	Description
W1	2-3	5V supply
W2	2-3	5V supply
W3	2-3	5V supply
W4	2-3	5V supply
W7	1-2	R4640 Off
W8	2-3	R4650 On
W9	2-3	R4650 On
W10	1-2	R4650 On
W11	1-2	R4650 On
W12	1-2	R4640 Off
J3	2-3	Use buffered clock
W5	1-2	R4640 Off

Table 1.6 79S440 Default Jumper Settings

Logic Analyzer Connections

A Corelis Logic Analyzer Pod, part #PI-R4650-Q, can be mounted on the top of the R4650 CPU, or part #PI-R4640-Q can be mounted on top of the R4640. Both parts can be used to connect to the HP Logic Analyzer, part #16500B.

The following sections provide information on the functional operation of the 79S440 attachment board. For detailed schematics, refer to Chapter 3.

Jumper or Switch Settings

The 79S440 can be configured to work in different modes. As discussed in the following sections, changing CPUs, clocking schemes, SyncIn Paths, or CPU voltages can be accomplished through a combination of jumpers.

CPU Selections

The S440 can support different CPUs in different footprints, R4650 or R4640. The S440 is shipped with the R4640 soldered on the board, the R4650 is socketed to the board. Only one CPU can be activated at a time through different jumper selections, as listed in Table 2.1

Jumpers	R4650 ON	Jumpers	R4640 ON
W5	1-2	W5	2-3
W7	1-2	W7	2-3
W8	2-3	W8	1-2
W9	2-3	W9	1-2
W10	1-2	W10	2-3
W11	1-2	W11	2-3
W12	1-2	W12	2-3

Table 2.1 R4650/R4640 CPU Options

R4640/R4650 Master Clock Selection

The R4640's master clock can be selected to be delayed by either 1 or 2 buffers, with respect to **TClock**. Enabling the desired buffer delay can be completed as shown in Table 2.2.

Jumper	Option	Description
W6	2-3	2 buffer delay
W6	1-2	3 buffer delay

Table 2.2 Master Clock/Buffer Delay Selections

R4640/R4650 Clock Selection
On the S440, it is possible to provide the input clock to the CPU through a copy of the **TClock** from the main board the S440 is plugged into, as shown in Table 2.3.

Jumper	Option	Description
J3	2-3	Use buffered clock for R4640/R4650 generated on S440
	1-2	Use copy of **TClock** from main board

Table 2.3   R4640/R4650 Clock Selections

Voltage Selection
The S440 board works only at 5V; however, voltage options on the board can be selected as shown in Table 2.4.

Jumper	Option	Description
W1	1-2	3.3V
	2-3	5V
W2	1-2	3.3V
	2-3	5V
W3	1-2	3.3V
	2-3	5V
W4	1-2	3.3V
	2-3	5V

Table 2.4 79S440 Voltage Selections

32-bit System Interface Selection
Both the R4640 and the R4650 can be configured to work in a 32-bit system bus interface. The R4650 can also be configured to work in a 64-bit system interface. This configuration selection is made at reset time through the CPU mode bit. Because the S440 is designed to support either the 32- or 64-bit system bus interface, no special modifications are required.

However, because of its 64-bit bus interface default setting, modifications to the S465 evaluation board are necessary. To change the S465 eval board to a 32-bit system bus interface, a new set of EPLD controllers—part #79S467—must be installed.   In addition, several of the S465's jumpers and switches must also be changed. For more information on changes to the jumpers and switches, refer to Chapter 3 of the *79S465 Evaluation Board Hardware User's Manual*.

Theory of Operation
The R4640 and R4650 are bus and upwardly software compatible to the ORION family. In the 64-bit bus mode, the R4650 maintains the same bus protocol as the R4700. In the 32-bit external bus, both the R4640 and R4650—when in 32-bit mode—maintain the R4700's bus protocol, but it has been extended to accommodate the 32-bit bus width.

The external bus protocol refers to the handshaking between the CPU and the external logic as well as timing for the various bus transactions. System logic and ASICs designed to interface with the R4700 must be

modified to support the R4640's or the R4650's 32-bit bus interface. Similarly, the external clock structure of the R4640 and the R4650 is different from that of the R4700, which provides greater flexibility to the system designer.

Clock Structure Differences

The R4700, R4640, and the R4650 have different input and output clock structures but maintain the same bus protocol.

R4700 Clocks

The R4700 implements the same clock structure as the first generation 64-bit devices, such as the R4000 and the R4400. The R4700 uses a single input clock—**MasterClock**—that is doubled internally by one PLL to generate the pipeline clock (PClk). A second PLL doubles **MasterClock** and then divides it by a constant number—from 2 to 8 as programmed during reset—to generate the output clocks—**RClock**, **TClock**, **MasterOut,** and **SyncOut**. These output clocks are used by the system logic to interface with the R4700 during read and write operations.

Figure 2.1 illustrates the architecture of the R4700's internal clock distribution tree. A more detailed explanation of these clocks is presented in the *IDT79R4600 & IDT79R4700 ORION Processor Hardware User's Manual*.
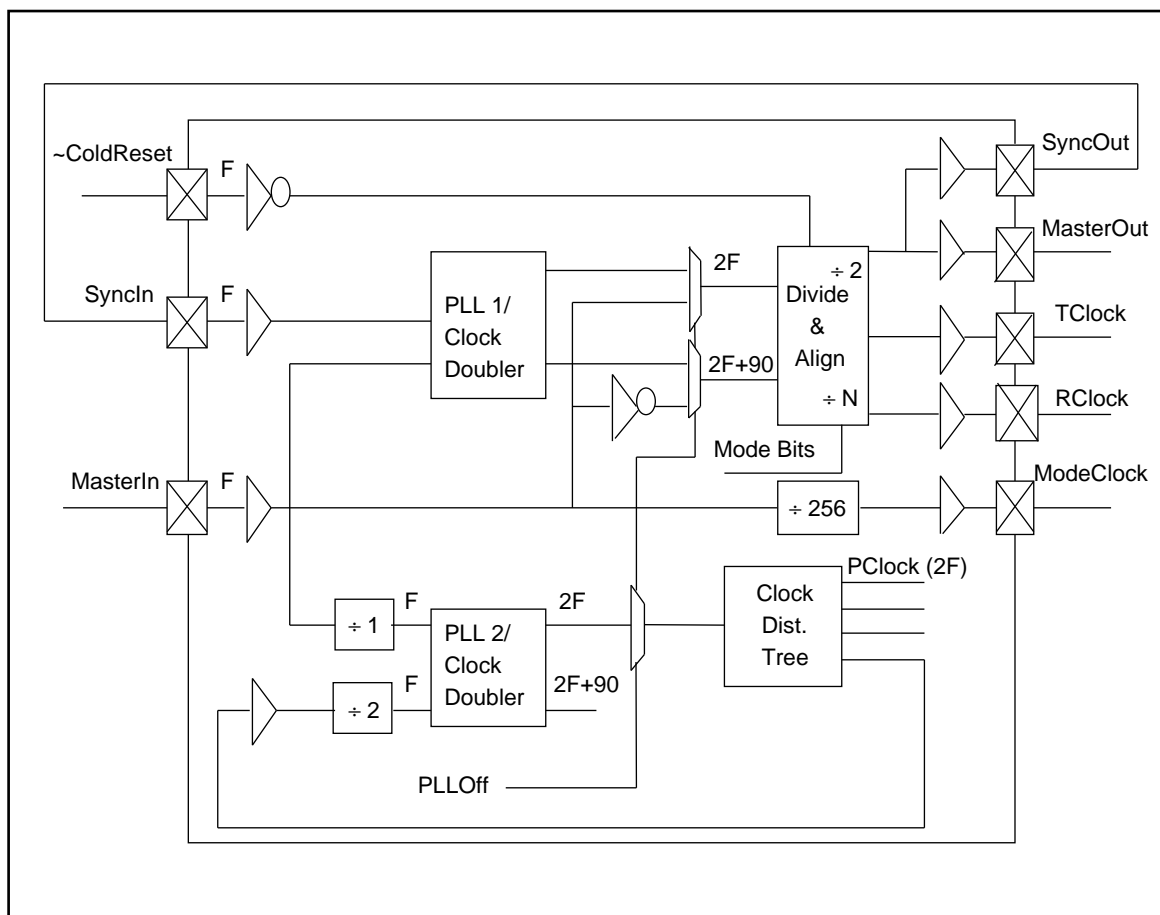

Figure 2.1 R4700 Internal Clock Circuitry

R4640 and R4650 Clocks

The architecture for the internal clock distribution tree of the R4640 and the R4650 is different from that of the R4700. Both the R4640 and R4650 use only a single input clock—**MasterClock**. **MasterClock** is multiplied internally using a single PLL by a constant number—from 2 to 8 as programmed during reset—to generate the pipeline clock (PClk). The R4640 and the R4650 do not generate an output clock. The **MasterClock** should be used as the system control logic clock. Both the R4640 and R4650 guarantee that the interface signals with the external system logic will be sampled using the rising edge of **MasterClock**.

An advantage of the R4640 and the R4650 is that the **MasterClock** frequency may be kept small. Similarly, the absence of output clocks from the R4640 and R4650 reduces the device's power consumption. This architecture allows several systems to synchronize using a single input clock at any frequency without being locked by the clocks provided by the CPU. This is an advantage for backplane applications where the input clock is provided from the backplane to several plugged-in cards.

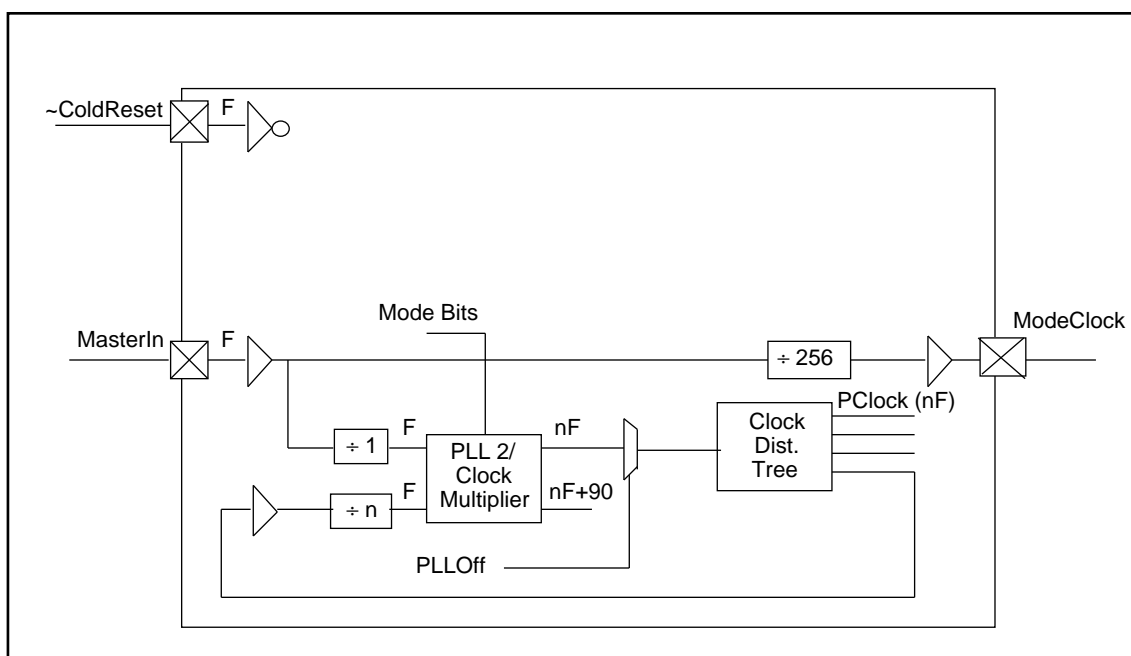Figure 2.2 illustrates the internal clock circuitry of the R4640 and R4650.

Figure 2.2 R4640/R4650 Internal Clock Circuitry

Generating R4700-Compatible Clocks

Systems using the R4650 in 64-bit system interface can use logic and ASIC previously developed to work with R4700, without modifications.

With modifications, to support the 32-bit bus width interface of the R4640 and the R4650, systems using the R4640 or R4650 can also use the logic and ASIC previously developed to work with the R4700. This mechanism requires the generation of **MasterOut**, **SyncOut**, **RClock,** and **TClock**, or alternatively, a subset of these according to the system requirements. More detail on these clocks is provided in the *IDT79R4600 & IDT79R4700 ORION Processor Hardware User's Manual*.

The clock distribution tree must be implemented at the input of the R4640 and R4650. The R4700's external clock generation is illustrated in Figure 2.3. In this case, a buffer is used to delay the input clock to R4640 or R4650. The output of the buffer is equivalent to **TClock**, **MasterOut,** and **SyncOut**. The input of the buffer is equivalent to **RClock**. For a tight delay between **RClock** and **TClock**, it is better to use a buffer that has a very narrow window for the minimum and the maximum input to output delays.

An example of this clock buffer type is the Motorola MC10H645 buffer, which guarantees a single nanosecond difference between the minimum and the maximum delays. In systems that use only the R4640 or only the R4650, the **SyncOut** to **SyncIn** path is irrelevant, since neither the R4640 the R4650 nor the system logic use these clocks. However, depending on the architecture of the system, the **MasterOut** could be relevant.
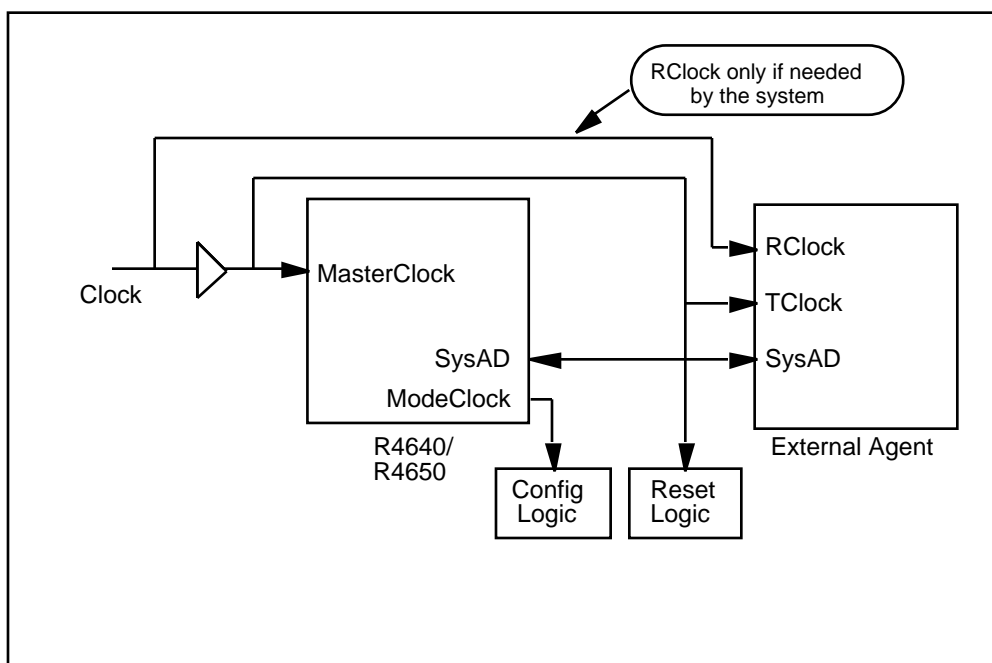
Figure 2.3 R4640/R4650 External Clock Generation Circuitry

Schematics

This chapter contains six schematic drawings for the 79S440 board.

R4640-MODULE PGA PLUG

INTEGRATED DEVICE TECHNOLOGY, INC.
179 PGA R4600 PLUG

R4640-MODULE-CLOCK-DISTRIBUTION & BUFFERING

INTEGRATED DEVICE TECHNOLOGY, INC.

R4640 & R4650 CLOCK DISTRIBUTION

DWG NO. S440

REV 2.0

DATE: 3-11-1996_10:48

SHEET 3 OF 6

SIZE RNN

P3_MODULE CPU BYPASS CAPACITORS

INTEGRATED DEVICE TECHNOLOGY, INC.

CAPACITORS

SIZE: CR
DWG NO.: S440
REV: 2.0

DATE: 2-28-1996_9:54
SHEET 4 OF 6

3 – 7

INTEGRATED DEVICE TECHNOLOGY, INC.

VOLTAGE REGULATOR

SIZE: CR   DWG NO.: S440   REV: 2.0

DATE: 2-28-1996_9:53   SHEET 6 OF 6

Power On LED - 3.3V

VCC3.3   NET_030   R5 330   GND

DS1 LED-GRN

5V to 3.3V Regulator

THICK Trace for 3.3 V

VCC3.3

LT1086CT-3.3 VR1

VIN VOUT GND

VCC

C46 100F 50V Aluminum

C47 22F 20V Tantalum

GND

NOTE: Allow room for the Heat Sink when doing the layout of the 3.3V regulator