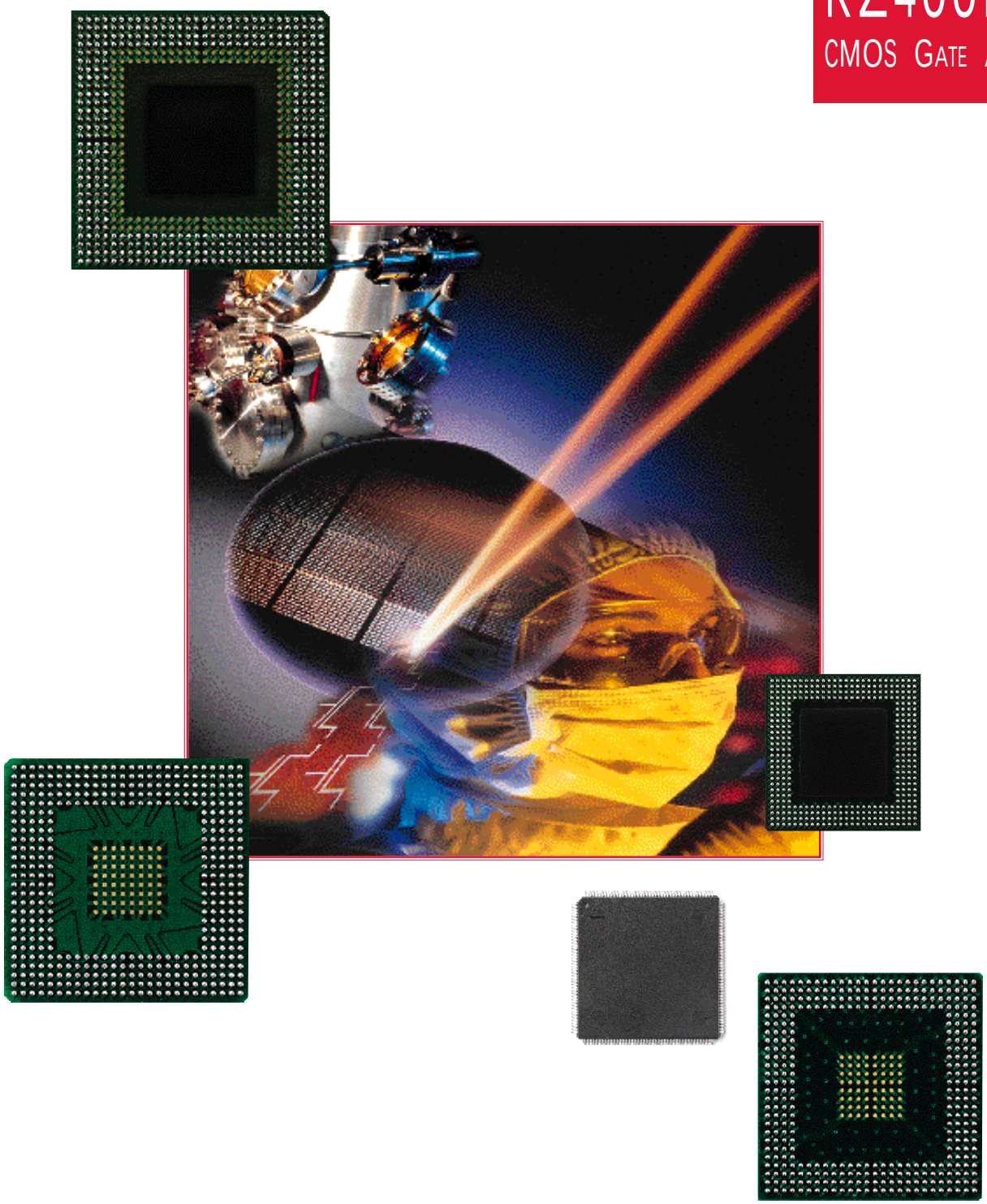
HIGH-DENSITY
HIGH-PERFORMANCE

KZ400GH
KZ400EH

CMOS GATE ARRAYS



KAWASAKI LSI

Overview

With the KZ400GH/KZ400EH CMOS Series, Kawasaki LSI offers an advanced generation of 0.35 micron gate arrays and embedded arrays. The Series provides cost-effective solutions for high-speed, highly integrated, yet low voltage applications in today's networking, computer and multimedia markets. Appropriate product applications include high-speed data routers/switches, 3D graphics and video encoders/decoders.

To satisfy these requirements, the KZ400GH/KZ400EH Series uses Kawasaki LSI's 0.35 µm DLM, TLM or QLM process technologies and an advanced cell architecture. This achieves high density, high speed and low power dissipation—comparable to standard cell products—while maintaining the quick turnaround of gate arrays. The KZ400GH/KZ400EH Series supports complex designs of up to 2 million gates and a system clock frequency as high as 200MHz. A variety of I/O buffers are available, including LVTTL, GTL+, HSTL, SSTL, LVDS, PCI, USB, Pseudo-ECL and OSC.

The KZ400GH/KZ400EH Series offers a wide selection of compilable memories such as metal-programmable RAMs and all-layer RAMs/ROMs. This helps you optimize designs, because the best compilable memory for a specific application may be chosen. Also, ASIC-DRAM is under development for graphics, image processing and networking applications which require the large capacity of memory buffers. For high-performance and fast time-to-market designs, the KZ400GH/KZ400EH Series offers various high-performance cores such as CPU (and its peripherals), JPEG, CAM (Content Addressable Memory), and analog functions (PLL, A/D Converter, D/A Converter).

You can also maximize the chip-level and system-level performance for complex designs by using Kawasaki LSI's design methodology. It includes rich libraries of accurately characterized cells, timing-driven synthesis, clock distribution schemes, test insertion, and a floor planner with interaction to synthesis on industry-standard tools.

Key Features

- 0.35 µm drawn channel length (0.29 µm effective)
- Double/triple/quadruple layer metal CMOS technologies
- High-density and high-performance cell architecture comparable to standard cell solutions
- Gate array architecture with 20 masterslices for fastest time-to-market designs
- Embedded arrays offered for high-speed complex designs
- Customized array options available for high volume designs
- Wide selection of I/O buffers: LVTTL, GTL+, HSTL, SSTL, LVDS, PCI, USB, PECL, OSC
- 3.3V or 2.5V operation voltage
- I/O drive: 2~24 mA
- Low power dissipation: 0.63 µW/MHz/gate at 3.3V
- Propagation delay of 130 ps (2NAND power gate, F.O.= 2)
- Clock skew management: PLL and clock distribution methodologies
- Six types of metal-programmable SRAM
- High-density (22K bits/mm^2) all-layer SRAM up to 256K bits
- Testability tools such as SCANTEST, IDDQ and JTAG
- Design system with open I/F to various front-end platforms
- ISO9001 certified on manufacturing and design quality since 1994

Core Library

The KZ400GH/KZ400EH Series library offers more than 300 robust macrocells, providing a variety of high-performance synthesis options. The macrocells are composed of different sized transistors, enabling you to optimize the design for speed, power and density. The macrocells have input slew-rate-dependent loading and offset delay, and non-linear output load-dependent delay parameters to produce accurately characterized timing. This results in the maximum performance achievable from the process technology. The core library is supplied for many industry-standard tools and HDL's, including Verilog HDL, VHDL, Synopsys, Mentor, ViewLogic and others.

I/O LIBRARY

The I/Os in the KZ400GH/KZ400EH Series are powered by 3.3 or 2.5V supplies. Kawasaki LSI also provides 5V-tolerant I/Os, which can receive signals from a 5V-powered device, yet output 3.3 or 2.5V. Slew-rate controlled buffers, input with pull-up, pull-down resistors and open drain outputs are also available. The KZ400GH/KZ400EH Series also supports high-speed and low-voltage swing I/Os such as LVTTL, GTL+, Pseudo-ECL (PECL), High-Speed Transceiver Logic (HSTL), Stub Series Terminated Logic (SSTL) and Low-Voltage Differential Signal (LVDS). For computer and peripheral applications, Kawasaki LSI support industry-standard buses with its PCI Bus I/O buffers and USB I/O buffers.

MEMORIES

Metal-Programmable Memory

The KZ400GH/KZ400EH Series has two types of compiled metal-programmable memory: High-Density (HD) RAM and Low-Power (LP) RAM. HD RAMs feature high performance and high density up to 7.13K bits/mm^2. HD RAMs are suitable for applications that need high-performance, high-density memories. The total capacity of an HD RAM is up to 36K bits per block.

LP RAMs feature high-performance and very low-power. The total capacity of an LP RAM is 16K bits. As an application example, LP RAMs are suitable for register files. Table 1 shows the performance and specifications of HD and LP RAMs.

Table 1 KZ400GH/KZ400EH Metal-Programmable Memories

		Total Bits	Word	Bit	Density	Access Time
High-Density RAM	1-p Async.	64~36K	64~4K	1~36	~7,125 bits/mm^2	2.6ns*
	2-p Async.	32~36K	32~4K	1~36	~3,454 bits/mm^2	3.1ns*
	1-p Sync	64~36K	64~4K	1~36	~6,890 bits/mm^2	2.9ns*
	2-p Sync.	32~36K	32~4K	1~36	~3,402 bits/mm^2	3.2ns*
Low-Power RAM	1-p Async.	1~16K	1~128	1~128	~3,369 bits/mm^2	2.4ns**
	2-p Async.	1~16K	1~128	1~128	~3,369 bits/mm^2	2.4ns**

*Access time is for 512-word x 8-bit configuration in typical condition.
**Access time is for 32-word x 8-bit configuration in typical condition.

All-Layer Memory

In the KZ400EH Series, higher density embedded memories are generated by all-layer memory compilers. All-layer memories feature extremely high-density, large-capacity, and high-performance, while offering low-power dissipation. The largest memory capacity is 256K bits for SRAM, and 1M bit for ROM. The bit density of 22K bits/mm^2 for the single-port SRAM is extremely high for an ASIC memory.

These Kawasaki LSI all-layer memories are tuned for high-performance, memory-intensive applications such as image processing, ATM switches, etc. If lower power is required, an Address Transition Detection (ATD) circuit can be optionally added. ATDdetects the address transition, then starts accessing the memory. After a certain period of time, it turns off the entire memory operation to cut off the DC current and prepare for the next address transition automatically. This option is very effective for power reduction when the operating frequency is less than 100MHz in SRAMs, and less than 50MHz in ROM.

Kawasaki LSI is now developing ASIC-DRAM as one of the all-layer memories offered; the size of a 256K bit block is targeted to be 60% of that of the all-layer single-port RAM, with a density of about 35K bits/mm^2. A 100MHz high-speed page mode operation can be achieved. Table 2 shows the performance specifications of all-layer memories.

Table 2 KZ400EH All-Layer Memories

		Total Bits	Word	Bit	Density	Access Time
SRAM	1-p Async.	16~256K	16~16K	1~64	~22,000 bits/mm^2	3.4ns*
	1-p Sync.	16~256K	16~16K	1~64	~22,000 bits/mm^2	2.4ns*
	2-p Sync.	16~64K	16~4K	1~64	~8,500 bits/mm^2	3.8ns*
ROM	1-p Sync.	64~1M	64~128K	1~128	~100,000 bits/mm^2	4.1ns*
DRAM***	1-p Sync.	2K~256K	1K~64K	1~64	35,000 bits/mm^2	20ns ($\overline{RAS}$)/4ns($\overline{CAS}$)**

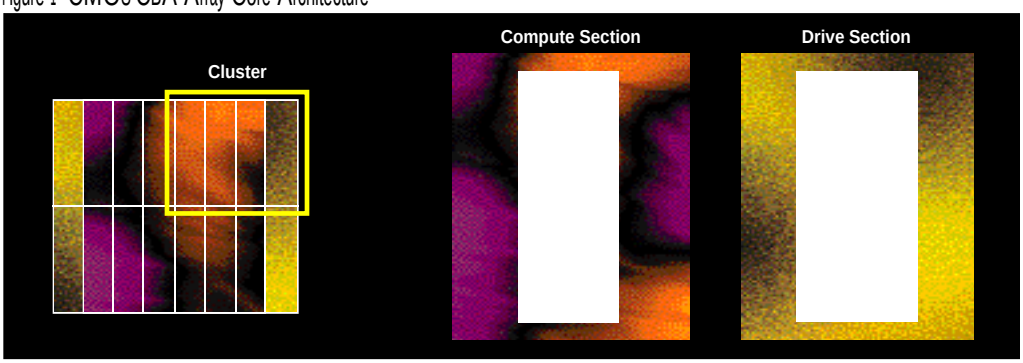
*The numbers are for 512-word x 8-bit configuration in typical condition.
**The numbers are row access time/column access time under worst case conditions.
***Under development

Array Architecture

The core cell cluster of the KZ400GH/KZ400EH Series as shown in Figure 1, is based on the CMOS-CBA® architecture licensed by Synopsys, Inc. It consists of two different unit cells: a compute cell and a drive cell. A compute cell contains four small PMOS and four small NMOS that are optimized for building logic and memory. A drive cell contains two large PMOS and two large NMOS that provide sufficient drive for global nets or large fanout. Statistical analysis has determined that a cluster of three compute cells and one drive cell provides optimal density for many design styles. In the conventional gate array, on the other hand, the size of the core cell is uniformly large to provide sufficient drive for the large fanout. Yet this results in the low gate density, as most nets have a small number of fanouts and do not require high drive.

With CBA, the smaller gate load and smaller wire load significantly improves performance, power and density compared to conventional gate arrays. These features are comparable to the same generation standard cell architecture. With this optimized cell architecture, KZ400GH/KZ400EH arrays achieve a gate density of up to 9,500 usable gates/mm^2.

Figure 1 CMOS-CBA Array Core Architecture



Array Family

Table 3 shows the 20 base arrays in the KZ400GH/KZ400EH Series. Array utilization depends on design, and typically varies from 33 to 46% in DLM (Double Layer Metal) technology, from 50 to 69% in TLM (Triple Layer Metal) technology, and from 66 to 90% in QLM (Quadruple Layer Metal). A compute cell or a drive cell is counted as a gate. Kawasaki LSI offers an option to compile and fabricate a custom sized array for high-volume designs.

Table 3 KZ400GH/KZ400EH Masterslice Selection

Array Index	Pad Count (by Pad Pitch)		Raw Gates	Usable Gates		
	Standard	Fine		DLM	TLM	QLM
006	108	112	61,500	28,100	42,200	55,300
009	128	136	87,600	38,200	57,400	76,500
013	152	160	126,700	52,600	78,900	105,200
016	168	180	156,800	63,100	94,700	126,300
019	184	196	190,100	74,400	111,600	148,900
027	216	232	266,300	99,000	148,500	198,100
031	232	252	309,100	112,300	168,400	224,600
036	248	268	355,200	126,100	189,200	252,300
040	264	284	404,500	140,600	210,900	281,200
046	280	304	462,400	157,100	235,700	314.200
050	292	316	501,300	167,900	251,900	335,900
058	312	340	577,600	190,600	288,800	381,200
064	328	356	640,000	211,200	320,000	422,400
069	340	372	685,600	226,200	342,700	452,400
077	360	392	774,400	255,500	387,200	511,100
108	424	464	1,081,600	356,000	540,800	713,800
144	488	536	1,440,000	475,200	720,000	950,400
207	584	640	2,073,600	684,200	1,036,800	1,368,500
262	656	720	2,624,400	866,000	1,312,200	1,732,100
307	708	780	3,069,500	1,012,900	1,534,700	2,025,800

Typical design both for DLM and TLM
A compute cell or a drive cell is counted as a gate.

MEGAFUNCTIONS AND ANALOG FUNCTIONS

Kawasaki LSI supports a number of megafunctions other than the compiled memories in the KZ400GH/KZ400EH Series. These megafunctions minimize design time and maximize performance of complex system chips. The KC80 is a very high-performance CPU core that is binary-compatible with the Zilog Z80®. A JPEG core is also available for imaging and data compression applications. Kawasaki LSI also offers an Address Processor Core or Content Addressable Memory (CAM) for high-performance broadband network and internetworking applications.

There are a number of analog functions under development for video signal processing applications, system clock management and frequency synthesis. These functions include 8 and 10-bit A/D converters, 8-bit D/A converters, operational amplifiers, comparators, Phase Locked Loops (PLL) and Voltage Controlled Oscillators (VCO).

CLOCK DISTRIBUTION

For maximum system performance, it is important to minimize not only board-level system clock skew, but also chip-level clock skew on a die. Kawasaki LSI provides several clocking methodologies to minimize on-chip clock skew.

Clock Buffer

This method is the most popular and has been well utilized in older technologies. It is simple and effective in cases where the number of clocked elements are less than a few hundred, or the clock skew requirement is not stringent. In the KZ400GH/KZ400EH Series, up to 200 flip-flops (depending on frequency) can be driven in a single stage, with special buffers for clocking.

Clock Tree Synthesis (CTS)

Clock Tree Synthesis is an automatic way to build a clock tree by balancing the far end delay with local buffers at the most appropriate physical location. The clock tree is synthesized with low driving inverters or buffers. Clock Tree Synthesis (CTS) is efficient when the number of clocked instances is very large or the clock skew requirement is stringent.

Clock Trunk with CTS

The clock trunk is a wide metal line which is connected to a special clock driver. It provides lower skew and a shorter delay than a clock buffer or CTS. In the KZ400GH/KZ400EH Series, a strong clock driver can be built with multiple special buffers for clocking, or can be configured with an I/O clock driver, which typically uses 2 to 3 I/O pads.

Packages

Kawasaki LSI has internal ceramic packaging capabilities, enabling accelerated prototype deliveries. Subcontractors are used for most of the cost-effective plastic packages that are popular in high volume designs. Kawasaki LSI also maintains close development relationships with key vendors, ensuring that the next generation of industry standard Ball Grid Arrays (BGA) will be offered to customers whose designs exceed 300 pins. Package offerings are shown in Table 4.

Table 4 KZ400GH/KZ400EH Package Selection

Package	Pin Count											
Skinny DIP	42	64										
PQFP	44	64	80	100	120*	128	144*	160*	176	208*	240*	304*
LQFP (1.4 mm thick body)	64	80	100	128	144	160	176	208				
PBGA	256	304	352	416	480	576						
TBGA	256	304	352	416	480	576	672					
PGA	144	180	208	256	280							

*Drop-in heat spreader available for high power dissipation

Test Methodology

To ensure a high-quality device, it is important to implement a test strategy with high fault coverage. Kawasaki LSI's test methodology for the KZ400GH/KZ400EH Series includes the following test solutions.

Internal Full Scan Testing

Internal Full Scan Testing is one of the most powerful test methodologies for automatic development of test vectors, achieving more than 95% stuck-at fault coverage for large synchronous designs. The Synopsys Test Compiler, which automatically performs testability rule checking, scan chain insertion and ATPG (Automatic Test Pattern Generation).

IDDQ Testing

IDDQ Testing is an effective methodology which detects various types of silicon defects without area or performance overhead. This methodology is supported by measuring the device's quiescent power-supply current on functional vectors selected by CM-iTest® from CrossCheck, a part of Duet Technologies, Inc. This test provides an easy way to improve the fault coverage of an ad-hoc test strategy.

JTAG (IEEE 1149.1 Boundary Scan Testing)

JTAG is supported by inserting boundary scan circuits into the system logic and providing test vectors and BSDL for the boundary scan logic. The TAP controller and associated logic is transparently inserted into the customer's netlist.

Process Monitoring

Process monitoring is performed by adding an AC measurement circuit into the device and measuring the AC delay. This AC measurement verifies that the device can operate at a required frequency.

Fault Simulation

Fault simulation is supported using the Cadence Verifault-XL simulator, which allows you to rapidly obtain fault coverage information for the applied test vectors.

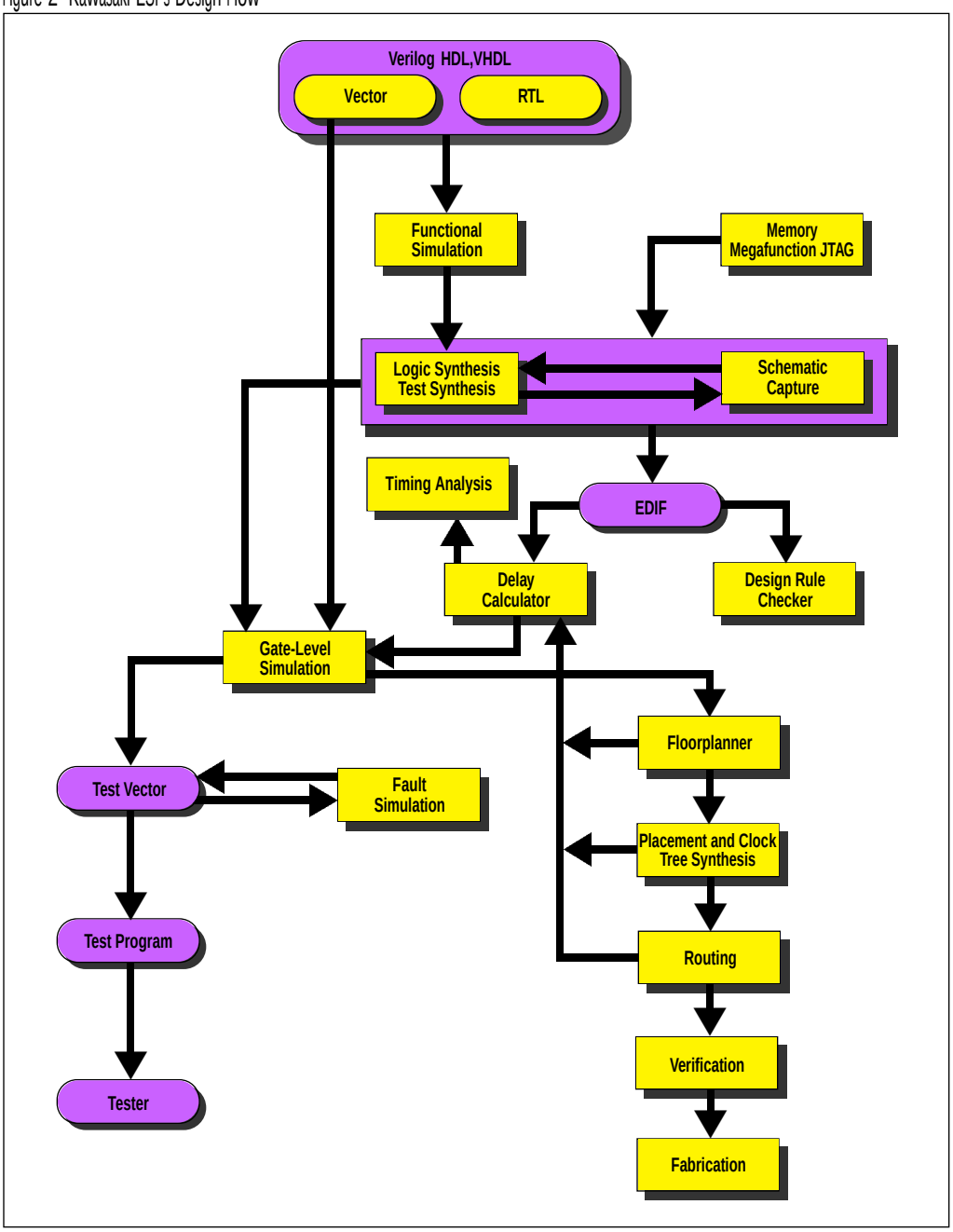
DESIGN SYSTEM

Kawasaki LSI's integrated top-down design flow is shown in Fig. 2. It allows you to start either with VHDL or Verilog-HDL, or from the gate-level, and choose from a wide assortment of schematic capture programs. Kawasaki LSI supports popular EDA tools, from companies such as Synopsys, Cadence, Mentor Graphics and ViewLogic.

Kawasaki LSI's Design Rule Checker and Delay Calculator can read EDIF netlists. Thus you have a choice of either VSS, Verilog, QuickSim II, ViewSim, V-System or IKOS Voyager, to read the delay files generated by the Delay Calculator for gate-level simulation. An accurate delay calculation method is provided, accounting for not only output-load-dependent delay, but also input-slew-rate-dependent offset delay, input-slew-rate-dependent loading delay and interconnect delay caused by wire resistance. This advanced calculation methodology, coupled with control of the physical layout, results in the implementation of the highest performance and most accurate designs.

The interfaces to these tools are industry-standard formats such as Verilog-HDL, VHDL, EDIF, SDF, PDEF and WGL, making it very easy for designers to migrate their designs to Kawasaki LSI's technologies. The design sign-off golden simulator is Verilog.

Figure 2 Kawasaki LSI's Design Flow



Electrical Characteristics

Tables 5 through 7 show the electrical characteristics of the KZ400GH/KZ400EH Series.

Table 5 Recommended Operating Conditions

Parameter	Symbol	Rating	Units
Power Supply Voltage	VDD	3.0~3.6	V
		2.3~2.7	V
Ambient Temperature	Ta	-40~+85	°C

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply Voltage	VDD	-0.3~+3.6	V
Input Voltage	VIN	-0.3~VDD+0.3	V
		0.3~+6.3	
Output Current	IOUT	±30	mA
Storage Temperature	TSTG	-55~+125	°C

Table 7 DC Characteristics

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
Vih	High-Input Voltage	LVTTL	2.0	–	–	V
		5V-tolerant LVTTL	2.0	–	–	V
		3.3V PCI	0.5 x VDD	–	–	V
Vil	Low-Input Voltage	LVTTL	–	–	0.8	V
		5V-tolerant LVTTL	–	–	0.8	V
		3.3V PCI	–	–	0.3 x VDD	V
V+	High-Input Voltage	LVTTL-Schmitt	–	1.8	2.3	V
V-	Low-Input Voltage	LVTTL-Schmitt	0.5	0.9	–	V
Vh	Hysteresis Voltage	LVTTL-Schmitt	0.4	–	–	V
Iih	High-Input Current	VIN=VDD	-10	–	+10	µA
Iil	Low-Input Current	VIN=VSS	-10	–	+10	µA
Voh	High-Output Voltage	Ioh=-2~-24mA	2.4	–	–	V
Vol	Low-Output Voltage	Iol=2~24mA	–	–	0.4	V
Ioz	3-State Lead Current	Voh=VSS	-10	–	+10	µA
		Vol=VDD	-10	–	+10	µA
Ipu	Active Pull-Up Current	VIN=VSS	-25	-66	-160	µA
Ipd	Active Pull-Down Current	VIN=VDD	25	66	160	µA
Idds	Static Stand-By Current	–	–	–	450*	µA

*The number is design-dependent.
ESDProtection:=2000V using MIL STD-883D 3015.6 and EIAJ:ED4701 C-111 B standards
Lock-up immunity:300mA injection current (room temp) using JEDEC No. 17 standard

Silicon Valley Office
Kawasaki LSI U.S.A., Inc.
4655 Old Ironsides Drive, Suite 265
Santa Clara, CA 95054
Tel: (408) 654-0180
Fax: (408) 654-0198

Eastern Area Office
Kawasaki LSI U.S.A., Inc.
501 Edgewater Drive, Suite 510
Wakefield, MA 01880
Tel: (617) 224-4201
Fax: (617) 224-2503

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