

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT

Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 38

SYSTEM CHARGER ISL6251AHAZ- PAGE 39

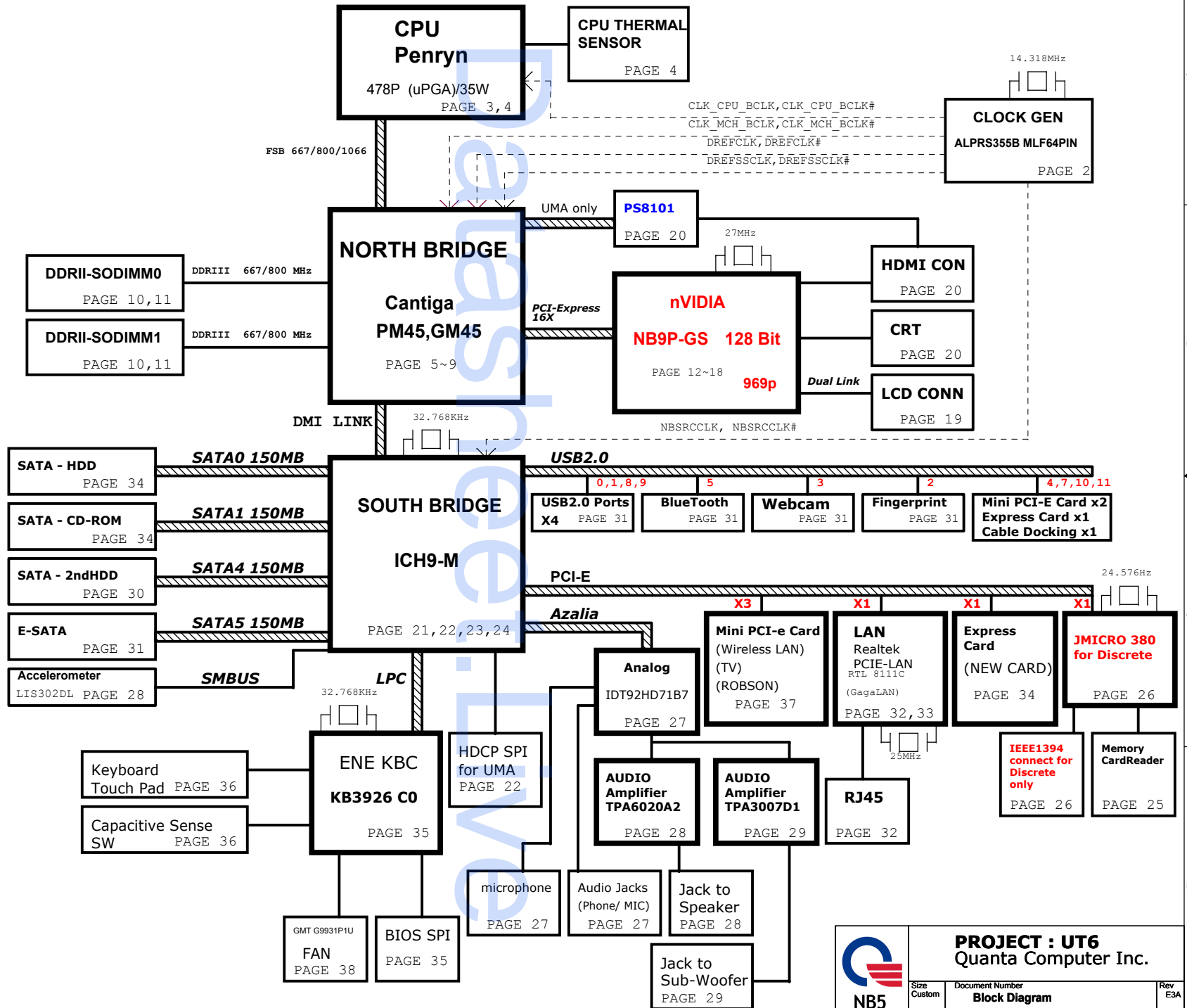
SYSTEM POWER ISL6237IRZ-T PAGE 40

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 44

VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 44

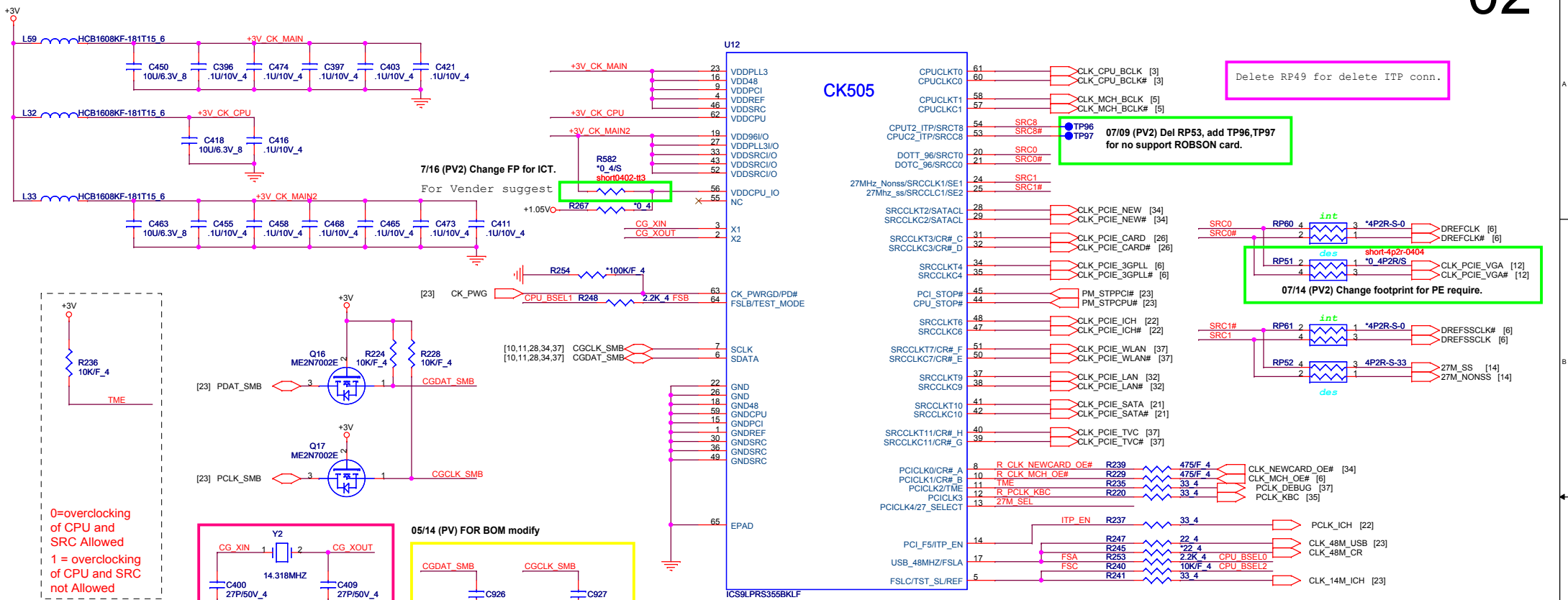
VGACORE(1.025V)Oz8118 PAGE 43

CPU CORE ISL6266A PAGE 42



PROJECT : UT6
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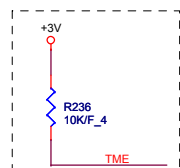
Size Custom	Document Number NB5	Rev E3A
Block Diagram		
Date: Friday, July 18, 2008	Sheet 1	of 46



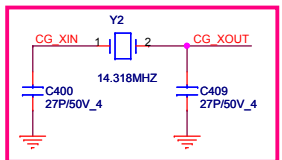
Delete RP49 for delete ITP conn.

07/09 (PV2) Del RP53, add TP96, TP97 for no support ROBSON card.

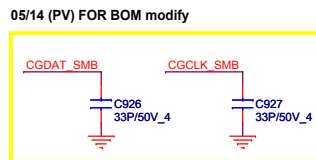
07/14 (PV2) Change footprint for PE require.



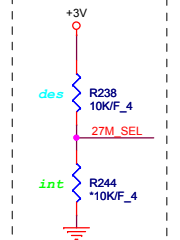
0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



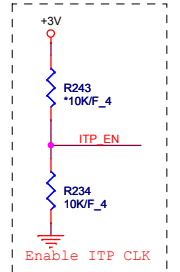
SI modified
C400, C409 change to 27p



05/14 (PV) FOR BOM modify



0=UMA
1 = External VGA

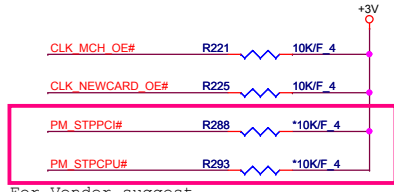


Enable ITP CLK

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

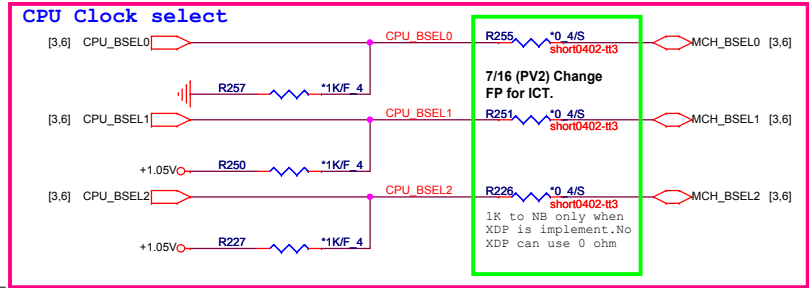
CK505 QFN64

- ICS ICS9LPRS355BKLF ALPRS355000
- Silego SLG8SP513VTR AL8SP513000
- Realtek RTM875N-606-VD-GR AL000875000

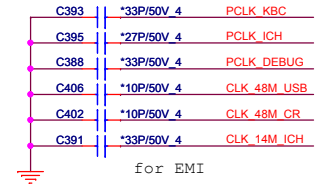


For Vender suggest

Q16 modified-0117



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

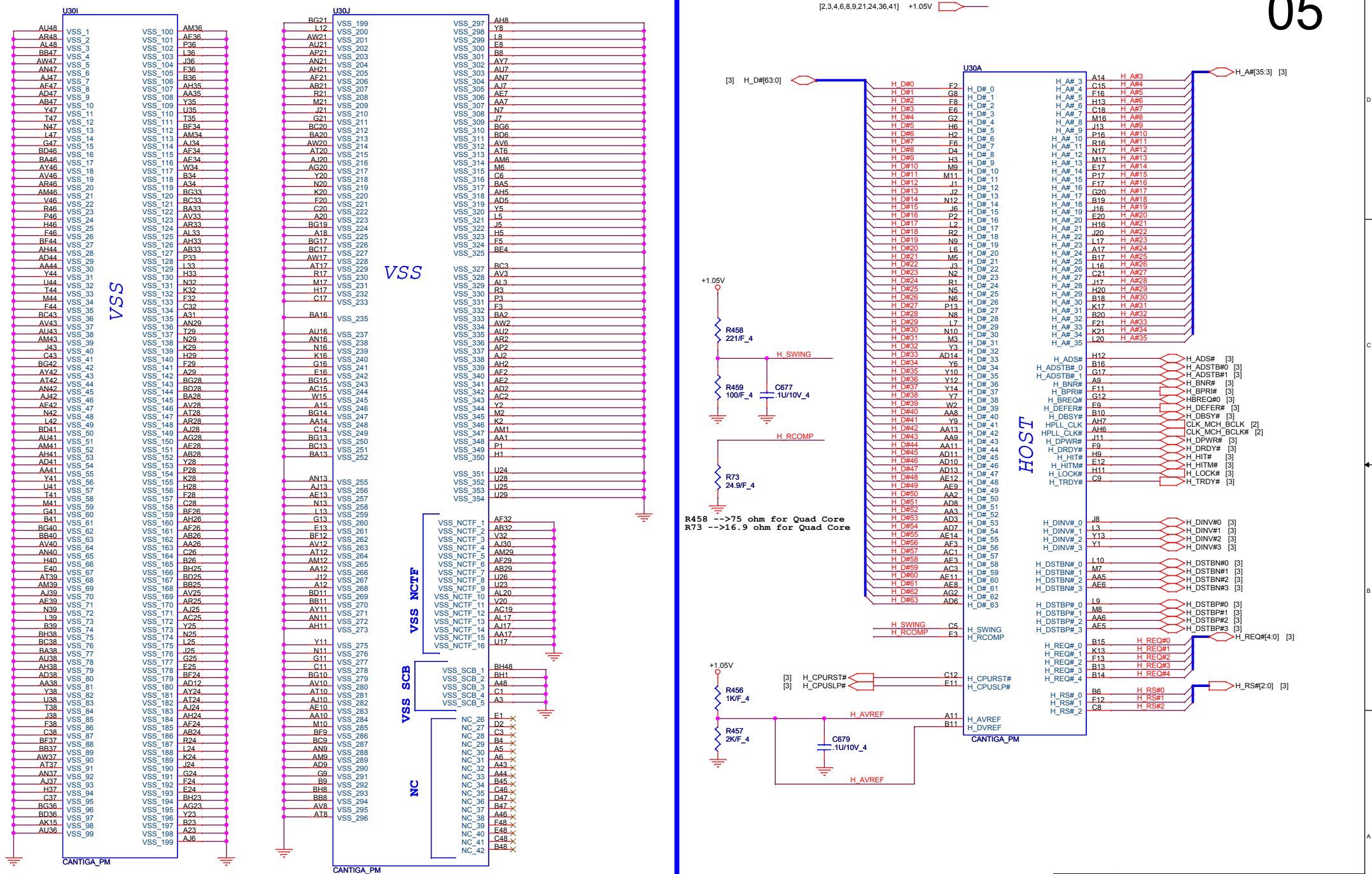


for EMI

PROJECT : UT6
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Size Custom	Document Number	Rev E3A
Clock Generator		
Date: Friday, July 18, 2008	Sheet 2 of 46	

[2,3,4,6,8,9,21,24,36,41] +1.05V



PROJECT : UT6
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NB5 Size Custom Document Number **Cantiga Host & VSS 1/5** Rev E3A

Date: Friday, July 18, 2008 Sheet 5 of 46

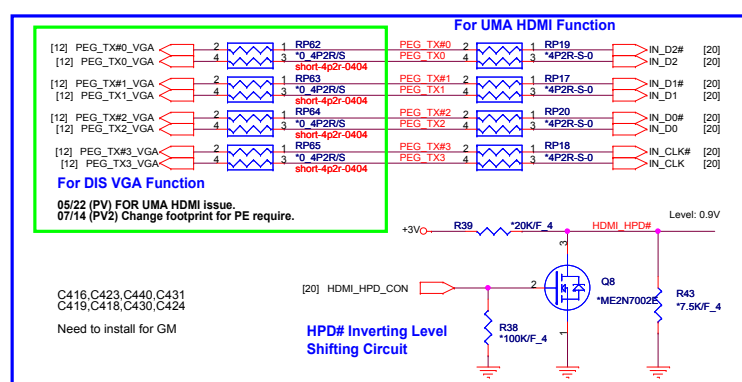
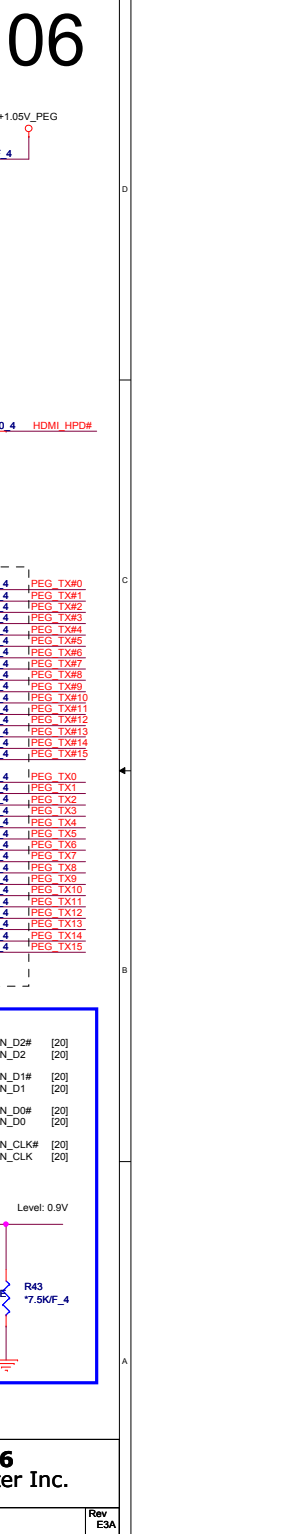
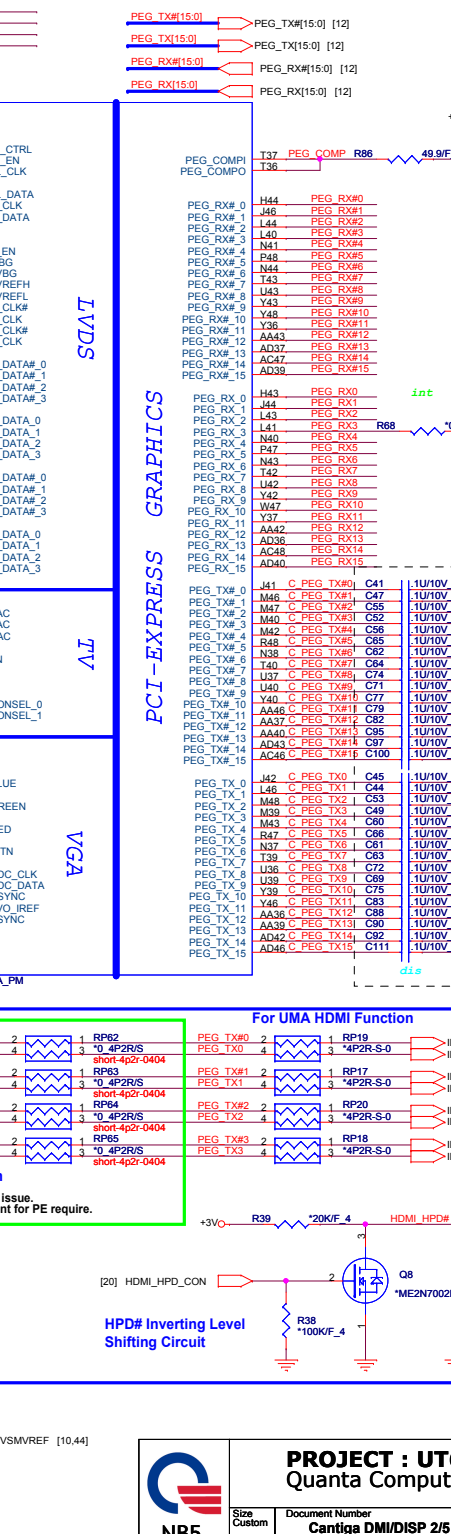
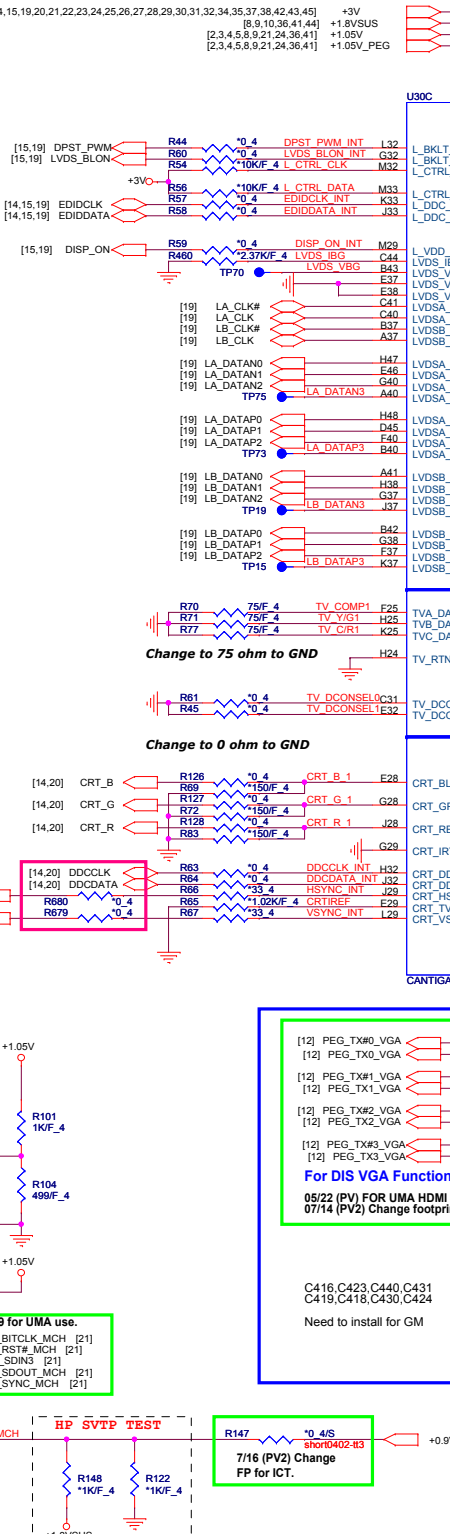
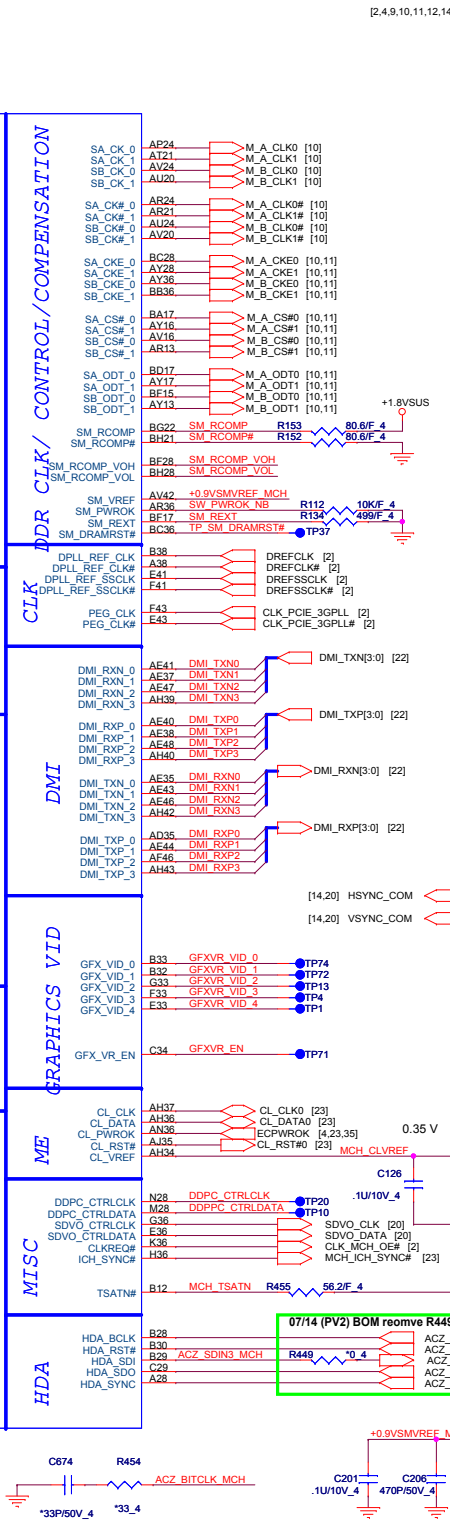
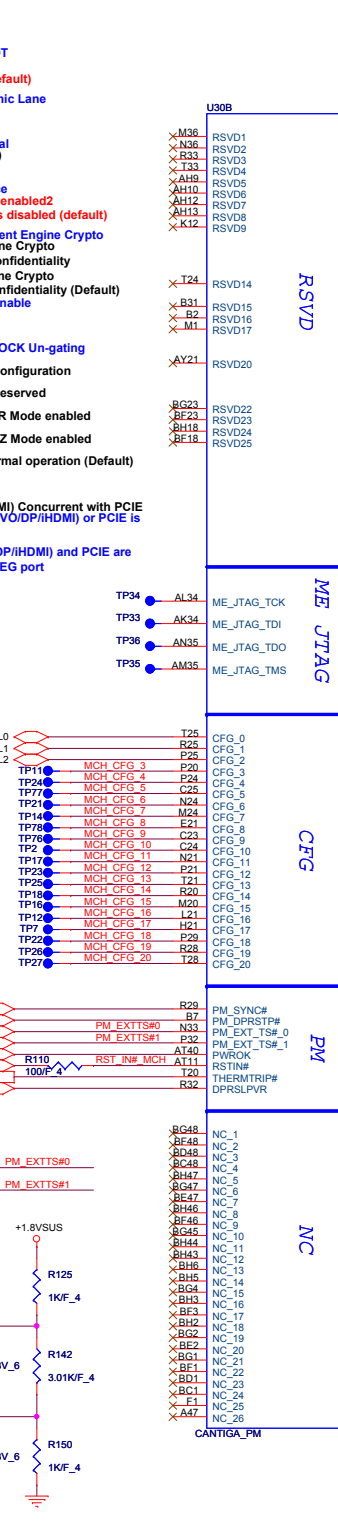
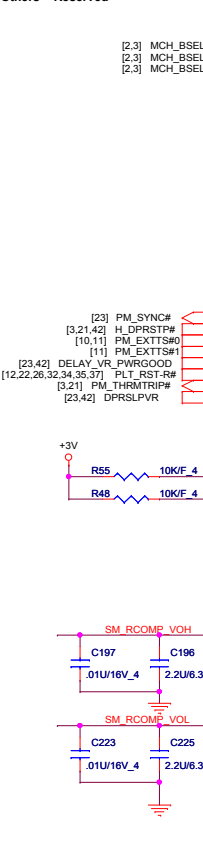
- MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)
- MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)
- MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)
- MCH_CFG_19 DMI Lane Reverse
Low = Normal operation (Default)
High = Reverse Lanes
- MCH_CFG_6 ITPM Host Interface
Low = The ITPM Host Interface is enabled
High = The ITPM Host Interface is disabled (default)
- MCH_CFG_7 Intel(R) Management Engine Crypto
Low: Intel(R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel(R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)
- MCH_CFG_10 PCIe Lookback Enable
Low = Enabled
High = Disabled (Default)
- MCH_CFG_12/13 XOR/ALL/CLOCK Un-gating
- MCH_CFG_13 MCH_CFG_12 Configuration

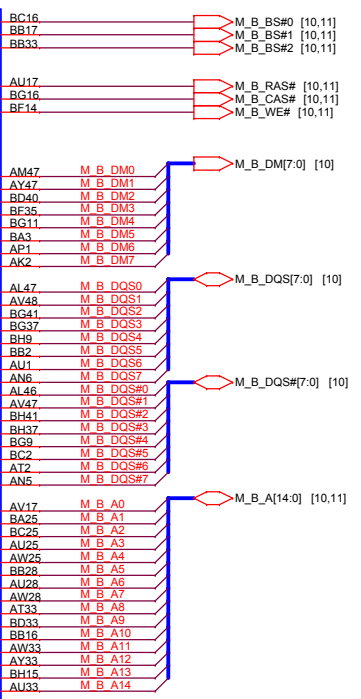
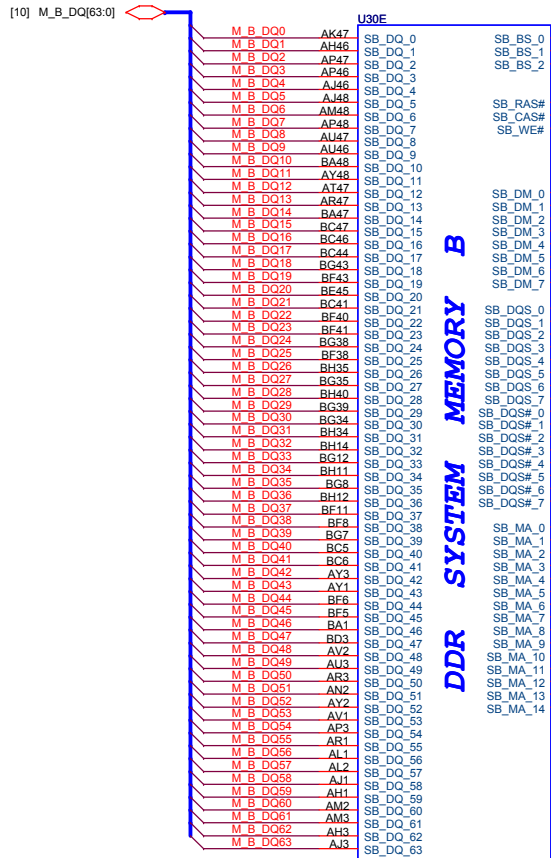
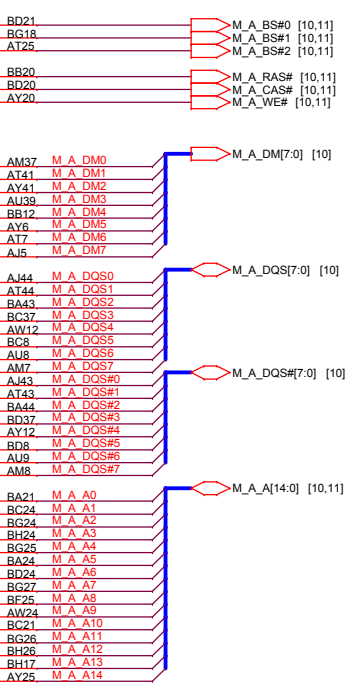
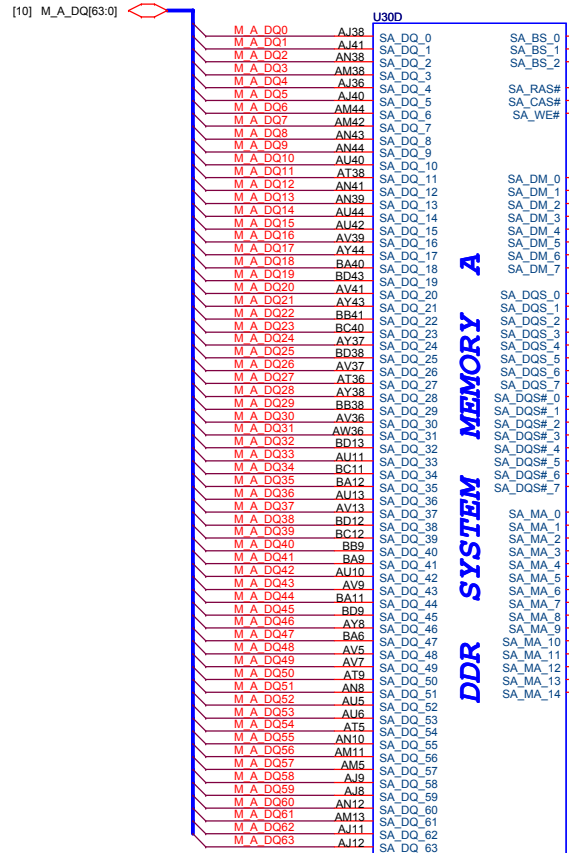
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)
- MCH_CFG_20

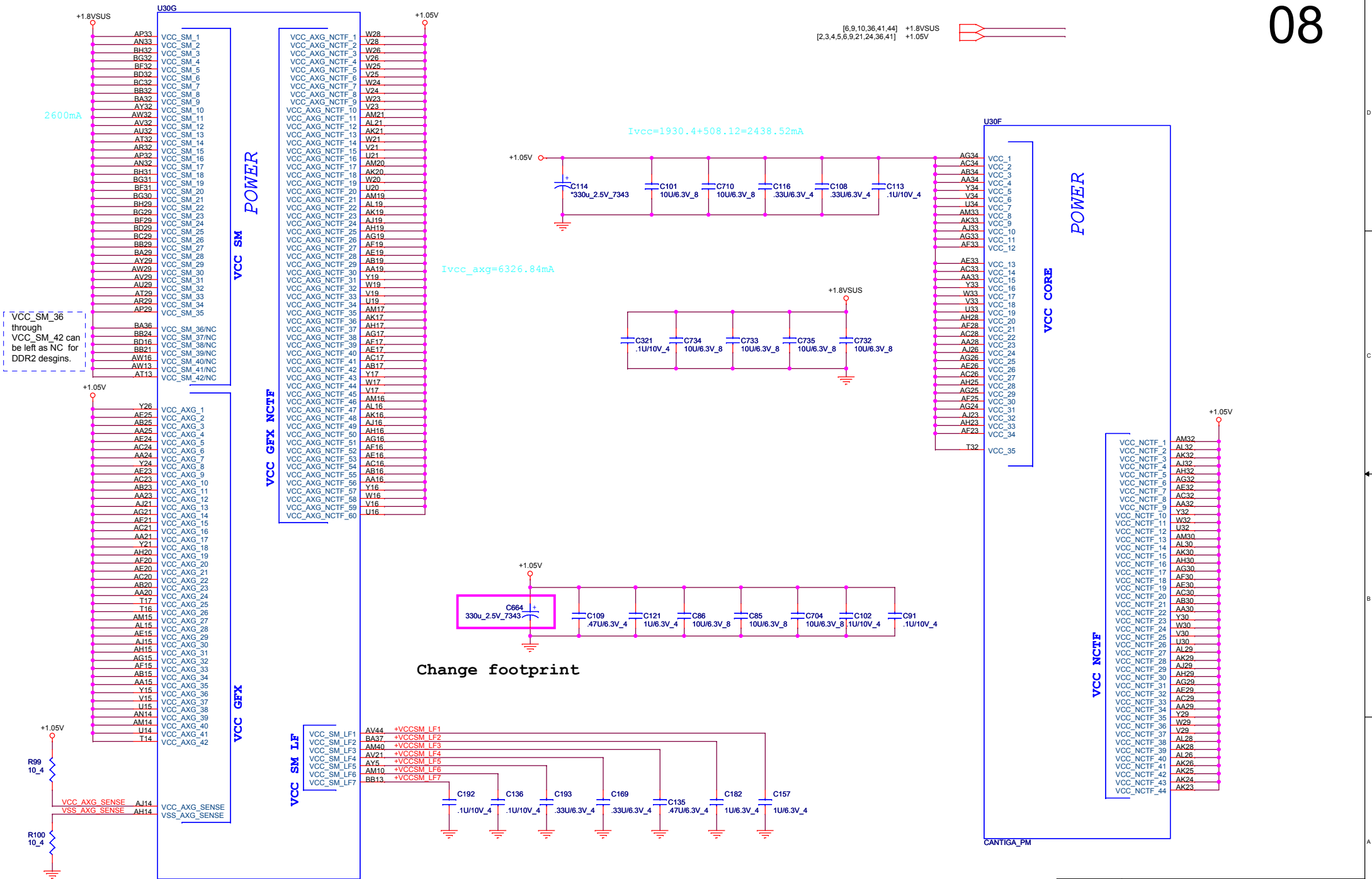
000	= FSB1066
010	= FSB800
011	= FSB667
Others	= Reserved

Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe
Low = Only digital display port (SDVO/DP/HDMI) or PCIe is operational (default)
High = Digital display port (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port

MCH_CFG2:0
000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved








VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desigs.

Change footprint

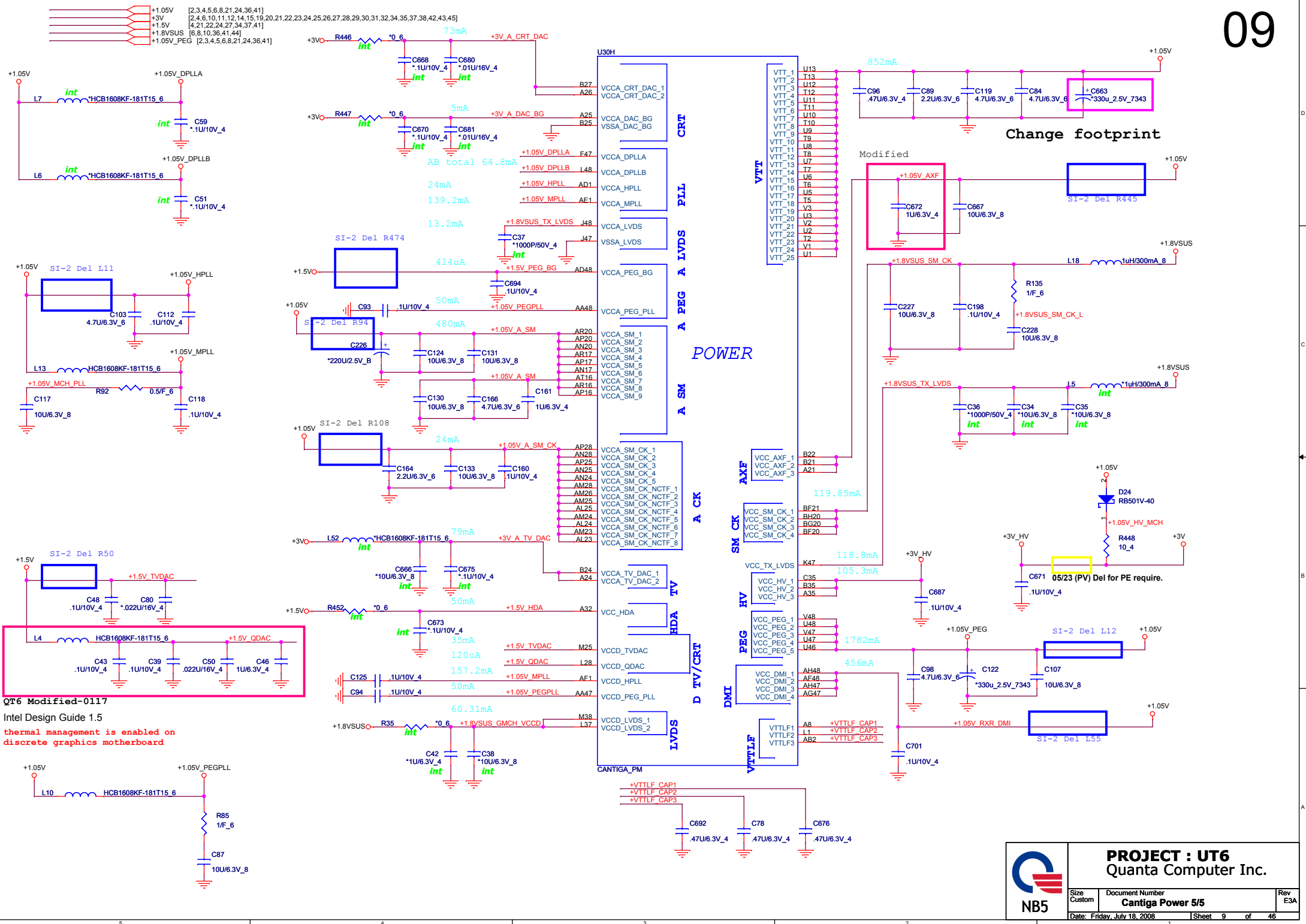


NB5

PROJECT : UT6
Quanta Computer Inc.

Size Custom Document Number
Cantiga Vcc 4/5 Rev E3A

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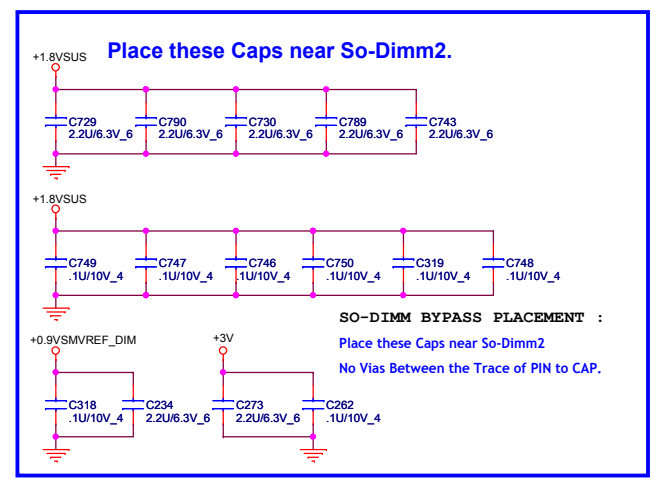
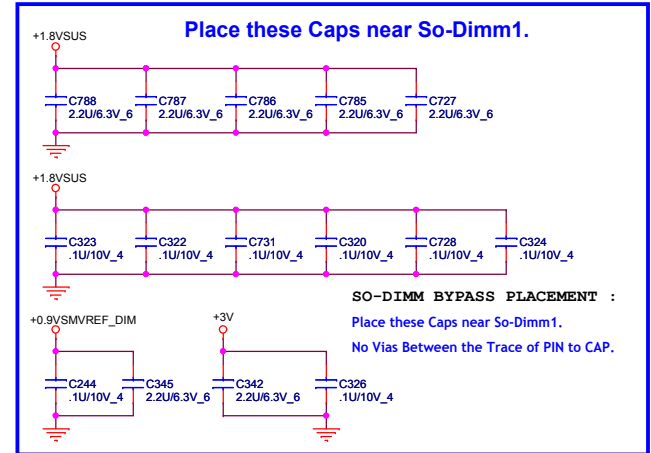
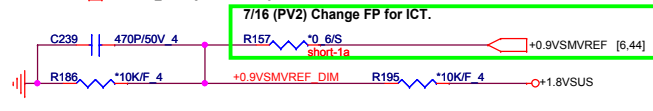
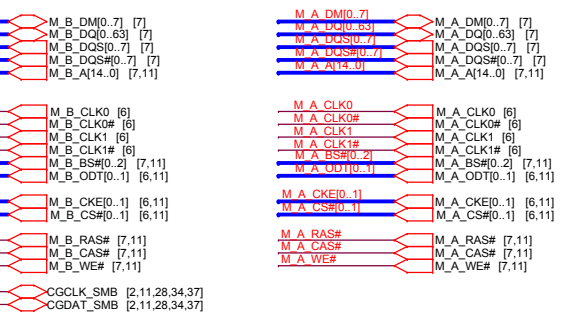
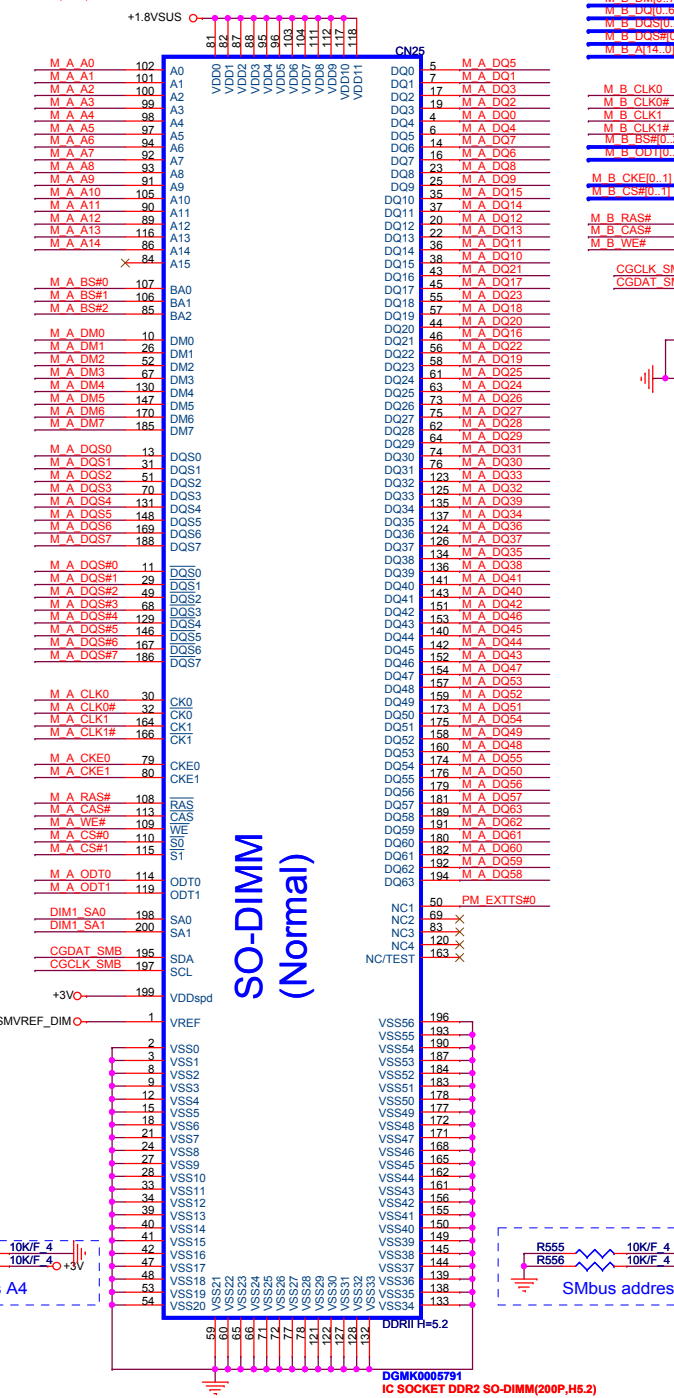
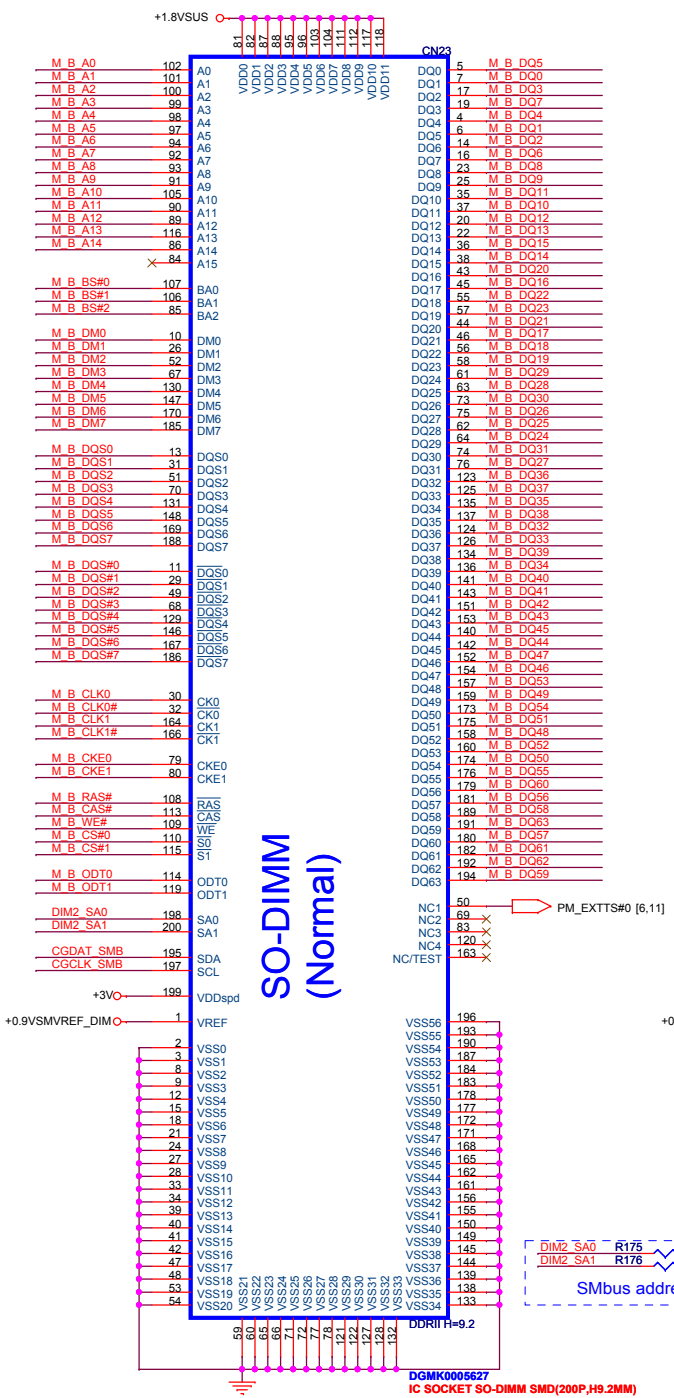
QT6 Modified-0117

Intel Design Guide 1.5
 thermal management is enabled on
 discrete graphics motherboard

	PROJECT : UT6 Quanta Computer Inc.	
	Size Custom Document Number Cantiga Power 5/5	Rev E3A
Date: Friday, July 18, 2008 Sheet 9 of 46		

[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]

[6,8,9,36,41,44]



PROJECT : UT6
Quanta Computer Inc.

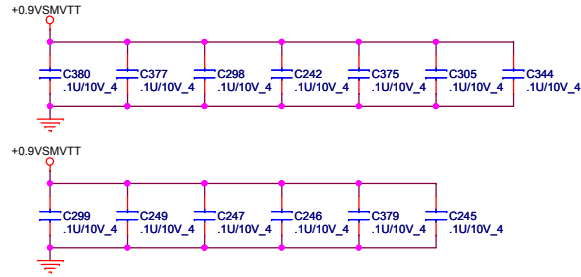
NB5

Size Custom Document Number **DDR2 DIMM** Rev E3A

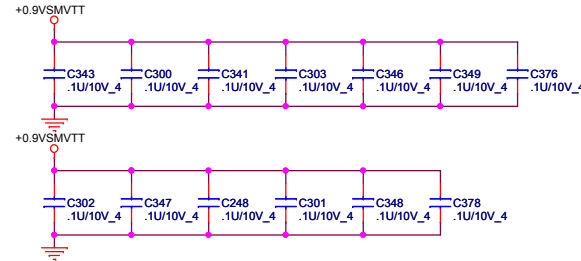
Date: Friday, July 18, 2008 Sheet 10 of 46

DDRII DUAL CHANNEL A,B.

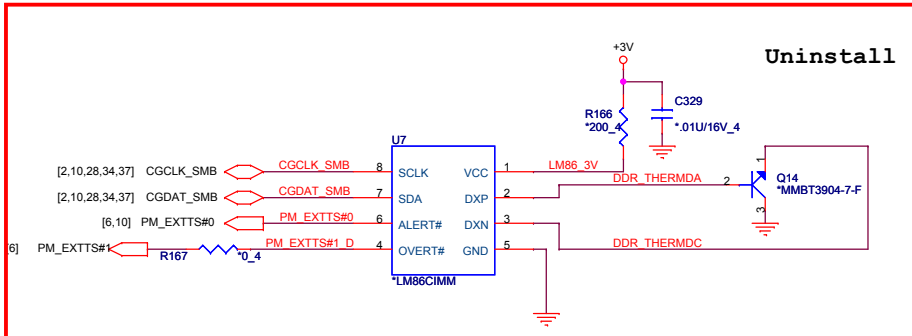
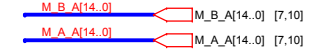
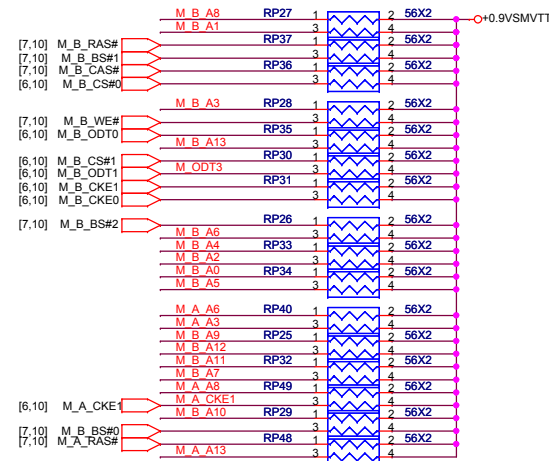
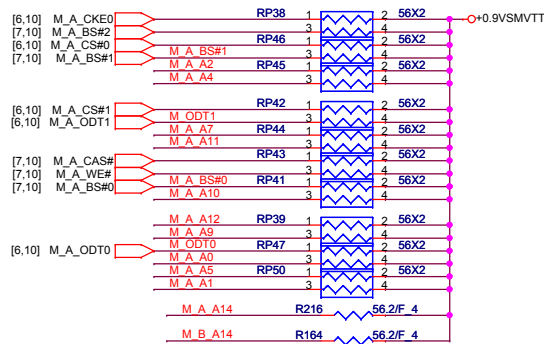
DDRII A CHANNEL



DDRII B CHANNEL

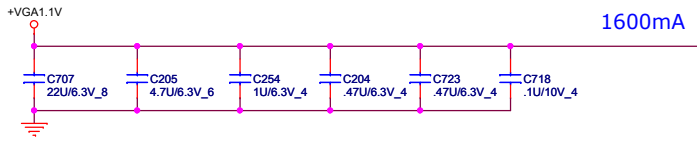
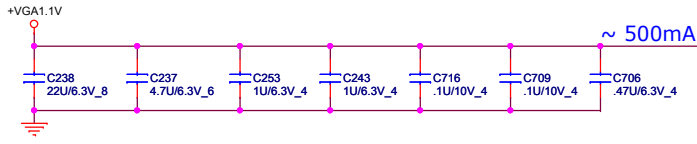


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

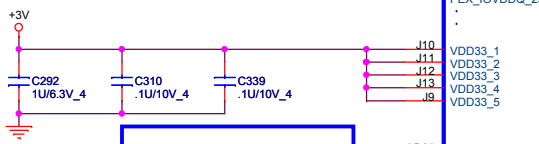


PROJECT : QT6
Quanta Computer Inc.

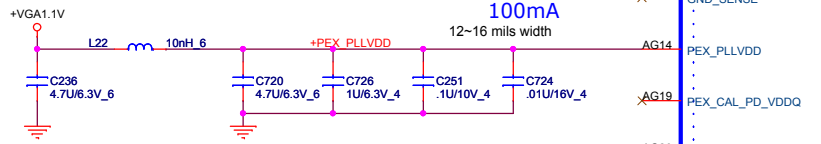
[2,4,6,9,10,11,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V [13,14,44] +VGA1.1V



Near BGA

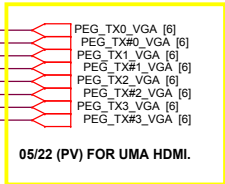


[43] VGA_SENSE SI-2 4/10 For Nvidia recommend.



U35A BGA969-NVIDIA-NB9P-GS COMMON

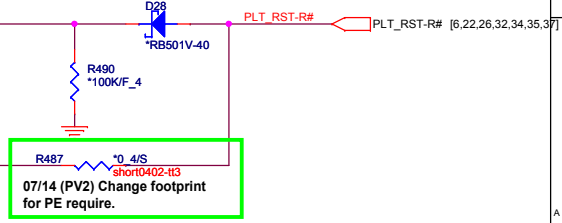
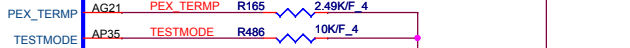
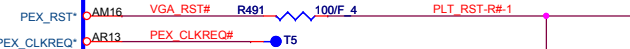
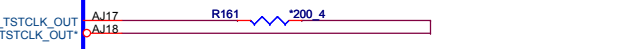
AK16	PEX_IOVDD_1	PEX_RX0	AP17	PEG_TX0_VGA
AK17	PEX_IOVDD_2	PEX_RX0*	AN17	PEG_TX#0_VGA
AK21	PEX_IOVDD_3	PEX_RX1	AN19	PEG_TX1_VGA
AK24	PEX_IOVDD_4	PEX_RX1*	AP19	PEG_TX#1_VGA
AK27	PEX_IOVDD_5	PEX_RX2	AR19	PEG_TX2_VGA
		PEX_RX2*	AR20	PEG_TX#2_VGA
		PEX_RX3	AP20	PEG_TX3_VGA
		PEX_RX3*	AN20	PEG_TX#3_VGA
AG11	PEX_IOVDDQ_1	PEX_RX4	AN22	PEG_TX4
AG12	PEX_IOVDDQ_2	PEX_RX4*	AP22	PEG_TX#4
AG13	PEX_IOVDDQ_3	PEX_RX5	AR22	PEG_TX5
AG15	PEX_IOVDDQ_4	PEX_RX5*	AP23	PEG_TX#5
AG16	PEX_IOVDDQ_5	PEX_RX6	AN23	PEG_TX#6
AG17	PEX_IOVDDQ_6	PEX_RX6*	AP23	PEG_TX6
AG18	PEX_IOVDDQ_7	PEX_RX7	AN25	PEG_TX7
AG22	PEX_IOVDDQ_8	PEX_RX7*	AP25	PEG_TX#7
AG23	PEX_IOVDDQ_9	PEX_RX8	AR25	PEG_TX8
AG24	PEX_IOVDDQ_10	PEX_RX8*	AN26	PEG_TX#8
AG25	PEX_IOVDDQ_11	PEX_RX9	AP26	PEG_TX9
AG26	PEX_IOVDDQ_12	PEX_RX9*	AN26	PEG_TX#9
AJ14	PEX_IOVDDQ_13	PEX_RX10	AN28	PEG_TX10
AJ15	PEX_IOVDDQ_14	PEX_RX10*	AP28	PEG_TX#10
AJ19	PEX_IOVDDQ_15	PEX_RX11	AR28	PEG_TX11
AJ21	PEX_IOVDDQ_16	PEX_RX11*	AP29	PEG_TX#11
AJ22	PEX_IOVDDQ_17	PEX_RX12	AN29	PEG_TX12
AJ24	PEX_IOVDDQ_18	PEX_RX12*	AP29	PEG_TX#12
AJ25	PEX_IOVDDQ_19	PEX_RX13	AN29	PEG_TX#12
AJ27	PEX_IOVDDQ_20	PEX_RX13*	AP31	PEG_TX13
AK18	PEX_IOVDDQ_21	PEX_RX14	AR31	PEG_TX14
AK20	PEX_IOVDDQ_22	PEX_RX14*	AP32	PEG_TX#14
AK23	PEX_IOVDDQ_23	PEX_RX15	AR34	PEG_TX15
AK26	PEX_IOVDDQ_24	PEX_RX15*	AP34	PEG_TX#15
AL16	PEX_IOVDDQ_25			



PCI EXPRESS

AL17	C PEG_RX0	C171	.1U/10V_4	PEG_RX0 [6]
AM17	C PEG_RX#0	C170	.1U/10V_4	PEG_RX#0 [6]
AM18	C PEG_RX1	C209	.1U/10V_4	PEG_RX1 [6]
AM19	C PEG_RX#1	C210	.1U/10V_4	PEG_RX#1 [6]
AL19	C PEG_RX2	C172	.1U/10V_4	PEG_RX2 [6]
AK19	C PEG_RX#2	C173	.1U/10V_4	PEG_RX#2 [6]
AL20	C PEG_RX3	C145	.1U/10V_4	PEG_RX3 [6]
AM20	C PEG_RX#3	C146	.1U/10V_4	PEG_RX#3 [6]
AM21	C PEG_RX4	C211	.1U/10V_4	PEG_RX4 [6]
AM22	C PEG_RX#4	C212	.1U/10V_4	PEG_RX#4 [6]
AL22	C PEG_RX5	C213	.1U/10V_4	PEG_RX5 [6]
AK22	C PEG_RX#5	C214	.1U/10V_4	PEG_RX#5 [6]
AL23	C PEG_RX6	C147	.1U/10V_4	PEG_RX6 [6]
AM23	C PEG_RX#6	C148	.1U/10V_4	PEG_RX#6 [6]
AM24	C PEG_RX7	C174	.1U/10V_4	PEG_RX7 [6]
AM25	C PEG_RX#7	C175	.1U/10V_4	PEG_RX#7 [6]
AL25	C PEG_RX8	C149	.1U/10V_4	PEG_RX8 [6]
AK25	C PEG_RX#8	C150	.1U/10V_4	PEG_RX#8 [6]
AL26	C PEG_RX9	C176	.1U/10V_4	PEG_RX9 [6]
AM26	C PEG_RX#9	C177	.1U/10V_4	PEG_RX#9 [6]
AM27	C PEG_RX10	C151	.1U/10V_4	PEG_RX10 [6]
AM28	C PEG_RX#10	C152	.1U/10V_4	PEG_RX#10 [6]
AL28	C PEG_RX11	C199	.1U/10V_4	PEG_RX11 [6]
AK28	C PEG_RX#11	C200	.1U/10V_4	PEG_RX#11 [6]
AK29	C PEG_RX12	C178	.1U/10V_4	PEG_RX12 [6]
AL29	C PEG_RX#12	C179	.1U/10V_4	PEG_RX#12 [6]
AM29	C PEG_RX13	C162	.1U/10V_4	PEG_RX13 [6]
AM30	C PEG_RX#13	C163	.1U/10V_4	PEG_RX#13 [6]
AM31	C PEG_RX14	C156	.1U/10V_4	PEG_RX14 [6]
AM32	C PEG_RX#14	C157	.1U/10V_4	PEG_RX#14 [6]
AM32	C PEG_RX15	C180	.1U/10V_4	PEG_RX15 [6]
AP32	C PEG_RX#15	C181	.1U/10V_4	PEG_RX#15 [6]

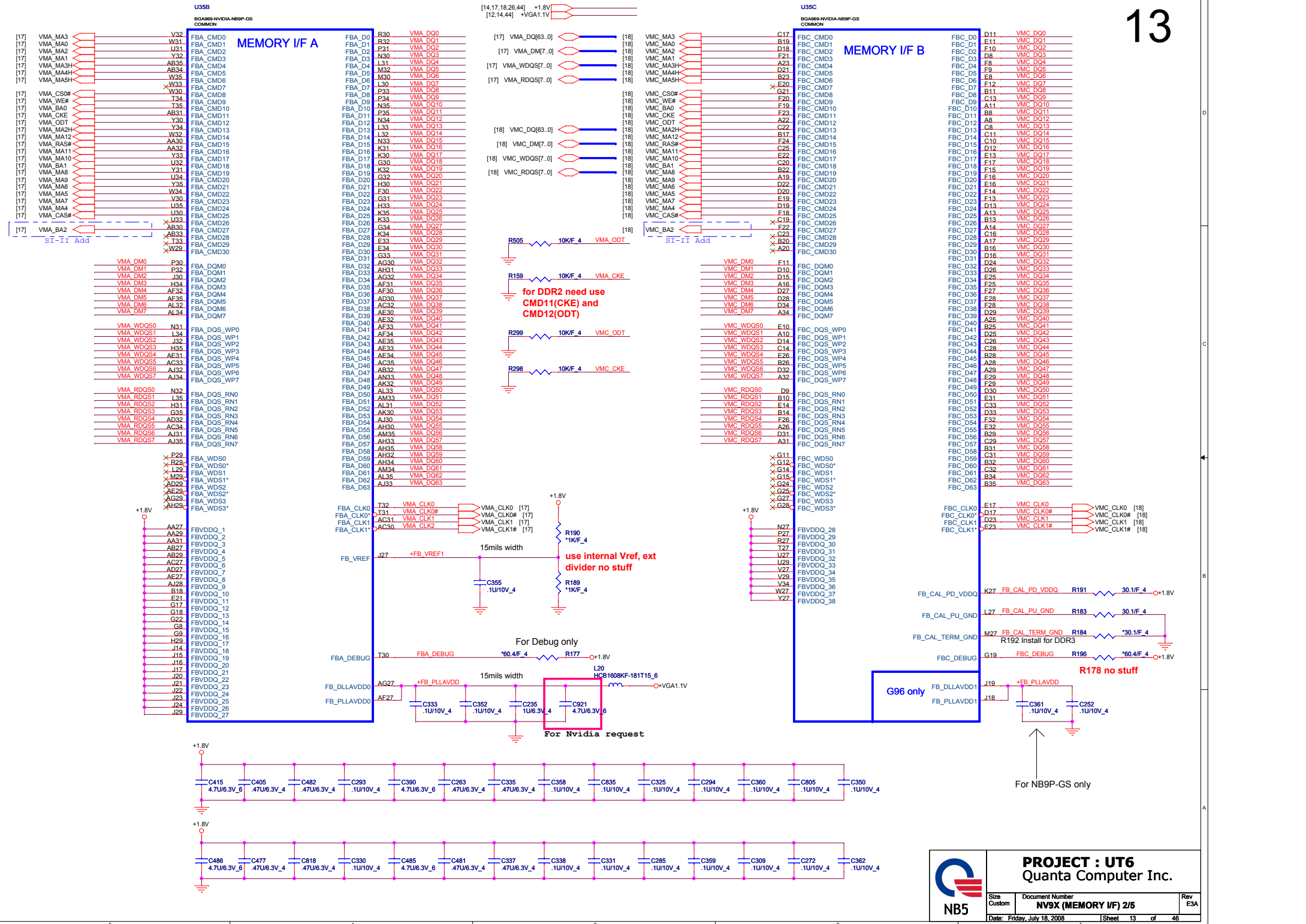
AR16	CLK_PCIE_VGA	CLK_PCIE_VGA [2]
AR17	CLK_PCIE_VGA#	CLK_PCIE_VGA# [2]



PROJECT : UT6
Quanta Computer Inc.

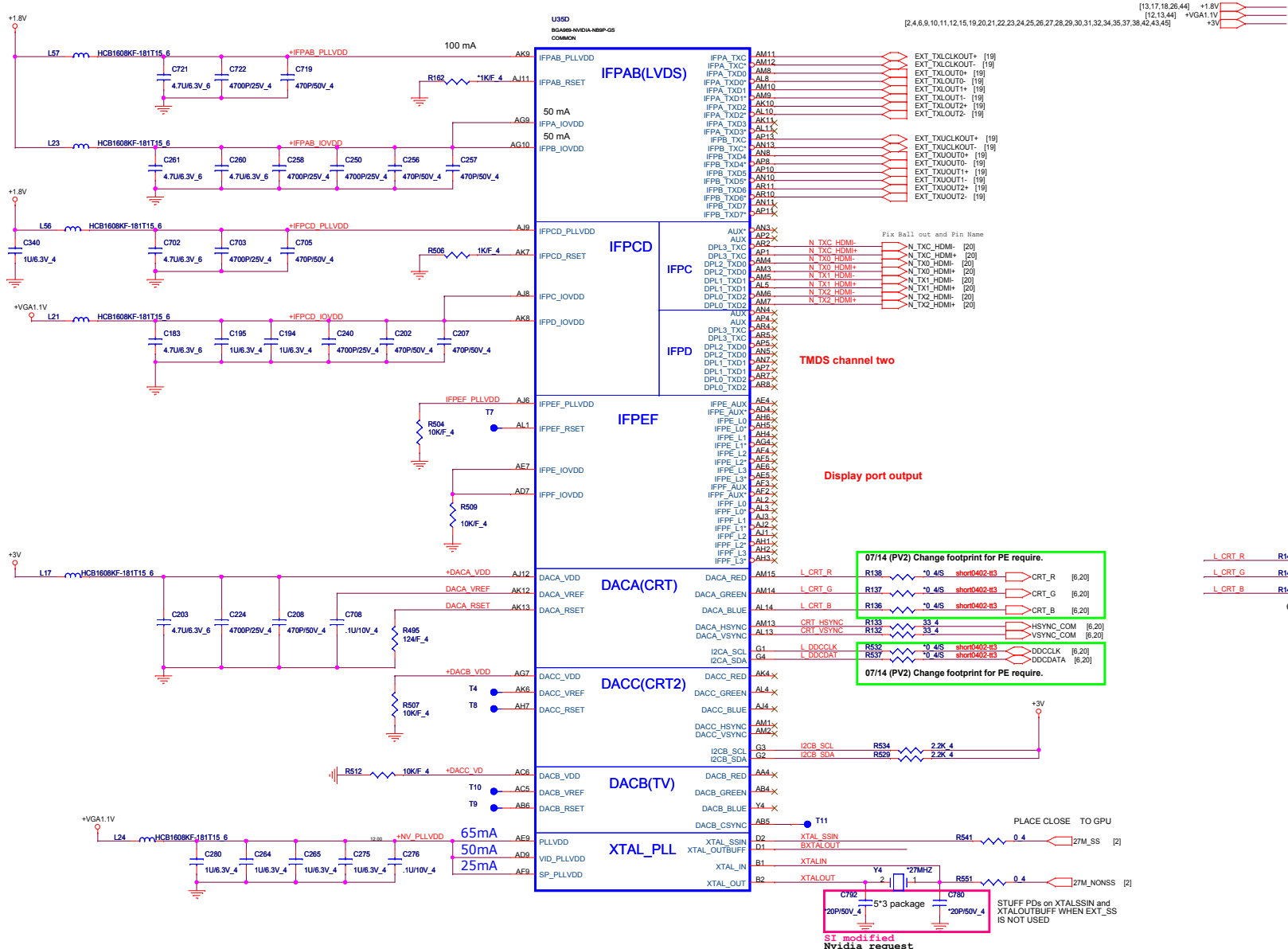
NB5

Size Custom	Document Number NV9X (PCIE I/F) 1/5	Rev E3A
Date: Friday, Jul 18, 2008	Sheet 12 of 46	



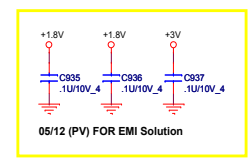
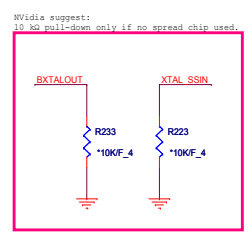
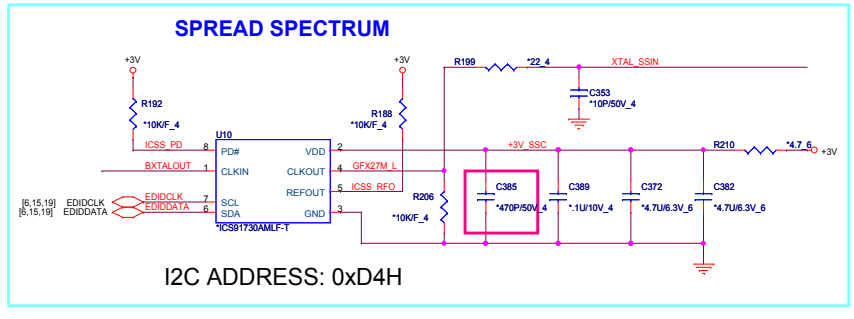
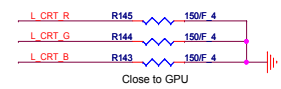
PROJECT : UT6
Quanta Computer Inc.

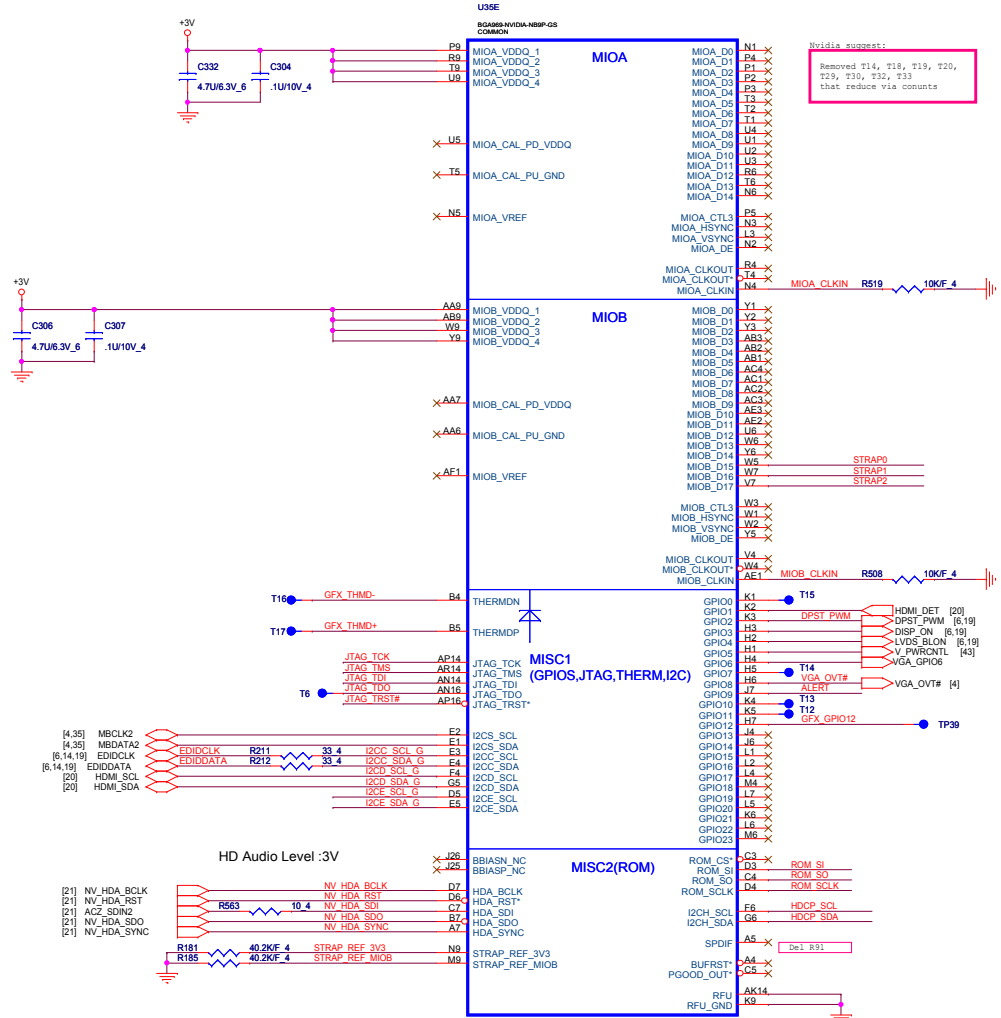
Size Custom	Document Number NV9X (MEMORY I/F) 2/5	Rev E3A
Date: Friday, July 18, 2008	Sheet 13 of 46	



07/14 (PV2) Change footprint for PE require.

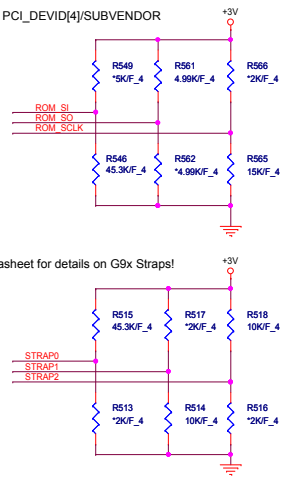
07/14 (PV2) Change footprint for PE require.





NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

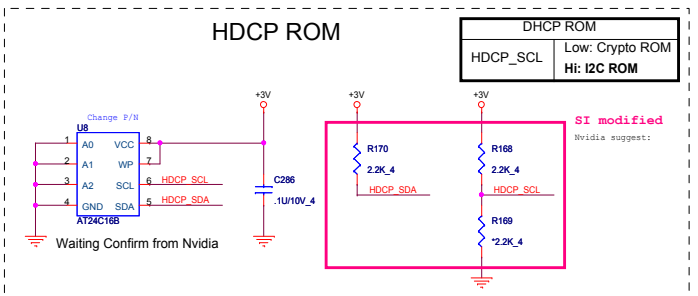
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit

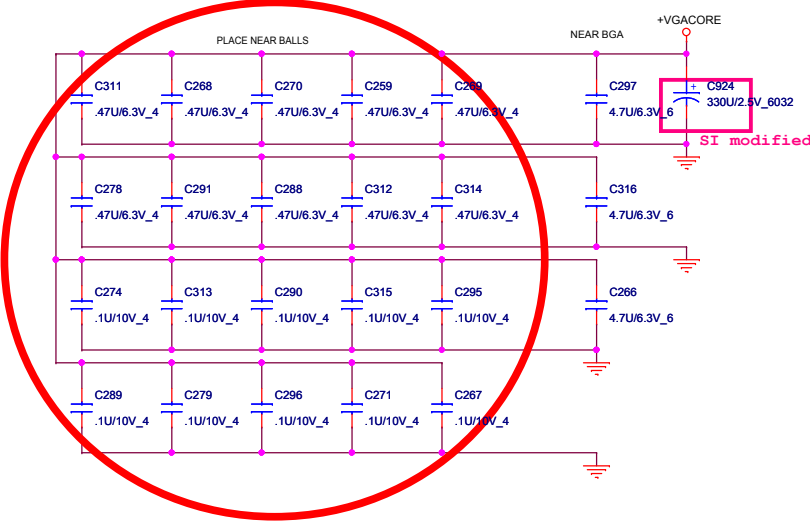
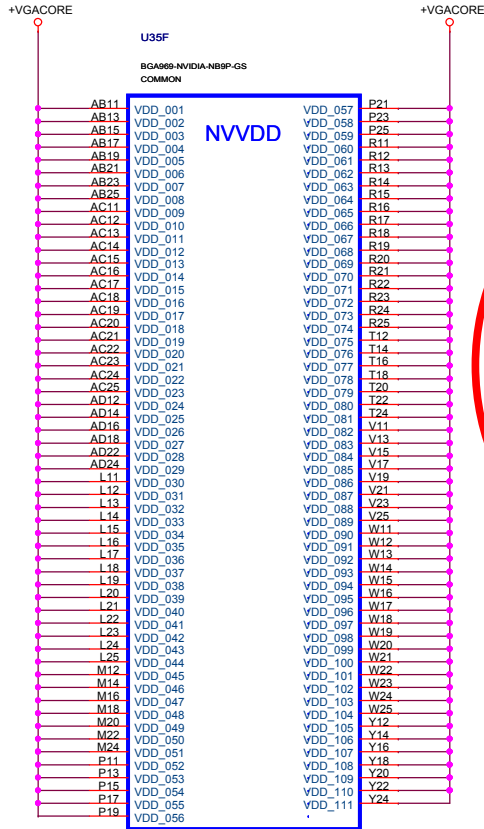


RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda HYB1S12161B2P-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elpida
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda

PCI_DEVID: STRAP2
NB9M-GE 0x06E 8 1000 default
NB9M-GS 0x06E 9 1001
NB9P-GE2 0x064 8 1000
NB9P-GS 0x064 9 1001 default

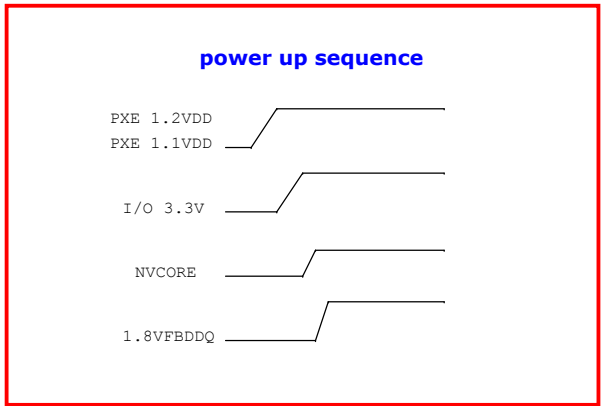
CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)

NVVDD Decoupling



Follow Design Guide DG-03276-001 4.7uF x3 and 0.47x10 uF instead of 0.1uF x10

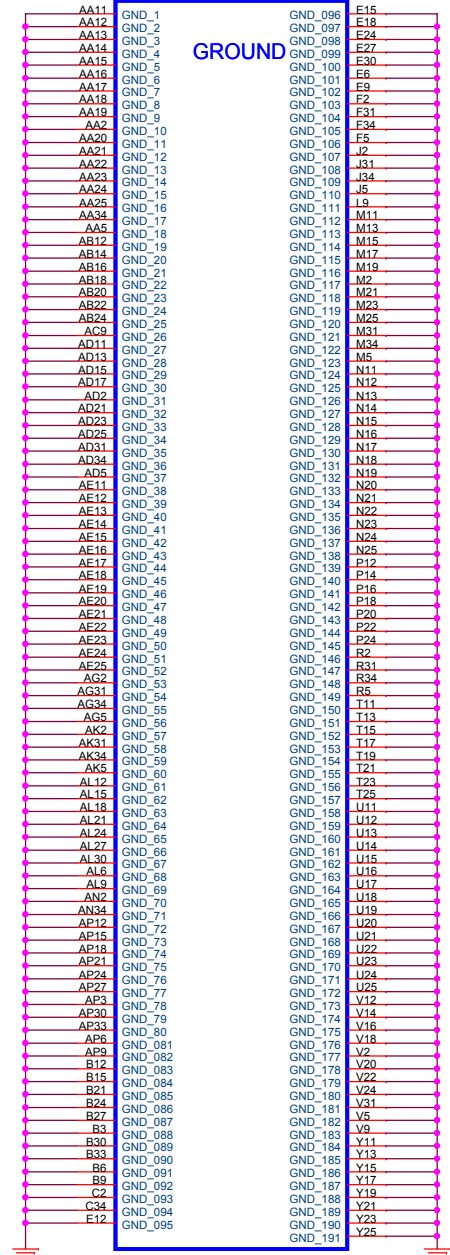
NB9M: VGACORE +0.90V (Normal) , +1.09V



[43] +VGACORE

U35G

BGA989-NVIDIA-NB9P-GS
COMMON



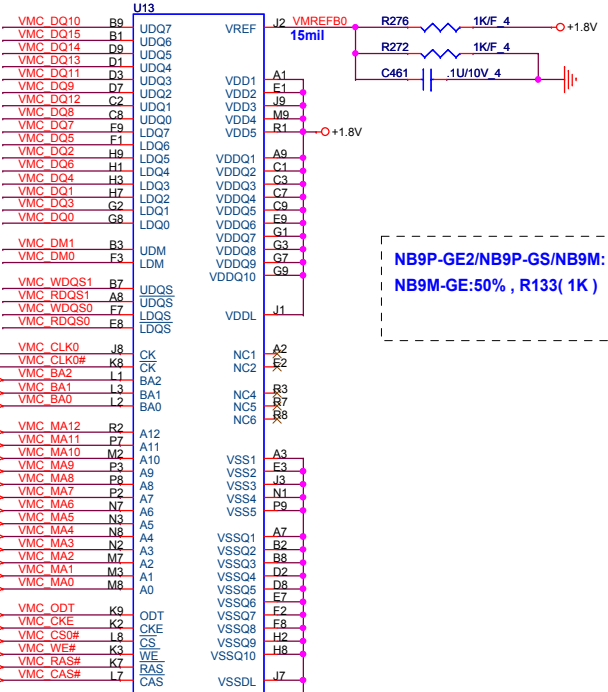
GROUND



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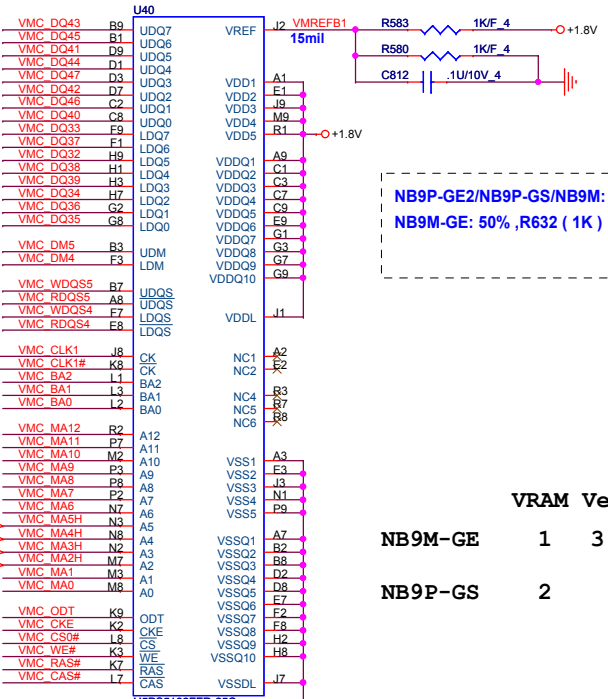
Size Custom	Document Number NV9X (POWER & GND) 5/5	Rev E3A
Date: Friday, July 18, 2008	Sheet 16 of 46	

[13,14,17,26,44] +1.8V



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R133(1K)

H5PS162FFR-25C
AKD5FG-TW03
IC SDRAM(84P) H5PS162FFR-25C(FBGA)

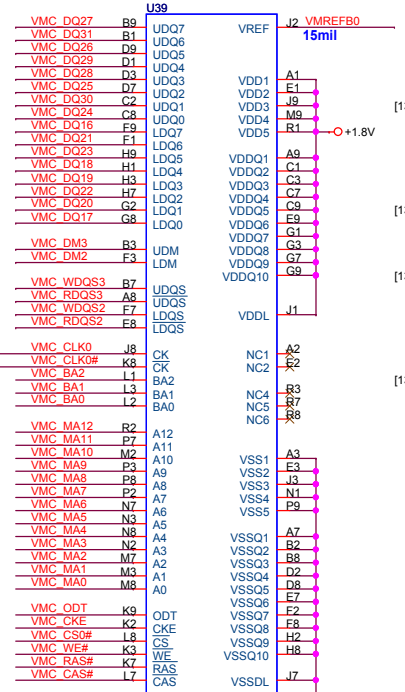


NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R632 (1K)

H5PS162FFR-25C
AKD5FG-TW03
IC SDRAM(84P) H5PS162FFR-25C(FBGA)

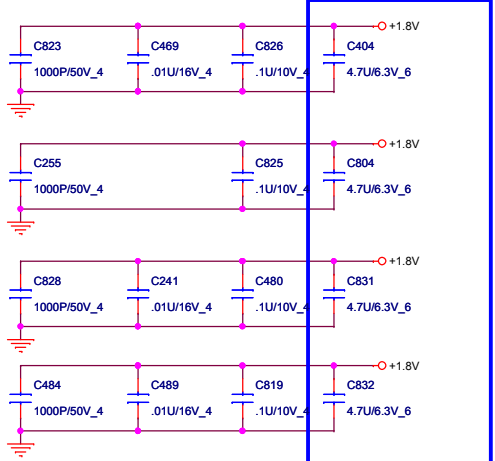
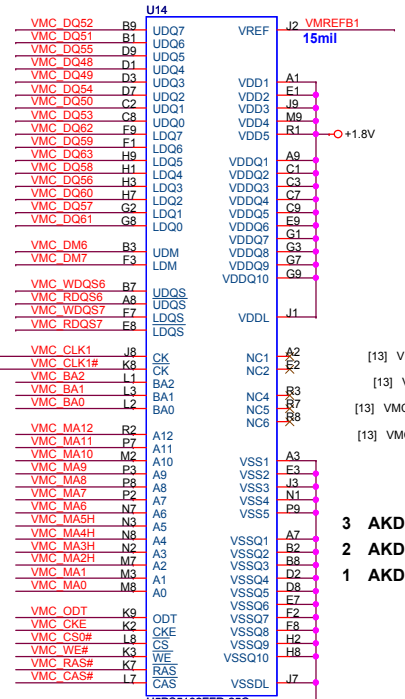
VRAM Vendor

NB9M-GE	1	3
NB9P-GS	2	



NB9M/NB9P-GS/NB9P-GE2: 475R

CS14752FB11 RES CHIP 475 1/16W +-1%(0402)



- [13] VMC_DQ[63..0]
- [13] VMC_DM[7..0]
- [13] VMC_WDS[7..0]
- [13] VMC_RDQS[7..0]

- 3 AKD5FG-T501 IC SDRAM(84P) K4N51163QG-HC25(FBGA) Samsung
- 2 AKD5FG-T*03 IC SDRAM(84P)HYB18T512161B2F-25(TFBGA) Qimonda
- 1 AKD5FG-TW31 IC SDRAM(84P) HY5PS121621CFP-25(FBGA) Hynix

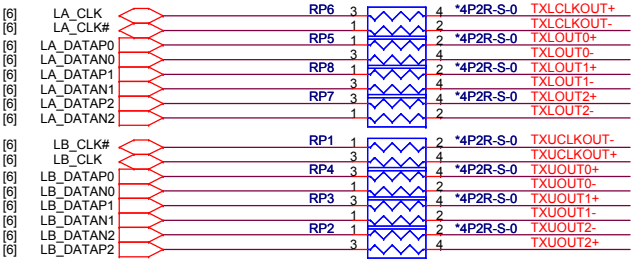


PROJECT : UT6
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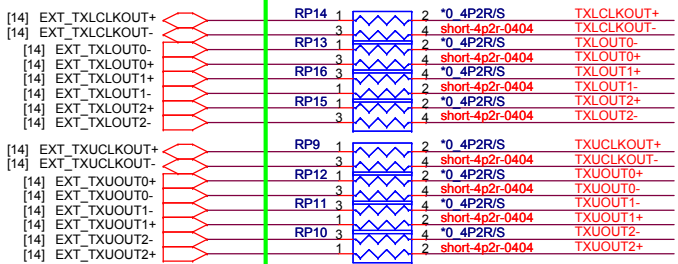
Size Custom	Document Number NV9X VRAM-2(GDDR2 BGA84)	Rev E3A
Date: Friday, July 18, 2008	Sheet 18	of 46

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

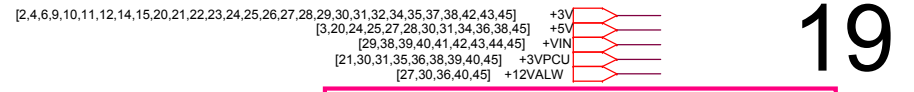
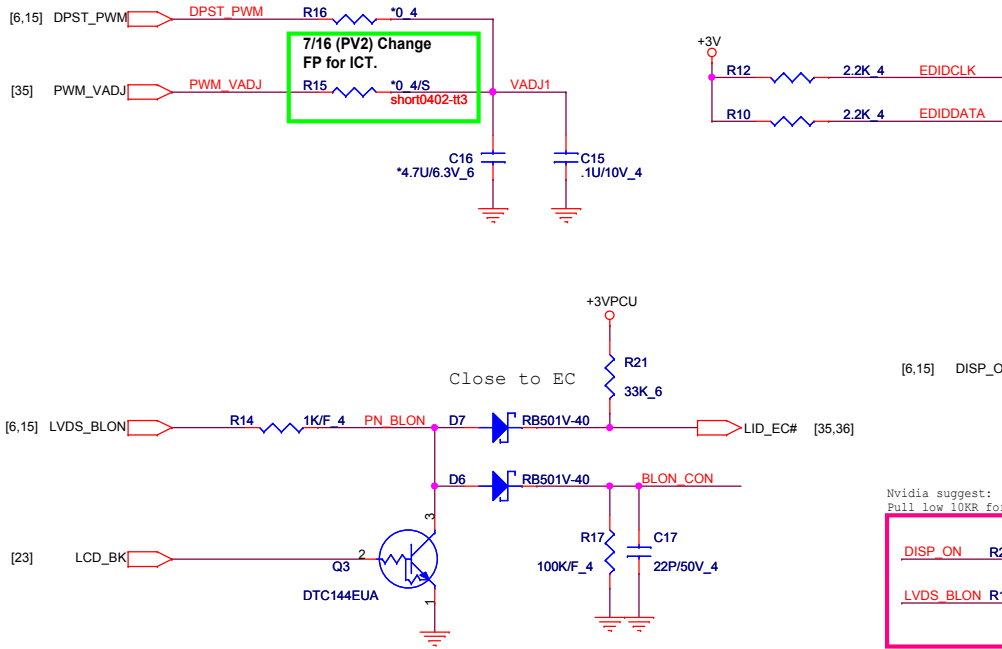
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

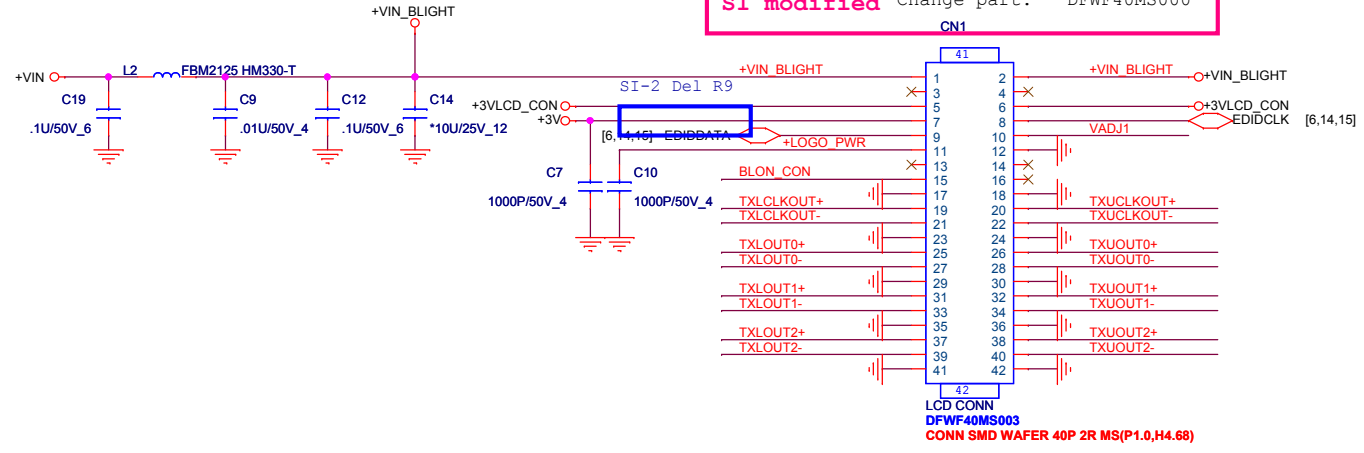


07/14 (PV2) Change footprint for PE require.



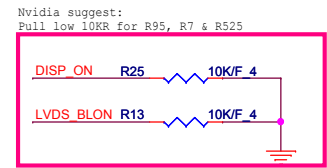
19

SI modified Change part: " DFWF40MS000



0090 use 100 ohm and must change back to 75ohm

SI modified
Del CN7, R88, C115
Remove Logo light2

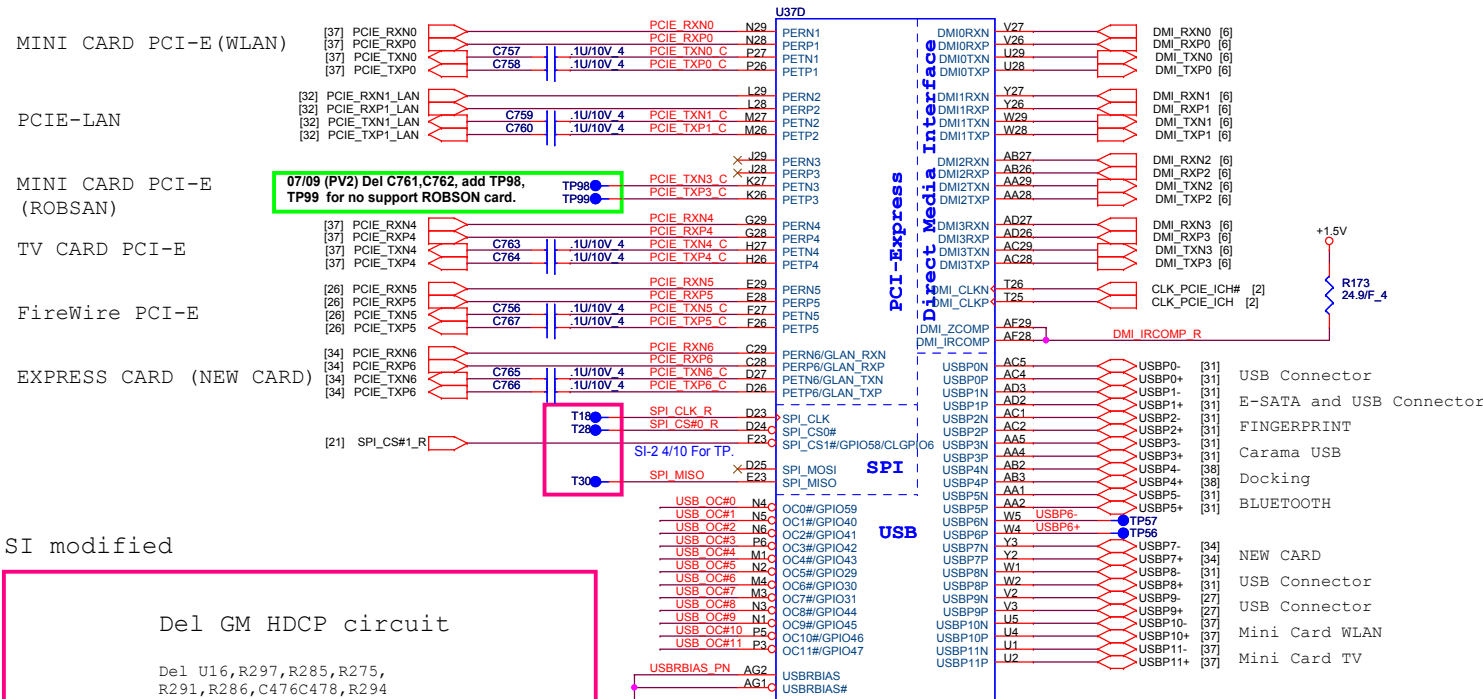


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Size B	Document Number LCD CONN/Lid function	Rev E3A
Date: Friday, July 18, 2008		Sheet 19 of 46

SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +1.5V
[23,31,37,41,42,43,45] +3V
[21,23,24,34,45] +3VS5



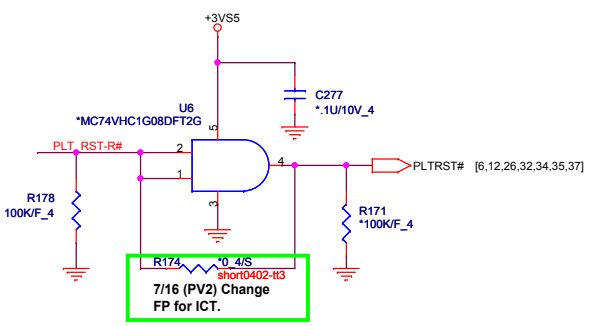
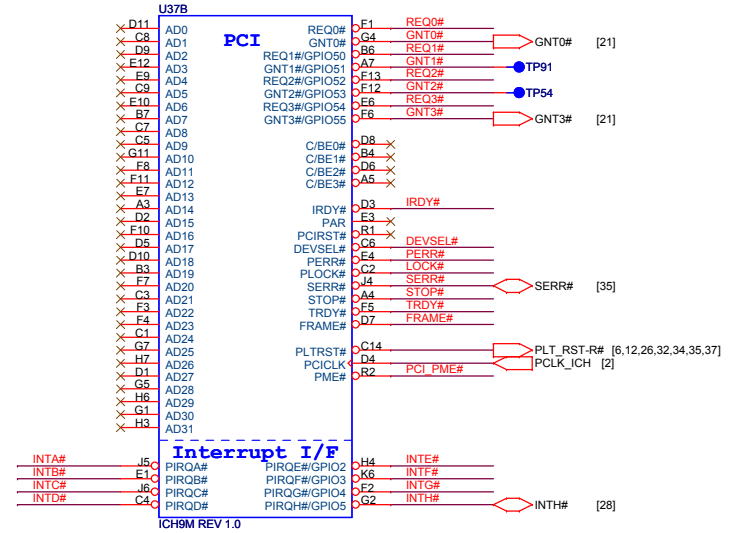
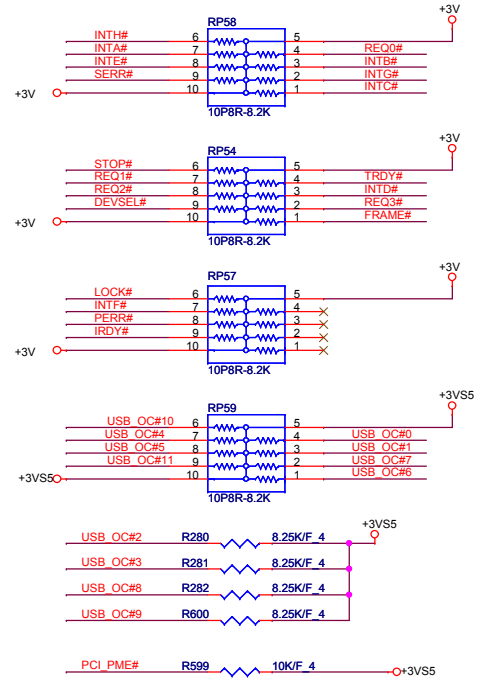
07/09 (PV2) Del C761,C762, add TP98, TP99 for no support ROBSON card.

SI modified

Del GM HDCP circuit

Del U16, R297, R285, R275, R291, R286, C476C478, R294

512K byte SPI ROM
For HDCP only
For GM HDCP



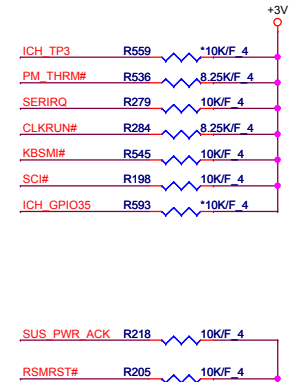
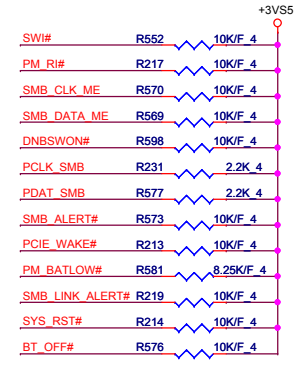
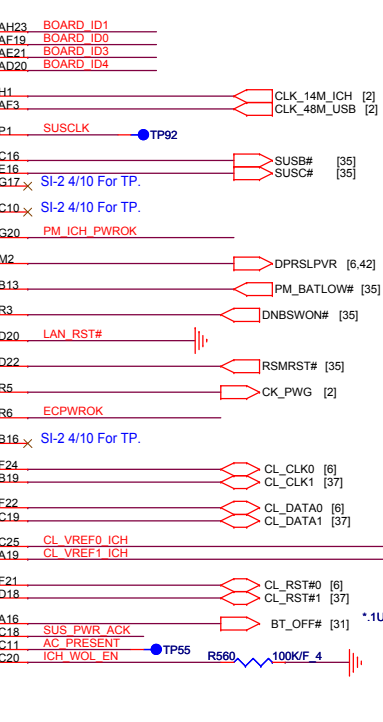
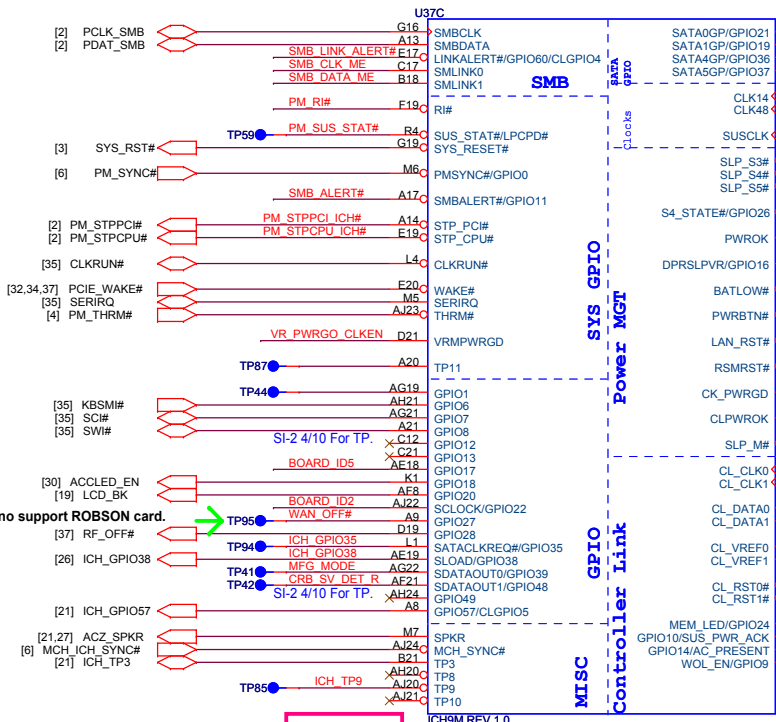
PROJECT : UT6
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NB5

Size Custom Document Number ICH9-M PCIE 2/4 Rev E3A

Date: Friday, July 18, 2008 Sheet 22 of 46

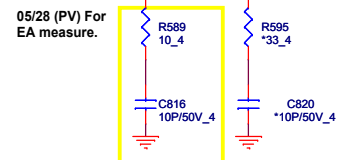
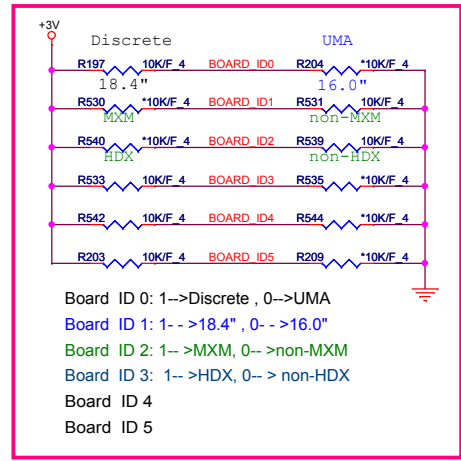
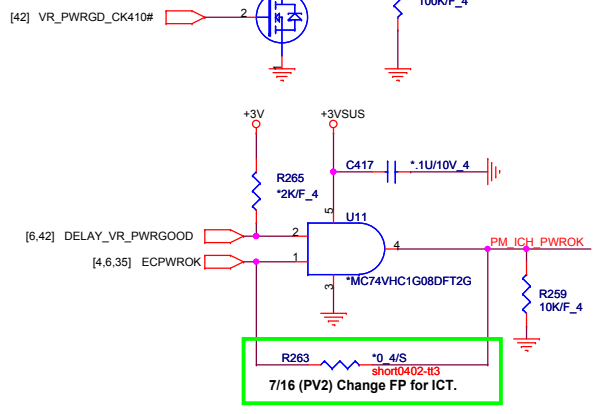
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
 [21,22,24,34,45] +3VS5
 [31,37,41,42,43,45] +3VSUS

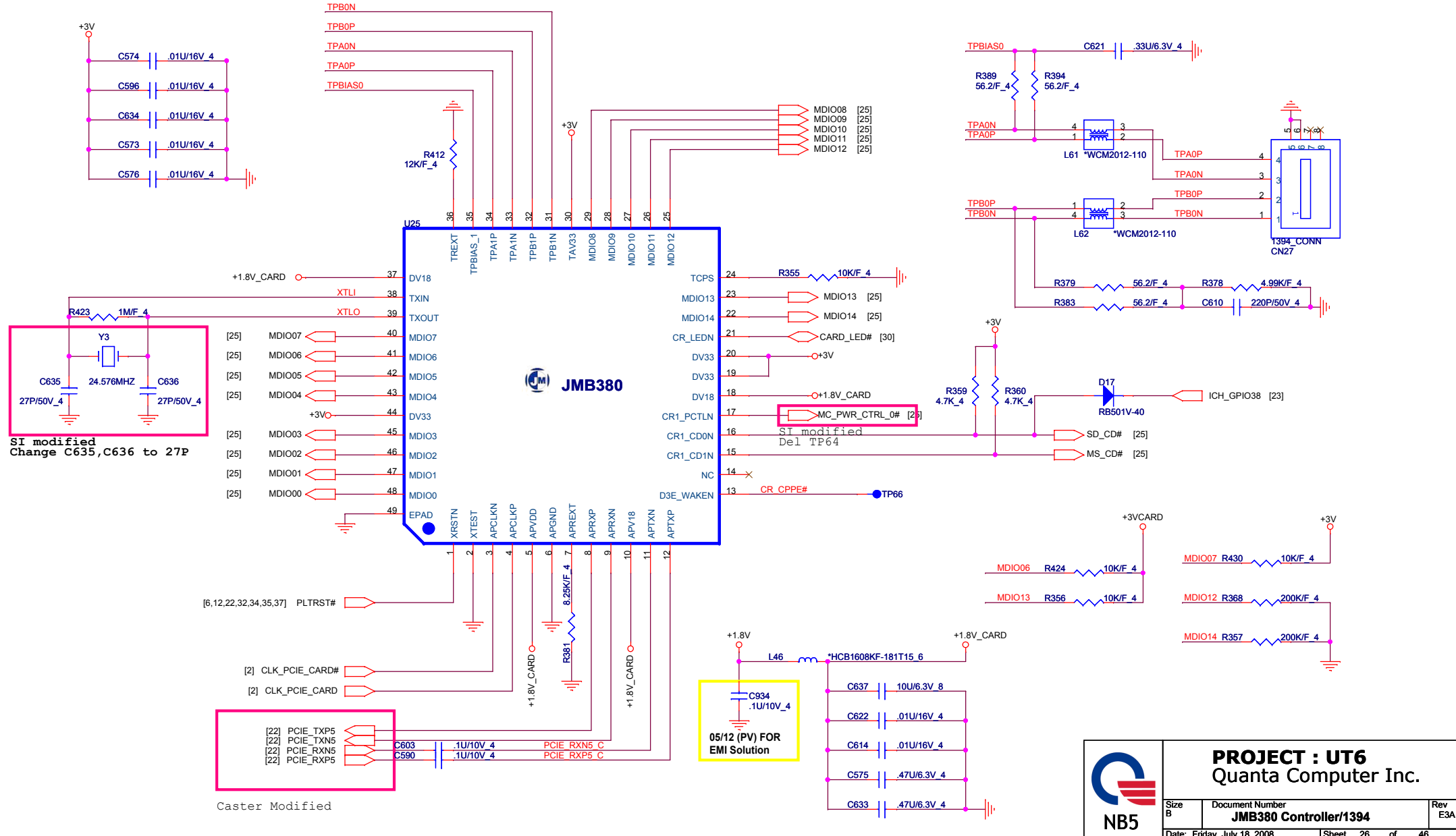


07/09 (PV2) Add TP95 for no support ROBSON card.

SI modified per T18, TP84, TP86

SI-2 Build
 Delete R574, G2 as Bios_Rec can be cover by Bios

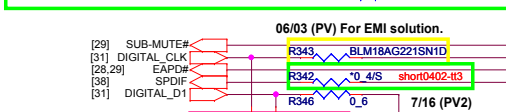




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Size B	Document Number JMB380 Controller/1394	Rev E3A
Date: Friday, July 18, 2008	Sheet 26 of 46	

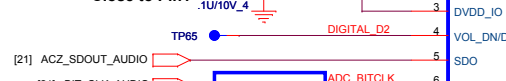
05/23 (PV) For IDT Dolby functionality.
07/14 (PV2) R697 change footprint for PE require.



06/03 (PV) For EMI solution.
07/16 (PV2) Change FP for ICT.



07/14 (PV2) Change footprint for PE require.



05/12 (PV) FOR EMI Solution



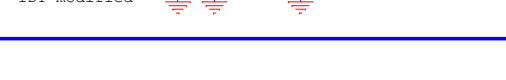
07/14 (PV2) Change footprint for PE require.



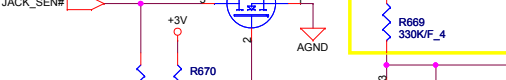
05/20 (PV) FOR Audio noise.



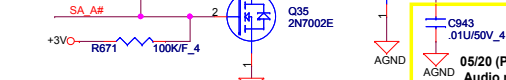
05/20 (PV) FOR Audio noise.



05/20 (PV) FOR Audio noise.

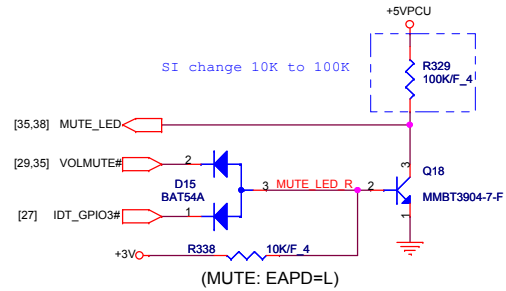
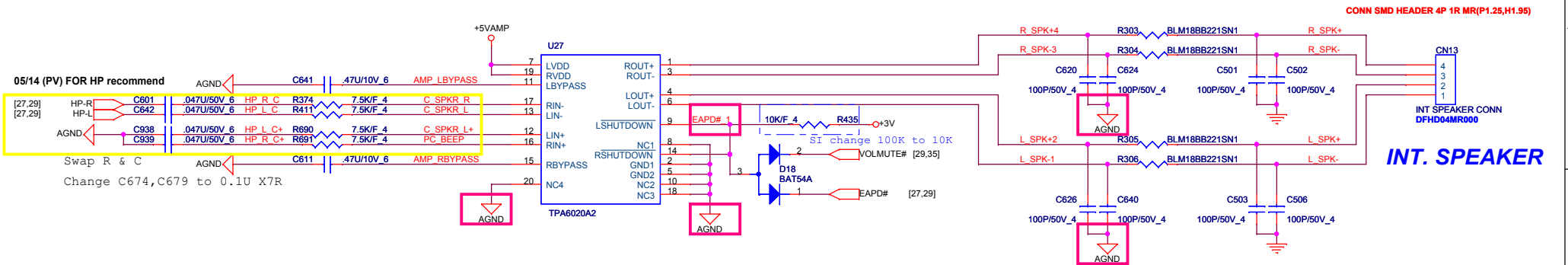


05/20 (PV) FOR Audio noise.



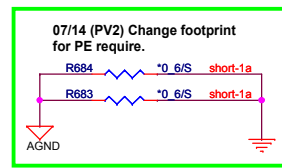
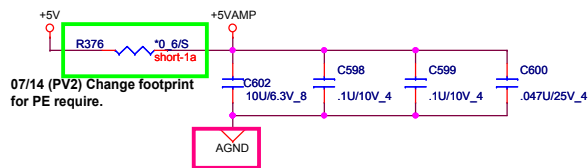
AUDIO AMPLIFIER

+3V [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,29,30,31,32,34,35,37,38,42,43,45]
 +5V [3,19,20,24,25,27,30,31,34,36,38,45]
 +5VPCU [27,35,40,41,42,43,44,45]
 +5VAMP [29]



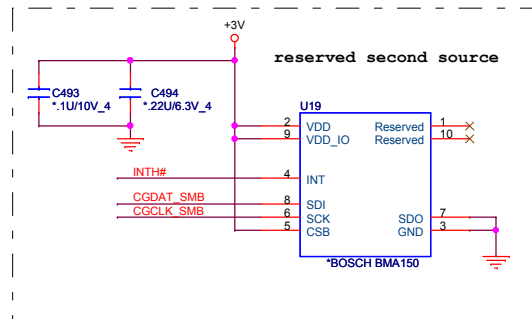
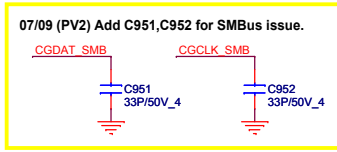
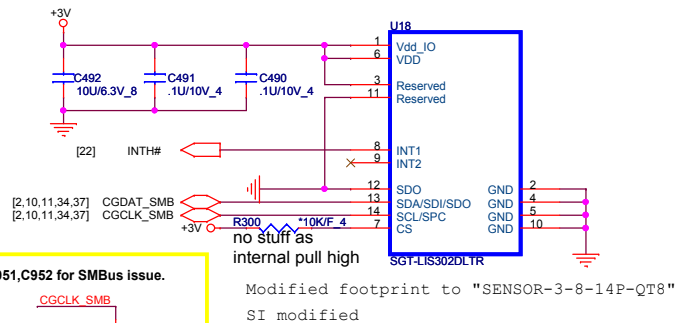
07/09 (PV2) Delete for 2ND FAN function.

Delete Gain set



Del R373, R677, R676
 Del AMP_GND to AGND

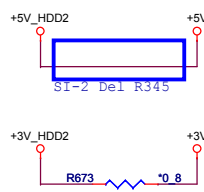
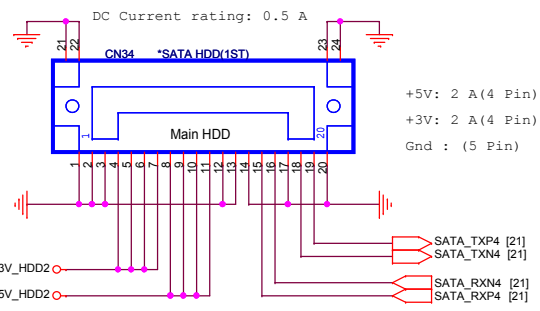
Accelerometer Sensor



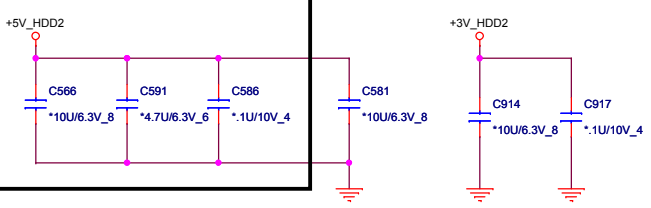
PROJECT : UT6
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Size Custom	Document Number AMP_TPA6017/Accelerometer	Rev E3A
Date: Friday, July 18, 2008	Sheet 28	of 46

SATA_2 CONNECTOR

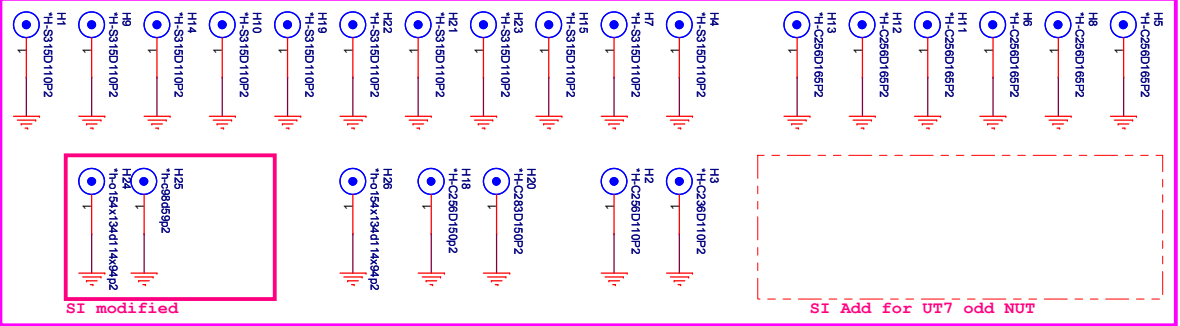


FOR UT7 2ND HDD ONLY.



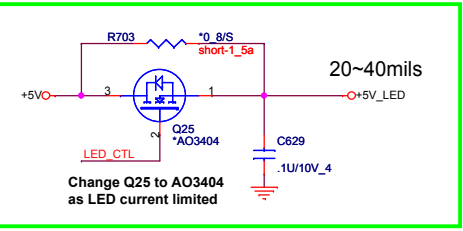
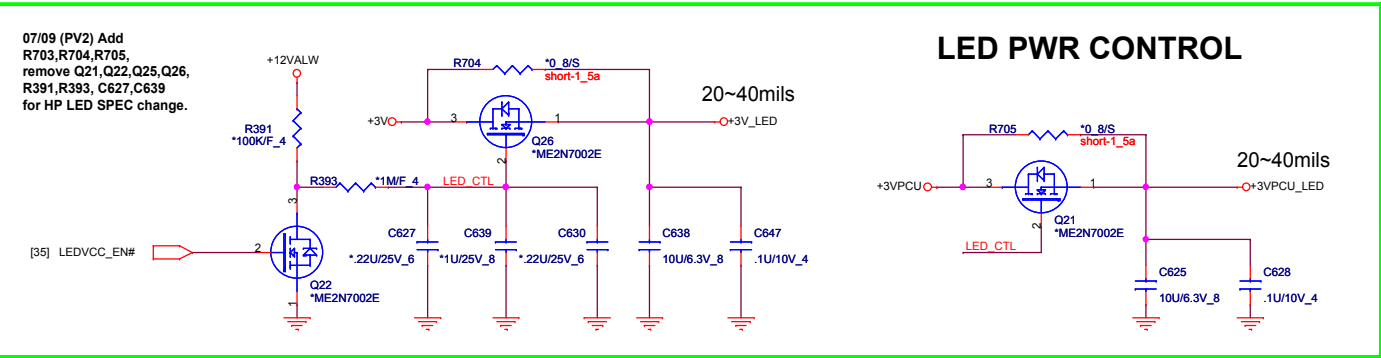
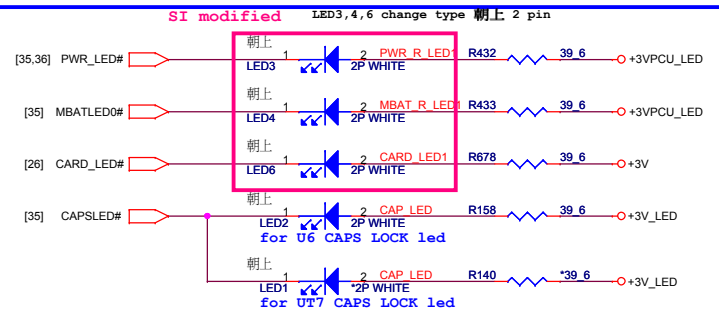
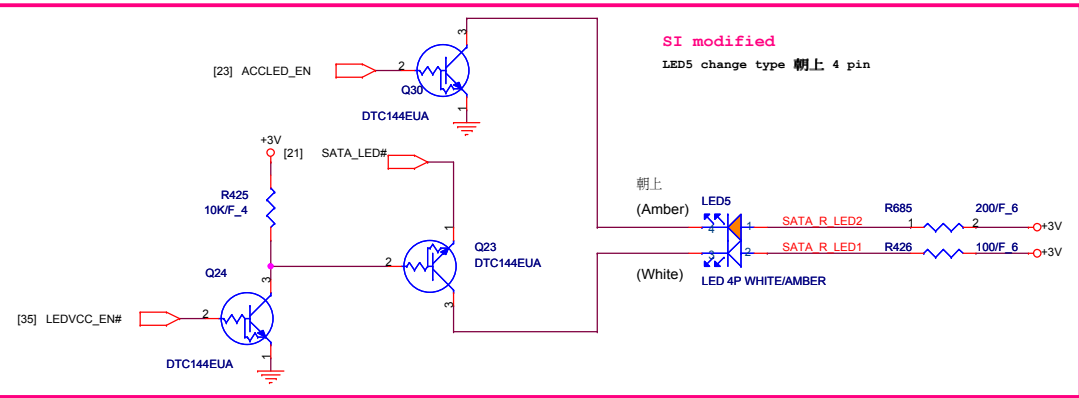
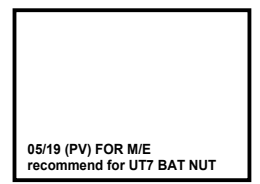
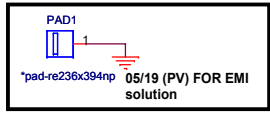
- +3VPCU_LED [36]
- +3V_LED [35]
- +5V [3, 19, 20, 24, 25, 27, 28, 31, 34, 36, 38, 45]
- +3V [2, 4, 6, 9, 10, 11, 12, 14, 15, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 31, 32, 34, 35, 37, 38, 42, 43, 45]
- +12VALW [19, 27, 36, 40, 45]

M/B Screw Hole

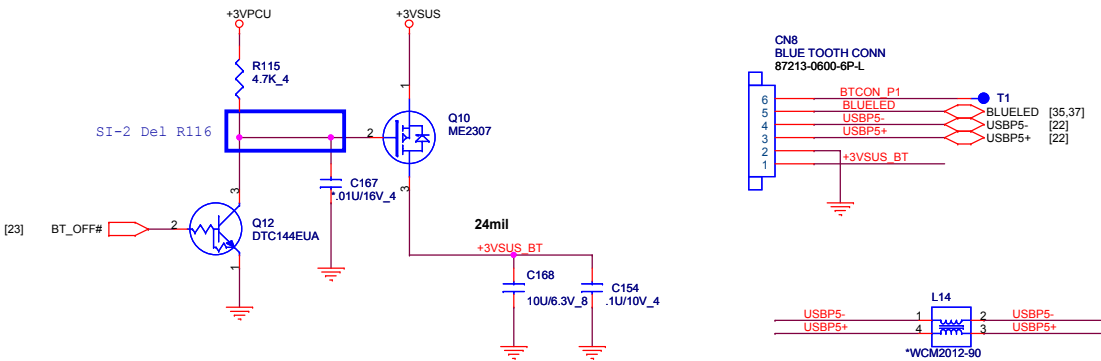


delete all PAD & change screw footprint

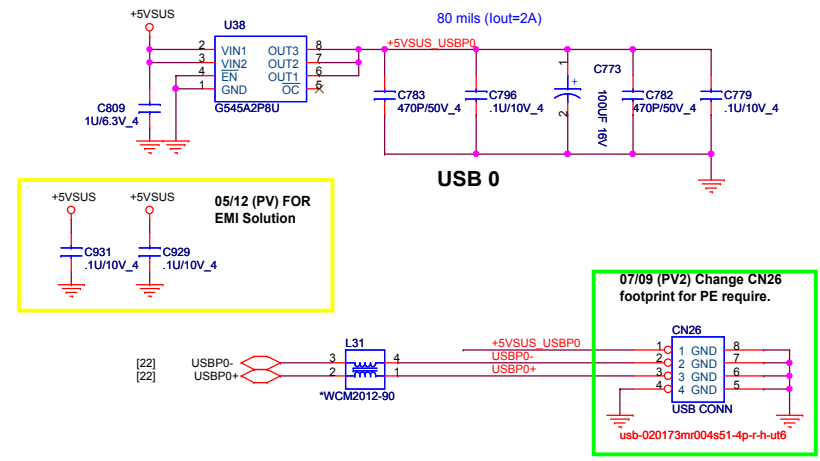
07/14 (PV2) Delete H16,H17 for no support ROBSON card.



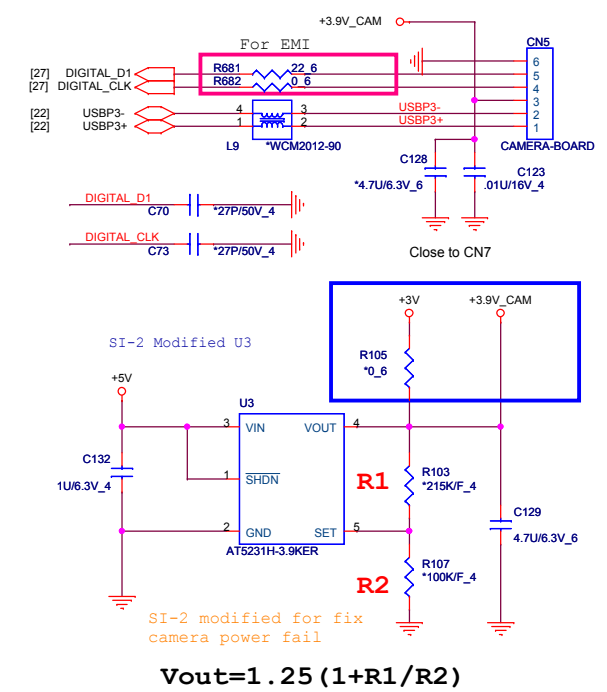
BLUETOOTH



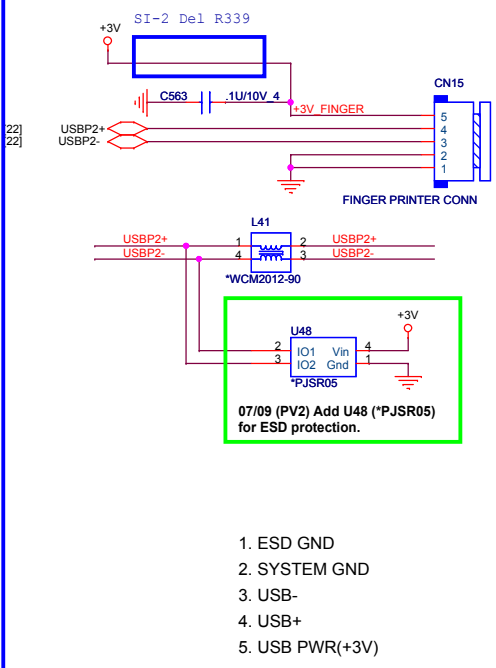
USBX1 and E-SATA



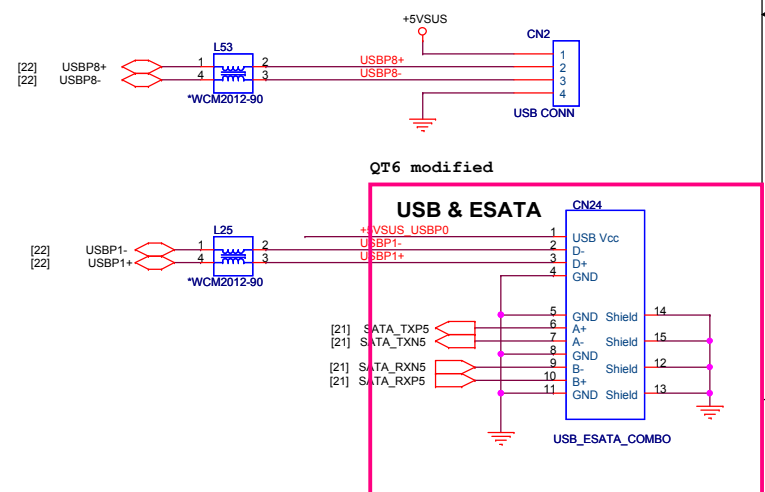
USB CAMERA /DIGITAL MIC CONNECT



USB fingerprint CON



1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

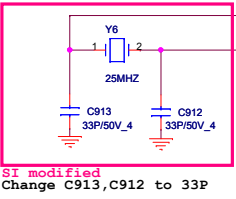
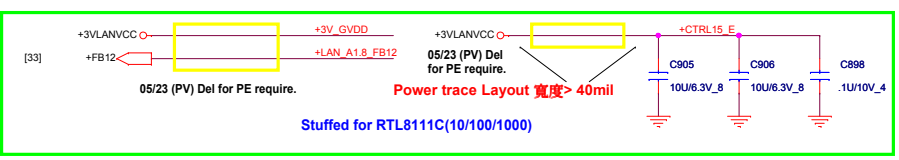


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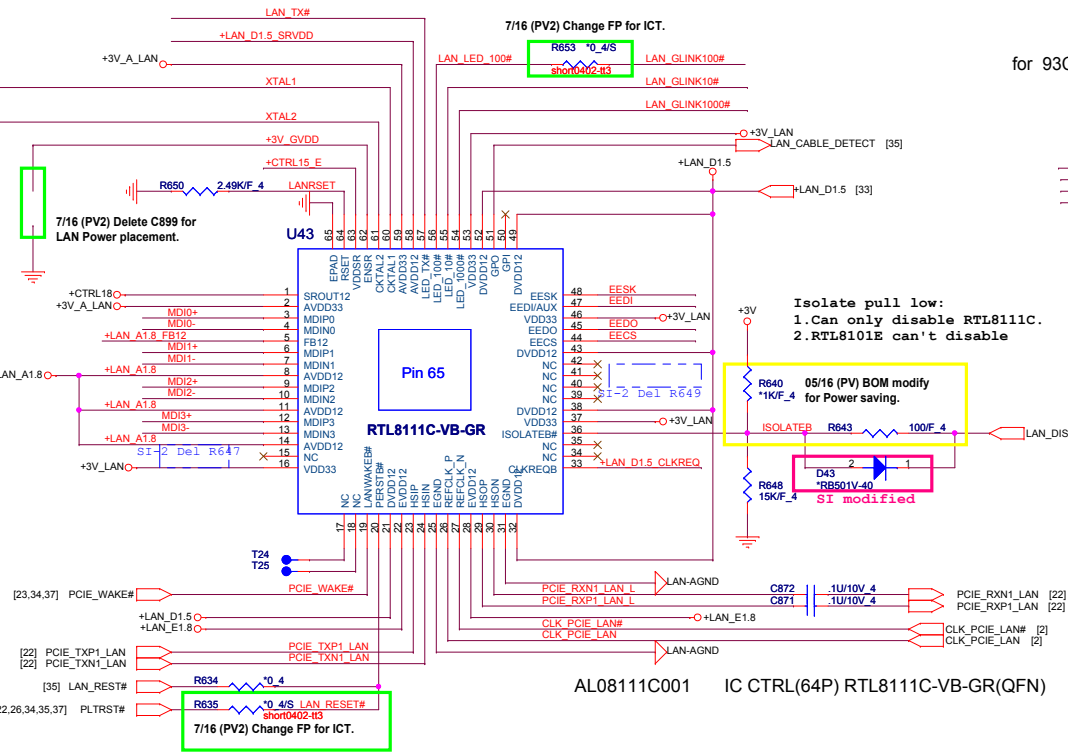
Size Custom	Document Number BT/WC/FT/TS/ESATA/USB	Rev E3A
Date: Friday, July 18, 2008		Sheet 31 of 46

T : Stuffed for RTL8111C(10/100/1000)

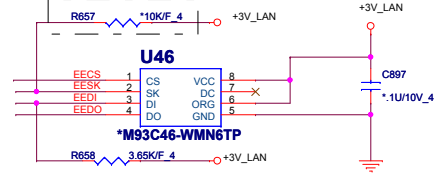
+LAN_D1.5 +LAN_D1.5_SRVDV 05/23 (PV) Del for PE require. +LAN_D1.5_CLKREQ Stuffed for 8102E/RTL8111C



SI modified change C913,C912 to 33P U18#63 wider than 40 mils U18#1 wider than 60 mils

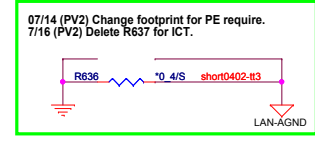


for 93C56 used. NC if 93C46 is used.



Isolate pull low: 1.Can only disable RTL8111C. 2.RTL8101E can't disable

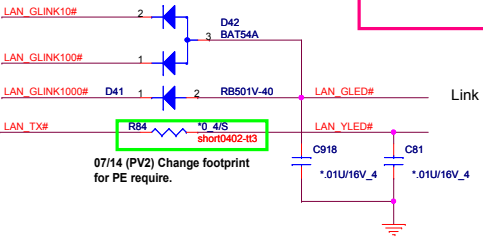
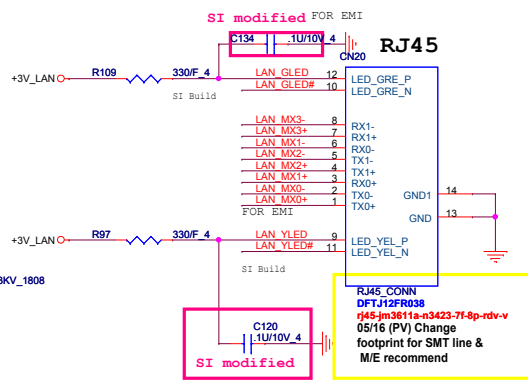
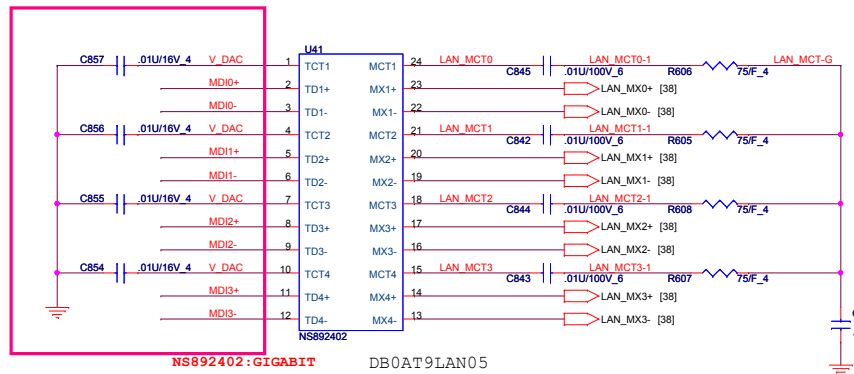
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



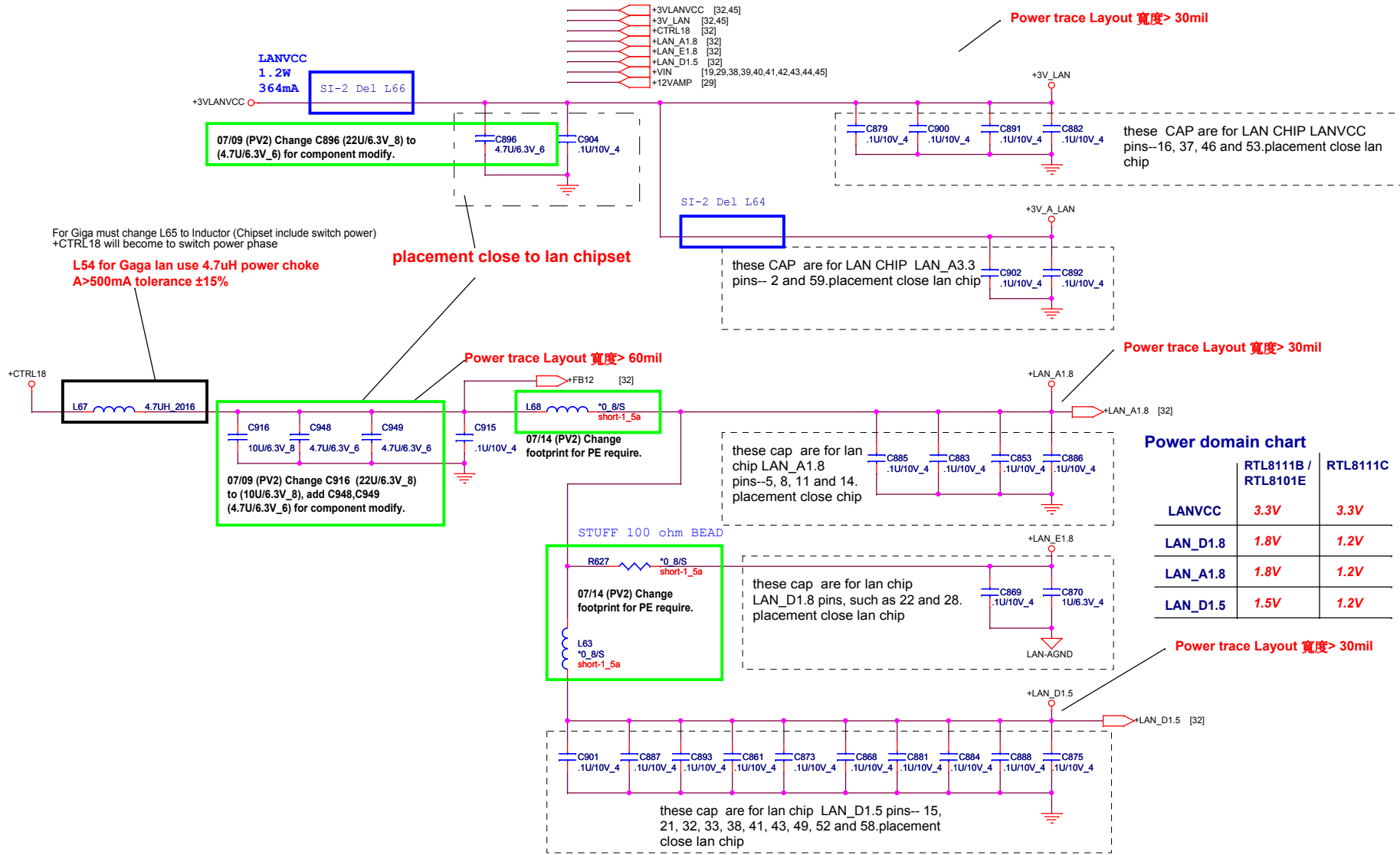
07/14 (PV2) Change footprint for PE require. 7/16 (PV2) Delete R637 for ICT.

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

Caster Modified



07/14 (PV2) Change footprint for PE require.



For Giga must change L65 to Inductor (Chipset include switch power)
+CTRL18 will become to switch power phase

L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%

07/09 (PV2) Change C896 (22U/6.3V_8) to (4.7U/6.3V_6) for component modify.

07/09 (PV2) Change C916 (22U/6.3V_8) to (10U/6.3V_8), add C948,C949 (4.7U/6.3V_6) for component modify.

07/14 (PV2) Change footprint for PE require.

07/14 (PV2) Change footprint for PE require.

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58. placement close lan chip

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53. placement close lan chip

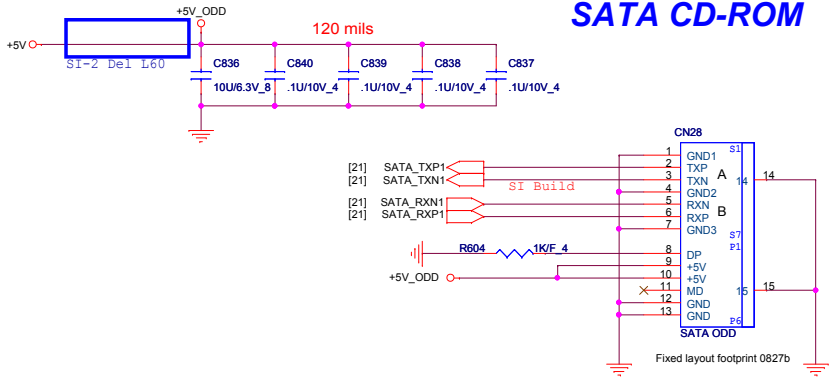
these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59. placement close lan chip

Power domain chart

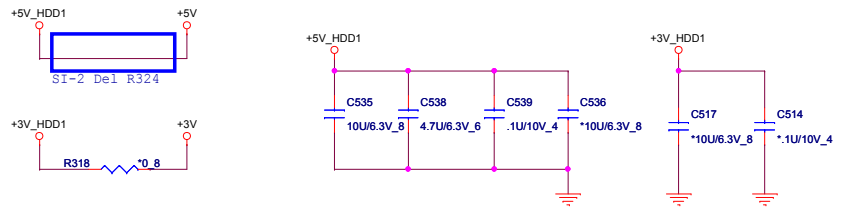
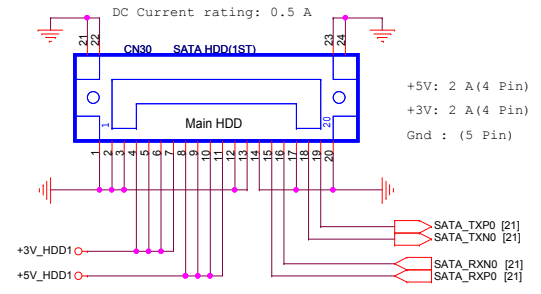
	RTL8111B / RTL8101E	RTL8111C
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

Power trace Layout 寬度 > 30mil

SATA CD-ROM

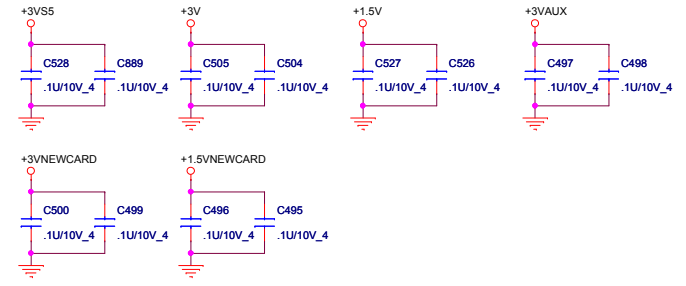
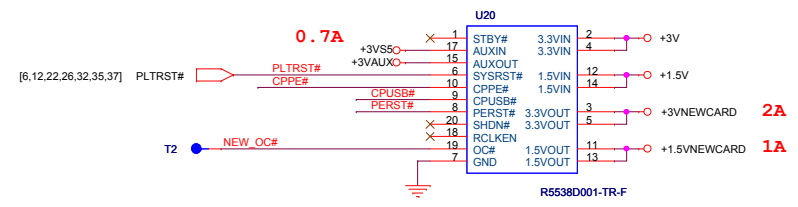
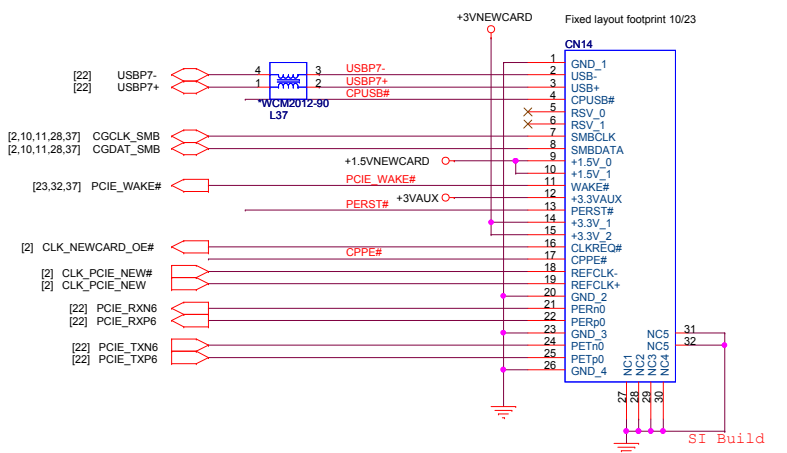


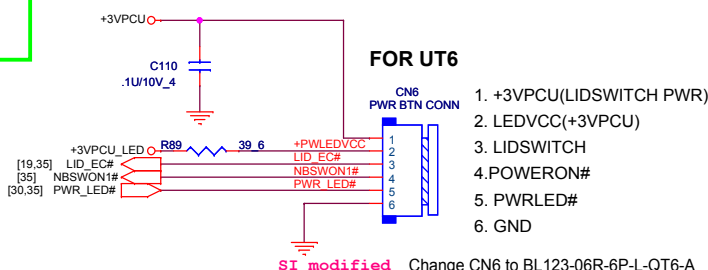
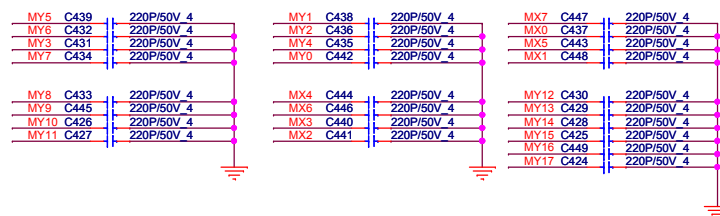
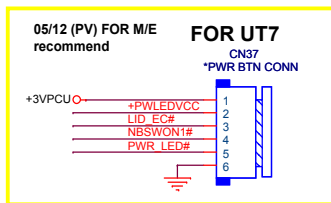
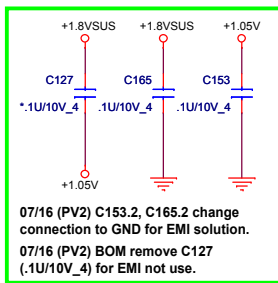
SATA_1 CONNECTOR



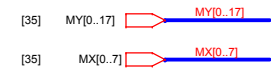
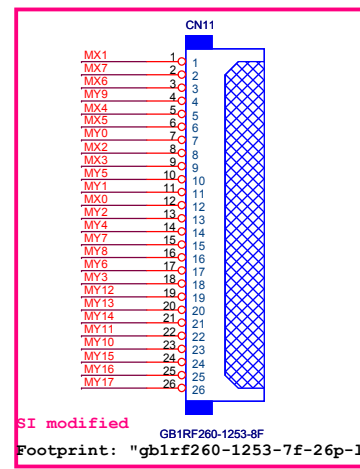
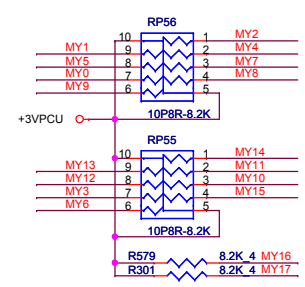
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

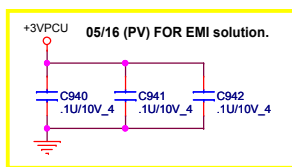
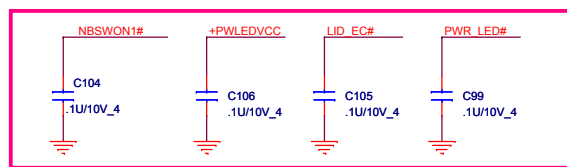




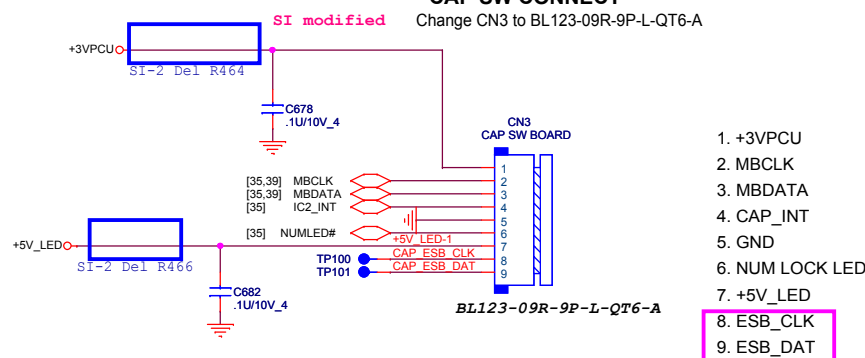
KEYBOARD PULL-UP



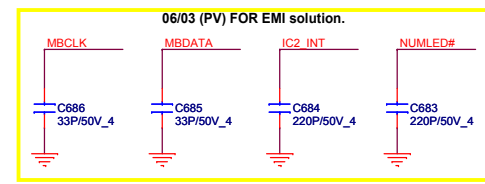
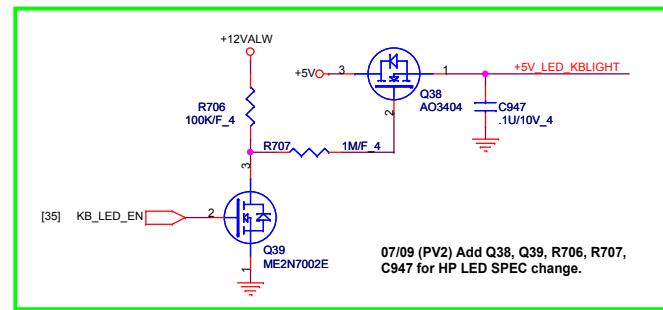
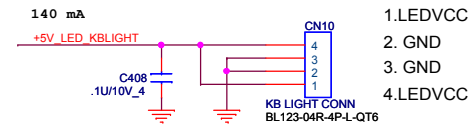
SI modified For EMI



CAP SW CONNECT

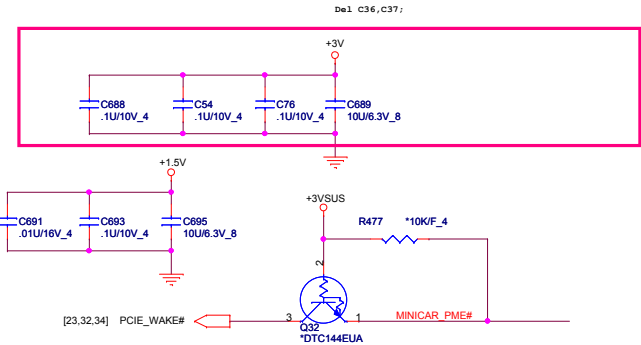
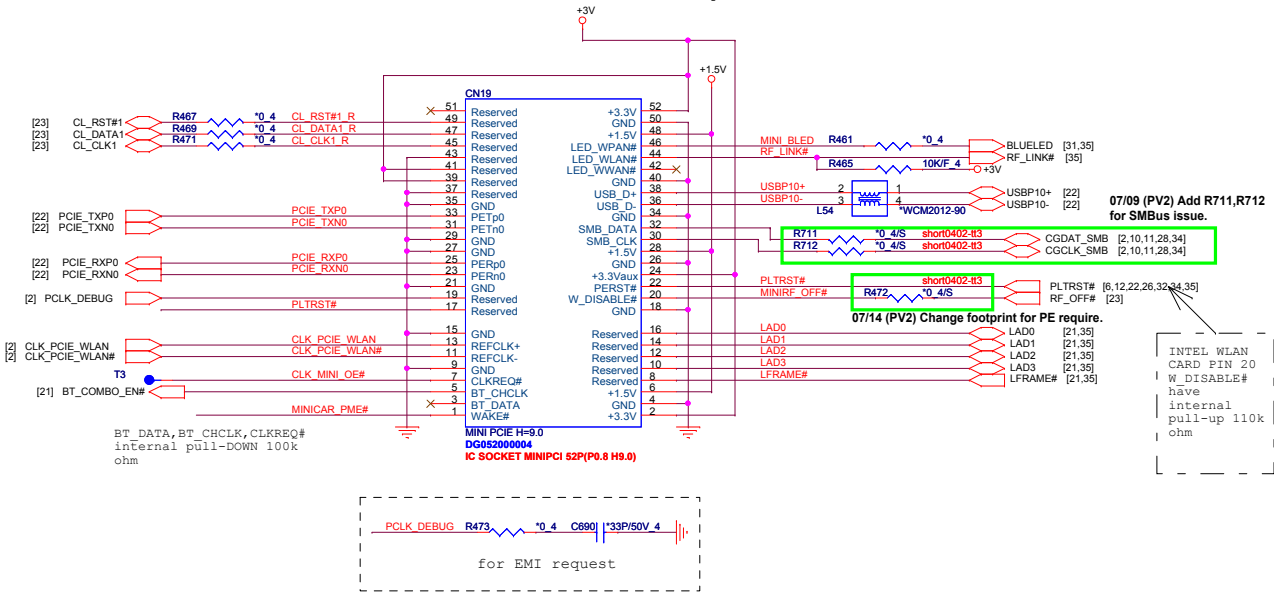


07/14 (PV2) Delete L69,L70,C922,C923 for EMI solution.

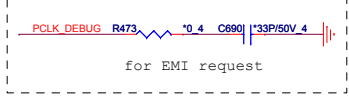


Mini PCI-E Card 1 WLAN

Delete R110,R78
+3V must have a 120mil plane
Each pin 25mil



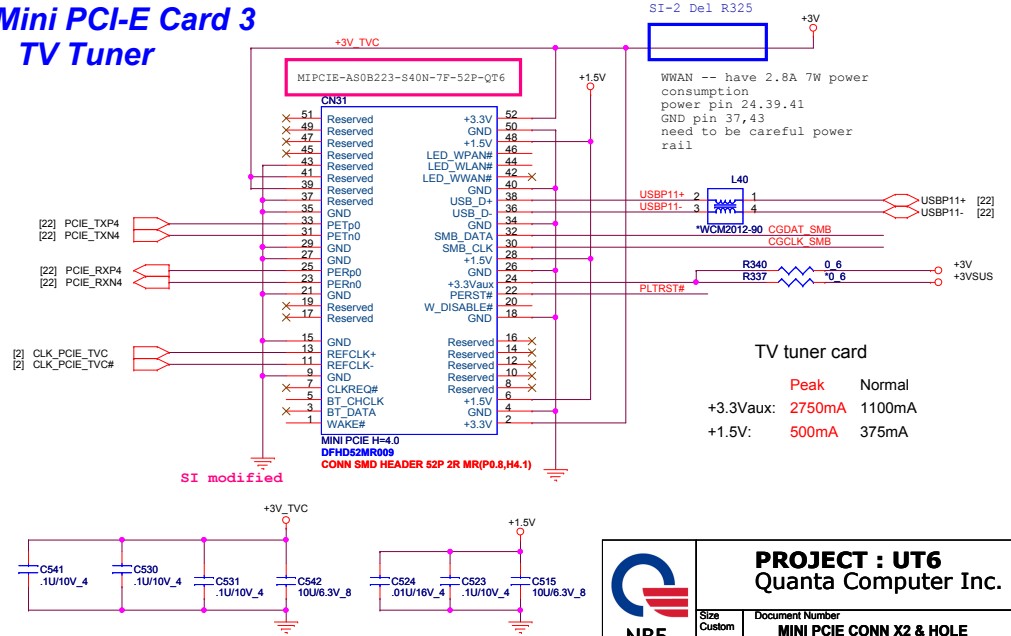
INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm



Mini PCI-E Card 2 ROBSON

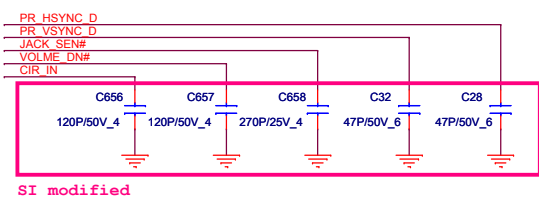
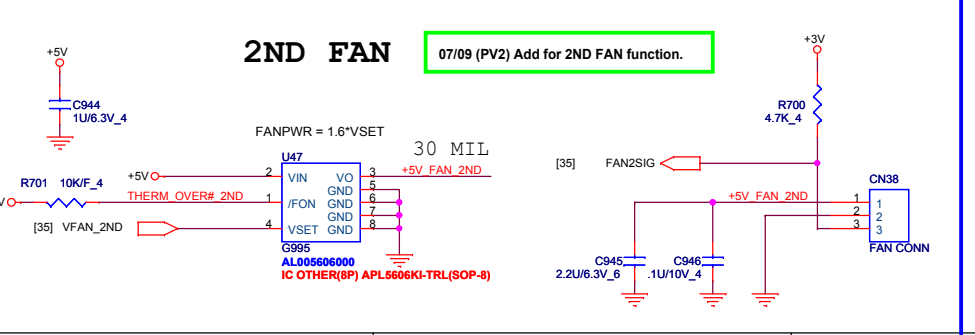
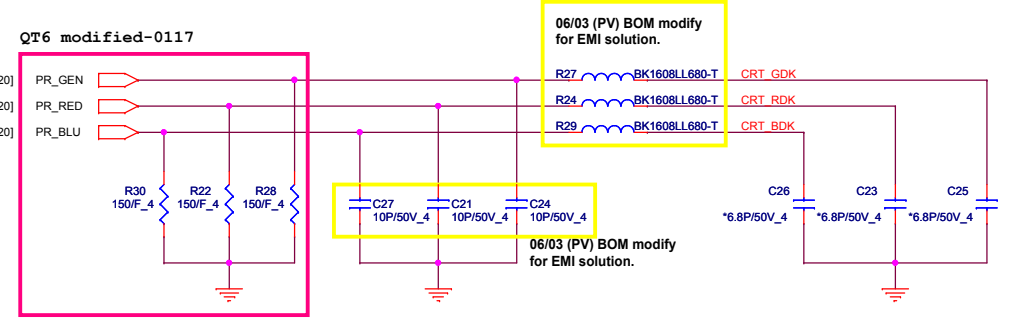
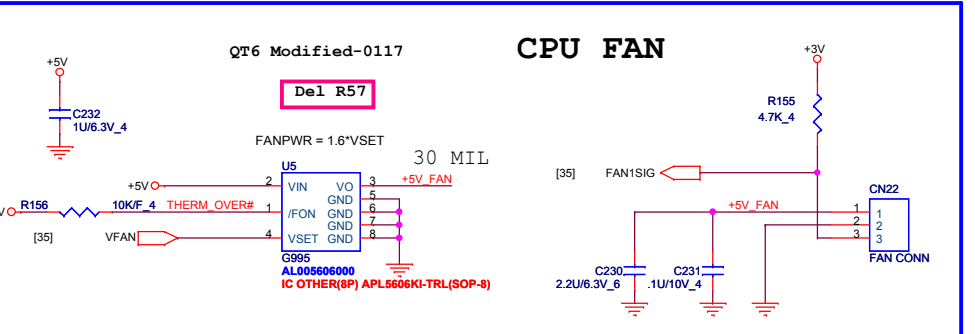
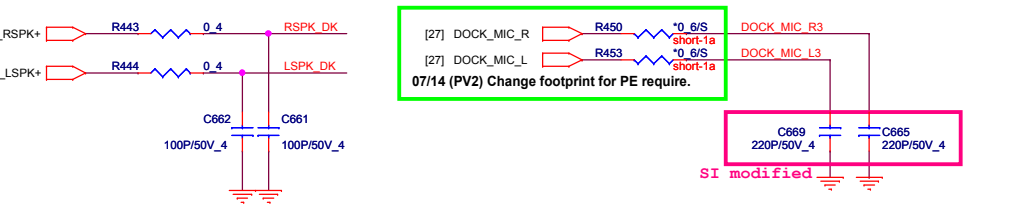
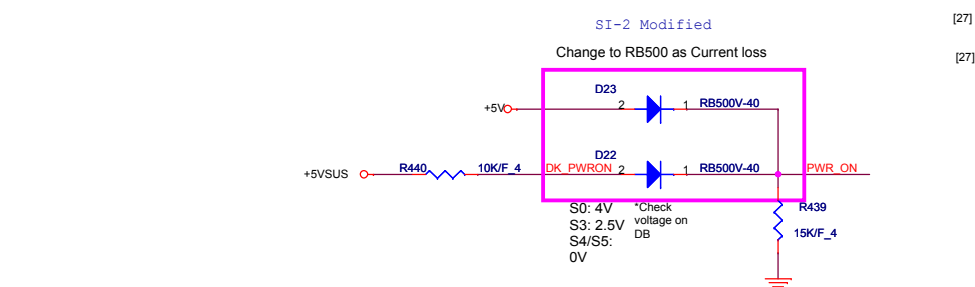
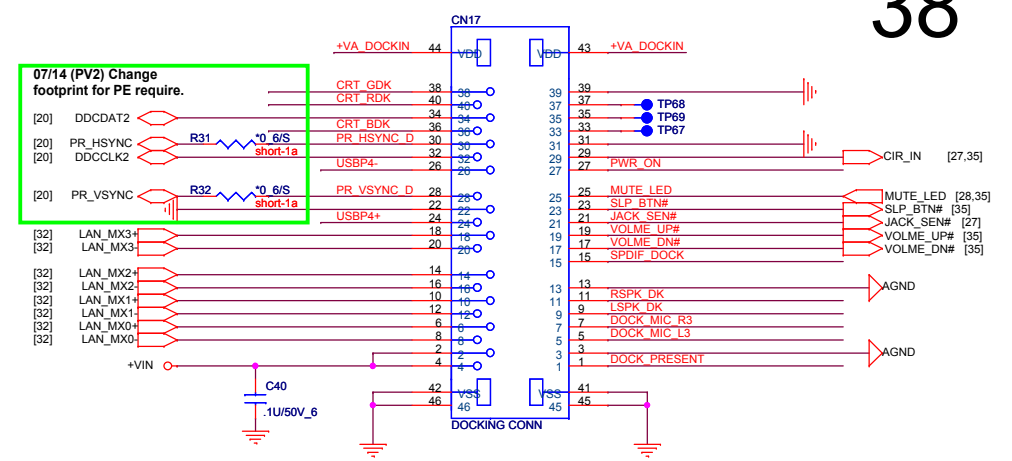
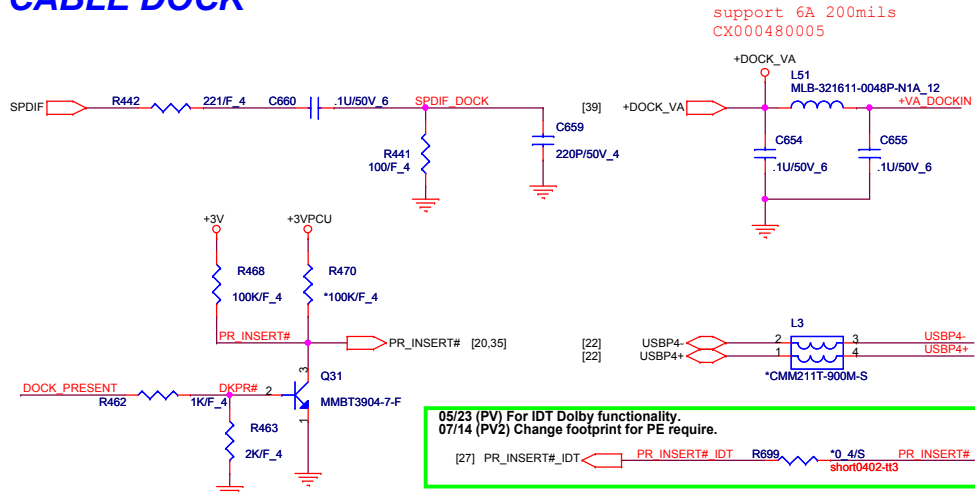
07/09 (PV2) Delete for no support ROBSON card.

Mini PCI-E Card 3 TV Tuner



PROJECT : UT6
Quanta Computer Inc.

Size Custom	Document Number	Rev E3A
MINI PCIE CONN X2 & HOLE		
Date: Friday, July 18, 2008	Sheet 37 of 46	



PROJECT : UT6
Quanta Computer Inc.

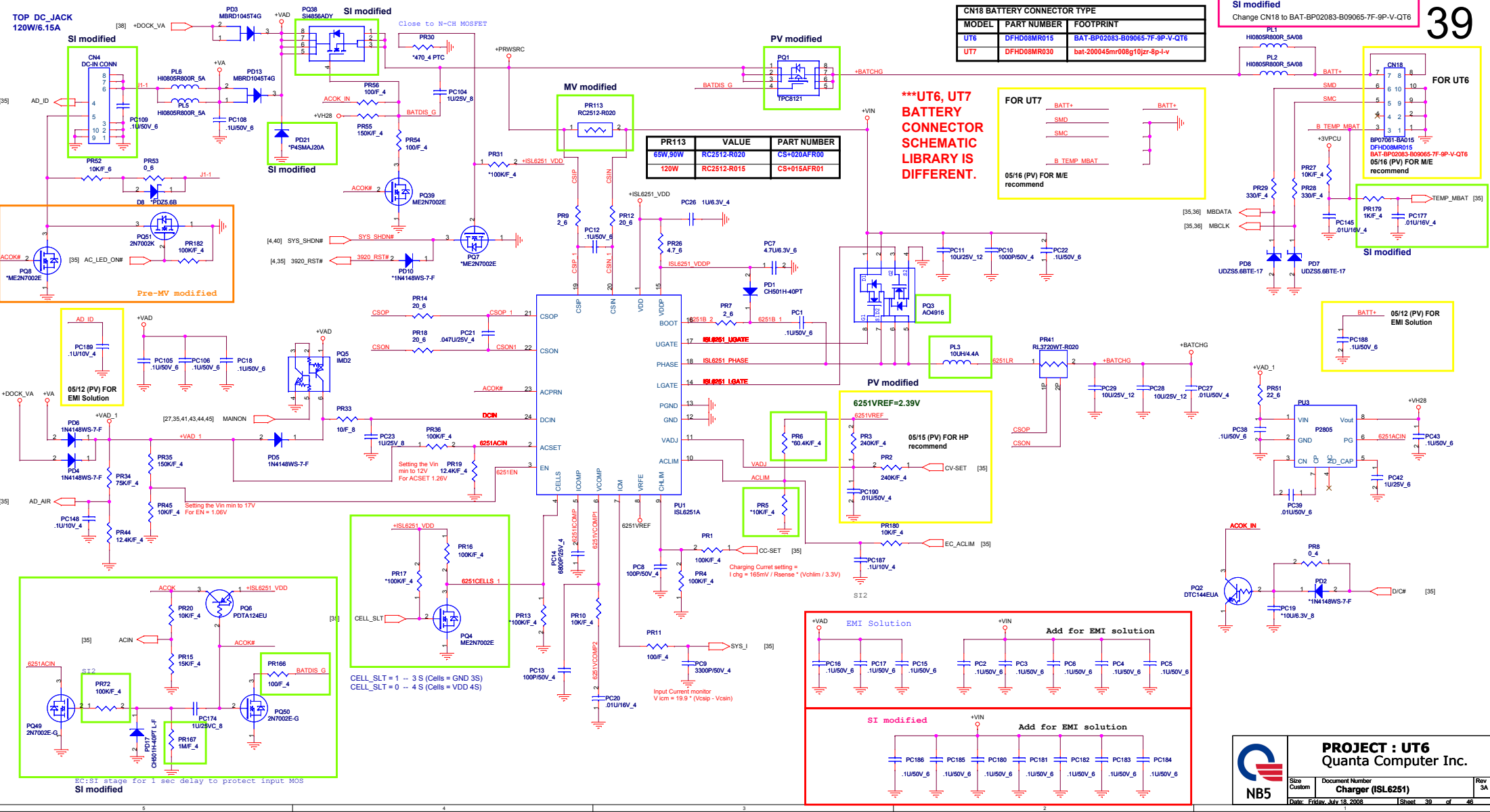
Size Custom	Document Number CABLE DOCKING/FAN	Rev E3A
Date: Friday, July 18, 2008	Sheet 38 of 46	

TOP_DC_JACK
120W/6.15A

CN18 BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT6	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT7	DFHD08MR030	bat-200045mr009g10jzr-8p1-v

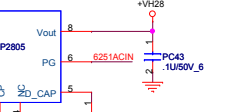
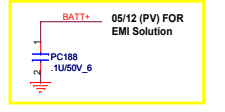
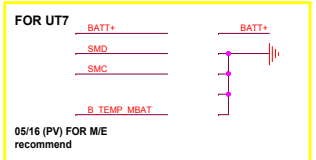
SI modified
Change CN18 to BAT-BP02083-B09065-7F-9P-V-QT6

39



PR113	VALUE	PART NUMBER
65W_90W	RC2512-R020	CS+020AFR00
120W	RC2512-R015	CS+015AFR01

*****UT6, UT7 BATTERY CONNECTOR SCHEMATIC LIBRARY IS DIFFERENT.**



CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

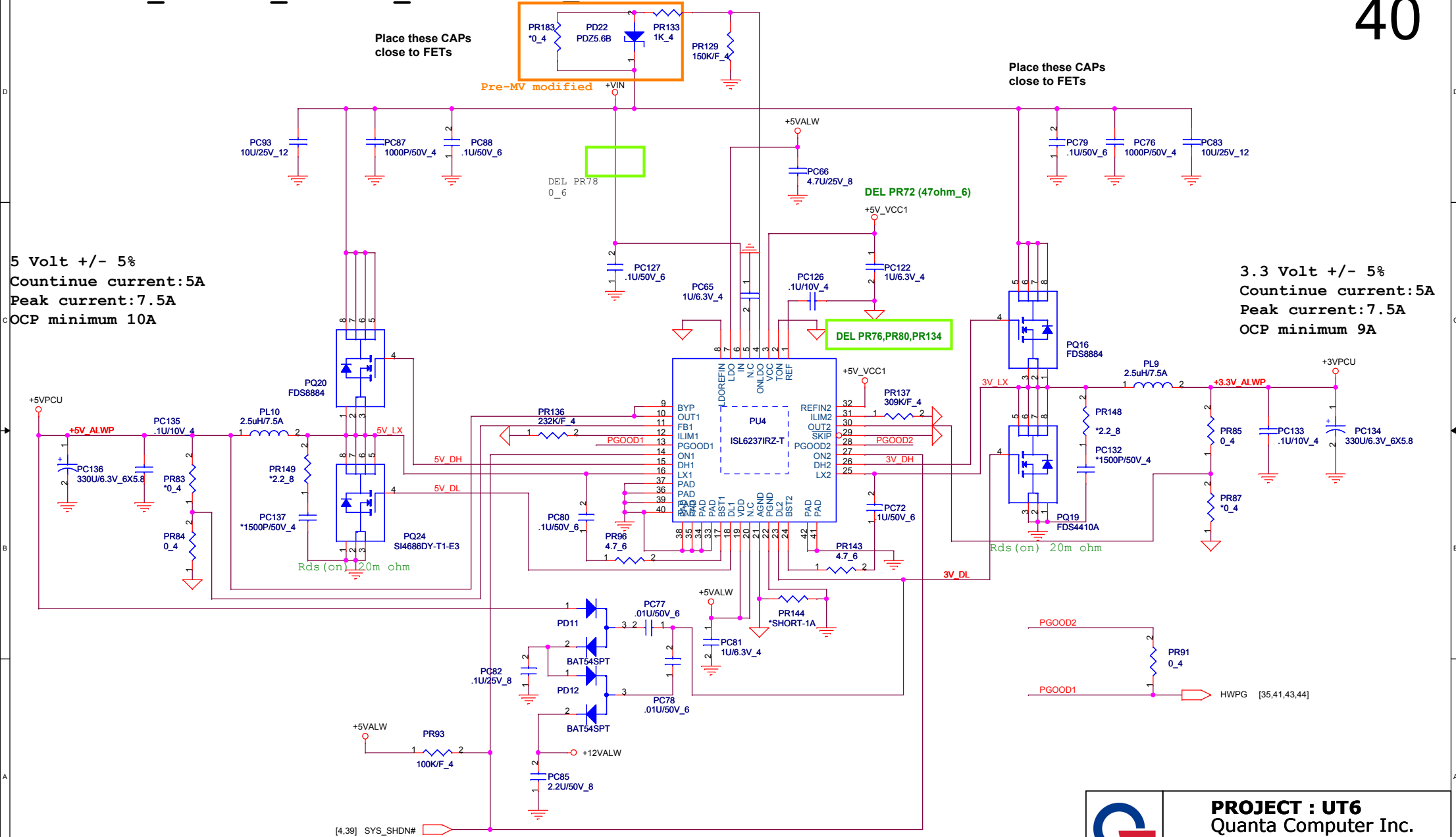
Input Current monitor
V_{icm} = 19.9 * (V_{csip} - V_{csin})

RC251 stage for 1 sec delay to protect input MOS
SI modified

PROJECT : UT6
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
Charger (ISL6251)		
Date: Friday, July 18, 2008		

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V ALW



5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A

Place these CAPs close to FETs

Place these CAPs close to FETs

Pre-MV modified

Rds(on) 20m ohm

Rds(on) 20m ohm

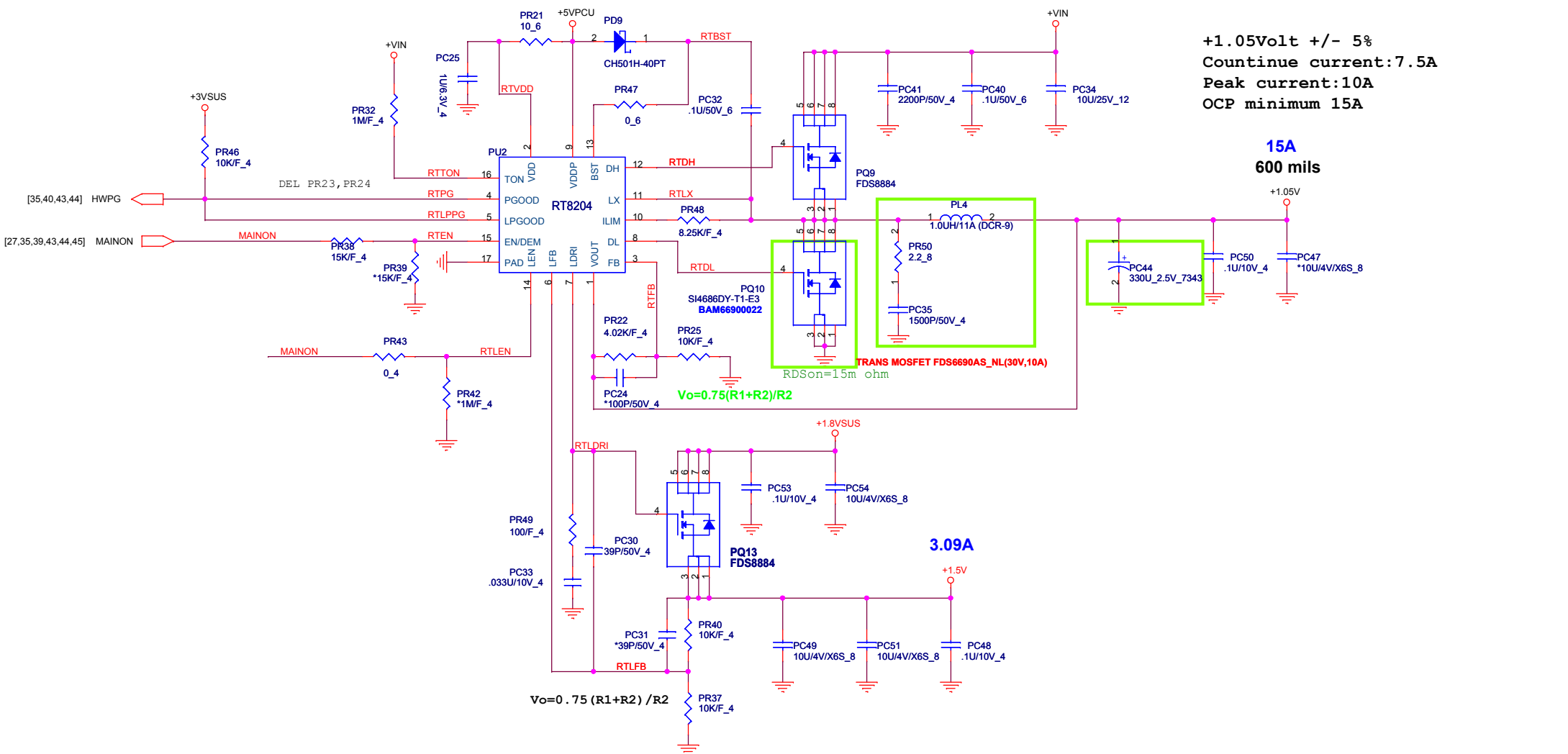
[4,39] SYS_SHDN#

PROJECT : UT6
 Quanta Computer Inc.



Size B	Document Number +5V/+3V (ISL6237)	Rev 3A
Date: Friday, July 18, 2008	Sheet 40 of 46	


VCCP1.05V & +1.5V



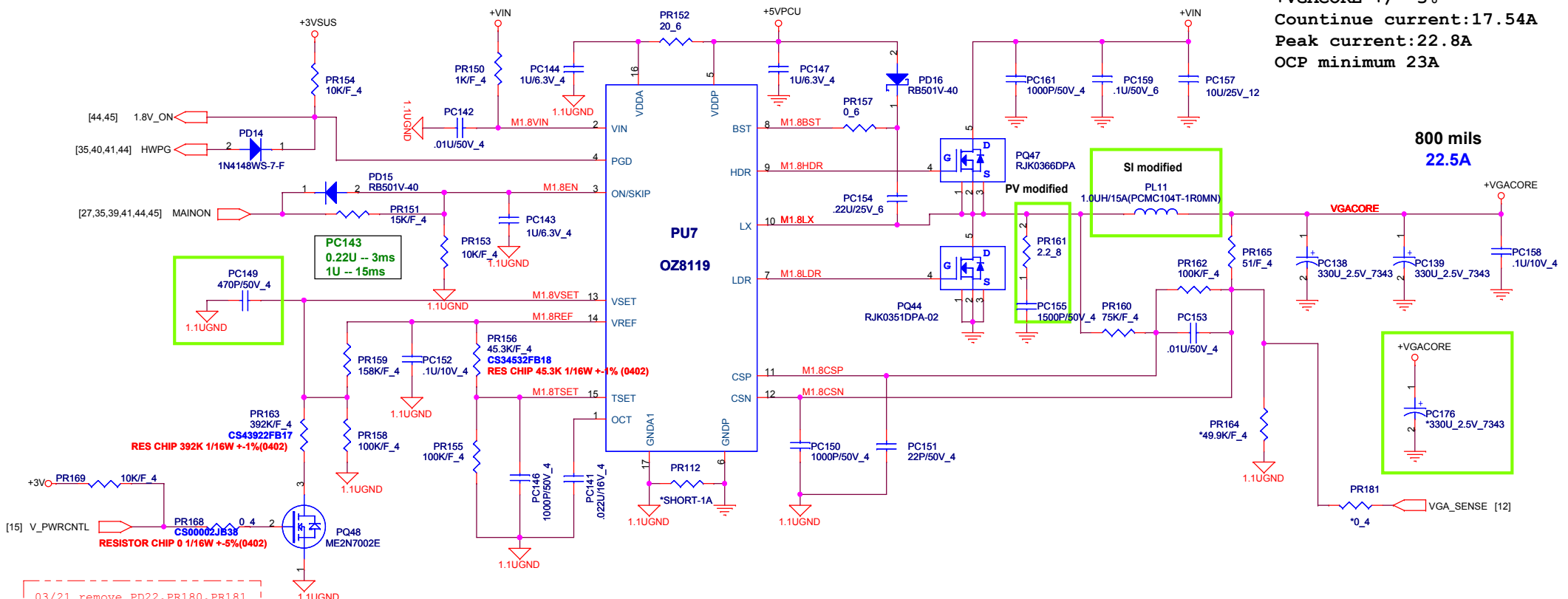
+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A

15A
600mils

3.09A

	PROJECT : UT6 Quanta Computer Inc.	
	Size B	Document Number +1.05V/+1.5V (RT8204)
Date: Friday, July 18, 2008		Sheet 41 of 46

+VGACORE +/- 3%
Continue current: 17.54A
Peak current: 22.8A
OCP minimum 23A



800 mils
22.5A

VREF=2.75V +/-1.5%

**NB9P-GS: PR163=392Kohm
 Output = 0.9V**

NB9M-GE: PR203=590Kohm
 NB9P-GS: PR203=768Kohm

CS45902FB10 RES CHIP 590K 1/16W +/-1%(0402)
 CS47682FB10 RES CHIP 768K 1/16W +/-1%(0402)

03/21 remove PD22, PR180, PR181

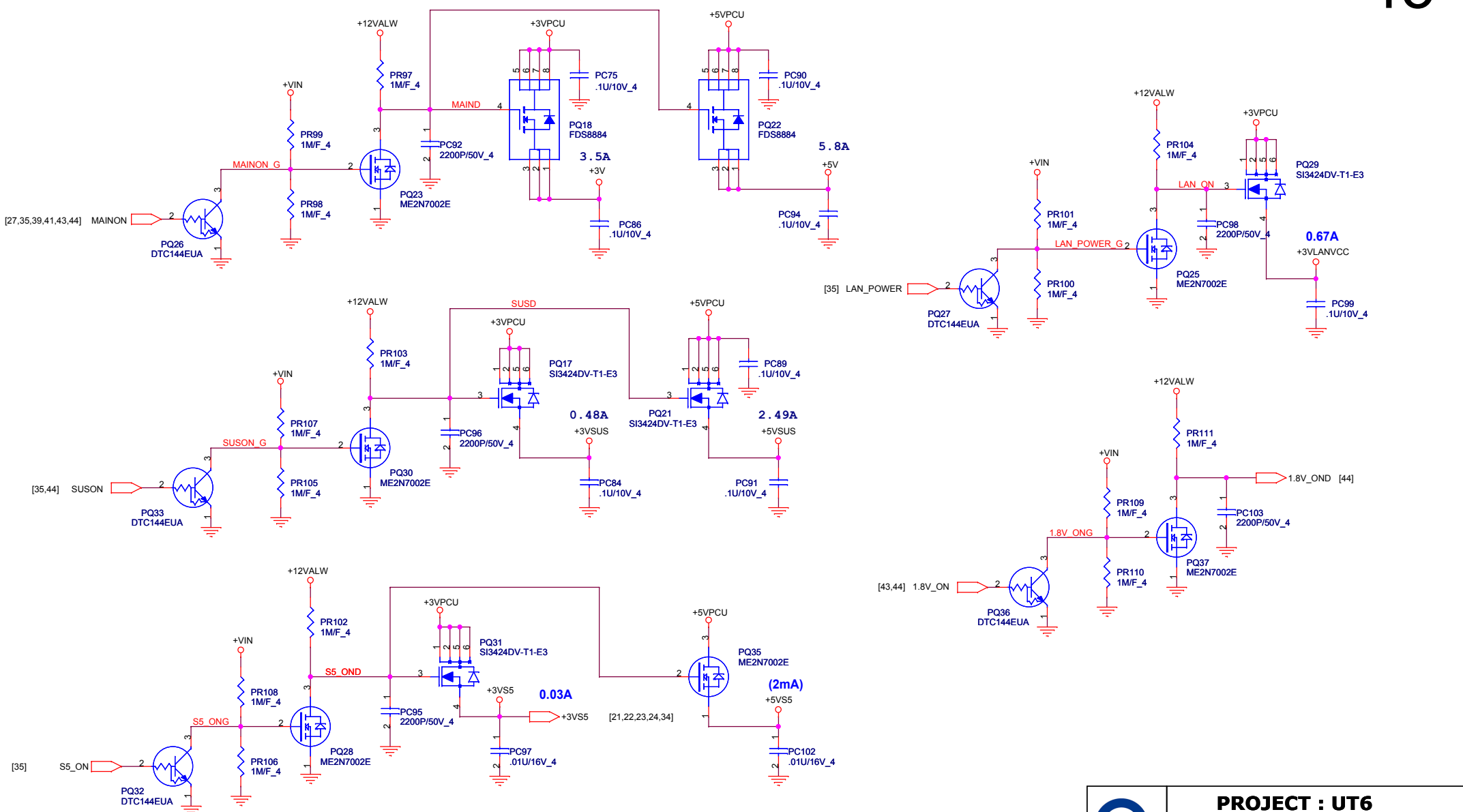
V_PWRCNTL	NB9P-GS
GPIO5	1.05V
Low	1.05V
High	0.9V

VGA_GPIO6	V_PWRCNTL		NB9P-GS	NB9M-GE
GPIO6	GPIO5			
Low	Low	MAX BAT	0.9V	0.9V
Low	High	SD DVD	0.9V	0.9V
High	Low	HD DVD	0.9V	0.9V
High	High	MAX PERF	1.05V	1.09V



PROJECT : UT6
 Quanta Computer Inc.


Size B	Document Number VGA CORE OZ8118	Rev 3A
Date: Friday, July 18, 2008	Sheet 43 of 46	



PROJECT : UT6
Quanta Computer Inc.

Size B	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 3A
Date: Friday, July 18, 2008	Sheet 45 of 46	

	Voltage level	AC MODE				DC MODE			
		S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLAVCC	3.3V +/- 5%	V				V			

	PROJECT : UT6 Quanta Computer Inc.	
	Size Custom Date: Friday, July 18, 2008	Document Number Voltage Sheet 46 of 46